Akhil Raj Baranwal

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Work Experience

Micron Technology — *Hyderabad, India*

ASIC Design Engineer — *Aug 2020 - Present*

- SoC verification of storage-controllers and post-silicon bringup.

CFAED - Techinsche Universität Dresden — *Dresden, Germany*

Guest Researcher — *Jan 2020 - June 2020*

- Worked with the Chair for Processor Design, CFAED, exploring accelerator designs for traditional RL problems.

Micron Technology — *Bengaluru, India*

Embedded Engineer Intern — *May 2019 - July 2019*

- Worked on encrypted high speed memory-trace collection and analysis of DRAM AXI traffic in PetaLinux environment

Adani Power Maharashtra Limited — *Tirora, India*

Summer Intern — *May 2018 - July 2018*

- Developed a rule-based interface based on GSM for controlling industrial machines spread across an area of more than 1600 acres.

Publications

ReLAccS: A Multi-level Approach to Accelerator Design for Reinforcement Learning on FPGA-based Systems — *Oct 2020*

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems — *DOI Hyperlink*

MemOReL: A Memory-oriented Optimization Approach to Reinforcement Learning on FPGA-based Embedded Systems — *Jun 2021*

Proceedings of the 2021 on Great Lakes Symposium on VLSI — *DOI Hyperlink*

Development of Completely Automated Poly Potential Portable Potentiostat — *Feb 2021*

ECS Journal of Solid State Science and Technology — *DOI Hyperlink*

Education

Birla Institute of Technology and Science, Pilani — *Hyderabad, India*

Bachelor of Electronics and Instrumentation Engineering — *July 2016 to Present*

- **Technische Universität Dresden**, Saxony, Germany — *Semester Abroad 2020 (Jan - July)*

Delhi Public School Ghaziabad — *Ghaziabad, India*

AISSCE, 93.8% — *2013 to 2015*

St. Mary's Convent School — *Ghaziabad, India*

CISCE, 91.2% — *2004 to 2013*

Projects

Implementation of RISC-like processor with write-through cache controller

Course Project *Aug 2019 - Nov 2019*

- 32-bit, 4-stage pipelined processor with Fetch, Decode, multiple Execute, and Writeback stages
- Dynamic scheduling of instructions with Tomasulo's approach and LRU based write-through cache for data.

P^4 (Poly Potential Portable Potentiostat) *Closed-source*

Undergrad Research *Aug 2019 - Dec 2019*

- Worked with the MMNE group to build P^4, an approximate Poly-Potential Portable Potentiostat based on the LMP91000EVM to perform simple electrochemical analysis.
- P^4 supports common electroanalysis routines and reduces the cost of a typical spectro-photometer by about 15-20 times.

ECSP *Closed-source*

Undergrad Research *Jan 2019 - Apr 2019*

- Worked with the MMNE group to build ECSP, an intelligent colorimeter able to back-estimate the dominant absorption spectra of a solution with characteristic wavelengths in the visible light range.
- ECSP features a precision of 1 nm with a standard deviation of 2.3% and reduces the cost of a typical spectro-photometer by about 150 times.

Fault Tolerant Network on Chips *Open-source*

Undergrad Research *Aug 2018 – Dec 2018*

- Worked with Prof Soumya J to propose a new algorithm for fault-tolerant network on chips focusing on a packet-routing strategy for link faults between routers that occur either during manufacturing or in-operation. The algorithm decides the shortest path as well as takes care of distributing the load evenly across the network grid.
- Extended the algorithm for Mesh and Torus topologies for both, routers and link-level faults.

xBITS

Undergrad Research *Dec 2017 - Aug 2018*

- Worked with Dr. Suman Kapur to create a medical device that can diagnose UTI (Urinary Tract Infections) almost 15 times quicker than conventional laboratory methods.
- The device employs an array of colour sensors that predict the contents of the specimen according to RGB absorbance values and a trained model.

VMS *Open-source*

Independent Project *May 2018 - July 2018*

- Python utility to sync multiple devices playing the same video using MQTT which syncs timestamps instead of video frames, offering significantly less network usage.

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