AKHIL RAJ BARANWAL

website

EDUCATION

B.E. in Electronics and Instrumentation Jul 2016 – Aug 2020
Birla Institute of Technology and Science, Pilani

PUBLICATIONS

- **MemOReL: A Memory-oriented Optimization Approach to Reinforcement Learning on FPGA-based Embedded Systems** [doi]
  Proceedings of the 2021 on Great Lakes Symposium on VLSI. (Pages: 339–346) Jun 2021
- **Development of Completely Automated Poly Potential Portable Potentiostat** [doi]
  ECS Journal of Solid State Science and Technology. (Volume: 10, Number: 2) Feb 2021
- **ReLAccS: A Multi-level Approach to Accelerator Design for Reinforcement Learning on FPGA-based Systems** [doi]]
  IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. (Volume: 40, Issue: 9, Page(s): 1754-1767) Oct 2020

WORK EXPERIENCE

- **ASIC Design Engineer, Micron Technology** Aug 2020 – Present
  SoC verification of storage-controllers and post-silicon bringup.
- **Guest Researcher, CFAED - Technische Universität Dresden** Jan 2020 – Jun 2020
  Worked with the Chair for Processor Design, CFAED under the guidance of Dr. Akash Kumar and Dr. S Sahoo, exploring accelerator designs for traditional RL problems.
- **Embedded Engineering Intern** May 2019 – Jul 2019
  Worked on encrypted high speed memory-trace collection and analysis of DRAM AXI traffic in PetaLinux.
- **Engineering Intern** May 2018 – Jul 2018
  Developed a rule-based interface based on GSM for controlling industrial machines spread across an area of more than 1600 acres.

PROJECTS

- **Poly Potential Portable Potentiostat** Aug 2019 – Dec 2019
  While with the MMNE Lab, built an approximate potentiostat to perform simple electrochemical analysis. It works at a fraction of the power and reduces the cost of a typical bench-top potentiostat by about 18 times.
- **ECSP** Jan 2019 – May 2019
  Designed an approximate spectrophotometer under the guidance of Dr. Sanket Goel. ECSP reduces the cost of a typical spectrophotometer by about 150 times.
- **Fault Tolerant Network on Chips** Aug 2018 – Dec 2018
  Worked under the guidance of Dr. Soumya J to propose a new algorithm for fault-tolerant network on chips focusing on a packet-routing strategy for link faults between routers that occur either during manufacturing or in-operation. Developed an elementary NoC simulator in Python.
- **Detecting UTI infections** 2017 – 2018
  Worked with Dr. Suman Kapur to create a medical device that can diagnose UTI (Urinary Tract Infections) almost 15 times quicker than conventional laboratory methods.

EXTRACURRICULAR

- All open source projects available at github.com/arbaranwal
- Helping underprivileged kids with education at Nirmaan Organisation
- Mentoring and teaching undergraduate students on varying topics spanning from elementary electronics to computer architecture (2017–2019)
- Head, Automation and Robotics Club, BITS Pilani, Hyderabad (2018–2019)