Oxford College of Engineering and Management

Gaindakot-2 Nawalpur

Couse Title: CMP 332 Computer Architecture

Assignment

1. What is addressing modes? Explain various addressing modes.
2. Define Computer Architecture and what are the instructions used in IAS computer? Explain each in detail.
3. Differentiate between Computer Architecture and Computer Organization. What are instructions set design issues of CPU?
4. What is micro operation? Explain the logical and arithmetic micro operation with examples.
5. Define VHDL. Explain about shift micro operations in detail.
6. Describe the basic ALU with its functional block diagram and operational truth table.
7. Define Instruction Cycle. Explain the basic components used in processor organization.
8. What is data path? Explain design principles for modern system.
9. Explain about each state of instruction cycle.
10. Explain in detail instruction cycle state diagram.
11. Perform $x \times y$, where $x= (-7)_{10}$ and $y= (5)_{10}$. Consider a 4 bit registers and x and y is represented in 2's complement representation.
12. Perform $6 \div 4$ using unsigned division algorithm.
13. Briefly explain the functioning of micro-programmed control unit with necessary block diagram.
14. Explain hardwired and micro-programmed control unit with their uses.
15. Define micro-instruction Sequencing Techniques. What are the micro- instruction formats used in Intel-Pentium? Explain each in detail.
16. Differentiate between Hardwired Control Unit and Micro programmed Control unit. Explain Horizontal Microinstruction format.
17. Differentiate between direct and associative mapping for cache memory.
18. Define cache hit ratio. Describe cache Read operation with a flowchart.
19. What is memory hierarchy? Briefly describe the concept of RAID.
20. Explain the associative mapping technique in cache memory and compare it with set associative mapping.
21. Why replacement algorithm is used in set associative mapping? Explain.
22. What are the limitations of programmed I/O? How these are improved in interrupt driven I/O? And how the limitations of Interrupt driven I/O are improved by DMA?
23. Describe programmed I/O and Interrupt Driven I/O.
24. Why are external devices not connected directly with bus computer system? Draw an internal structure of I/O module.
25. Differentiate between RISC and CISC.

26. Assume that pipeline has K=8 segment and execute n=120 tasks in sequence. Let the time taken to process a sub-operation in each segment is 40s. calculate the speed up ratio in the pipeline.
27. What do you mean by register windows? Discuss how does it help to improve the performance of procedure calling?
28. What are the RISC instruction? Explain the various pipelining Hazards in instruction pipelining and its solution.
29. A non pipeline system takes 40ns to process a task. The same task can be processed in a six segment pipeline with clock cycle of 10ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speed that can be achieved?
30. What is Register Renaming? Explain the role of overlapped register window in RISC processor.
31. What do you mean by multiprocessors system? Describe flynn's classification with all types.
32. What is cache coherence? Explain hardware and software for Cache Coherence.
33. Define flynn's Taxonomy? Draw different interconnection structure of multiprocessor system and describe it with necessary diagram.
34. Explain the Dual Core and Quad core processors.
35. Explain the software performance issues of multi core computer.