Unit 3
Instruction Cycle

T-state

→ It is the time period of a single cycle of the clock frequency.

Machine Cycle

→ The number of T-states required performing a read or a write operation either from memory or I/O.

→ A machine cycle may consist of three to six T-states.

Instruction Cycle

→ It is the total number of machine cycles required to execute a complete instruction.

Machine Cycles of 8085 microprocessor

i) Op-code fetch cycle

→ The MP uses this cycle to take the op-code of an instruction from the memory location to processor.

→ The op-code is taken from memory and transferred to instruction register for decoding and execution.

→ The time required to complete this cycle is 4 to 6 T-states.

ii) Memory read cycle

→ The MP executes these cycles to read data from memory.

→ The address of memory location is given by instruction.

→ The time required to complete the memory read cycle is 3 T-states.

iii) Memory write cycle

→ The MP executes these cycles to write data to memory.

→ The address of memory is given by instructions.

→ The time required to complete the memory write cycle is 3 T-states.

iv) I/O read cycle

→ The MP executes these cycles to read data from I/O devices.

→ The address of I/O port is given by instruction.

→ The time required to complete the I/O read cycle is 3 T-states.

v) I/O write cycle

→ The MP executes these cycles to write data into I/O devices.

→ The address of I/O port is given by instruction.

→ The time required to complete the I/O write cycle is 3 T-states.

vi) Interrupt acknowledge cycle

→ In the response to interrupt request input **INTR**, the MP executes these cycles to get information from the interrupting devices.

→ The time required to complete this cycle is 3 T-states.

Fetch & Execute Operation: Timing Diagram

→ The graphical representation of status of various signals involved during a machine cycle with respect to time is called timing diagram.

→ This gives basic idea of what is happening in the system when the instruction is getting fetched and executed, at what instant which signal is getting activated.

→ The signals involved during machine cycle are CLK, $A_{15} – A_8$, $AD_7 – AD_0$, IO/M(bar), RD(bar), WR(bar) and S_1, S_0.

IO/M(bar)	S_1	S_0	Operation
0	0	0	Halt
0	0	1	Memory write
0	1	0	Memory read
0	1	1	Op-code fetch
1	0	1	IO write
1	1	0	IO read
1	1	1	Interrupt acknowledge

Timing diagram for op-code fetch cycle

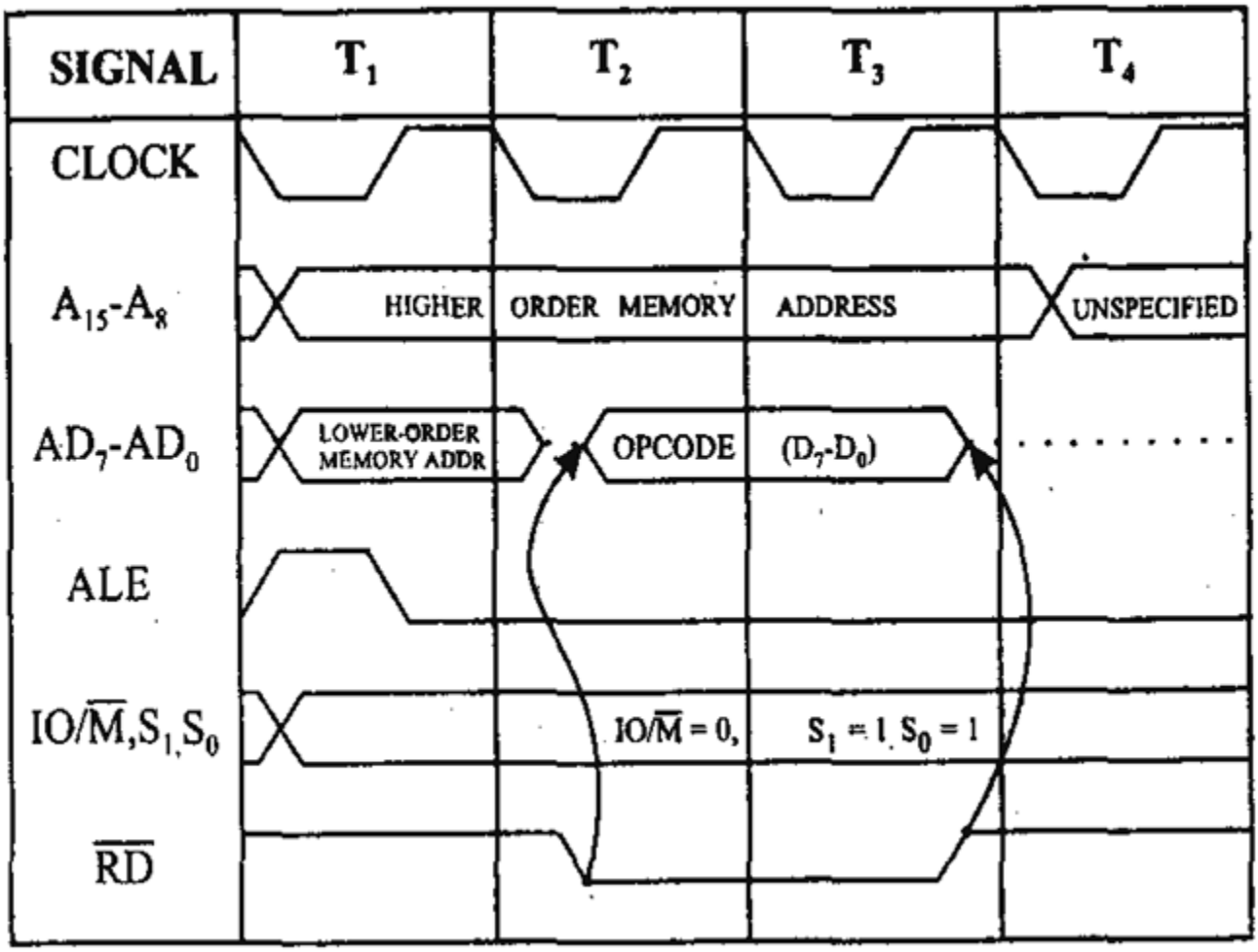

Fig: Timing Diagram for Op-code Fetch Machine Cycle

The op-code fetch timing diagram can be explained as below:

i) The MP places the 16-bit memory address from the program counter on address bus. At time period T_1, the higher order memory address is placed on the address lines $A_{15} – A_8$. When ALE is high, the lower address is placed on the bus $AD_7 – AD_0$. The status signal IO/M(bar) goes low indicating the memory operation and two status signals $S_1 = 1$, $S_0 = 1$ to indicate op-code fetch operation.

ii) At time period T_2, the MP sends RD(bar) control line to enable the memory read. When memory is enabled with RD(bar) signal, the op-code value from the addressed memory location is placed on the data bus with ALE low.

iii) The op-code value is reached at processor register during T_3 time period. When data (op-code value) is arrived, the RD(bar) signal goes high. It causes the bus to go into high impedance state.

iv) The op-code byte is placed in instruction decoder of MP and the op-code is decoded and executed. This happens during time period T_4.

Timing diagram for memory read cycle

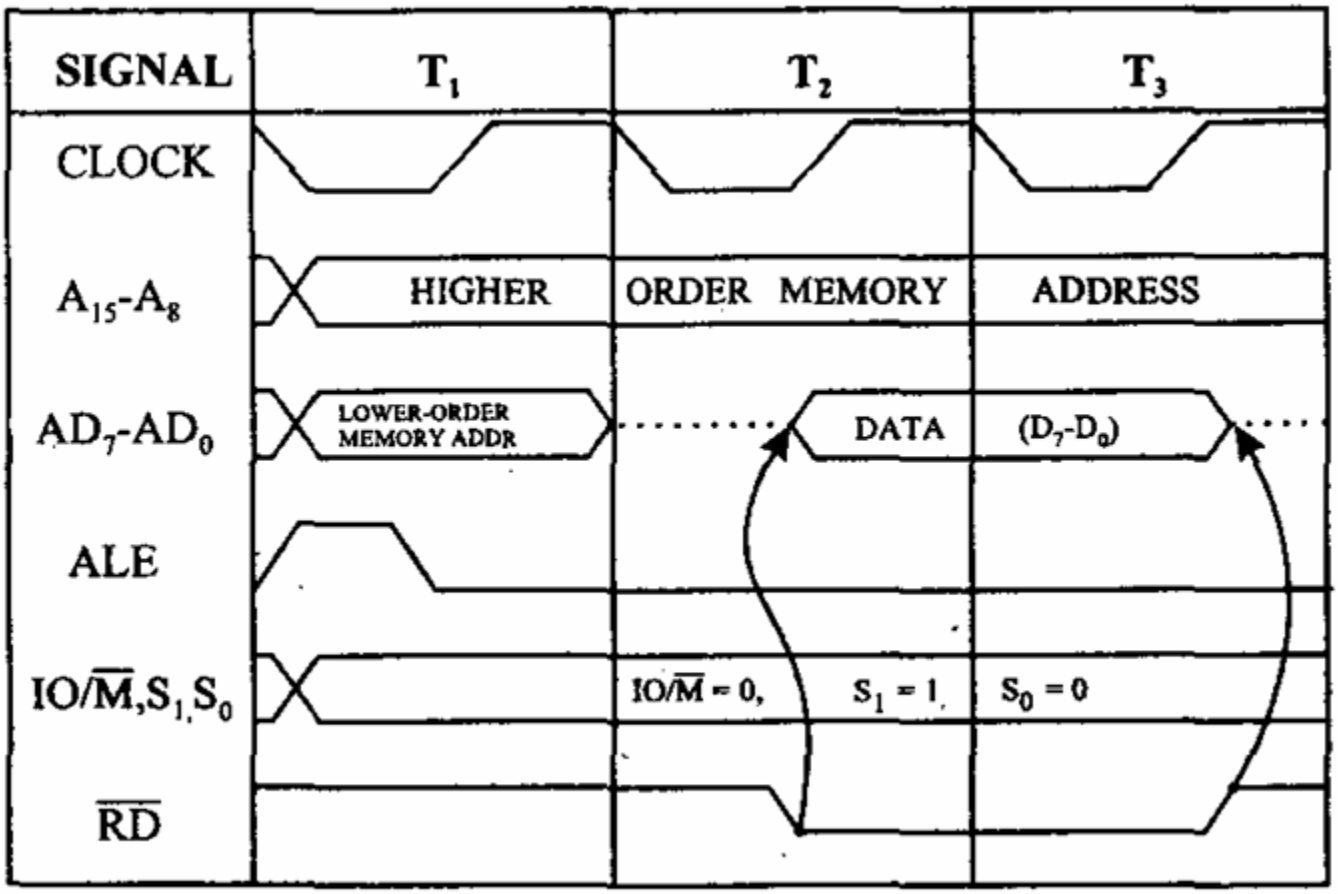

Fig: Timing Diagram for Memory Read Machine Cycle

The memory read timing diagram can be explained as below:

i) The MP places the 16-bit memory address from the program counter on address bus. At time period T_1, the higher order memory address is placed on the address lines $A_{15} – A_8$. When ALE is high, the lower address is placed on the bus $AD_7 – AD_0$. The status signal IO/M(bar) goes low indicating the memory operation and two status signals $S_1 = 1$, $S_0 = 0$ to indicate memory read operation.

ii) At time period T_2, the MP sends RD(bar) control line to enable the memory read. When memory is enabled with RD(bar) signal, the data from the addressed memory location is placed on the data bus with ALE low.

iii) The data is reached at processor register during T_3 state. When data is arrived, the RD(bar) signal goes high. It causes the bus to go into high impedance state.

Timing diagram for memory write cycle

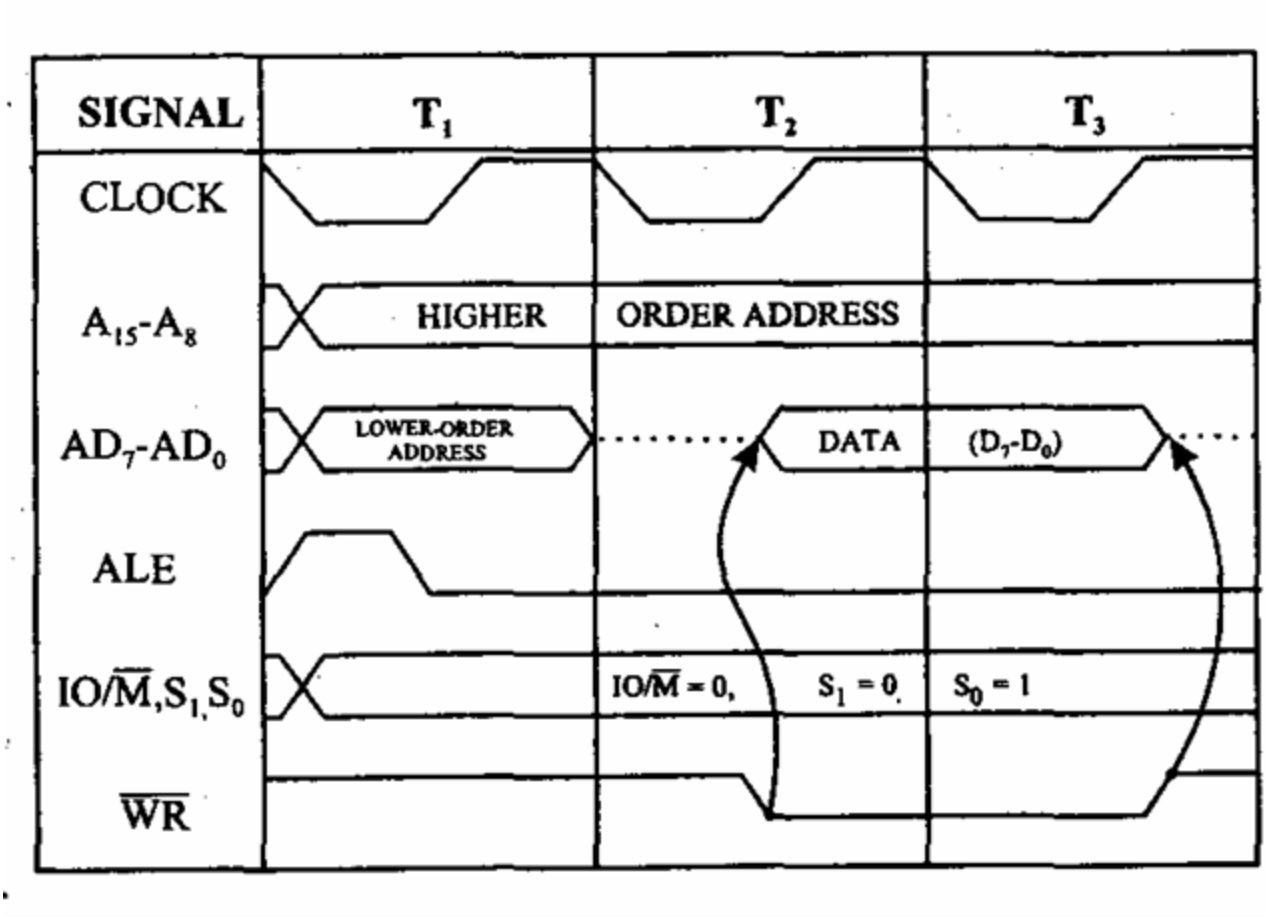

Fig: Timing Diagram for Memory Write Machine Cycle

The memory write timing diagram can be explained as below:

i) The MP places the 16-bit memory address from the program counter on address bus. At time period T_1, the higher order memory address is placed on the address lines $A_{15} – A_8$. When ALE is high, the lower address is placed on the bus $AD_7 – AD_0$. The status signal IO/M(bar) goes low indicating the memory operation and two status signals $S_1 = 0$, $S_0 = 1$ to indicate memory write operation.

ii) At time period T_2, the MP sends WR(bar) control line to enable the memory write. When memory is enabled with WR(bar) signal, the data from the processor is placed on the addressed location with ALE low.

iii) The data is reached at memory location during T_3 state. When data is reached, the WR(bar) signal goes high. It causes the bus to go into high impedance state.

Timing diagram for I/O read cycle

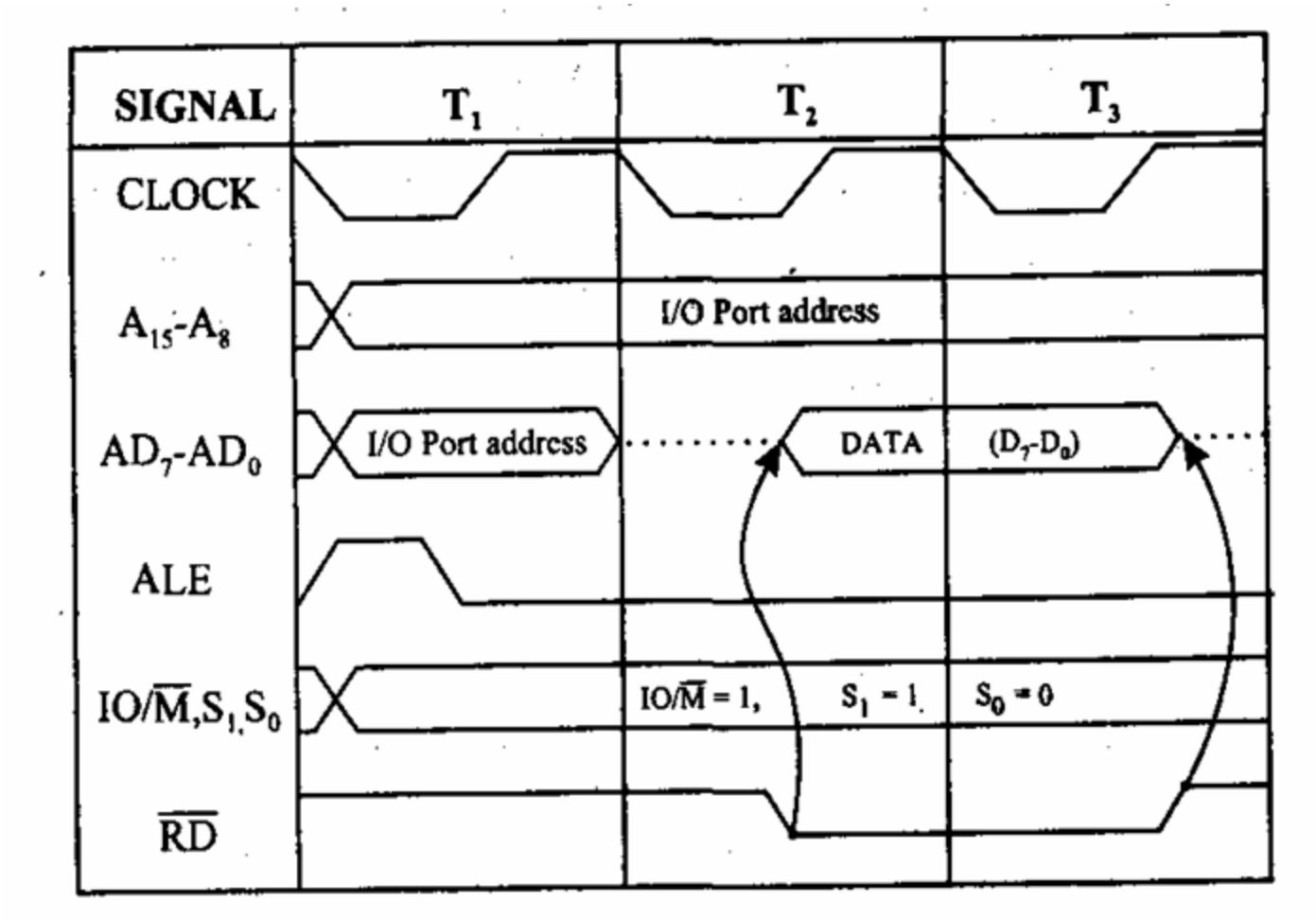

Fig: Timing Diagram for I/O Read Machine Cycle

Describe yourself.

Timing diagram for I/O write cycle

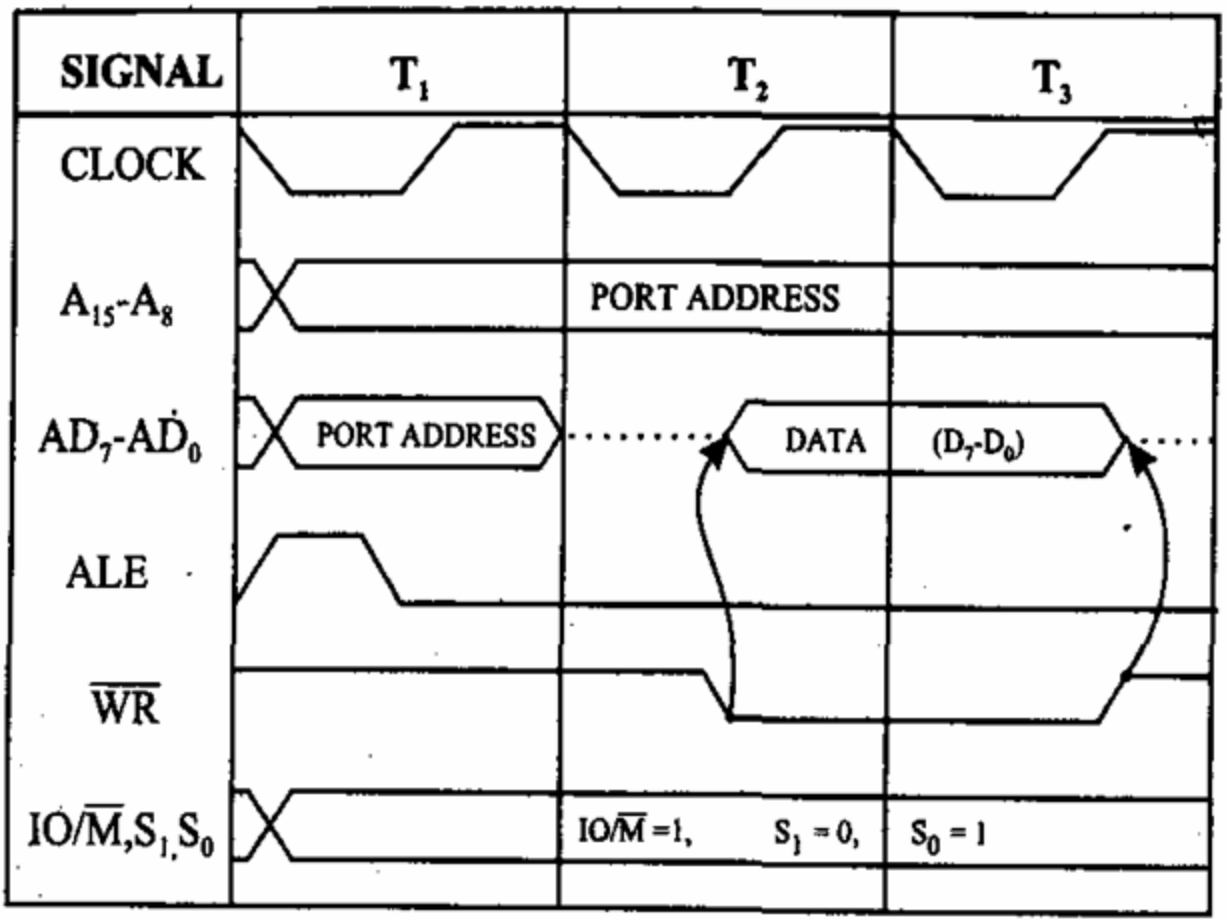

Fig: Timing Diagram for I/O Write Machine Cycle

Describe yourself.

Timing Diagram of MOV, MVI, IN, OUT, LDA, STA

i) MOV

E.g. MOV A, B

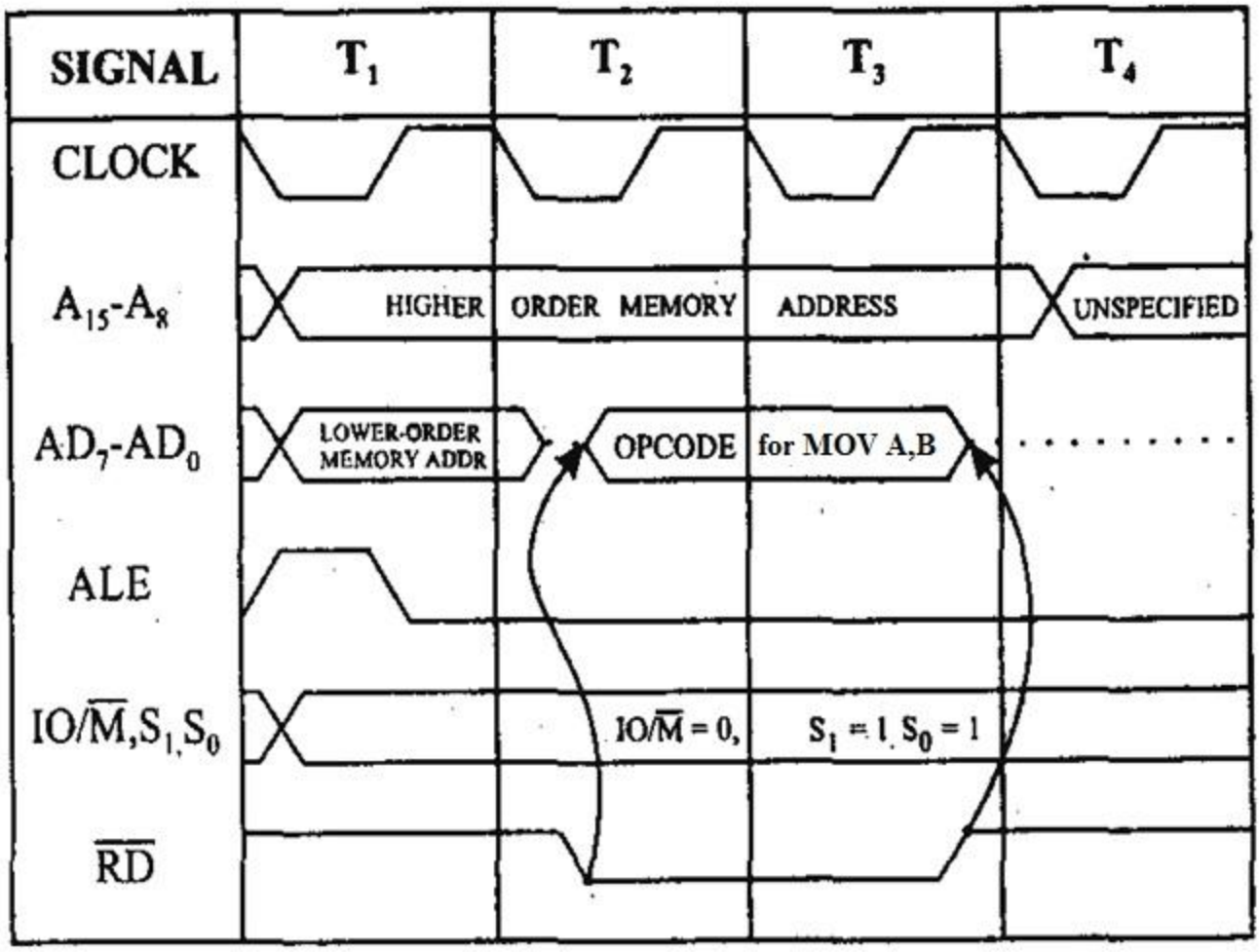

Fig: Timing Diagram for MOV A,B

ii) MVI

Timing diagram for MVI B, 43H

→ Fetching the Op-code 06H from the memory 2000H. (OF machine cycle)

→ Read (move) the data 43H from memory 2001H. (memory read)

Address	Mnemonics	Opcode
2000	MVI B, 43_H	06_H
2001		43_H

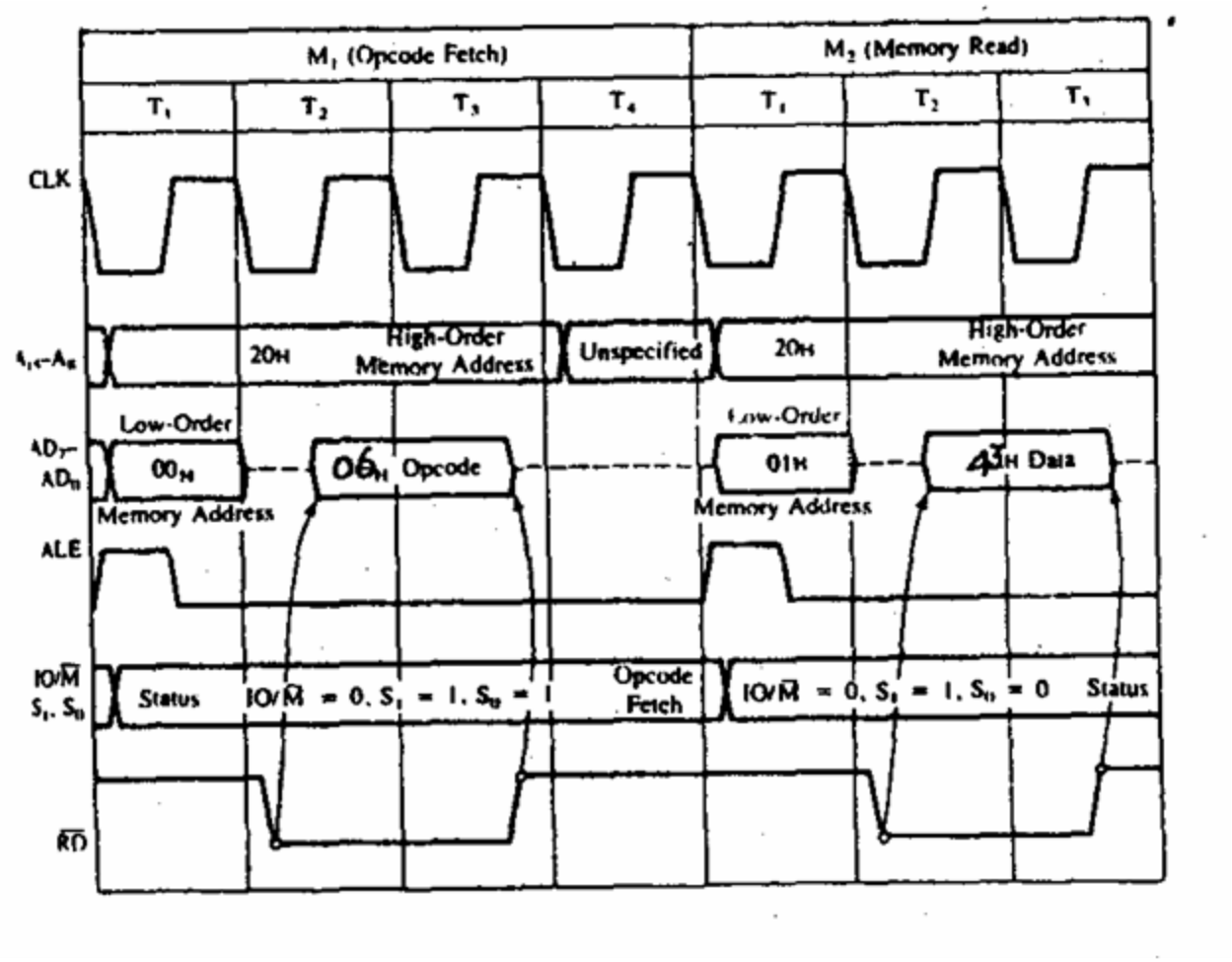

Fig: Timing Diagram for MVI B, 43H

iii) IN

Timing diagram for IN C0H

→ Fetching the Op-code DBH from the memory 4125H.

→ Read the port address C0H from 4126H.

→ Read the content of port C0H and send it to the accumulator.

→ Let the content of port is 5EH.

Address	Mnemonics	Opcode
4125	IN $C0_H$	DB_H
4126		$C0_H$

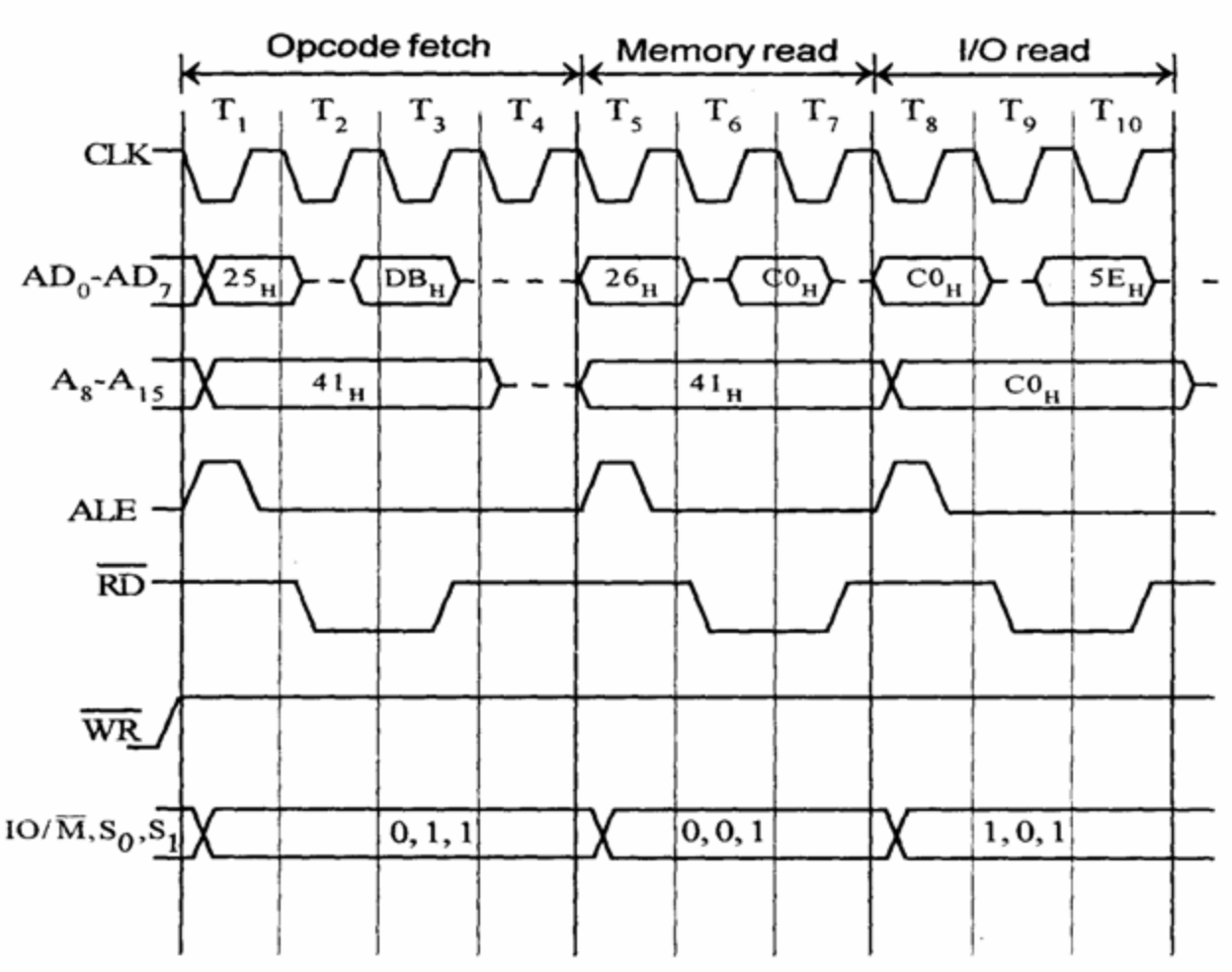

Fig: Timing Diagram for IN C0H

iv) OUT

E.g. OUT 07H

Do yourself.

v) LDA

E.g. LDA 2030H

Do yourself.

vi) STA

Timing diagram for STA 526AH

→ STA means Store Accumulator -The content of the accumulator is stored in the specified address (526A).

→ The op-code of the STA instruction is said to be 32H. It is fetched from the memory 41FFH (see fig). - OF machine cycle

→ Then the lower order memory address is read (6A). – Memory Read Machine Cycle

→ Read the higher order memory address (52).- Memory Read Machine Cycle

→ The combination of both the addresses is considered and the content from accumulator is written in 526A. – Memory Write Machine Cycle

→ Assume the memory address for the instruction and let the content of accumulator is C7H. So, C7H from accumulator is now stored in 526A

Address	Mnemonics	Opcode
4125	IN $C0_H$	DB_H
4126		$C0_H$

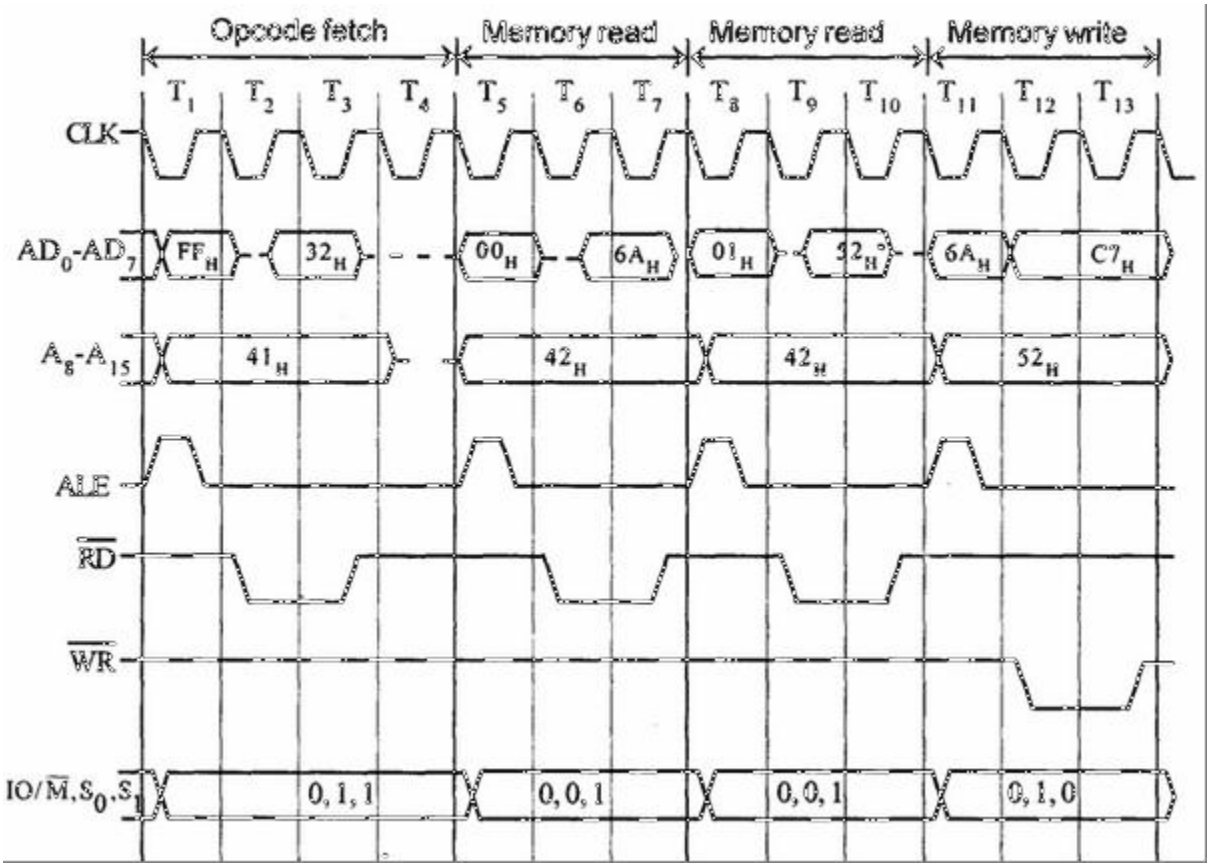

Fig: Timing Diagram for STA 526AH

Fetch and Execute Overlap

→ The instruction cycle consists fetching the instruction from memory called fetch cycle and decode & execute the instruction called execution cycle.

→ During the fetch, the instruction is read from the memory. During execution, instruction is decoded and then executed. Decoding of instruction need not to be referenced (i.e. memory reference).

→ So, during execution of instruction, there is a time that does not need memory. At that time, we can fetch the instruction from memory. This fetching of next instruction while execution of an instruction is known as fetch and execute overlap.