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Implementation of CORDIC-based Soft and Hard Demappers for a DVB-S2 Receiver

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***Abstract*—Soft-Decision demapping is of paramount importance for the FEC decoding subsystem of the DVB-S2 receiver achieving the near Shannon-limit performance claimed by the DVB-S2 standard. In the context of the receiver under development, the Hard-Decision Demapper generates hard-symbols for the Decision Feedback Equalizer used to overcome the nonlinearities caused by the satellites transponders. The main goal of the Demappers, in the DVB-S2 receiver project, is converting the received symbols into soft-bits, hard-bits or hard-symbols. The Soft and Hard-Decision Demappers implemented make use of the CORDIC algorithm to obtain module and phase information of the received baseband complex symbols. This work presents the functionality, the architecture, FPGA prototyping results, and VLSI logical and physical synthesis of both Demappers.**

I. Introduction

The Second Generation Digital Video Broadcasting System for Satellite broadcasting and unicasting (DVB-S2) has been consolidated as one of the most common choices regarding Digital TV (DTV). Under the same conditions, it achieves about 30% of capacity gain over its predecessor standard DVB-S. Due to its spectral efficiency, it is used as downlink for DVB-RCS2. DVB-S2 has been specified around three key concepts: best transmission performance, total flexibility and reasonable receiver complexity that allows different modulations and error protection levels to be used on a frame by frame basis [1]. It is able to cope with any existing satellite transponder characteristics, with a large variety of spectrum efficiencies and Carrier-to-Noise ratio (C/N) requirements.

The Demappers presented in this work are going to be integrated in a DVB-S2 receiver under development, to generate soft-decisions for the FEC decoding subsystem and hard-symbols for Decision Feedback Equalizer. Nevertheless, Hard Demapper can be also used for other applications, such as Decision-Directed Synchronization. In an early project stage the Hard Demapper was used to generate hard-bits for the first proof of concept of the DVB-S2 receiver presented in [2].

The remainder of the paper is organized as it follows: Sec. II describes the functionality of each demapper and the CORDIC algorithm. Sec. III details the implemented architectures. Sec. IV presents the implementation results. And Sec. V concludes the paper.

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II. System Description

This section is devoted to provide a system-level view of both Hard and Soft Demappers. The proposed Demappers architectures make use of CORDIC algorithm, so this block will be also introduced.

A. CORDIC

The CORDIC algorithm, introduced in [3], has several applications [4]. It is an iterative arithmetic computing algorithm capable of evaluating various elementary functions, as shown in Table I, using an unified shift-and-add approach.

TABLE I. Unified CORDIC Functions

Coordinates	Rotation	Vectoring
Circular	$x_n = K(x_0 \cos z_0 - y_0 \sin z_0)$	$x_n = K\sqrt{(x_0^2 + y_0^2)}$
	$y_n = K(y_0 \cos z_0 + x_0 \sin z_0)$	$y_n = 0$
	$z_n = 0$	$z_n = z_0 - \arctan\left(\frac{y_0}{x_0}\right)$
Linear	$x_n = x_0$	$x_n = x_0$
	$y_n = y_0 + x_0 z_0$	$y_n = 0$
	$z_n = 0$	$z_n = z_0 - \frac{y_0}{x_0}$
Hyperbolic	$x_n = K_h(x_0 \cosh z_0 + y_0 \sinh z_0)$	$x_n = K_h\sqrt{(x_0^2 - y_0^2)}$
	$y_n = K_h(y_0 \cosh z_0 + x_0 \sinh z_0)$	$y_n = 0$
	$z_n = 0$	$z_n = z_0 + arctanh\left(\frac{y_0}{x_0}\right)$

Due to its flexibility and low resources usage, CORDIC is an alternative architecture for implementation of several algorithms in DSP and VLSI that make use of elementary trigonometric functions and multiplication-accumulation operations. The basic concept of CORDIC is vector rotation by means of decomposing the desired rotation angle into the weighted sum of a set of n predefined elementary rotation angles (α_i). The rotation for each of the n angles can be accomplished by means of simple shift-and-add operations. The CORDIC algorithm is described in Eq. 1.

$$\begin{aligned} x_{n+1} &= x_n - m\sigma_n y_n 2^{-s(m,n)} \\ y_{n+1} &= y_n + \sigma_n x_n 2^{-s(m,n)} \\ z_{n+1} &= z_n - \sigma_n \alpha(n) \end{aligned} \tag{1}$$

Where,

$m = 1$	:	circular coordinate;
$m = -1$	:	hyperbolic coordinate;
$m = 0$	:	linear coordinate;
$s(m, i)$	:	is the shift factor;
σ_n	:	is the sign of z_n;
x_0, y_0 and z_0	:	are the input variables.

B. Hard Demapper

The main objective of the Hard-Decision Demapper (HD) is to convert complex baseband symbols into bit streams. It adopts different methods for each modulation. Nevertheless, all the methods basically consist on checking if the received complex symbol lies within a specific decision region around a given constellation point. Fig. 1 presents three examples of those regions, for 8-PSK, 16-APSK and 32-APSK. As matter of simplicity, the DVB-S2 baseband modulation constellations, presented in [1], are not reproduced here.

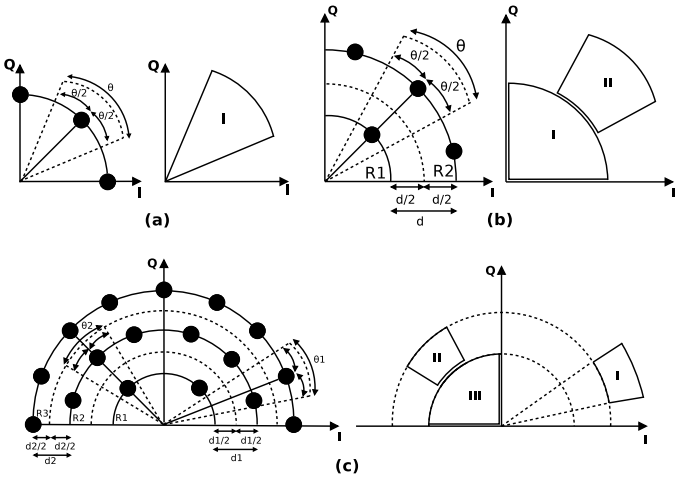


Fig. 1. Decision Regions of (a) 8-PSK, (b) 16-APSK and (c) 32-APSK

For QPSK modulation, the signs (positive or negative) of in-phase (I) and quadrature (Q) components of the received complex signals are analyzed, obtaining their respective quadrants, so, hard-bits or hard-symbols can be obtained.

Given three adjacent symbols, the decision regions of 8-PSK are defined as the region delimited by two bisectors of each adjacent pair of symbols, as can be seen in Fig. 1(a).

In the case of 16-APSK, the decision regions are defined for two cases. The first takes into account the bisectors of two pairs of adjacent symbols placed in the outer constellation radius, R2, as well as an imaginary circle equally distant of R2 and the inner constellation circle, R1. An example of that decision region is area II in Fig. 1(b). For the second case, the decision regions are defined for the received symbols that have module smaller than the imaginary circle between R1 and R2. In this case, the hard-decisions are done by checking in which quadrant the received symbol lies in. Area I in Fig. 1(b) is an example of that.

Based on the previous explanations, it is straightforward to derive the decision regions for the 32-APSK. Nevertheless it is worth to mention that this modulation has three radii in its constellation, as can be seen in Fig. 1(c).

C. Soft Demapper

Instead of providing hard-bits, the Soft-Decision Demapper (SD) delivers an extra number of bits per bit of the symbol constellation, i.e., the soft-bits. The soft-decision is essential for the DVB-S2 Forward Error Correction (FEC) system achieve quasi-error-free performance near Shannon-limit [5].

A widespread soft-decision computation method is the so called Log-Likelihood Rate (LLR). However, this method uses exponential and logarithm operations that increases hardware complexity to obtain soft-bits. To reduce the complexity, various SD methods have been proposed, being MAX the most used method. Even not using exponential and logarithm operations, its complexity is considerably large regarding the one adopted in this work.

The implementation presented here is based on different reference methods for each modulation, which were derived from MAX method seeking a lower hardware complexity. QPSK SD uses the method presented in [6]. 8-PSK SD is a slightly modified version of the solution proposed in [6]. 16-APSK SD is based in the decision regions presented in [7], but with others LLR equations derived in this work. Until the moment, 32-APSK SD has not been implemented.

In general, the LLRs are computed based on I&Q component values, the estimated noise variance (σ^2), and a set of constants, as shown in Eq. 2. For higher order modulations, the most significant LLRs are obtained by using other methods. The quantized LLRs are the soft-bits.

$$L(b) = (K_1 I + K_2 Q)/\sigma^2 \tag{2}$$

For b_0 and b_1 of QPSK modulation, the constant pair (K_2, K_1) are respectively set as ($\sqrt{2}$, 0) and (0, $\sqrt{2}$).

8-PSK SD case provides three soft-bits, b_0, b_1 and b_2. For b_0 and b_1, the input symbols are rotated by $-\pi/8$, generating I_r and Q_r. They are used in Eq.2 with the same constants of QPSK SD. For b_2, I and Q are used in the Eq. 2, and constants are selected according to Table II.

TABLE II. COEFFICIENTS FOR EQ.2 FOR 8-PSK

Decision Region	K_1	K_2
$I \geq 0, Q \geq 0$	0.707	-0.293
$I < 0, Q \geq 0$	-0.293	-0.707
$I < 0, Q < 0$	-0.707	0.293
$I \geq 0, Q < 0$	0.293	0.707

Finally, for 16-APSK modulation, the third and the fourth soft-bits are calculated according to the equations presented in Table III. The complex symbol components, depending on θ (I_θ and Q_θ), are the remapped symbol components, i.e. $|I|$ and $|Q|$, rotated by $\theta_{ref} - \theta$. Where $|\cdot|$, is the module operation. It is worth to mention that the input symbols are remapped to the first quadrant to take advantage of the symmetry, and all the reference values are defined by the boundaries of the decision regions in this quadrant.

TABLE III. EQUATIONS FOR BITS 2 AND 3 OF 16-APSK

Decision region	Equation
$R < R_{ref}, \theta \geq \theta_{ref}$	$(R - R_{ref})/\sigma^2$
$R < R_{ref}, \theta < \theta_{ref}$	$-\max(\lvert\,\lvert I\rvert - I_{ref}\,\rvert, \lvert\,\lvert Q\rvert - Q_{ref}\,\rvert)/\sigma^2$
$R \geq R_{ref}, \theta < \theta_{ref}$	$-\max(\lvert\,\lvert I\rvert - I_{\theta}\,\rvert, \lvert\,\lvert Q\rvert - Q_{\theta}\,\rvert)/\sigma^2$
$R \geq R_{ref}, \theta \geq \theta_{ref}$	$\min(R - R_{ref}, \max(\lvert\,\lvert I\rvert - I_{\theta}\,\rvert, \lvert\,\lvert Q\rvert - Q_{\theta}\,\rvert))/\sigma^2$

III. Proposed Architecture

A. CORDIC

The implementation of the CORDIC described in Sec.III-A is an iterative hardware, which is structured as a cell array integrated in one block. This block can operate in one of the operation modes and coordinates shown in Table I. The number of iterations and precision are configurable.

The CORDIC iteration cell is made of 3 add-sub, 1 mux, 3 registers and 2 wired shift blocks, as detailed in the Fig. 2. The number of cells, n, is defined by the iteration parameter, which is, usually, equals or less than the width of the input signals. In order to obtain a -π to +π coverage range, a special cell of $\pi/2$ is inserted in the first iteration, which differs of others iterations by not having any shifter. Due the iterative approach of the CORDIC, the first valid computed value at the CORDIC output has a initial latency that depends on n. For instance, assuming that n is 14, the result will be delayed $14 + 1$ clock cycles. The advantages of these approach are the short critical path in each cell and a higher throughput, since the CORDIC block can be feed with new entries on each new clock cycle.

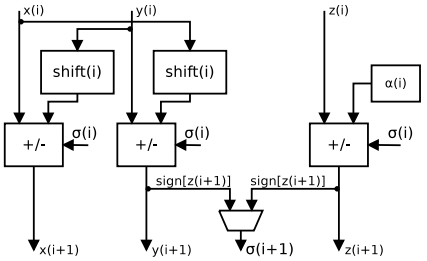


Fig. 2. Structure of a CORDIC iteration and its equations

B. Hard Demapper

The HD is implemented as a set of comparisons depending on the decision regions, which are defined by the modulation type. Fig. 3 shows the HD architecture.

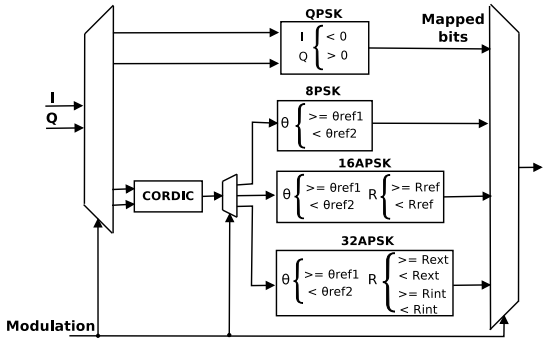


Fig. 3. Hard Demapper Architecture

When working in QPSK mode, the signs of the I&Q components define the symbol quadrant. Each quadrant is related to a specific pair of hard-bits. The analysis, in 8-PSK modulation, is done with the angle θ calculated by the CORDIC. The computed angle is compared to a group of reference angle intervals, related to each constellation symbols, so the three hard-bits can be defined. In the 16-APSK mode, besides the angle, the radius, R, of the symbol, is also computed by the CORDIC and compared to stored reference values. With this information in hand is possible to define the correct hard-bits. Similar to 16-APSK, the 32-APSK HD analyses radius and the angle calculated by the CORDIC. The difference is the existence of two groups of reference angles, θ_1 and θ_2, based on internal and external radius, R_1 and R_2.

The CORDIC is instantiated in circular coordinate and vectoring mode operation, as described in Table I.

C. Soft Demapper

The SD instantiates a sub-block to each mode to obtain the LLRs according to the formulas and methods presented in Sec. II. The structure called LLR Calc (LLR Calculator), formed by a sum and three multipliers implements the Eq. 2.

The microarchitecture of the QPSK SD is illustrated in Fig. 4(a). As it can be seen, each LLR Calc adopts only one K, due to simplifications in Eq. 2. In this way, one multiplier and the sum are discarded. The value of the remaining constant K is $\sqrt{2}$, as already mentioned in Sec. III-C.

Fig. 4(b) presents the microarchitecture of the 8-PSK SD. This structure brings two new elements: the Rotate Symbol and a LUT. The LUT stores K_1 and K_2, both applied to compute the LLR of b_2, and the Rotate Symbol performs a rotation in order to reuse the QPSK microarchitecture for b_0 ad b_1 . K_1 and K_2 values are in Table II.

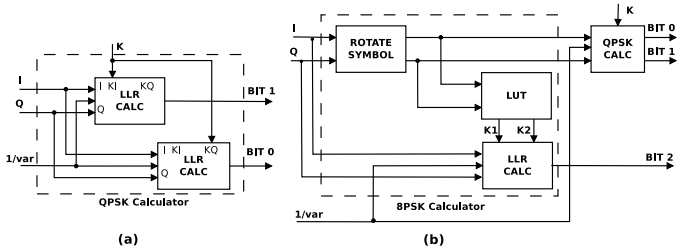


Fig. 4. Microarchitecture of (a) QPSK and (b) 8-PSK Soft Demappers

The soft-bits, b_1 and b_0, of the 16-APSK SD, are obtained using QPSK microarchitecture. The other soft-bits, i.e. b_2 and b_3, are calculated using the 16-APSK Bit Calc (16-APSK Bit Calculator) block, presented in Fig. 5. The Absolute Symbol block provides the remapped symbol mentioned in Sec. III-C. As in Sec. III-B, the CORDIC provides the θ and R, which are used to define the decision regions where the received symbol lays in. Next, it is chosen between (I_{ref}, Q_{ref}) or (I_θ, Q_θ) components, which pair is used to computed the Chessboard distance from the remapped symbol. I_θ and Q_θ are provided by the Symbol Adjustment. Also, after the definition of the decision region, the 16-APSK LLR Calc (16-APSK LLR Calculator) performs one of the Table III operations. The difference between the structures used to compute b_2 and b_3 is the reference values adopted, that change due to symmetry. The Absolute Symbol, the Symbol Adjustment and the CORDIC were reused in order to reduce hardware complexity. Each operation in SD was implemented using pipeline stages aiming at to achieve a higher throughput.

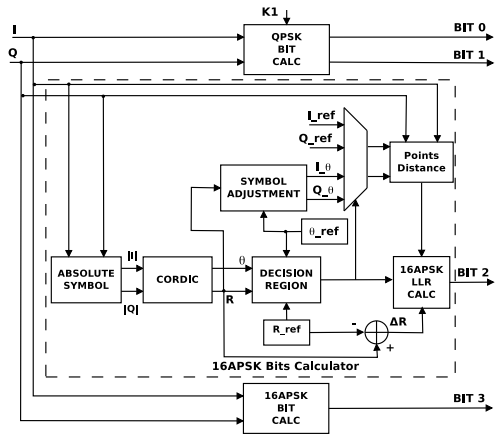


Fig. 5. Microarchitecture of 16-PSK Soft Demapper

IV. Implementation Results

The HD and SD were implemented using the architecture defined in Sec. III. A golden model was created, using GNU Octave high-level interpreted language, to validate the functionality of the VHDL codes. The validated VHDL codes were prototyped in FPGA (Stratix IV GX). The prototyping results are presented in the Table IV. According to the obtained results, the maximum frequencies that the SD and HD can operate are 111.54 MHz and 110.07 MHz, respectively.

TABLE IV. FPGA prototyping results for Altera's Stratix IV

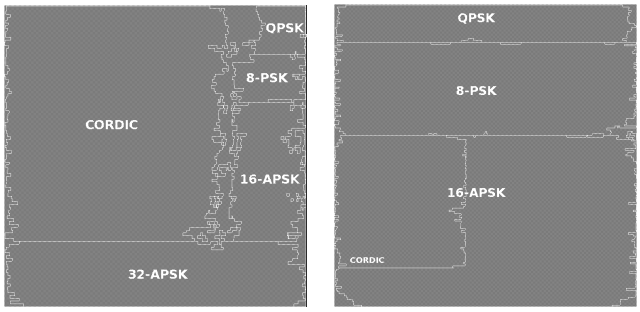
Module	Combinational ALUTs HD/SD	Memory ALUTs HD/SD	Registers HD/SD	Memory Bits HD/SD	DSP (18-bits) HD/SD
QPSK	44/283	0/0	34/74	0/0	0/4
8PSK	68/768	0/0	35/308	0/0	0/10
16-APSK	106/2028	0/2	49/1 657	0/1088	0/8
32-APSK	179/-	0/-	60/-	0/-	0/-
CORDIC	1 031/927*	16/0	834/811*	0/0	0/0
Total	1 905/3 224	16/2	1 327/2 039	0/1088	0/22

The HD and the SD were logically synthesized with the Encounter RTL Compiler, [8], using a 65 *nm* HVT library from Global Foundries working in 1.08 V at 62.5 *MHz*. The back-end was only carried on with the base clock frequency, since it was the one relevant in our project. Table V shows the cells usage for each block of HD and SD, including glue logic. It is important to note that the CORDIC is a internal block in 16-APSK SD microarchitecture so its cells are included in the final amount of the SD cells(*).

TABLE V. Logical synthesis results for $65nm$ CMOS

	Hard Demapper		Soft Demapper	
Module	**Cells**	**Area (μm^2)**	**Cells**	**Area (μm^2)**
QPSK	120	708	2 630	10 628
8-PSK	271	796	6 806	30 371
16-APSK	1 031	2 391	15 065	91 537
32-APSK	2 225	5 105	—	—
CORDIC	4 282	28 084	4 282*	28 080*
Total	9 410	45 112	24 698	132 919

The results of physical synthesis is showed in the Table VI. The back-end *amoeba* view of both blocks is in Fig. 6, where the Fig. 6(a) presents the HD and the Fig. 6(b) the SD.



(a) Hard Demapper (b) Soft Demapper

Fig. 6. Back-end amoeba view

TABLE VI. Physical synthesis results for $65nm$ CMOS

Demapper	Gates	Dimensions (μm)	Area (μm^2)	Density (%)	Power (mW)
Hard	22 944	170 × 170	28 900	76.215	0.7102
Soft	61 857	290 × 290	84 100	70.610	4.007

V. Conclusion

This paper presents the implementation of a Hard-Decision Demapper and a Soft-Decision Demapper, using CORDIC to obtain the angle and radius of the input symbols in a mapping constellation. Both Demappers were prototyped in FPGA. Logical and physical synthesis were also performed targeting the Global Foundry 65 *nm* technology. The results achieved show that SD uses a larger area and power consumption than HD. Both are justified by the soft-bits. In this work each soft-bit is represented by six bits and the symbols by sixteen bits.

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