Considerare la seguente architectura MIPS64:

|  |  |  |
| --- | --- | --- |
| * + Integer ALU: 1 clock cycle   + Data memory: 1 clock cycle   + FP multiplier unit: pipelined 7 stages | * + FP arithmetic unit: pipelined 2 stages   + FP divider unit: not pipelined unit that requires 8 clock cycles   + branch delay slot: 1 clock cycle, and the branch delay slot disabled | * + forwarding enabled   + è possibile completare lo stage EXE di una istruzione in modo out-of-order. |

* Facendo riferimento al frammento di codice riportato, si mostrino le tempistiche relative all’esecuzione ciascuna istruzione e si calcoli il numero totale di clock cycles necessari per eseguire completamente il programma:

for (i = 0; i < 100; i++) {

v5[i] = ((v1[i]/v2[i]) + v3[i]);

v6[i] = ((v3[i]/v4[i]) + v1[i]\*v2[i]);}

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| .data |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Clock  cycles |
| daddui r1, r0, 0x7 | F | D | E | M | W |  |  |  |  |  |  | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| daddu r2, r0, r0 |  | F | D | E | M | W |  |  |  |  |  | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| j check |  |  | F | D | E | M | W |  |  |  |  | 1 |  |  |  | C’è anche la parte di check che prende 3 | | | | | | | | | | | | | | | | |  |  |  |  |  |  |  |  |
| **loop:** lb r3, a(r2) |  |  |  | F | - | - | - | - |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 7 |  |  |  |  |  |  |  |  |  |  |  |  |
| lb r4, b(r2) |  |  |  |  | F | D | E | M | w |  |  | 2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| daddu r6, r0, r0 |  |  |  |  |  | F | D | E | M | W |  |  | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **is\_odd**: andi r5, r4, 0x1 |  |  |  |  |  |  | F | D | E | M | W |  |  | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| bnez r5, add\_odd |  |  |  |  |  |  |  | F | S | D | E | M | W |  | 2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **Cont**: dsll r3, r3, 0x1 |  |  |  |  |  |  |  |  |  | F | - | - | - | - |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **Add**: dadd r6, r6, r3 |  |  |  |  |  |  |  |  |  |  | F | D | E | M | W |  | 2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| J cont |  |  |  |  |  |  |  |  |  |  |  | F | D | E | M | W |  |  |  |  |  |  |  | 4 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  | F | - | - | - | - |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **Cont**: dsll r3, r3, 0x1 |  |  |  |  |  |  |  |  |  |  |  |  |  | F | D | E | M | W |  | 2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| dsrl r4, r4, 0x1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | F | D | E | M | W |  | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| bnez r4, is\_odd |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | F | - | D | E | M | W | 2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | F | - | - | - | - |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| sb r6, res(r2) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | F | D | E | M | W | 2 |  |  |  |  |  |  |  |  |  | | |  | | |  |  |
| daddui r2, r2, 0x1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | F | D | E | M | W |  | 1 |  |  |  |  |  |  | | |  | | | | |  |
| Ch: bne r2, r1, loo |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | F | - | D | E | M | W | 2 |  |  |  |  |  |  |  |  |  |  |  |  |  |
| j end\_loop |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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|  | 6 + 7\*(6+2\*(1+2+2+2+1+2) + 2\*(1+2+1+1+2)) + 4= 290 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 3306 |
|  |  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |  |
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Considerando il programma precedente, lo si ottimizzi in modo da eliminare per quanto possibile gli stalli del programma usando le tecniche note come rescheduling e register renaming. Si calcoli il tempo di esecuzione del nuovo programma nella stessa architettura evidenziando il miglioramento ottenuto.

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| .data |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Clock  cycles |
|  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| **is\_odd**: andi r5, r4, 0x1 |  |  |  | |  |  |  | F | D | E | M | W |  |  | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| bnez r5, add\_odd |  |  |  | |  |  |  |  | F | S | D | E | M | W |  | 2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **Cont**: dsll r3, r3, 0x1 |  |  |  | |  |  |  |  |  |  | F | D | E | M | W |  | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| dsrl r4, r4, 0x1 |  |  |  | |  |  |  |  |  |  |  | F | D | E | M | W |  | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 5 |
| bnez r4, is\_odd |  |  |  | |  |  |  |  |  |  |  |  | F | - | D | E | M | W |  |  | 2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 |
|  |  |  |  | |  |  |  |  |  |  |  |  |  |  | F | - | - | - | - |  |  | **2** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 |
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|  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | **2** |
|  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 |
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|  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 |
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|  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 |
|  | **Speedup hamdal = 1.2X ----** 3206/**2706 = 1.2X** | | | | | | | | | | | | | | | | | | | **Speedup = 1.4X 🡪 fraction (9+9)\*100/3206 = 0.56** | | | | | | | | | | | | | | | | | |  |
| Total |  | | |