02LQD Specification and Simulation of Digital Systems

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1. Combinational circuit design

The proposed solution makes use of if then else and case when constructs in two different architectures. In both case, under direct condition of the if statement or the case one, only cases when there is only a 1 in the 'm' input and A = 0 are specified. Other cases set A = 1.
The all-0 input is considered as don't care because supposed to never happen (there is at least a guard in the museum). A test bench is included to test the output behavior.

There are no differences w.r.t. the handed solution.

2. FSM design

The proposed solution is based on a Mealy FSM with 5 states, where the initial state is the so called "C", that work as a init state. The FSM is supposed to work starting with at least three zeros as input after reset, as described in the specifications, otherwise the output behavior will be not correct for the first 3 clock cycles.

The test bench included with this report is written in VHDL and can test both the Verilog version and the VHDL version of the solution. It includes a self-test code that makes use of a 4-bit shift register. Each input is shifted inside this register at each clock period. Assertions are used to compare the expected z output with the z output of the device under test.

There are no differences w.r.t. the handed solution.

3. HLSM design

The proposed solution is based on a Moore HLSM with 4 states, where the initial state is the so called "wait_start". The middle one, "check", is used to handle correctly the case where n = 0. A test bench is included to test the output behavior.

The only difference w.r.t. the handed solution is the size of the output (and the size of internal registers R0 and R1 of course). In the handed solution I wrote that only 13 bits are needed, instead we need 14 bits to represent correctly the 16^{th} number of the Jacobsthal series (the output was correct until the 15^{th} number).