

02LQD Specification and Simulation of Digital Systems

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1. Combinational circuit design (2 points)

The proposed solution makes use of if then else and case when constructs in two different architectures. In both case, under direct condition of the if statement or the case one, only cases when there is only a 1 in the 'm' input and $A = 0$ are specified. Other cases set $A = 1$.

There are no differences w.r.t. the handed solution.

2. FSM design (16 points)

The proposed solution is based on a Mealy FSM with 5 states, where the initial state is the so called "C". The FSM is supposed to work starting with at least three zeros as input as described in the specifications, otherwise the output behavior will be not correct for the first 3 clock cycles.

There are no differences w.r.t. the handed solution.

3. HLSM design (12 points)

The proposed solution is based on a Moore FSM with 4 states, where the initial state is the so called "wait_start". The middle one, "check", is used to handle correctly the case where $n = 0$.

The only difference w.r.t. the handed solution is the size of the output (and the size of internal registers R0 and R1 of course). In the handed solution I wrote that only 13 bits are needed, instead we need 14 bit to represent correctly the 16th number of the Jacobsthal series.