UNIT 2

The 8086 Microprocessor: Architecture, Register organization, 8086 signal description, Physical memory organization, Minimum and Maximum mode system and timing diagrams, Addressing modes, 8086 Instruction Set and Assembler Directives, Assembly Language example programs,

Stack structure of 8086, Interrupt structure of 8086, Interrupt vector table, Procedures and macros.

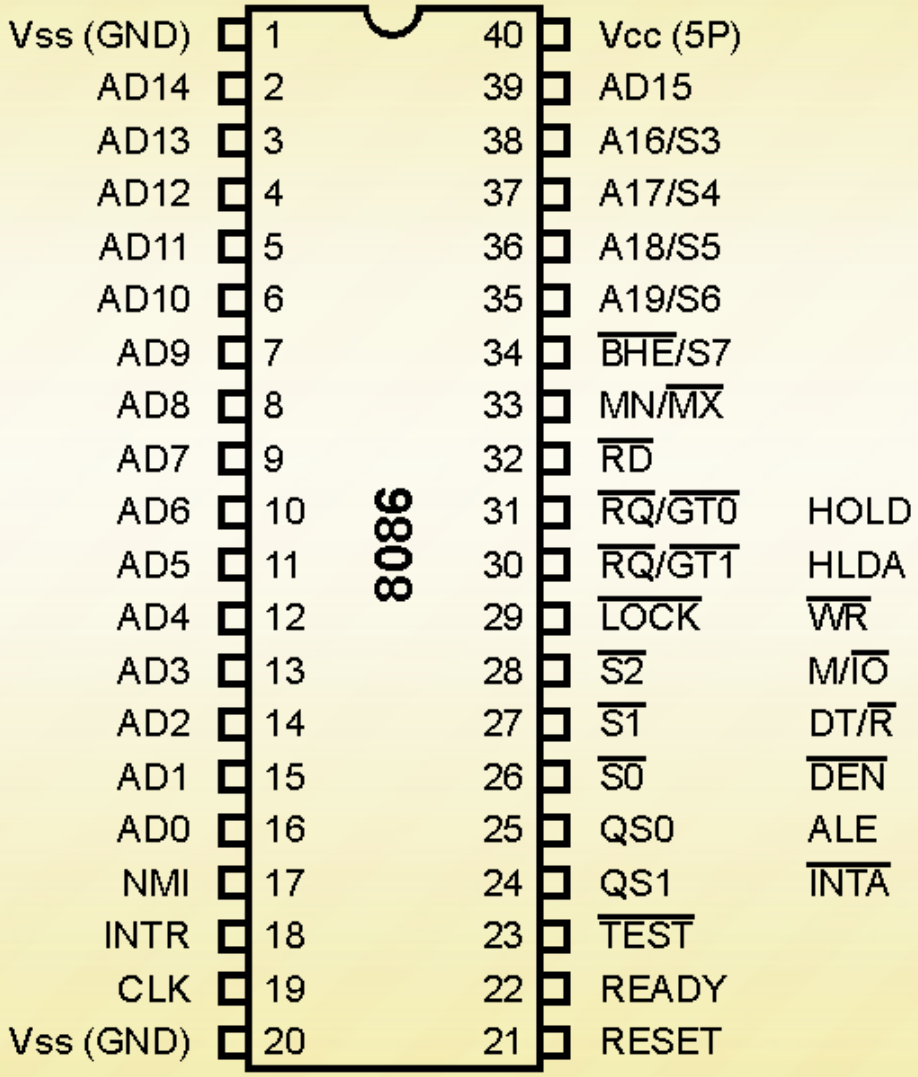
Intel 8086

- Intel 8086 was launched in 1978.
- It was the first 16-bit microprocessor.
- This microprocessor had major improvement over the execution speed of 8085.
- It is available as 40-pin Dual-Inline-Package (DIP).

Intel 8086

- It is available in three versions:
  - 8086 (5 MHz)
  - 8086-2 (8 MHz)
  - 8086-1 (10 MHz)
- It consists of 29,000 transistors.

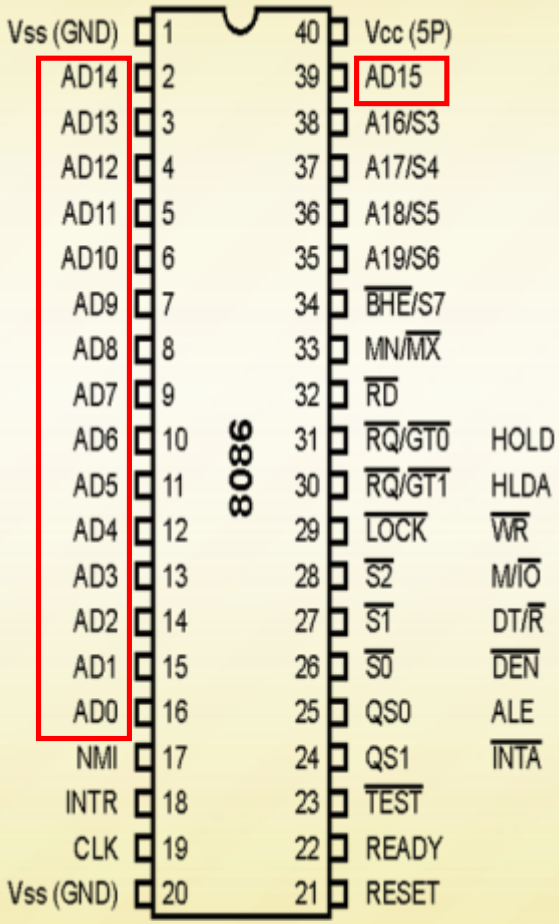
Pin Diagram of Intel 8086



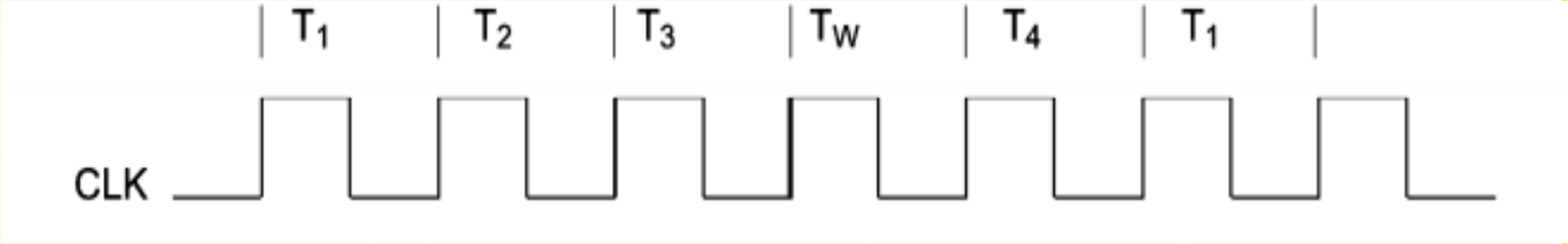
$AD_0 - AD_{15}$

Pin 16-2, 39 (Bi-directional)

- These lines are multiplexed bi-directional address/data bus.
- During T_1, they carry lower order 16-bit address.
- In the remaining clock cycles, they carry 16-bit data.
- AD_0-AD_7 carry lower order byte of data.
- AD_8-AD_{15} carry higher order byte of data.



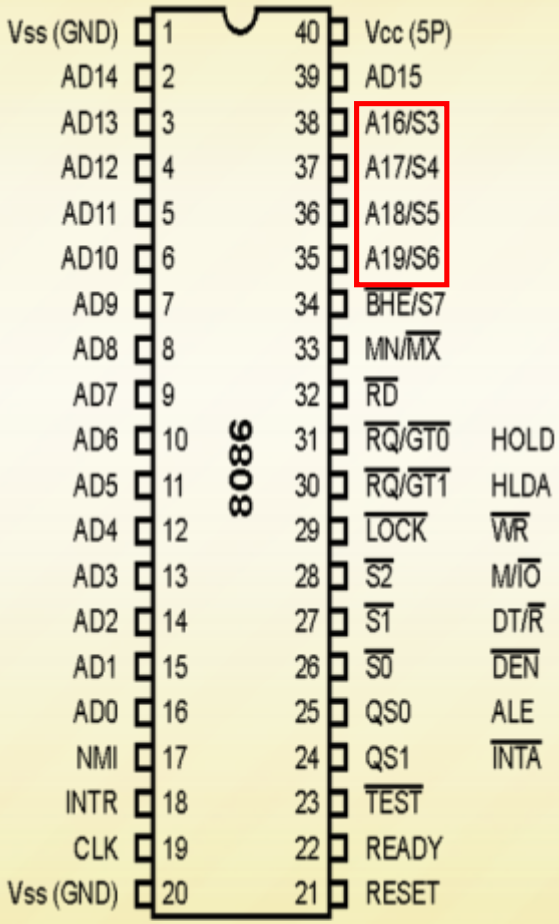
One machine cycle/Bus cycle



A_{19}/S_6, A_{18}/S_5, A_{17}/S_4, A_{16}/S_3

Pin 35-38 (Unidirectional)

- These lines are multiplexed unidirectional address and status bus.
- During T_1, they carry higher order 4-bit address.
- In the remaining clock cycles, they carry status signals.



S6: Logic 0.

S5: Indicates condition of IF flag bits.

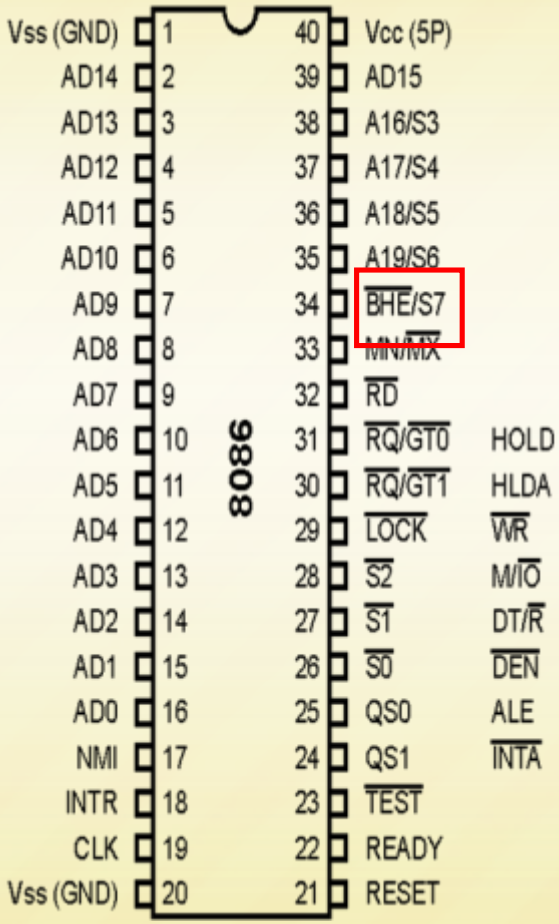
S4-S3: Indicate which segment is accessed during current bus cycle:

S4	S3	*Function*
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment

$\overline{BHE}$ / S_7

Pin 34 (Output)

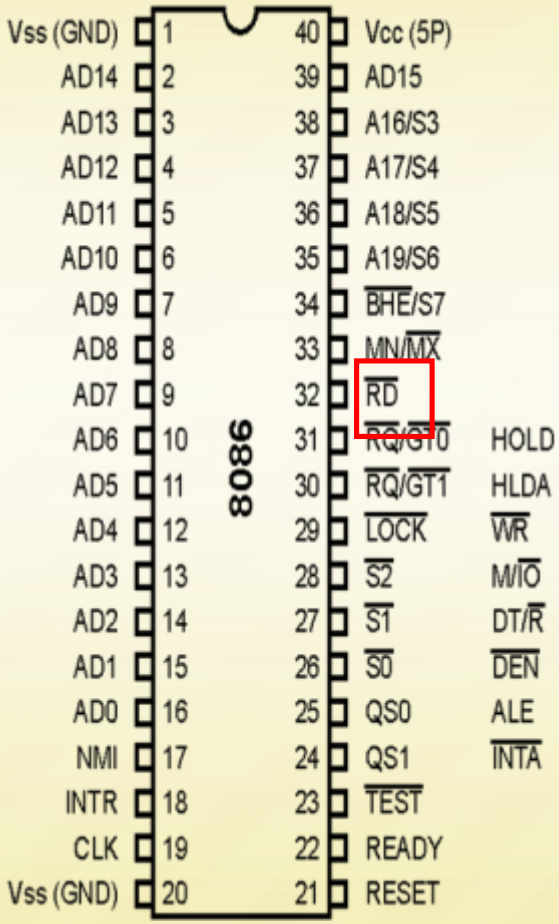
- BHE stands for Bus High Enable.
- BHE signal is used to indicate the transfer of data over higher order data bus (D_8 – D_{15}).
- 8-bit I/O devices use this signal.
- It is multiplexed with status pin S_7.



$\overline{RD}$ (Read)

Pin 32 (Output)

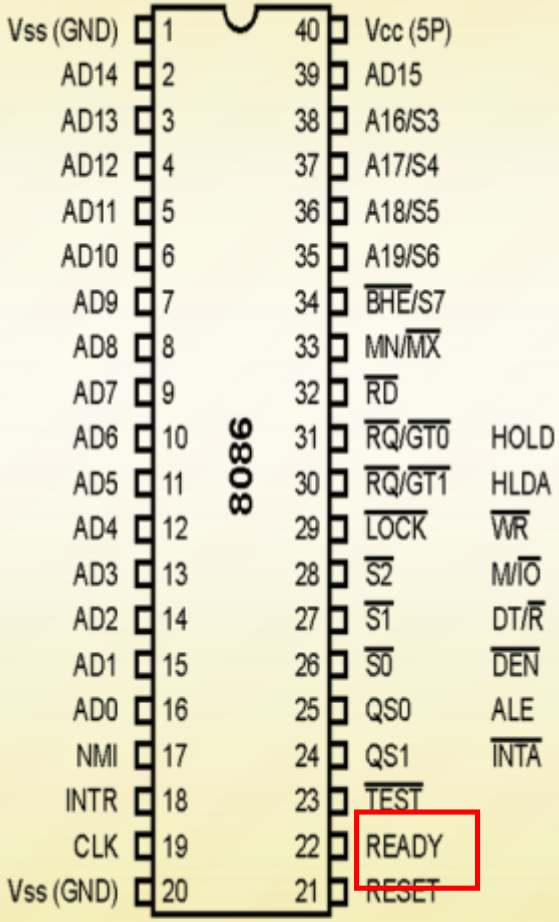
- It is a read signal used for read operation.
- It is an output signal.
- It is an active low signal.



READY

Pin 22 (Input)

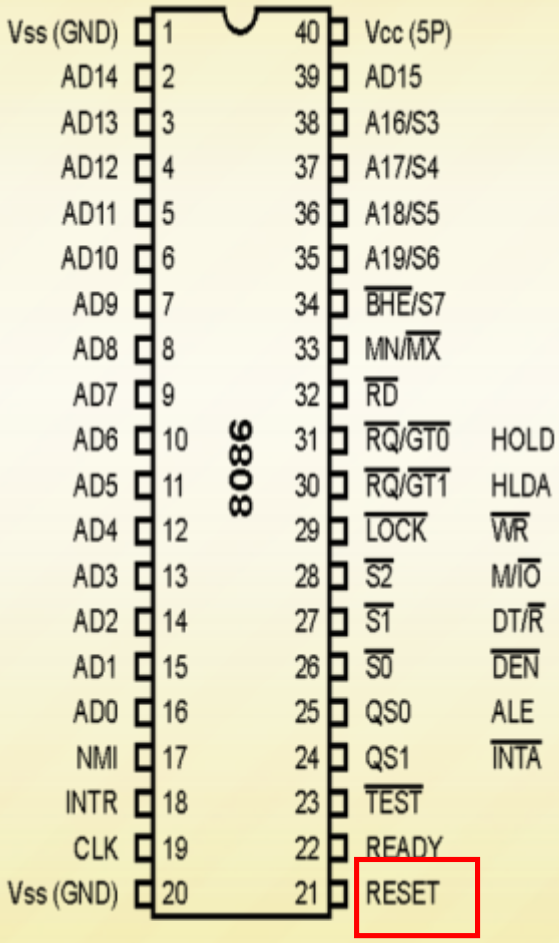
- This is an acknowledgement signal from slower I/O devices or memory.
- It is an active high signal.
- When high, it indicates that the device is ready to transfer data.
- When low, then microprocessor is in wait state.



RESET

Pin 21 (Input)

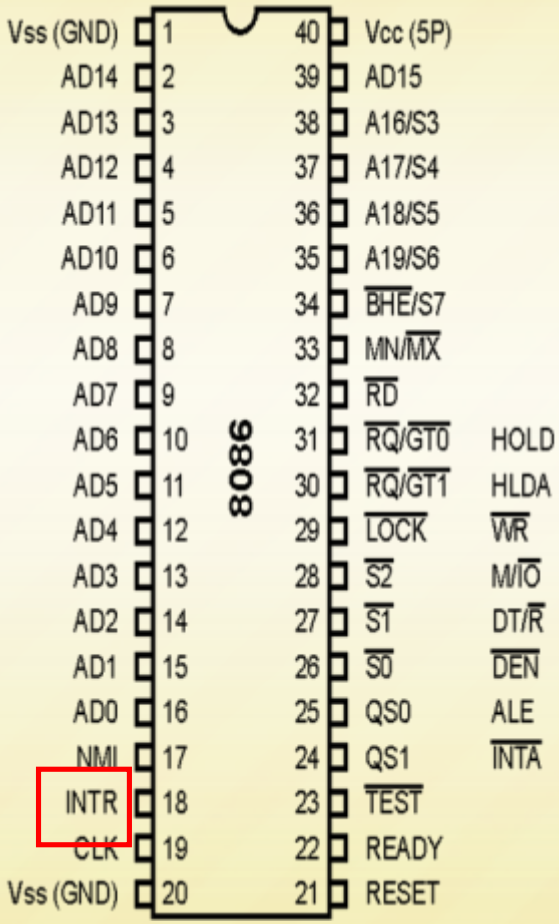
- It is a system reset.
- It is an active high signal.
- When high, microprocessor enters into reset state and terminates the current activity.
- It must be active for at least four clock cycles to reset the microprocessor.



INTR

Pin 18 (Input)

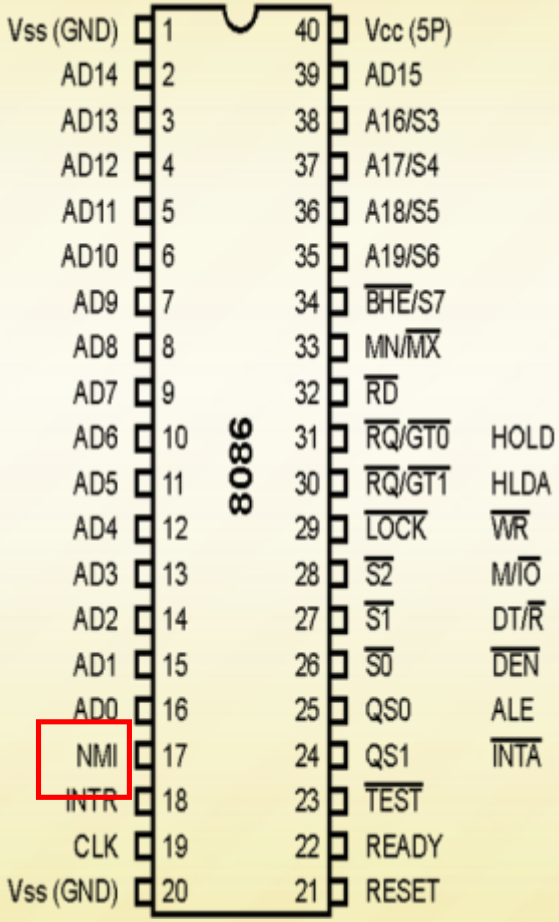
- It is an interrupt request signal.
- It is active high.
- It is level triggered.



NMI

Pin 17 (Input)

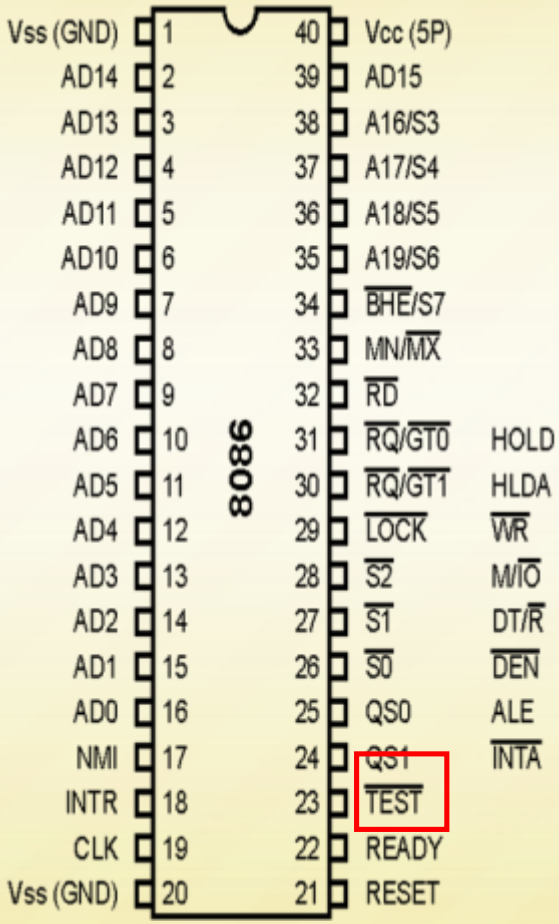
- It is a non-maskable interrupt signal.
- It is an active high.
- It is an edge triggered interrupt.



$\overline{\text{TEST}}$

Pin 23 (Input)

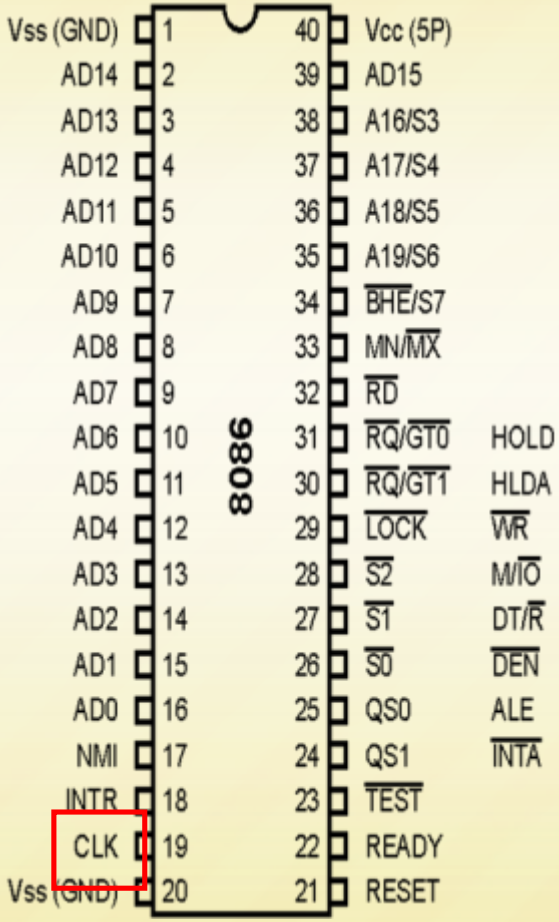
- It is used to test the status of math co-processor 8087.
- The $\overline{\text{BUSY}}$ pin of 8087 is connected to this pin of 8086.
- If low, execution continues else microprocessor is in wait state.



CLK

Pin 19 (Input)

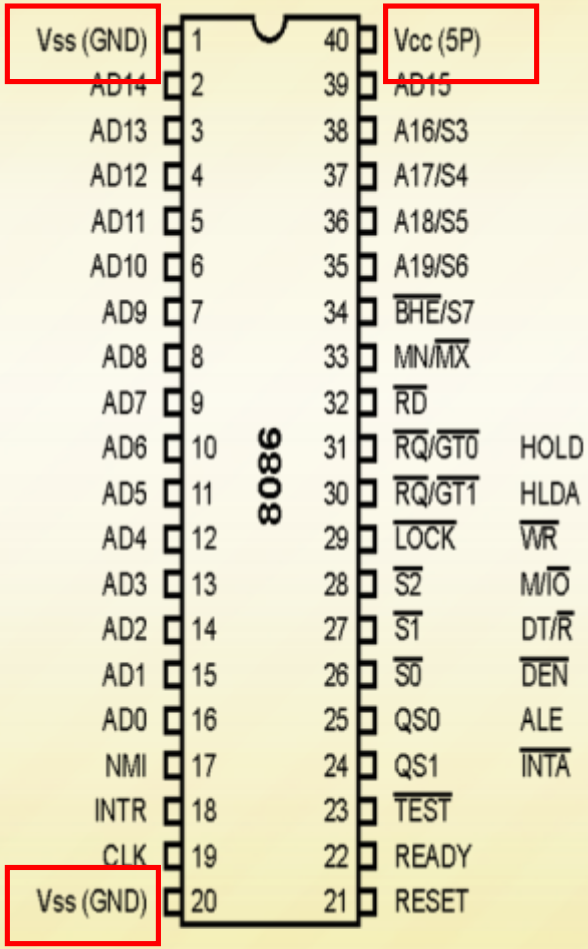
- This clock input provides the basic timing for processor operation.
- It is asymmetric square wave with 33% duty cycle.
- The range of frequency of different versions is 5 MHz, 8 MHz and 10 MHz



V_{CC} and V_{SS}

Pin 40 and Pin 20 (Input)

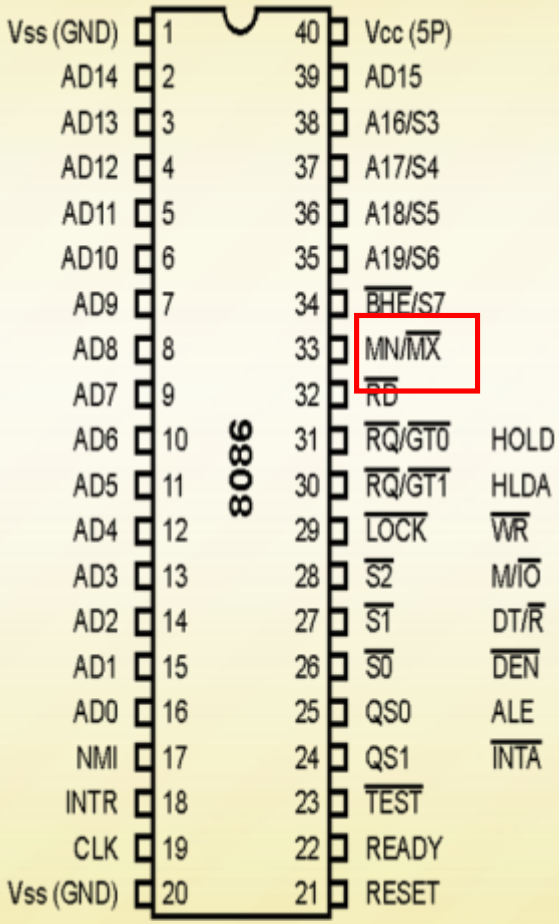
- V_{CC} is power supply signal.
- +5V DC is supplied through this pin.
- V_{SS} is ground signal.



MN / $\overline{MX}$

Pin 33 (Input)

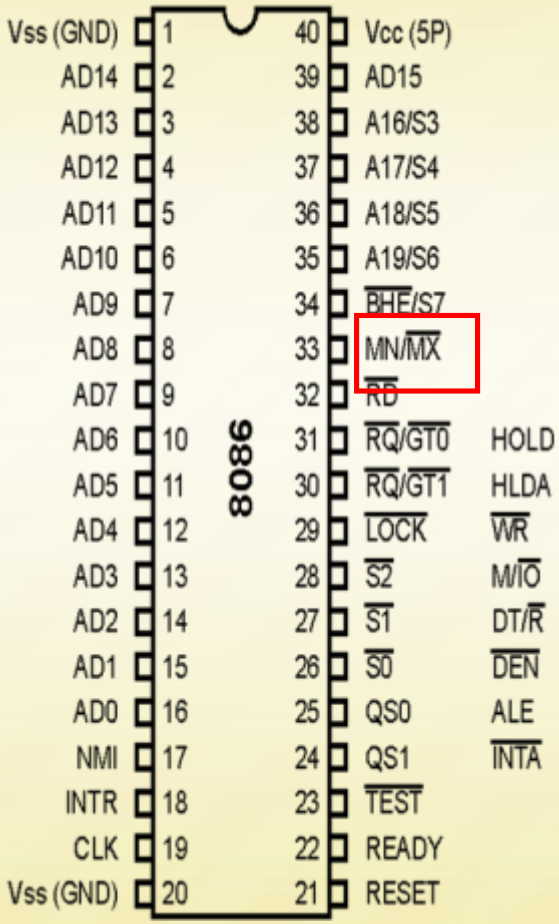
- 8086 works in two modes:
  - Minimum Mode(single processor mode)
  - Maximum Mode(multiprocessor mode)
- If MN/$\overline{MX}$ is high, it works in minimum mode.
- If MN/$\overline{MX}$ is low, it works in maximum mode.



MN / $\overline{MX}$

Pin 33 (Input)

- Pins 24 to 31 issue two different sets of signals.
- One set of signals is issued when CPU operates in minimum mode.
- Other set of signals is issued when CPU operates in maximum mode.

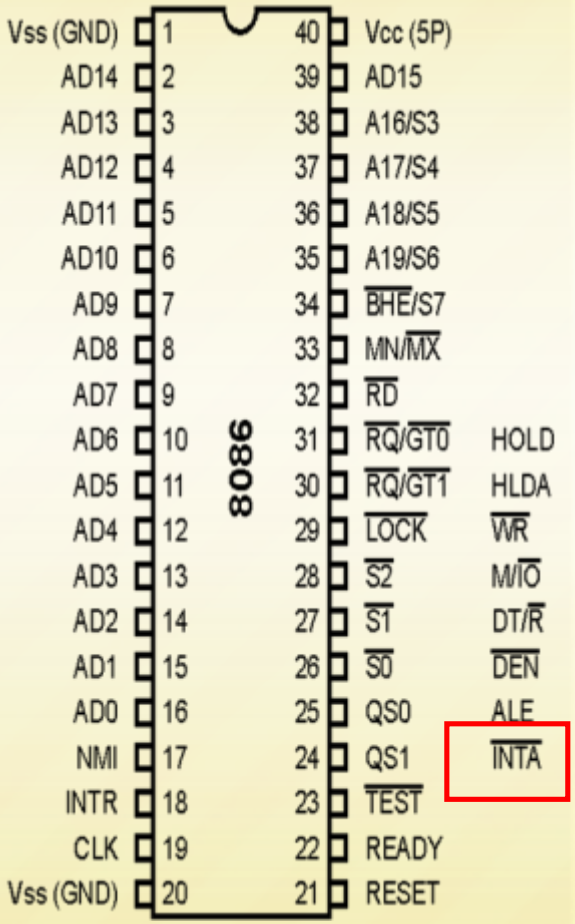


Pin Description for Minimum Mode

$\overline{\text{INTA}}$

Pin 24 (Output)

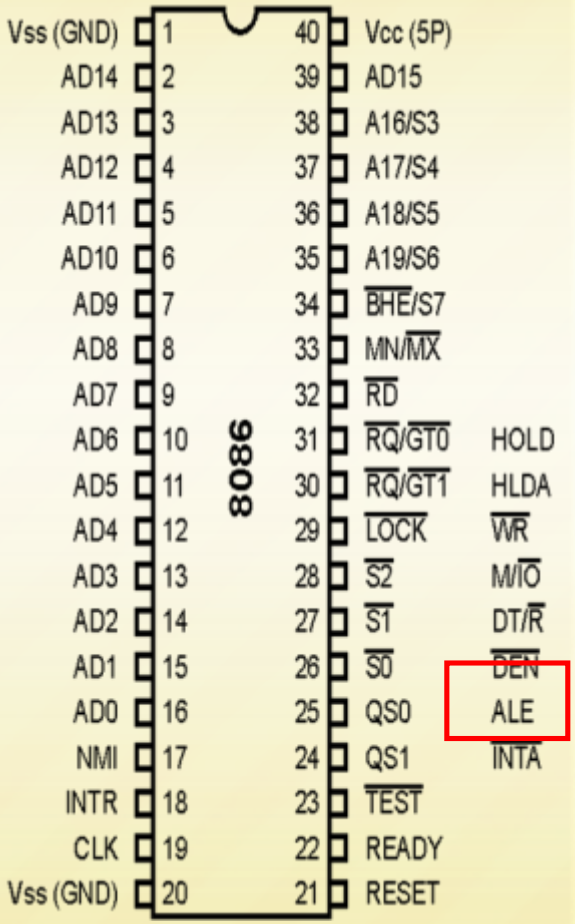
- This is an interrupt acknowledge signal.
- When microprocessor receives INTR signal, it acknowledges the interrupt by generating this signal.
- It is an active low signal.



ALE

Pin 25 (Output)

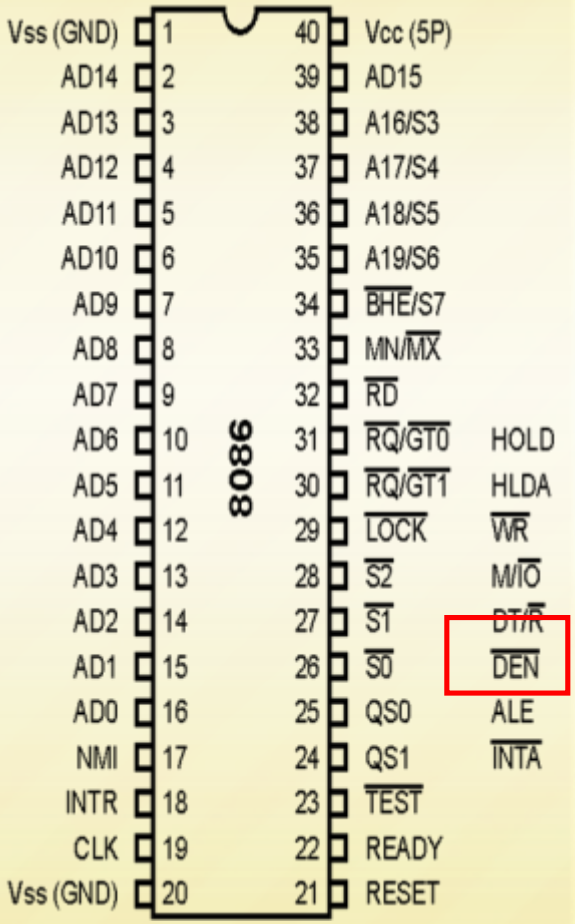
- This is an Address Latch Enable signal.
- It indicates that valid address is available on bus AD_0 – AD_{15}.
- It is an active high signal and remains high during T_1 state.
- It is connected to enable pin of latch 8282.



$\overline{\text{DEN}}$

Pin 26 (Output)

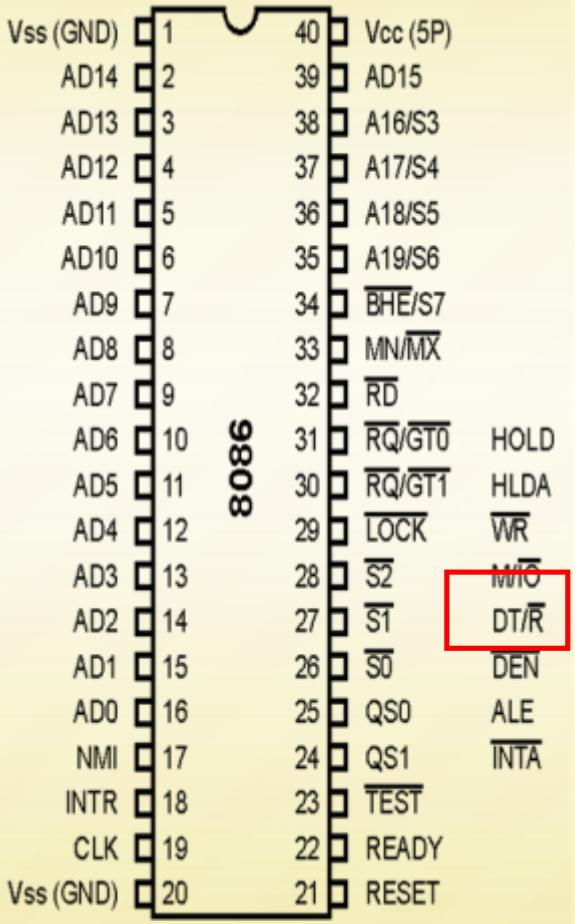
- This is a Data Enable signal.
- This signal is used to enable the transceiver 8286.
- Transceiver is used to separate the data from the address/data bus.
- It is an active low signal.



DT / $\overline{R}$

Pin 27 (Output)

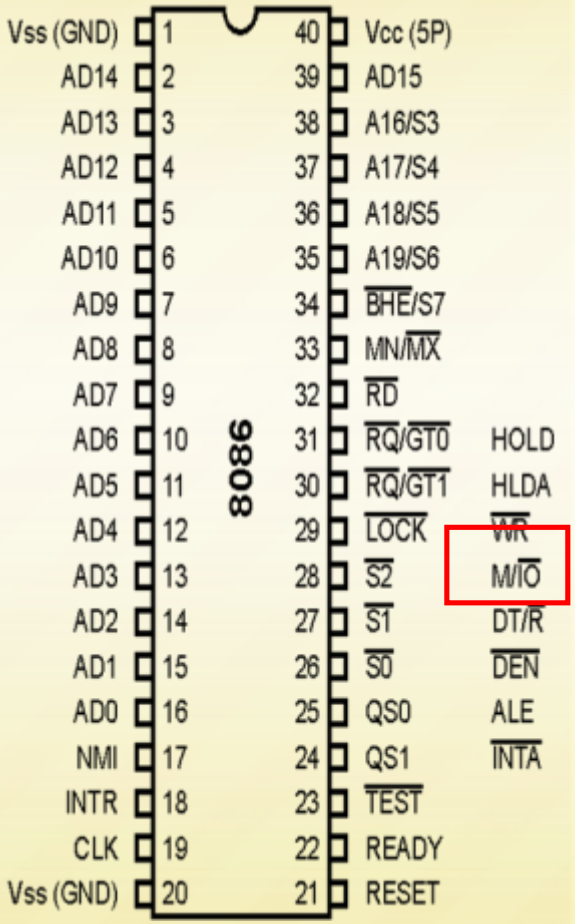
- This is a Data Transmit/Receive signal.
- It decides the direction of data flow through the transceiver.
- When it is high, data is transmitted out.
- When it is low, data is received in.



M / $\overline{IO}$

Pin 28 (Output)

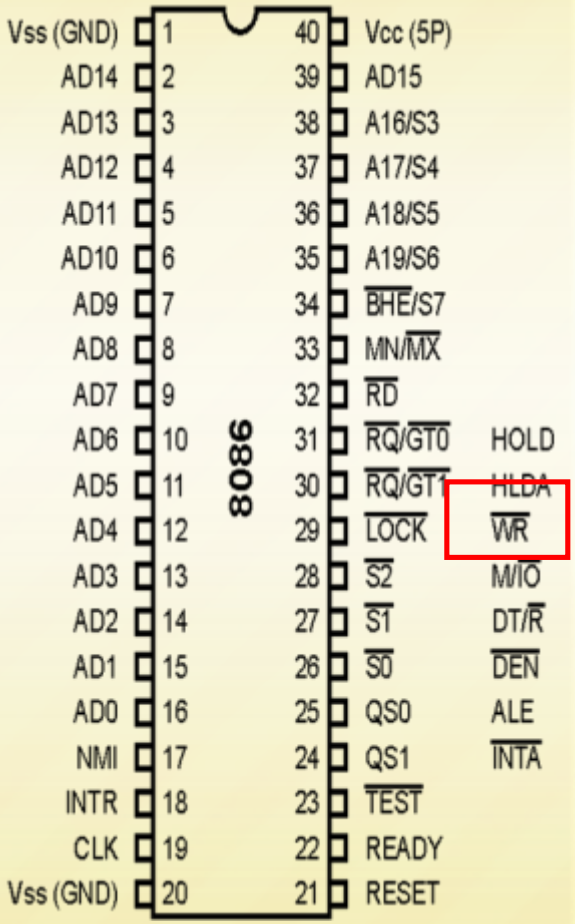
- This signal is issued by the microprocessor to distinguish memory access from I/O access.
- When it is high, memory is accessed.
- When it is low, I/O devices are accessed.



$\overline{WR}$

Pin 29 (Output)

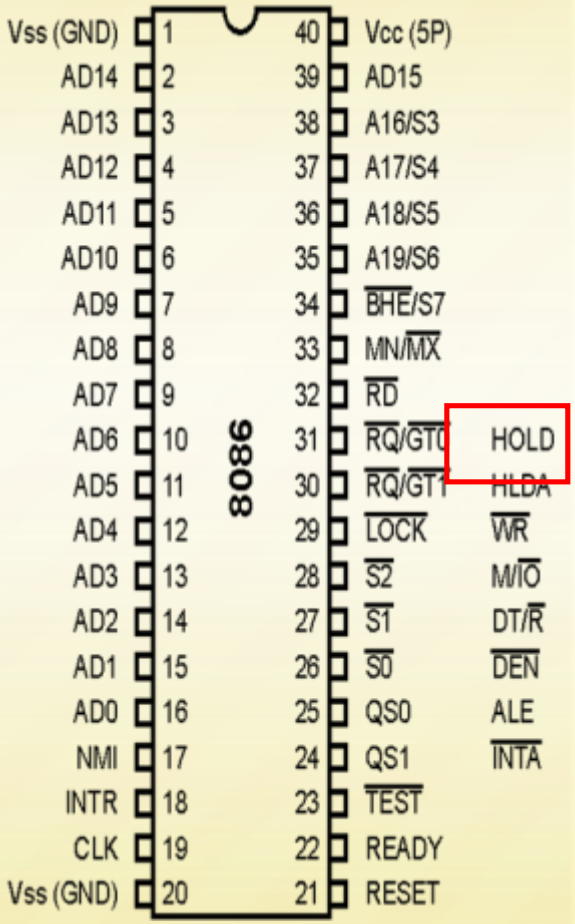
- It is a Write signal.
- It is used to write data in memory or output device depending on the status of M/IO signal.
- It is an active low signal.



HOLD

Pin 31 (Input)

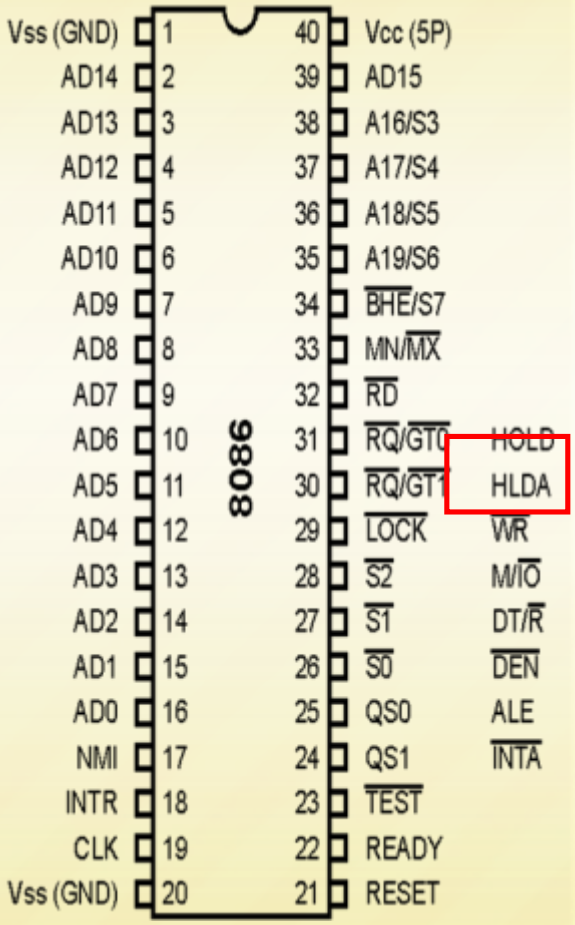
- When DMA controller needs to use address/data bus, it sends a request to the CPU through this pin.
- It is an active high signal.
- When microprocessor receives HOLD signal, it issues HLDA signal to the DMA controller.



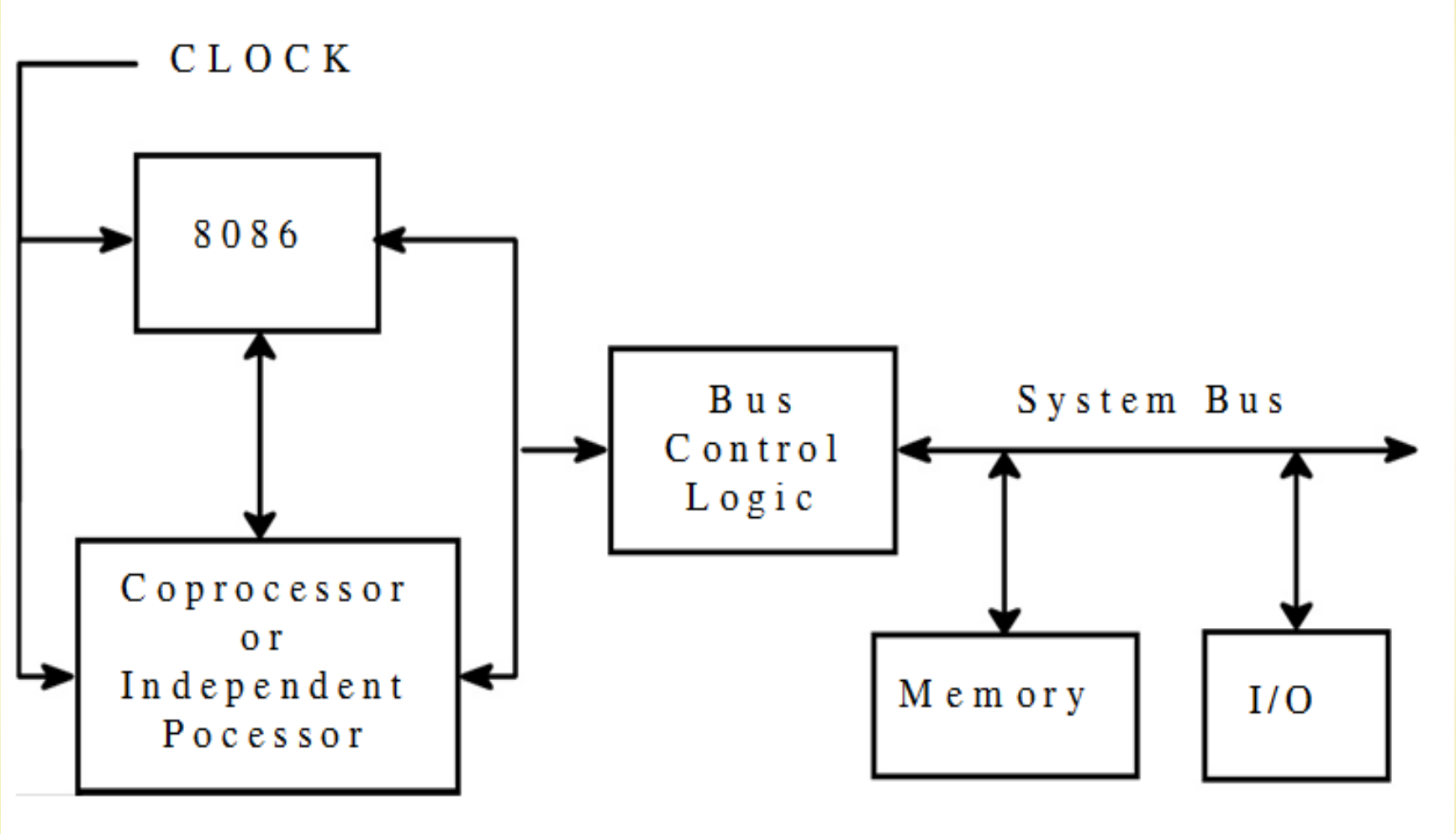
HLDA

Pin 30 (Output)

- It is a Hold Acknowledge signal.
- It is issued after receiving the HOLD signal.
- It is an active high signal.



Pin Description for Maximum Mode

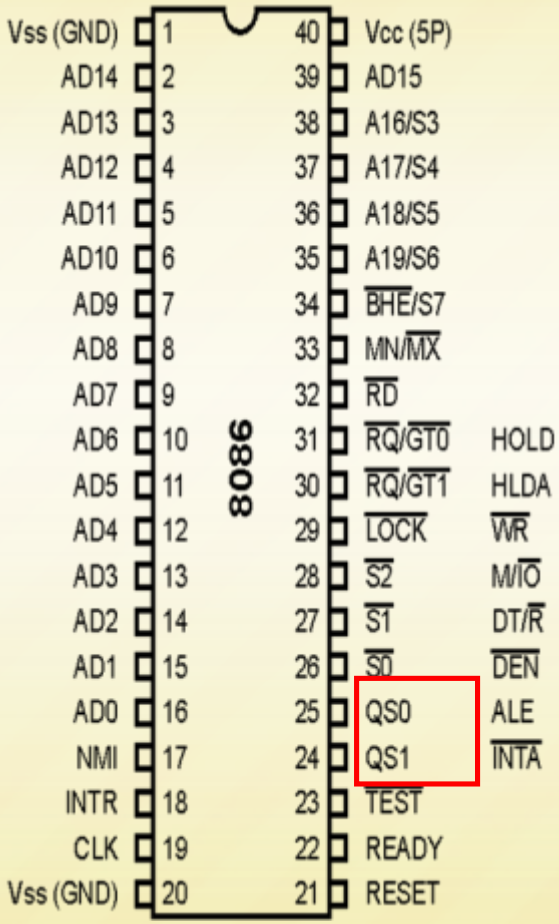

CLOCK
8086
Coprocessor
or
Independent
Pocessor
Bus
Control
Logic
System Bus
Memory
I/O

QS_1 and QS_0

Pin 24 and 25 (Output)

- These pins provide the status of instruction byte queue.

QS_1	QS_0	Status
0	0	No operation
0	1	1st byte of opcode from queue
1	0	Empty queue
1	1	Subsequent byte from queue



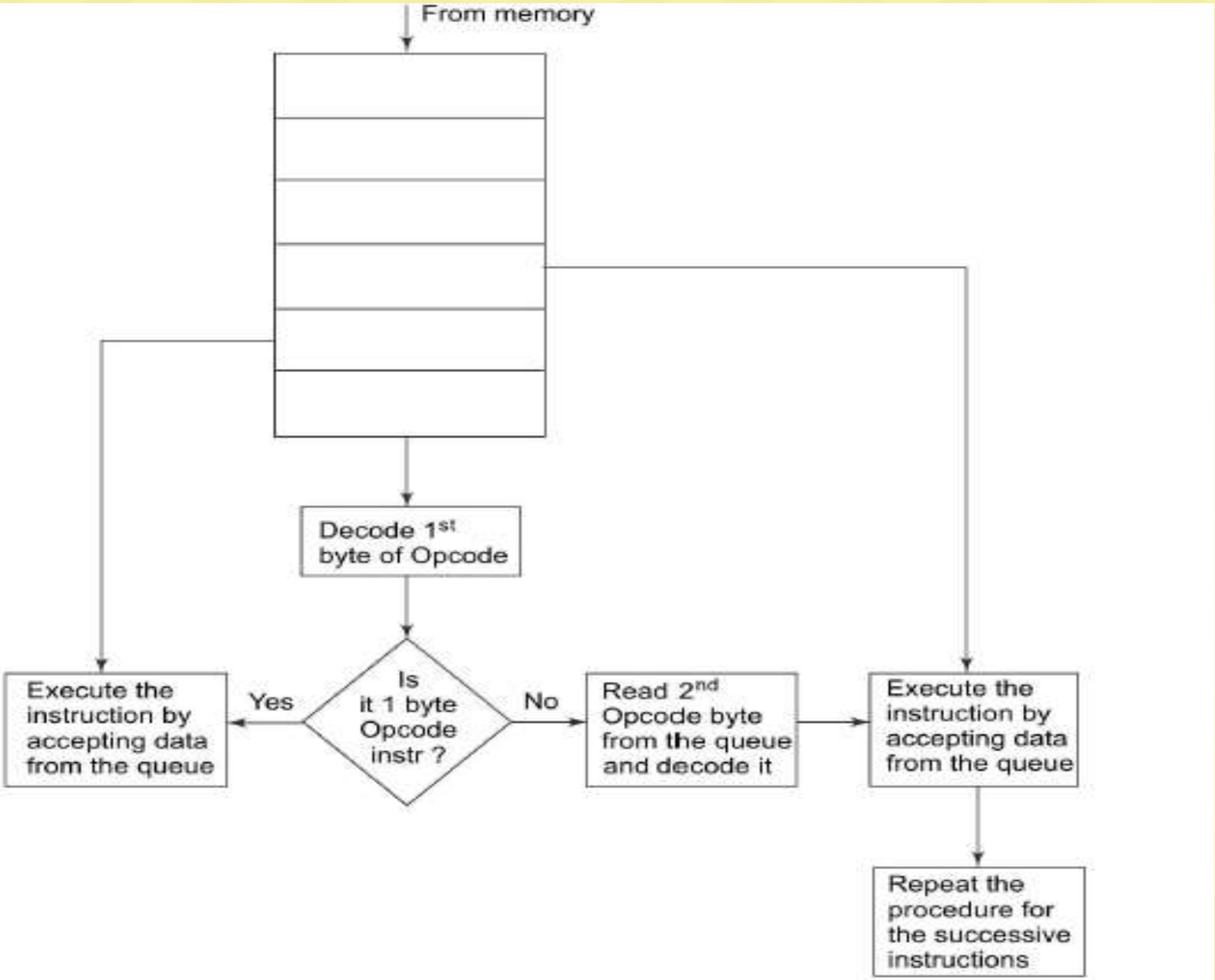
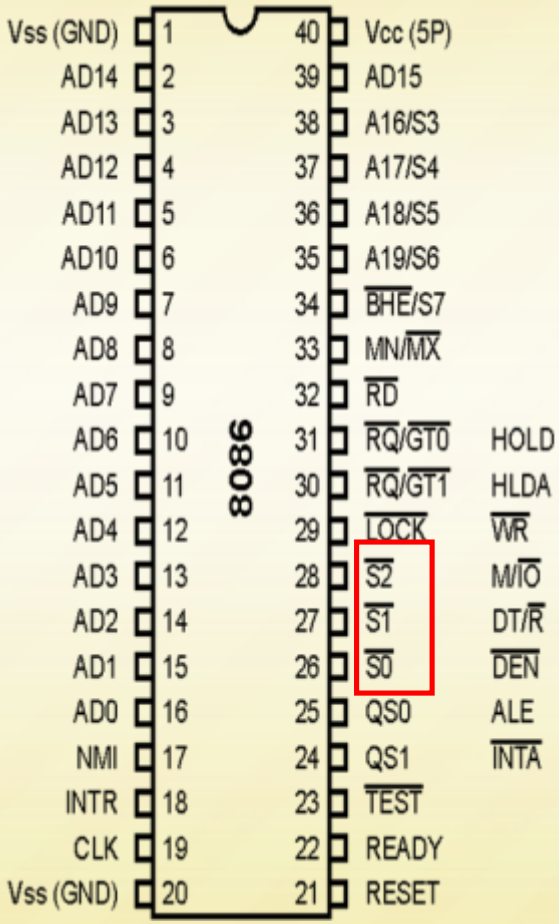


Fig. 1.6 ***The Queue Operation***

$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$

Pin 26, 27, 28 (Output)

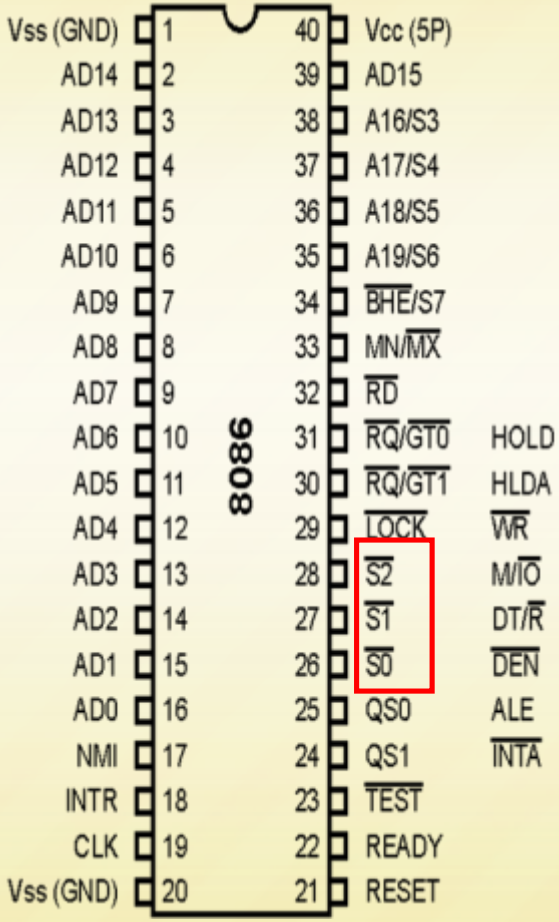
- These status signals indicate the operation being done by the microprocessor.
- This information is required by the Bus Controller 8288.
- Bus controller 8288 generates all memory and I/O control signals.



$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$

Pin 26, 27, 28 (Output)

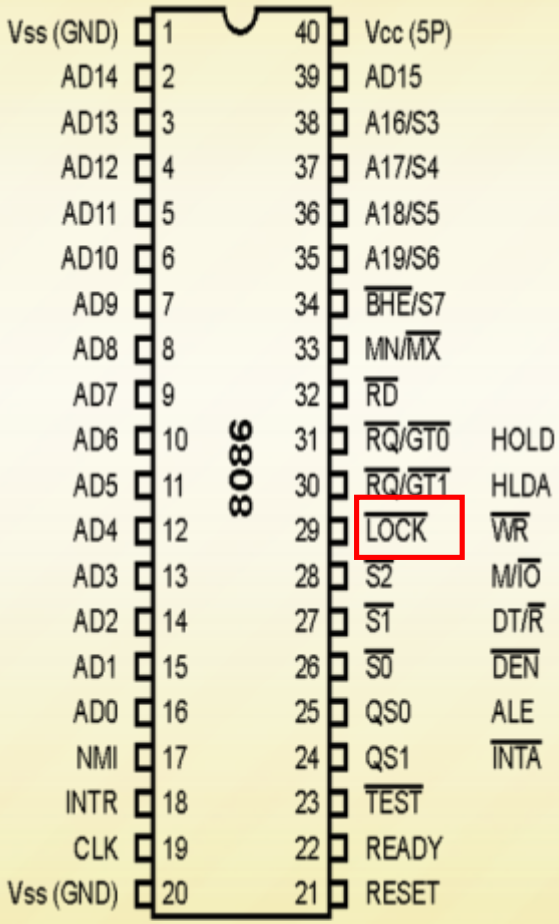
$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Status
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Opcode Fetch
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	Passive



$\overline{\text{LOCK}}$

Pin 29 (Output)

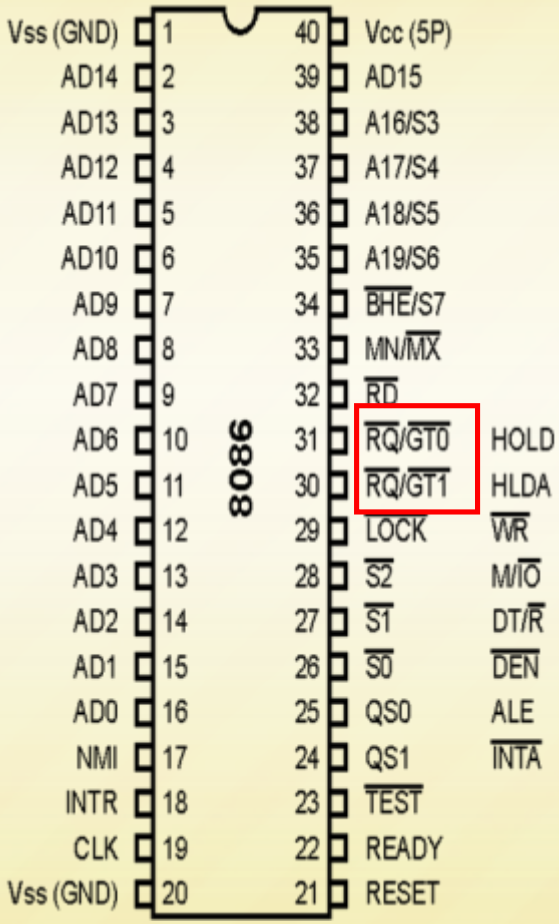
- This signal indicates that other processors should not ask CPU to relinquish the system bus.
- When it goes low, all interrupts are masked and HOLD request is not granted.
- This pin is activated by using LOCK prefix on any instruction.



$\overline{RQ}/\overline{GT}_1$ and $\overline{RQ}/\overline{GT}_0$

Pin 30 and 31 (Bi-directional)

- These are Request/Grant pins.
- Other processors request the CPU through these lines to release the system bus.
- After receiving the request, CPU sends acknowledge signal on the same lines.
- $\overline{RQ}/\overline{GT}_0$ has higher priority than $\overline{RQ}/\overline{GT}_1$.



Physical memory organization

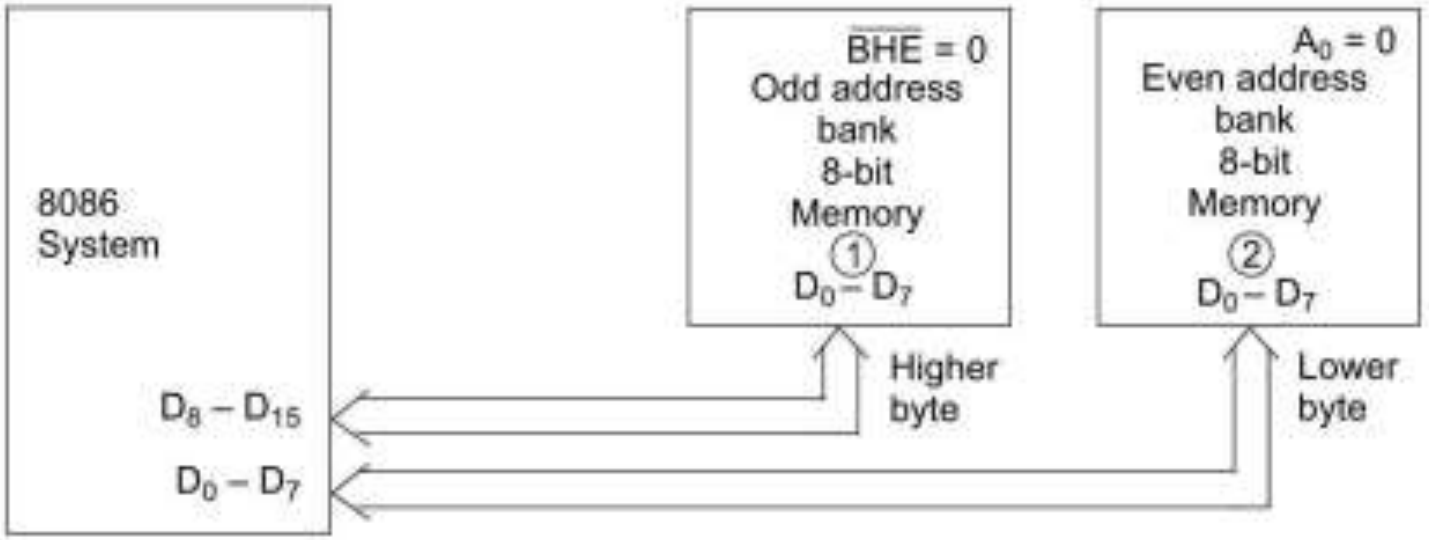


Fig. 1.7 *Physical Memory Organisation*

- In 8086 based system,1MB memory is physically organized as an odd bank and an even bank, each of 512kbytes,addressed in parallel by processor.
- Byte data with an even bank address is transferred on D7-D0, while the byte data with odd address is transferred on D15-D8 bus lines.
- The processor provides two enable signals, $\overline{BHE}$ and A0 for selection of either even or odd or both the banks.
- Commercially available memory chips are only 1 Byte size that is they can store only one byte in one memory location.
- To store 16bit data, two successive memory locations are used and the lower byte of 16 bit data can be stored in first memory location while the second byte is stored in next location.

- In a 16 read or write operation both of these bytes will be read or written in a single machine cycle.
- Bits D0-D7 of a 16 bit data will be transferred over D0 - D7 (lower byte)of 16 bit data bus to/from 8bit memory(2).
- Bits D8-D15 of the 16 bit data will be transferred over D8 - D15 (higher byte)of the 16 bit data bus to/from 8 bit memory(1).
- The lower byte of a 16 bit data is stored at the first address of the map 00000H and is to be transferred over D0-D7 of the microprocessor bus. So 00000H must be in 8 bit memory(2).
- Higher byte of the 16 bit data is stored in the next address 00001H is to be transferred over D8-D15 of the microprocessor bus. So the address 00001H must be in 8 bit memory(1).

Table 1.2 *Bus High Enable and A_0*

$\overline{BHE}$	A_0	*Indication*
0	0	Whole word (2 bytes)
0	1	Upper byte from or to odd address.
1	0	Lower byte from or to even address
1	1	None

- The complete memory map of 8086 is filled with 16 bit data, all the lower bytes(D0- D7)will be stored in the 8 bit even memory bank and all the higher bytes(D8-D15) will be stored in 8 bit odd memory bank .

- Thus the complete memory map of 8086 system is divided into even and odd address memory banks.

- If 8086 transfer a 16 bit data to/from memory, both of these banks must be selected for 16 bit operation.

- To maintain the upward compatibility with 8085, 8086 must be able to implement 8 bit operations.
- The first 8 bit operation with an even memory bank and second one is 8 bit operation with odd memory bank.
- The two signals A0 and $\overline{BHE}$ solve the problem of selection of appropriate memory banks.
- Certain memory locations are preserved for specific CPU operations. The locations from FFFF0H to FFFFFH are reserved for operations including jump to initialization program and I/O processor initialization.
- The locations from 00000H to 003FFH are reserved for interrupt vector table.
- The interrupt structure provides space for a total of 256 interrupt vectors(1KB locations).