UNIT 3

Peripheral Devices and their characteristics: Introduction, Input-Output Interface, Modes of Transfer-Programmed I/O, Priority Interrupt, Direct memory Access, Input – Output Processor (IOP), Intel 8089 IOP, Standard I/O interfaces – PCI, USB, SCSI.

Input – Output Processor (IOP)

- The IOP is similar to a CPU except that it is designed to handle the details of I/O processing.
- Unlike the DMA controller that must be set up entirely by the CPU, the IOP can fetch and execute its own instructions.
- IOP instructions are specially designed to facilitate I/O transfers.
- In addition, the IOP can perform other processing tasks, such as arithmetic, logic, branching, and code translation.

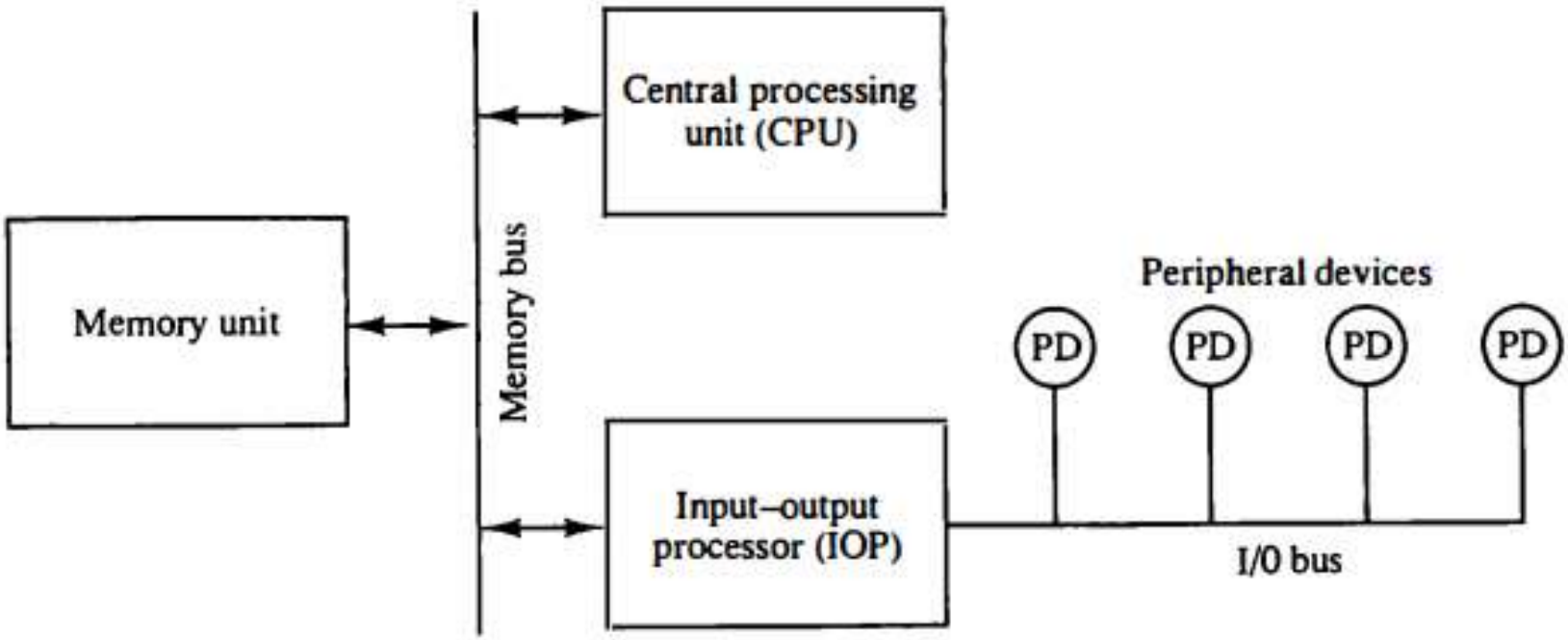


Figure 11-19 Block diagram of a computer with I/O processor.

- The memory unit occupies a central position and can communicate with each processor by means of direct memory access.
- The CPU is responsible for processing data needed in the solution of computational tasks.
- The IOP provides a path for transfer of data between various peripheral devices and the memory unit.
- The data formats of peripheral devices differ from memory and CPU data formats.
- The IOP must structure data words from many different sources.

- The communication between the IOP and the devices attached to it is similar to the program control method of transfer.

- In most computer systems, the CPU is the master while the IOP is a slave processor.

- The CPU is assigned the task of initiating all operations, but I/O instructions are executed in the IOP.

- CPU instructions provide operations to start an I/O transfer and also to test I/O status conditions needed for making decisions on various I/O activities.

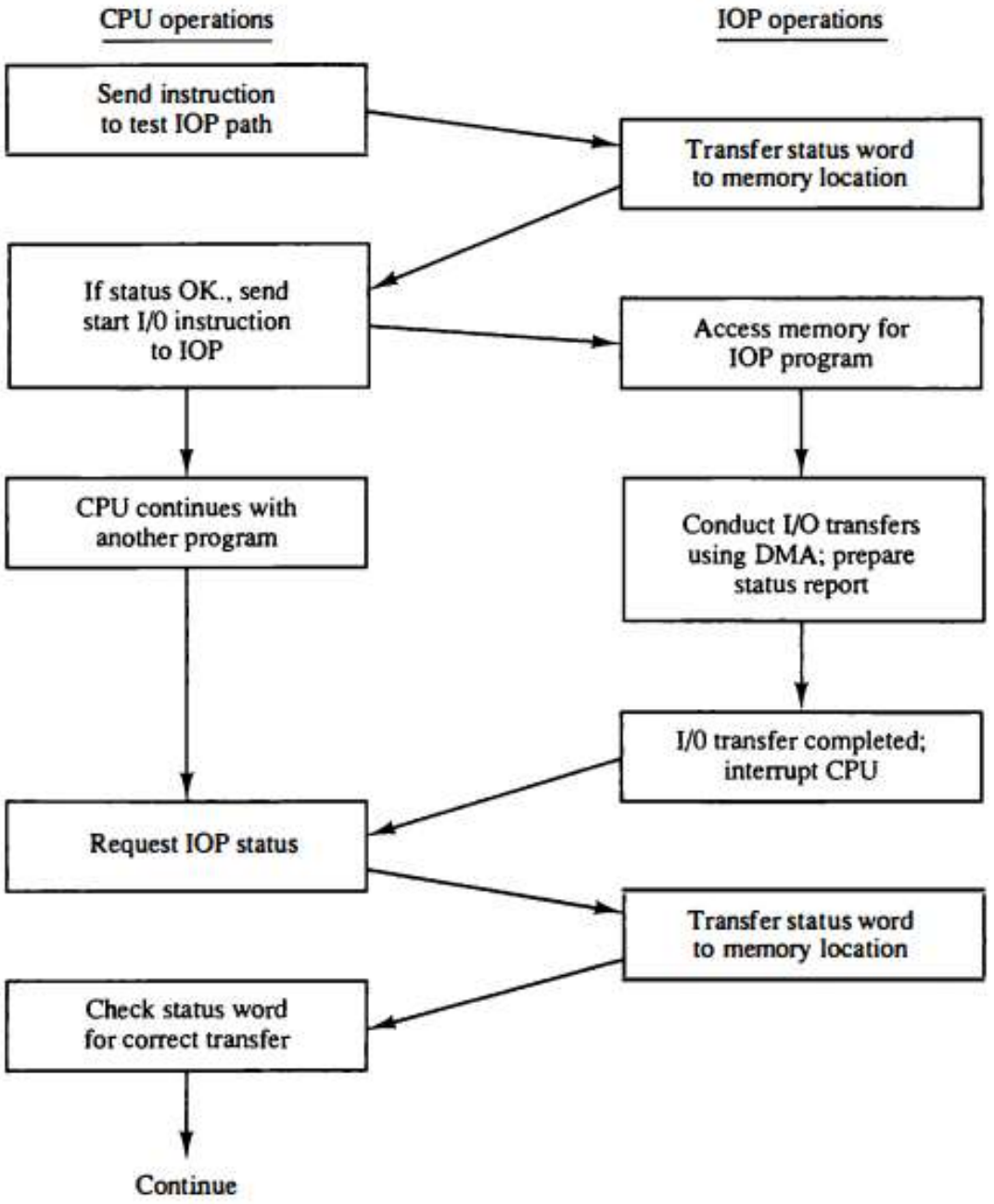
- The IOP, in turn, typically asks for CPU attention by means of an interrupt.

- It also responds to CPU requests by placing a status word in a prescribed location in memory to be examined later by a CPU program.

- When an I/O operation is desired, the CPU informs the IOP where to find the I/O program and then leaves the transfer details to the IOP.

CPU-IOP Communication

Figure 11-20 CPU-IOP communication.



- The CPU sends an instruction to test the IOP path.
- The IOP responds by inserting a status word in memory for the CPU to check.
- The bits of the status word indicate the condition of the IOP and I/O device, such as IOP overload condition, device busy with another transfer, or device ready for I/O transfer.

- The CPU refers to the status word in memory to decide what to do next.
- If all is in order, the CPU sends the instruction to start I/O transfer.
- The memory address received with this instruction tells the IOP where to find its program.
- The CPU can now continue with another program while the IOP is busy with the I/O program.
- Both programs refer to memory by means of DMA transfer.

- When the IOP terminates the execution of its program, it sends an interrupt request to the CPU.

- The CPU responds to the interrupt by issuing an instruction to read the status from the IOP.
- The IOP responds by placing the contents of its status report into a specified memory location.
- The IOP takes care of all data transfers between several I/O units and the memory while the CPU is processing another program.

- The IOP and CPU are competing for the use of memory, so the number of devices that can be in operation is limited by the access time of the memory.

Intel 8089 IOP

- The Intel 8089 I/O processor is contained in a 40-pin integrated circuit package.
- Within the 8089 there are two independent units called channels.
- Each channel combines the general characteristics of a processor unit with those of a direct memory access controller.
- The 8089 is designed to function as an IOP in a Microcomputer system where the Intel 8086 microprocessor is used as the CPU.

- The 8086 CPU initiates an I/O operation by building a message in memory that describes the function to be performed.

- The 8089 IOP reads the message from memory, carries out the operation, and notifies the CPU when it has finished.

- The 8089 IOP has 50 basic instructions that can operate on individual bits, on bytes, or 16-bit words.

- The IOP can execute programs in a manner similar to a CPU except that the instruction set is specifically chosen to provide efficient input-output processing.

- The instruction set includes general data transfer instructions, basic arithmetic and logic operations, conditional and unconditional branch operations, and subroutine call and return capabilities.

- The set also includes special instructions to initiate DMA transfers and issue an interrupt request to the CPU.

- It provides efficient data transfer between any two components attached to the system bus, such as I/O to memory, memory to memory, or I/O to I/O.

- The 8086 functions as the CPU and the 8089 as the IOP.

- The two units share a common memory through a bus controller connected to a system bus, which is called a "multibus" by Intel.

- The IOP uses a local bus to communicate with various interface units connected to I/O devices.

- The CPU communicates with the IOP by enabling the channel attention line.

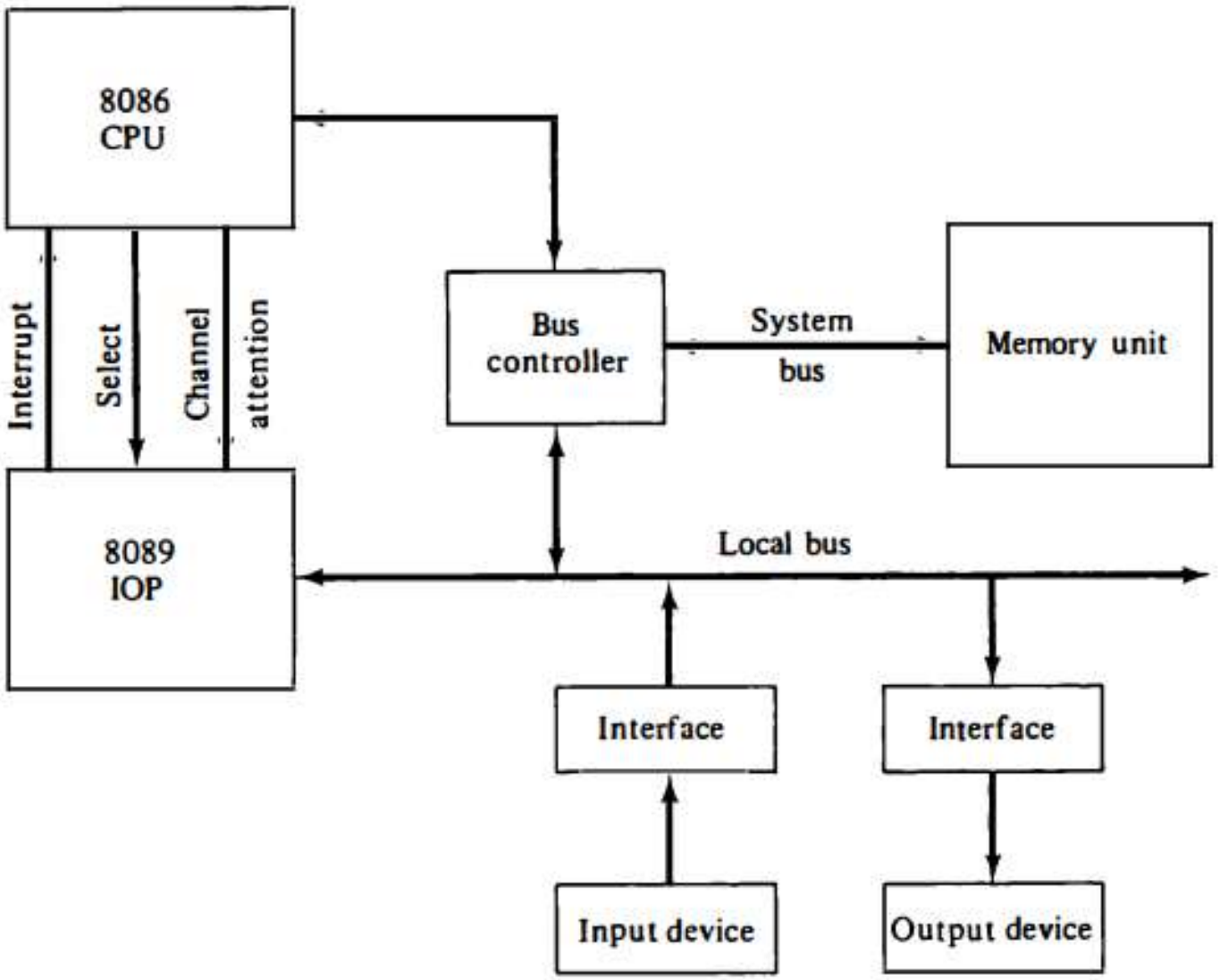


Figure 11-23 Intel 8086/8089 microcomputer system block diagram.

- The select line is used by the CPU to select one of two channels in the 8089.
- The IOP gets the attention of the CPU by sending an interrupt request
- The CPU and IOP communicate with each other by writing messages for one another in system memory.
- The CPU prepares the message area and signals the IOP by enabling the channel attention line.

- The IOP reads the message, performs the required I/O functions, and executes the appropriate channel program.

- When the channel has completed its program, it issues an interrupt request to the CPU.

- The communication scheme consists of program sections called "blocks," which are stored in memory.

- Each block contains control and parameter information as well as an address pointer to its successor block.

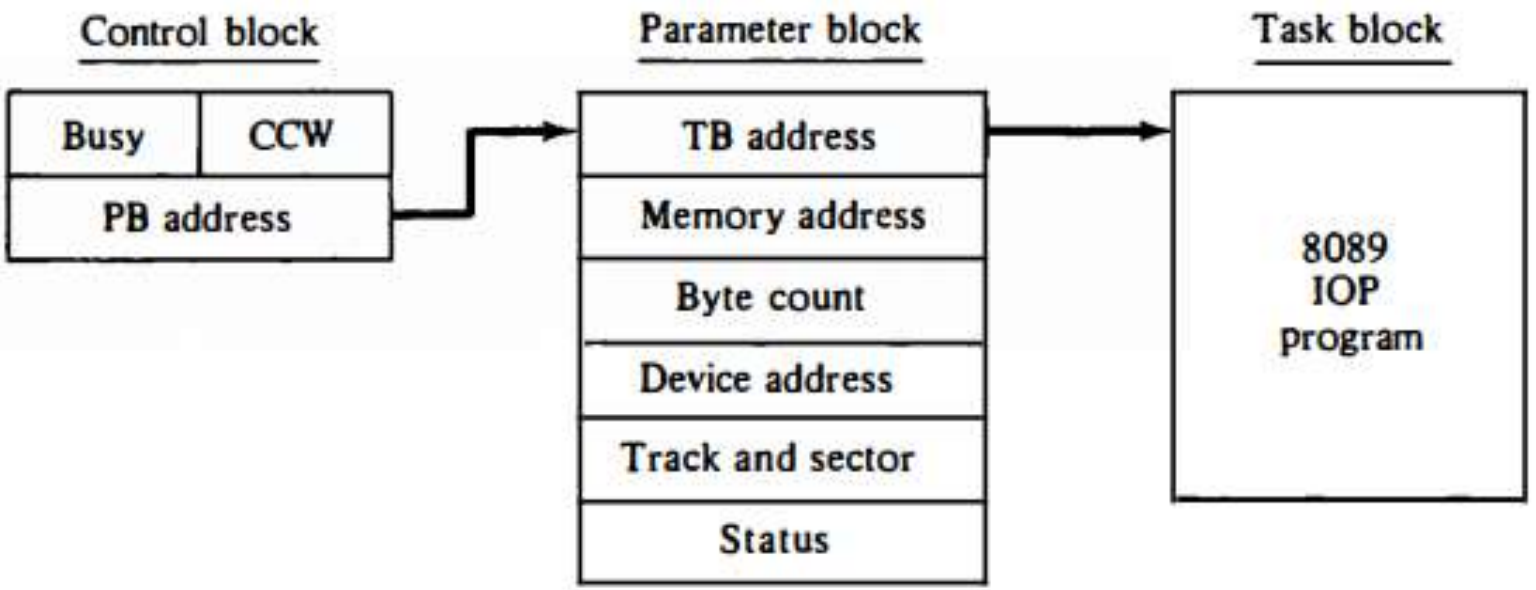


Figure 11-24 Location of information in memory for I/O operations in the Intel 8086/8089 microcomputer system.

- The address of the control block is passed to each IOP channel during initialization.
- The busy flag indicates whether the IOP is busy or ready to perform a new I/O operation.
- The CCW (channel command word) is specified by the CPU to indicate the operation required from the IOP.
- The CPU and IOP work together through the control and parameter blocks.
- The CPU obtains use of the shared memory after checking the busy flag to ensure that the IOP is available.

- The CPU then fills in the information in the parameter block and writes a "start operation" command in the CCW.

- After the communication blocks have been set up, the CPU enables the channel attention signal to inform the IOP to start its I/O operation.

- The CPU then continues with another program.

- The IOP responds to the channel attention signal by placing the address of the control block into its program counter.
- The IOP refers to the control block and sets the busy flag.
- It then checks the operation in the CCW.
- The PB (parameter block) address and TB (task block) address are then transferred into internal IOP registers.

- The IOP starts executing the program in the task block using the information in the parameter block.
- The entries in the parameter block depend on the I/O device.
- The parameters listed in Fig are suitable for data transfer to or from a magnetic disk.
- The memory address specifies the beginning address of a memory buffer.
- The byte count gives the number of bytes to be transferred.

- The device address specifies the particular I/O device to be used.
- The track and sector numbers locate the data on the disk.
- When the I/O operation is completed, the IOP stores its status bits in the status word location of the parameter block and interrupts the CPU.
- The CPU can refer to the status word to check if the transfer has been completed satisfactorily.