UNIT 2

The 8086 Microprocessor: Architecture, Register organization, 8086 signal description, Physical memory organization, Minimum and Maximum mode system and timing diagrams, Addressing modes, 8086 Instruction Set and Assembler Directives, Assembly Language example programs, Stack structure of 8086, Interrupt structure of 8086, Interrupt vector table, Procedures and macros.

Minimum and Maximum mode system and timing diagrams

Minimum Mode 8086 System

- The microprocessor 8086 is operated in minimum mode by strapping its MN/MX pin to logic 1.
- In this mode, all the control signals are given out by the microprocessor chip itself. There is a single microprocessor in the minimum mode system.
- The remaining components in the system are latches, transreceivers, clock generator, memory and I/O devices.
- Latches are generally buffered output D-type flip-flops like 74LS373 or 8282. They are used for separating the valid address from the multiplexed address/data signals and are controlled by the ALE signal generated by 8086.

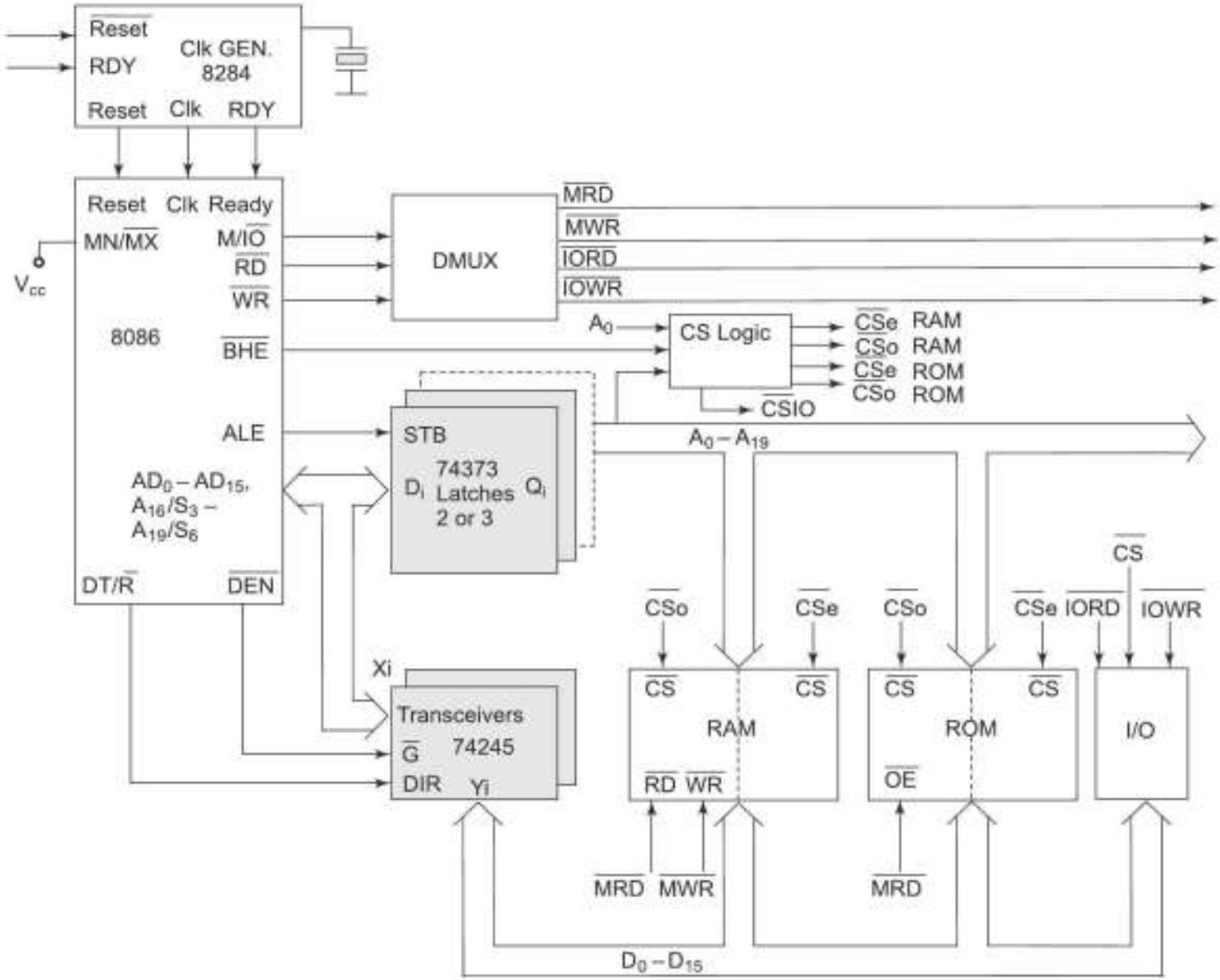


Fig. 1.13 *Minimum Mode 8086 System*

- Transreceivers are the bidirectional buffers and some times they are called as data amplifiers. They are required to separate the valid data from the time multiplexed address/data signals. They are controlled by two signals namely, $\overline{DEN}$ and DT/$\overline{R}$.

- The $\overline{DEN}$ signal indicates the direction of data, i.e. from or to the processor.

- The system contains memory for the monitor and users program storage. Usually, EPROM are used for monitor storage, while RAM for users program storage. A system may contain I/O devices.

- The opcode fetch and read cycles are similar. Hence the timing diagram can be categorized in two parts, the first is the timing diagram for read cycle and the second is the timing diagram for write cycle.

- The read cycle begins in T1 with the assertion of address latch enable (ALE) signal and also M /$\overline{IO}$ signal. During the negative going edge of this signal, the valid address is latched on the local bus.

- The $\overline{BHE}$ and A0 signals address low, high or both bytes. From T1 to T4 , the M/$\overline{IO}$ signal indicates a memory or I/O operation.
- At T2, the address is removed from the local bus and is sent to the output. The bus is then tristated. The read ($\overline{RD}$) control signal is also activated in T2.
- The read ($\overline{RD}$) signal causes the address device to enable its data bus drivers. After $\overline{RD}$ goes low, the valid data is available on the data bus.
- The addressed device will drive the READY line high. When the processor returns the read signal to high level, the addressed device will again tristate its bus drivers.

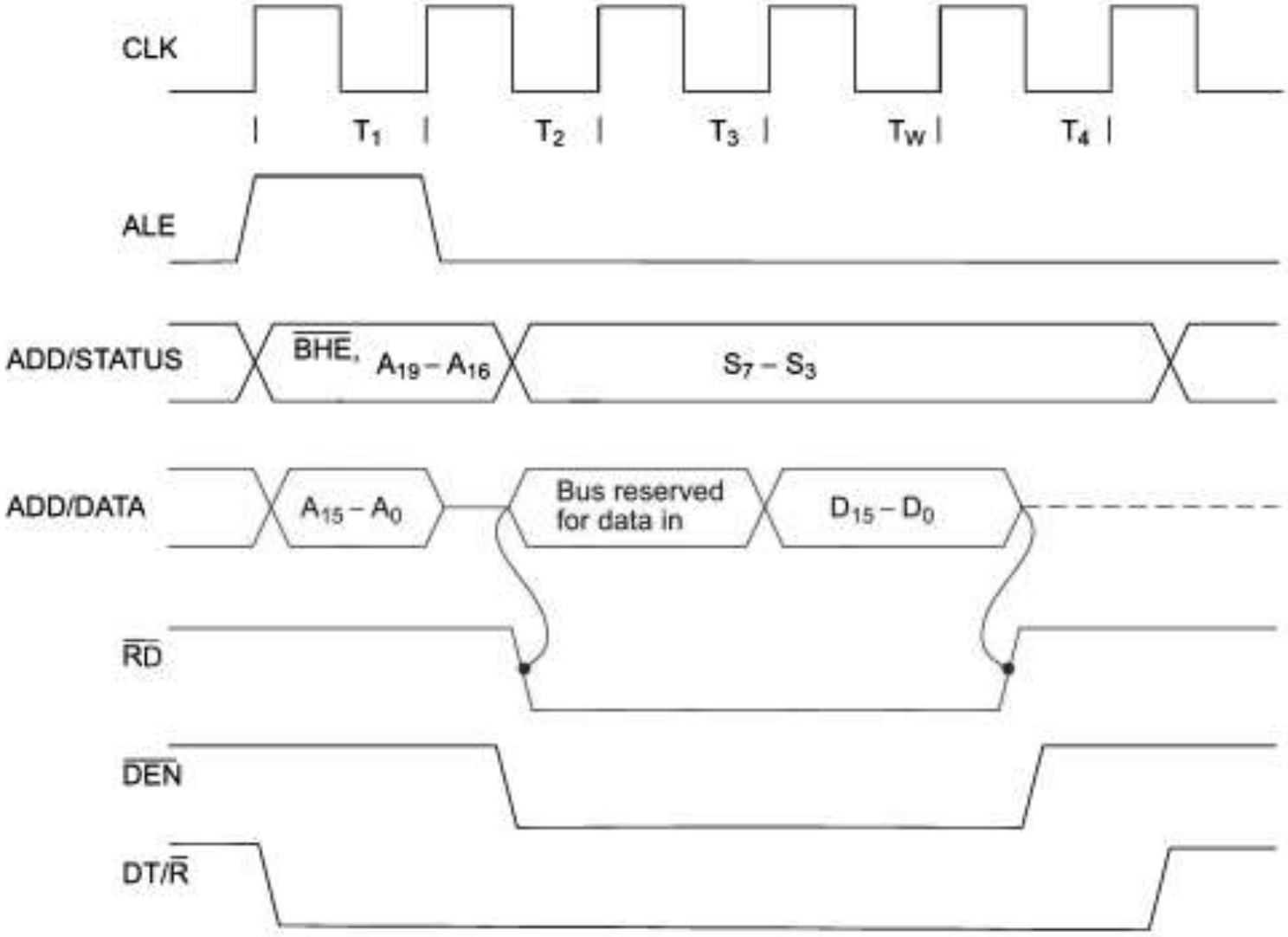


Fig. 1.14(a) *Read Cycle Timing Diagram for Minimum Mode*

- A write cycle also begins with the assertion of ALE and the emission of the address.
- The M/$\overline{IO}$ signal is again asserted to indicate a memory or I/O operation. In T2, after sending the address in T1, the processor sends the data to be written to the addressed location.
- The data remains on the bus until middle of T4 state. The $\overline{WR}$ becomes active at the beginning of T2 (unlike $\overline{RD}$ is somewhat delayed in T2 to provide time for floating).
- The $\overline{BHE}$ and A0 signals are used to select the proper byte or bytes of memory or I/O word to be read or write.
- The M/$\overline{IO}$, $\overline{RD}$ and $\overline{WR}$ signals indicate the type of data transfer as specified in table below.

$M/\overline{IO}$	$\overline{RD}$	$\overline{DEN}$	*Transfer Type*
0	0	1	I/O read
0	1	0	I/O write
1	0	1	Memory read
1	1	0	Memory write

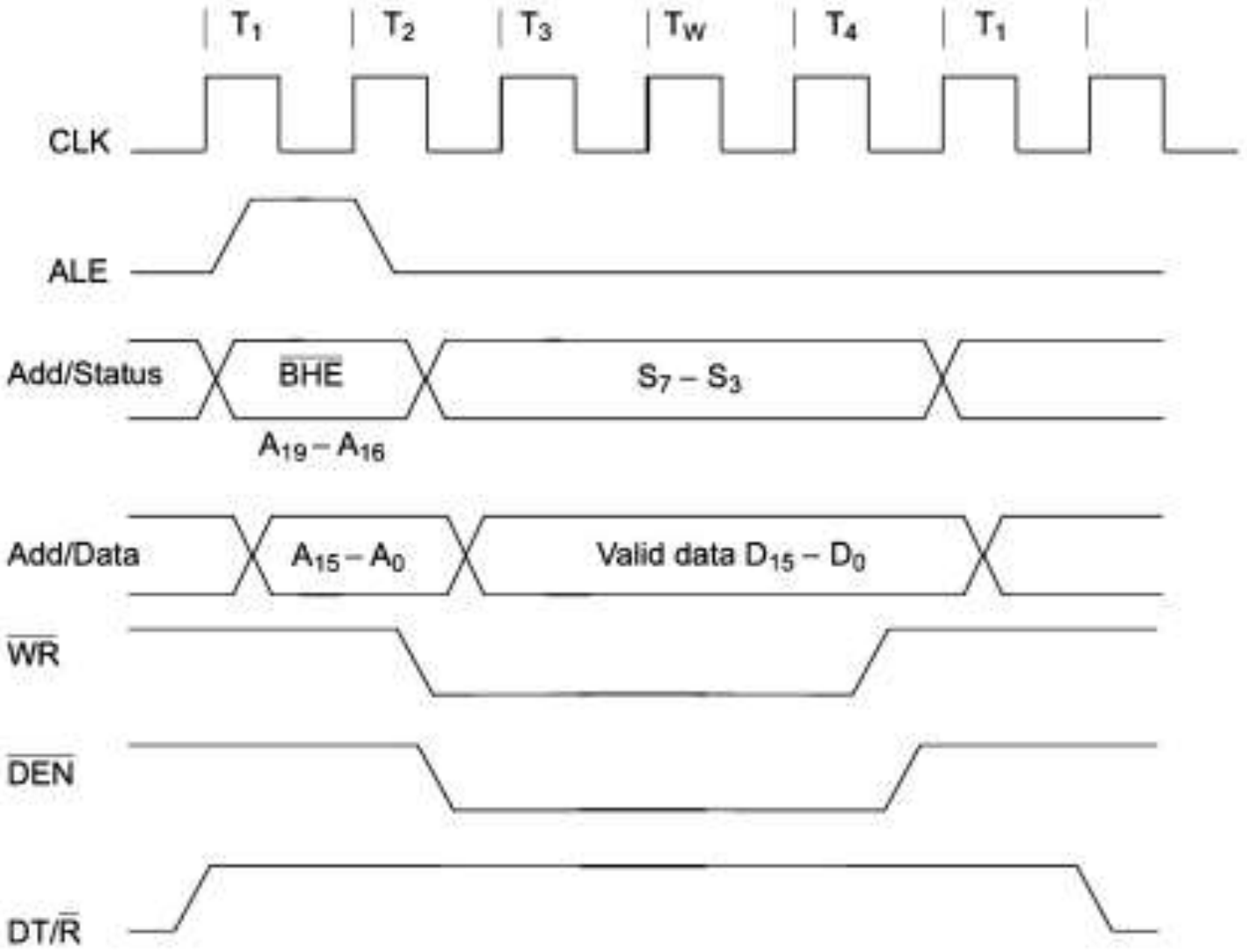


Fig. 1.14(b) *Write Cycle Timing Diagram for Minimum Mode Operation*

***Hold Response sequence*:**

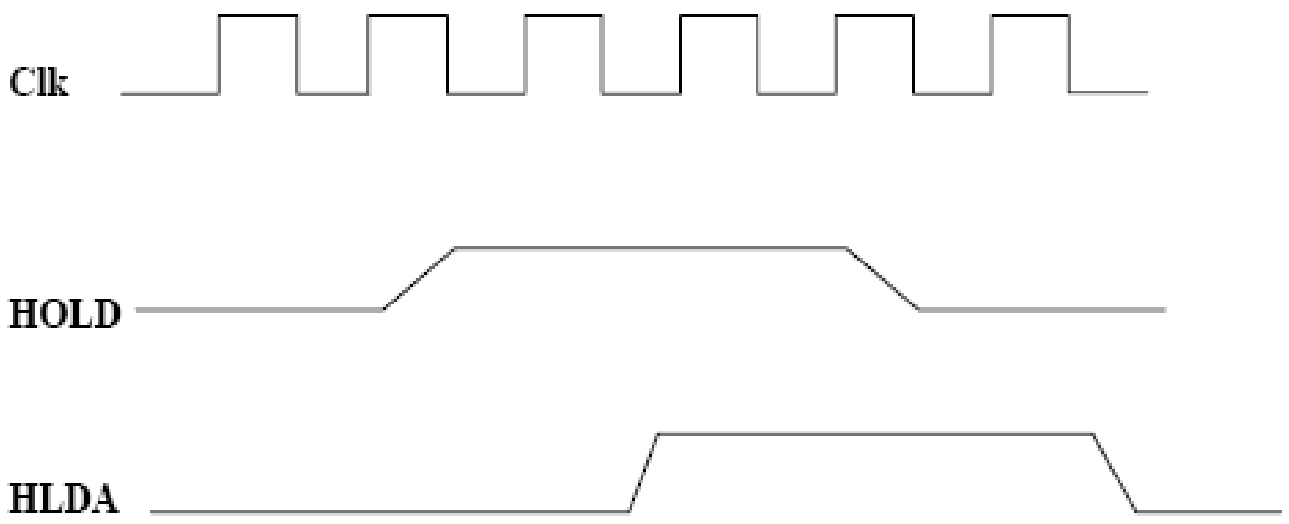
- The HOLD pin is checked at leading edge of each clock pulse.

  If it is received active by the processor before T4 of the previous cycle or during T1 state of the current cycle, the CPU activates HLDA in the next clock cycle and for succeeding bus cycles, the bus will be given to another requesting master.

- The control of the bus is not regained by the processor until the requesting master does not drop the HOLD pin low.

- When the request is dropped by the requesting master, the HLDA is dropped by the processor at the trailing edge of the next clock.

Hold Response Timing Cycle



Bus Request and Bus Grant Timings in Minimum Mode System

Maximum Mode 8086 System

- In the maximum mode, the 8086 is operated by strapping the MN/$\overline{MX}$ pin to ground.
- In this mode, the processor derives the status signal $\overline{S2}$, $\overline{S1}$, $\overline{S0}$. Another chip called bus controller derives the control signals using this status information .
- In the maximum mode, there may be more than one microprocessor in the system configuration. The components in the system are same as in the minimum mode system.
- The basic function of the bus controller chip IC8288, is to derive control signals like $\overline{RD}$ and $\overline{WR}$ (for memory and I/O devices), $\overline{DEN}$, DT/$\overline{R}$, ALE etc. using the information by the processor on the status lines.

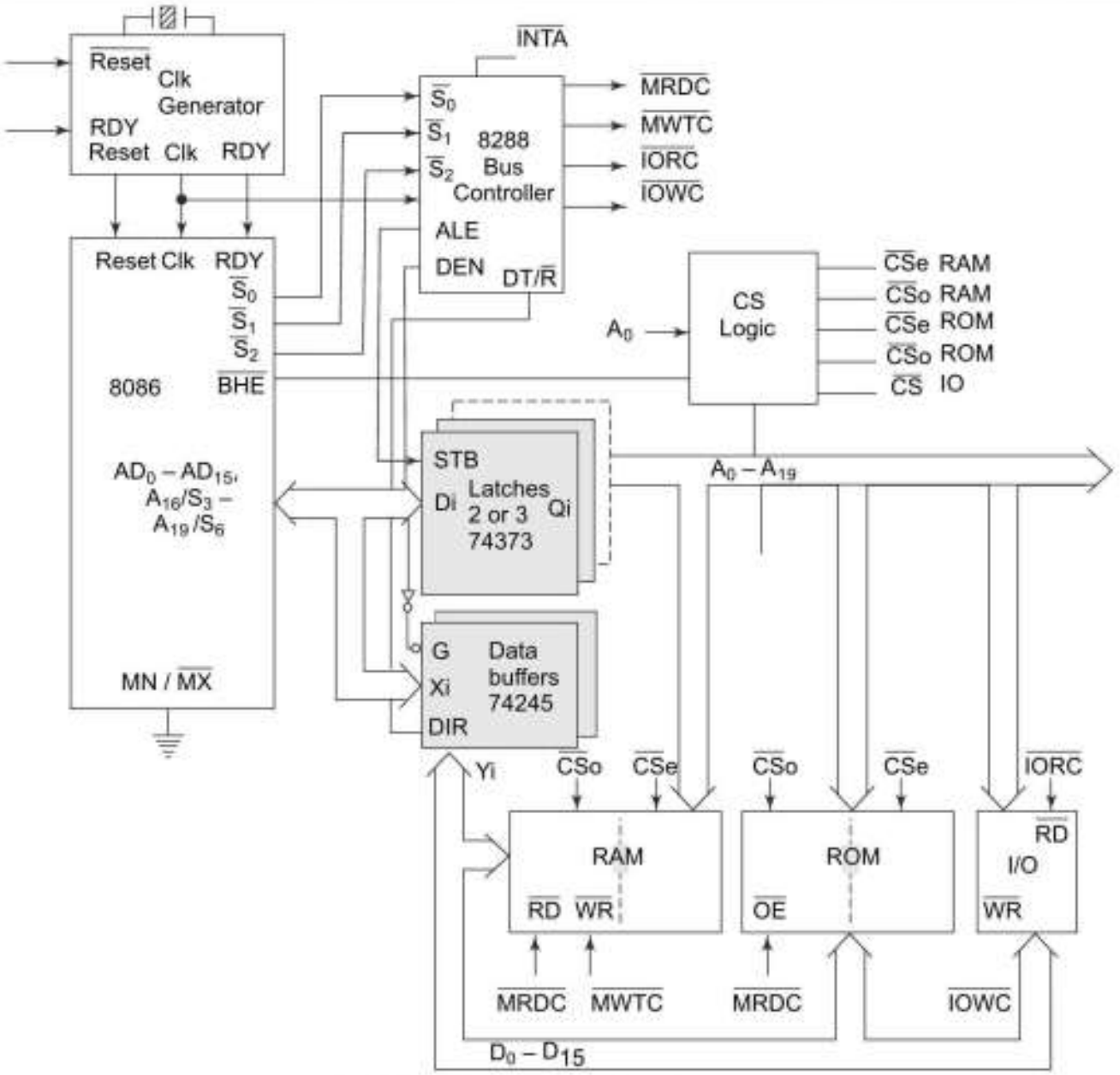


Fig. 1.15 *Maximum Mode 8086 System*

- The bus controller chip has input lines $\overline{S2}$, $\overline{S1}$, $\overline{S0}$ and CLK. These inputs to 8288 are driven by CPU.
- It derives the outputs ALE, DEN, DT/$\overline{R}$, $\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$ and $\overline{AIOWC}$. The AEN, IOB and CEN pins are specially useful for multiprocessor systems.
- $\overline{AEN}$ and IOB are generally grounded. CEN pin is usually tied to +5V. The significance of the MCE/$\overline{PDEN}$ output depends upon the status of the IOB pin.
- $\overline{INTA}$ pin used to issue two interrupt acknowledge pulses to the interrupt controller or to an interrupting device.

- $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$ are I/O read command and I/O write command signals respectively . These signals enable an IO interface to read or write the data from or to the address port.
- The $\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$ are memory read command and memory write command signals respectively and may be used as memory read or write signals.
- All these command signals instructs the memory to accept or send data from or to the bus.
- Here the only difference between in timing diagram between minimum mode and maximum mode is the status signals used and the available control and advanced command signals.

- $\overline{S0}$, $\overline{S1}$, $\overline{S2}$ are set at the beginning of bus cycle.8288 bus controller will output a pulse as on the ALE and apply a required signal to its DT / $\overline{R}$ pin during T1.
- In T2, 8288 will set $\overline{DEN}$=1 thus enabling transceivers, and for an input it will activate $\overline{MRDC}$ or $\overline{IORC}$. These signals are activated until T4.
- For an output, the $\overline{AMWC}$ or $\overline{AIOWC}$ is activated from T2 to T4 and $\overline{MWTC}$ or $\overline{IOWC}$ is activated from T3 to T4.
- The status bit $\overline{S0}$ to $\overline{S2}$ remains active until T3 and become passive during T3 and T4.
- If read input is not activated before T3, wait state will be inserted between T3 and T4.

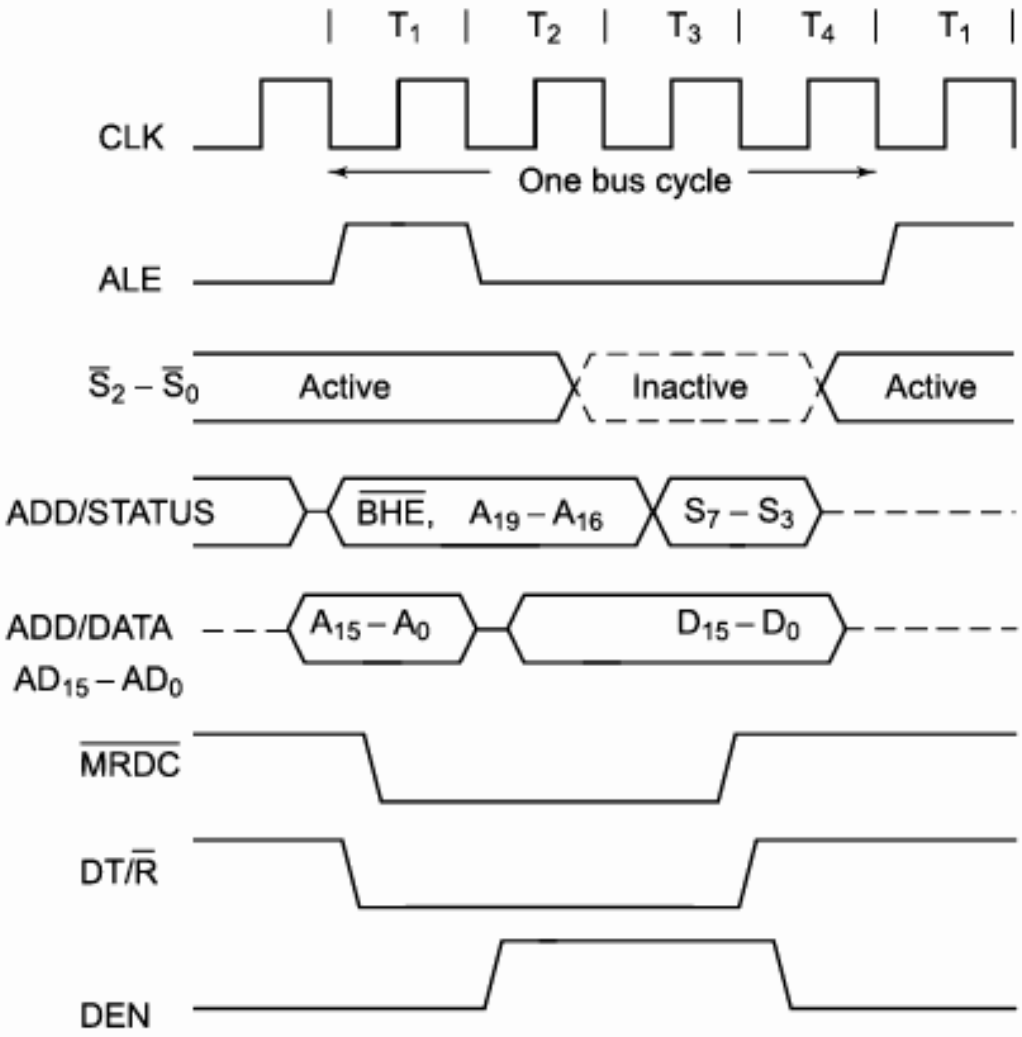


Fig. 1.16 (a) *Memory Read Timing in Maximum Mode*

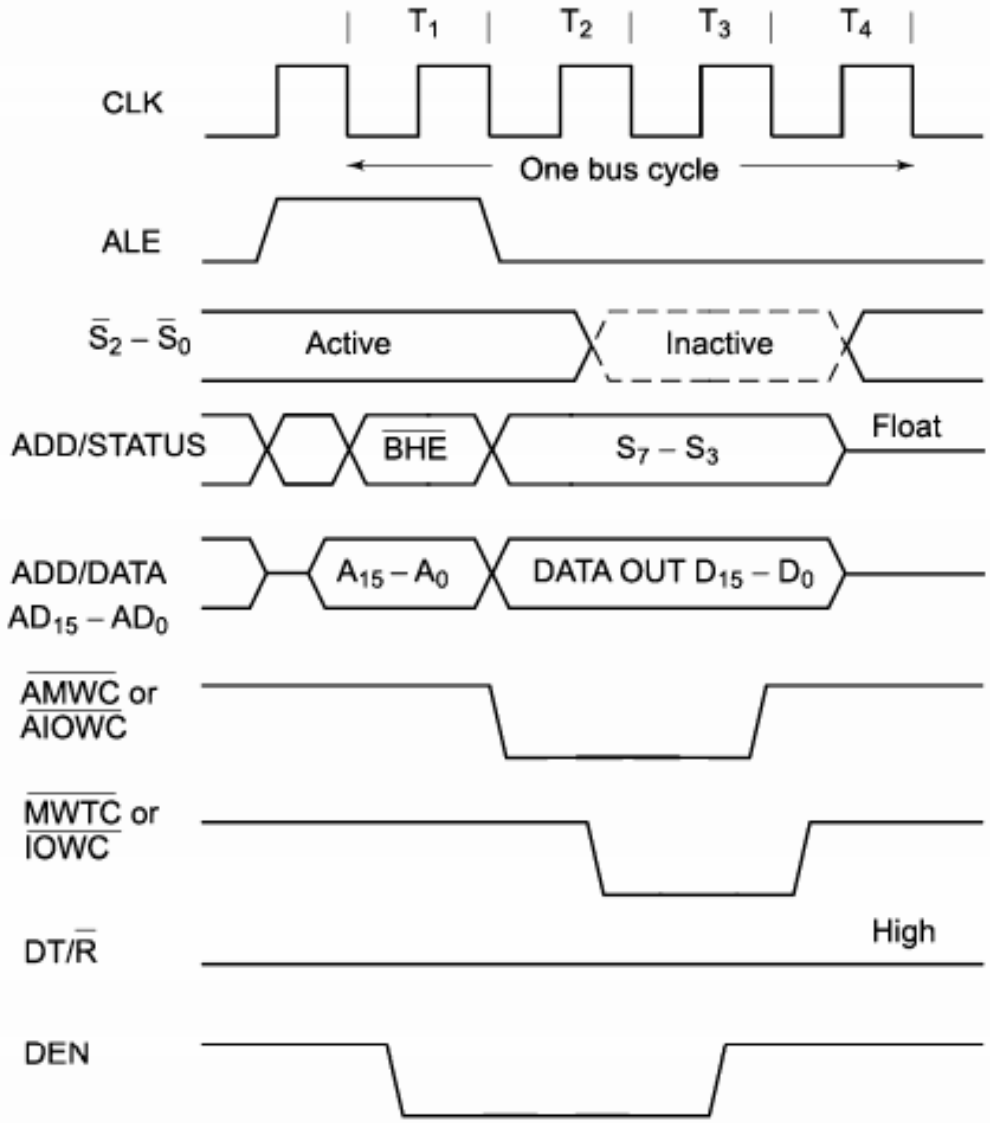


Fig. 1.16(b) *Memory Write Timing in Maximum Mode*

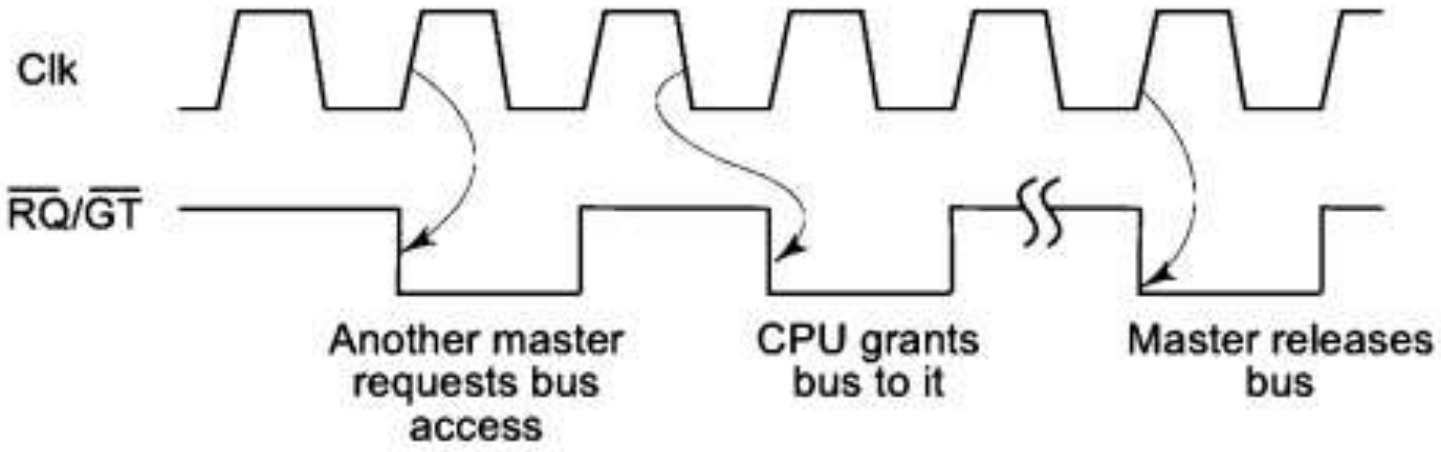


Fig. 1.16 (c) $\overline{RQ}/\overline{GT}$ ***Timings in Maximum Mode***