Amiga

A500_R6

Rev.1.37 (02.09.2012)

CSR{_IKASUZE!-AI-NO-DOKI-DOKIPENGUIN-LAND-MD}

Revision History

REV	DESCRIPTION	DATE	APRVL	MANAGER
-	For older Revision 3/5 boards			
	see schematic 312511-01			
1	PCB Revision 6a/7 Production	04/27/89	GRR	

ECO Log

ECO NUMBER	DESCRIPTION	DATE
880283	Add E Clock Termination	03/03/89

Jumpers and Stuff

REF	TYPE	DESCRIPTION	PAGE
JP1	BLOB	Keyboard Reset	7
JP2	BLOB	Memory Addr. C0 vs 08	2
JP3	BLOB	Expansion RAS Select	3
JP4	BLOB	NTSC/PAL Selection	2
JP5	BLOB	Genlock Clock Select	2
JP6	BLOB	7MHz Clock Option	7
JP7	BLOB	Expansion/Tick Option	3/6
JP8	BLOB	Light Pen Port Select	6
JP10	BLOB	RS232 Audio I/O Cutout	4
JP11	BLOB	TTL vs RS170 Comp Sync	5

Connectors

REF	TYPE	DESCRIPTION	PAGE
CN1	DB9P	Mouse/Joystick 1	2
CN2	DB9P	Mouse/Joystick 2	2
CN3	RCA-J	Right Audio Output	4
CN4	RCA-J	Left Audio Output	4
CN5	DB23S	External Floppy	7
CN6	DB25P	RS232 Serial Port	6
CN7	DB25S	Parallel Printer Port	6
CN8	SQ DIN	Power Supply Connector	8
CN9	DB23P	Video Output	5
CN10	RCA-J	Composite Video	5
CN11	DIL-34	Internal Floppy Signal	7
CN12	SIL-4	Internal Floppy Power	8
CN13	SIL-8	Keyboard Connector	6
P1	EDGE86	Expansion Connector	7
CNX	RA-56H	Mem. Exp. Main-Board	3

Signal Glossary

SIGNAL	DESCRIPTION (AREA)	PAGES
28MHZ	28.63636 MHz Master Clock	2
7MHZ	7.15909 MHz Processor Clock	2,5
A[23:1]	Processor Address Bus (68000)	2,3,7
ACK	Data Acknowledge (Parallel Port)	6
AS	Address Strobe (68000)	2,7
AUDIN	Audio Input (RS232 Port)	4,6
AUDOUT	Audio Output (RS232 Jack)	4,6
BEER	Bus Error (68000)	2,7
BG	Bus Grant (68000)	2,7
BGACK	Bus Grant Acknowledge (68000)	2,7
BLISS	Blitter Slowdown (Chips)	2
BLIT	Chip Memory Access (Chips)	2,7
BR	Bus Request (68000)	2,7
BUSY	Device Busy (Parallel Port)	6
CASL/U	Column Address Strobe (DRAM)	2,3
CCK/CCKQ	Color Clock / Quadrature (Chips)	2,4,7
CDAC	7.15909 MHz Quadrature Clock (Chips)	2,5,7
CHNG	Media Change (Floppy)	6,7
CLKRD/WR	Read-Time Clock Read / Write (RTC)	2,9
COMP	Monochrome Composite Video (Video)	5
CSYNC	Composite Sync (Video)	2,5
CTS	Clear to Send (RS232 Port)	6
D[15:0]	Processor Data Bus (68000)	2,3,6,7
DIR	Step Direction (Floppy)	6,7
DKRD	Disk Read Data (Floppy)	4,7
DKWD	Disk Write Data (Floppy)	4,7
DKWE	Disk Write Enable (Floppy)	4,7
DMAL	Chip DMA Request Line (Chips)	2,4
DRA[8:0]	DRAM Address Bus (DRAM)	2,3
DRD[15:0]	DRAM Data Bus (DRAM)	2,3,4,5
DSR	Data Set Ready (RS232 Port)	6
DTACK	Data Transfer Acknowledge (68000)	2,3,7
DTR	Data Terminal Ready (RS232 Port)	6
E	Peripheral Enable Clock (68000)	2,6,7
EXTICK	Expansion Present / RTC Tick	2,3
FC[2:0]	Function Code (68000)	2,7
FIRE0/1	Fire Button 0/1 (Joysticks)	2,5,6
HLT	Processor Halt (68000)	2,7
HSYNC	Horizontal Sync (Video)	2,5,6
INDEX	Index Pulse (Floppy)	6,7
INT[2,3,6]	Interrupt Request (Chips)	2,4,6,7
IORESET	I/O Reset	6,7
IPL[2:0]	Interrupt Priority Level (68000)	2,4,7
KBCLOCK	Keyboard Clock (Keyboard)	6
KBDATA	Keyboard Data (Keyboard)	6
KBRESET	Keyboard Reset (Keyboard)	6
LDS/UDS	Upper / Lower Data Strobes (68000)	2,7
LED	Power On LED / Audio Filter Disable	4,6
LEFT/RIGHT	Left Right Audio (Audio)	4

SIGNAL	DESCRIPTION (AREA)	PAGES
LPEN	Light Pen Trigger (Joysticks)	2,6
MTR	Motor On (Floppy)	4,6
MTR0	Motor On - Drive 0 (Floppy)	4,6,7
M0V/M0H	Mouse 0 Quadrature V/H (Joysticks)	5
M1V/M1H	Mouse 1 Quadrature V/H (Joysticks)	5
OVL	Overlay ROM over RAM	2,6
OVR	Override System Decoding	2,7
PIXELSW	Genlock Pixel Switch (Video)	5
POT0X/0Y	Pot Lines 0 X/Y (Joysticks)	4,5
POT1X/1Y	Pot Lines 1 X/Y (Joysticks)	4,5
POUT	Paper Out (Parallel Port)	6
PPD[7:0]	Parallel Port Data (Parallel Port)	6
RAMEN	RAM Enable (Chips)	2
REGEN	Chip Register Enable (Chips)	2
RAS0/1	Row Address Strobe (DRAM)	2,3
RDY	Drive Ready (Floppy)	6,7
RESET	General Reset	6,7
RGA[8:1]	Register Address Bus (Chips)	2,4,5
R/G/B	Red / Green / Blue (Video)	5
RI	Ring Indicate (RS232 Port)	6
ROMEN	ROM Enable (ROM)	2,3
RTS	Request to Send (RS232 Port)	6
RST	Processor Reset (68000)	2,4,7
RXD	Receive Data (RS232 Port)	4,6
RW	Processor Read/Write (68000)	2,6,7
SEL	Select (Parallel Port)	6
SEL[3:0]	Drive Select (Floppy)	4,6,7
SIDE	Side Select (Floppy)	6,7
STEP	Step In/Out Command (Floppy)	6,7
TRK0	Track Zero Sense (Floppy)	6,7
TXD	Transmit Data (RS232 Port)	4,6
VMA	Valid Memory Address (68000)	2,6,7
VPA	Valid Peripheral Address (68000)	2,7
VSYNC	Vertical Sync (Video)	2,5,6
WE	Write Enable (DRAM)	2,3
WPROT	Write Protect Sense (Floppy)	6,7
XCLK	External Genlock Clock (Video)	2,5
XCLKEN	External Clock Enable (Video)	2,5
XRDY	External Data Ready	2,5

Key Components

REF	CHIP	DESCRIPTION	PAGE
U1	68000	68000 Processor	2
U2	8370	Fat Agnus - NTSC	2
	8371	Fat Agnus - PAL	alt
	8372	Agnus HR	alt
U3	8364	Paula	4
U4	8362	Denise	5
	8373	Denise HR	alt
U5	5719	Gary	2,4
U6	asst	ROM 128Kx16, 200 nS	3
U7-8	8520	Amiga VIA, 1 MHz	6
U14	LF347	BiMOS Op-Amp	4
	TL084	BiMOS Op-Amp	alt
U38	1488	EIA Line Driver	4
U39	1489	EIA Line Receiver	4
U42	NE555	Timer	7
U16-19	asst	DRAM 1Mx1, 150 nS	3
U20-23	asst	DRAM 1Mx1, 150 nS	9
X1	OSC	TTL 28.63636 MHz NTSC	2
	OSC	TTL 28.37512 MHz PAL	alt
HY1	asst	Video Hybrid	5

ATTEMPT TO FORCE NODE NUMBERS VIA SEQUENCE

VCC +12V -12V +VID AUDIO EXP +5X +12X

A PAGE FOR SHARON AND VONNIE TO USE

DRAWN BY: G. Robbins DATE 04/27/89
CHKD:
ENGR: GRR 09/09/88
APPR:
USED ON C/A500 NEXT ASSY 312006

Commodore

Schematic A500 R6a/7
C/A500 Main Board
"Rock Lobster"

SIZE C 312007 REV 1
SCALE SHEET 1 OF 8
PATH: /USER/B52_LIB/ROCK_LOBSTER_REV6.X SHEET1

A500 Rev 6a/7 PCB

Note: Various components are for EMI Control
and may be loaded with funny things...

JP2 controls where expansion ram maps to:
A23 -> C00000 (default), A19 -> 080000

XR1 is added to some boards per ECO 880283

Rock Lobster

04/27/89

A500 Rev 6a/7 PCB

PROCESSOR AND OTHER USEFUL COMPONENTS

DRAWN BY: G. Robbins	DATE 04/27/89	Commodore	
CHKD:			
ENGR: GRR	09/09/88	Schematic A500 R6a/7 C/A500 Main Board "Rock Lobster"	
APPR:			
USED ON C/A500	NEXT ASSY 312006	SIZE C	312007 REV 1
		SCALE	SHEET 2 OF 8

PATH: /USER/B52_LIB/ROCK_LOBSTER.REV6.X SHEET2

A500 Rev 6a/7 PCB

CNX

RAM

U34

U35

JP7A

JP3

ROM

SPARE

Note: RP105-RP111 are optional internal bus termination, and are not normally loaded.

Note: JP3 swaps internal vs. expansion ram

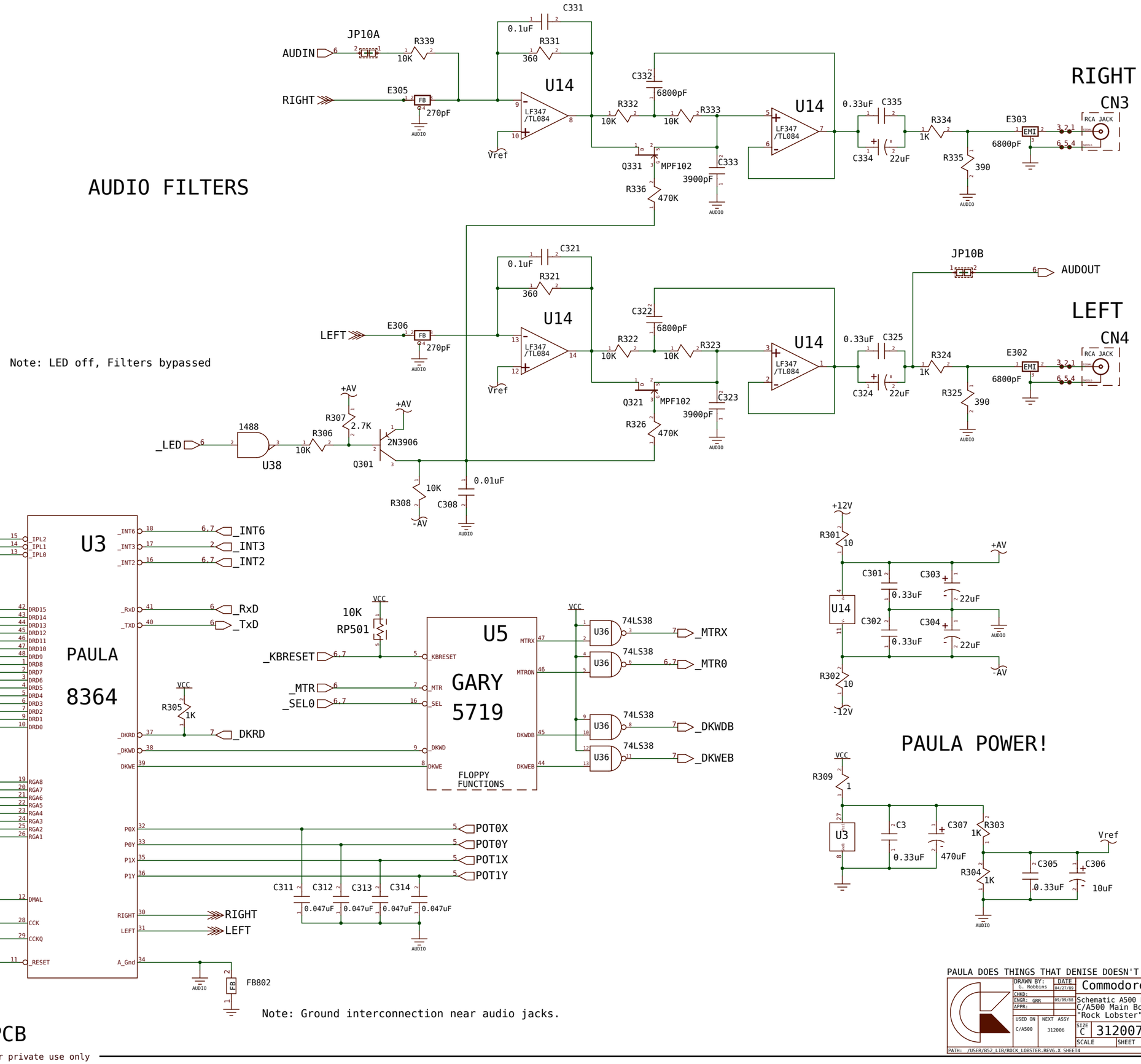
MEMORY AND...WELL, I USED TO REMEMBER

DRAWN BY: G. Robbins	DATE 04/27/89	Commodore
CHKD:		Schematic A500 R6a/7 C/A500 Main Board "Rock Lobster"
ENGR: GRR	09/09/88	
APPR:		
USED ON C/A500	NEXT ASSY 312006	SIZE C 312007 REV 1
		SCALE SHEET 3 OF 8

PATH: /USER/B52_LIB/ROCK_LOBSTER.REV6.X_SHEET3

AUDIO FILTERS

Note: LED off, Filters bypassed



Note: Ground interconnection near audio jacks.

A500 Rev 6a/7 PCB

PAULA DOES THINGS THAT DENISE DOESN'T

DRAWN BY: G. Robbins	DATE 04/27/89	Commodore	
CHKD:			
ENGR: GRR	09/09/88	Schematic A500 R6a/7 C/A500 Main Board "Rock Lobster"	
APPR:			
USED ON C/A500	NEXT ASSY 312006	SIZE C	312007 REV 1
		SCALE	SHEET 4 OF 8

PATH: /USER/B52 LIB/ROCK LOBSTER.REV6.X SHEET4

A500 Rev 6a/7 PCB

Note: Pin 2 and 21 of HY1 connected internally

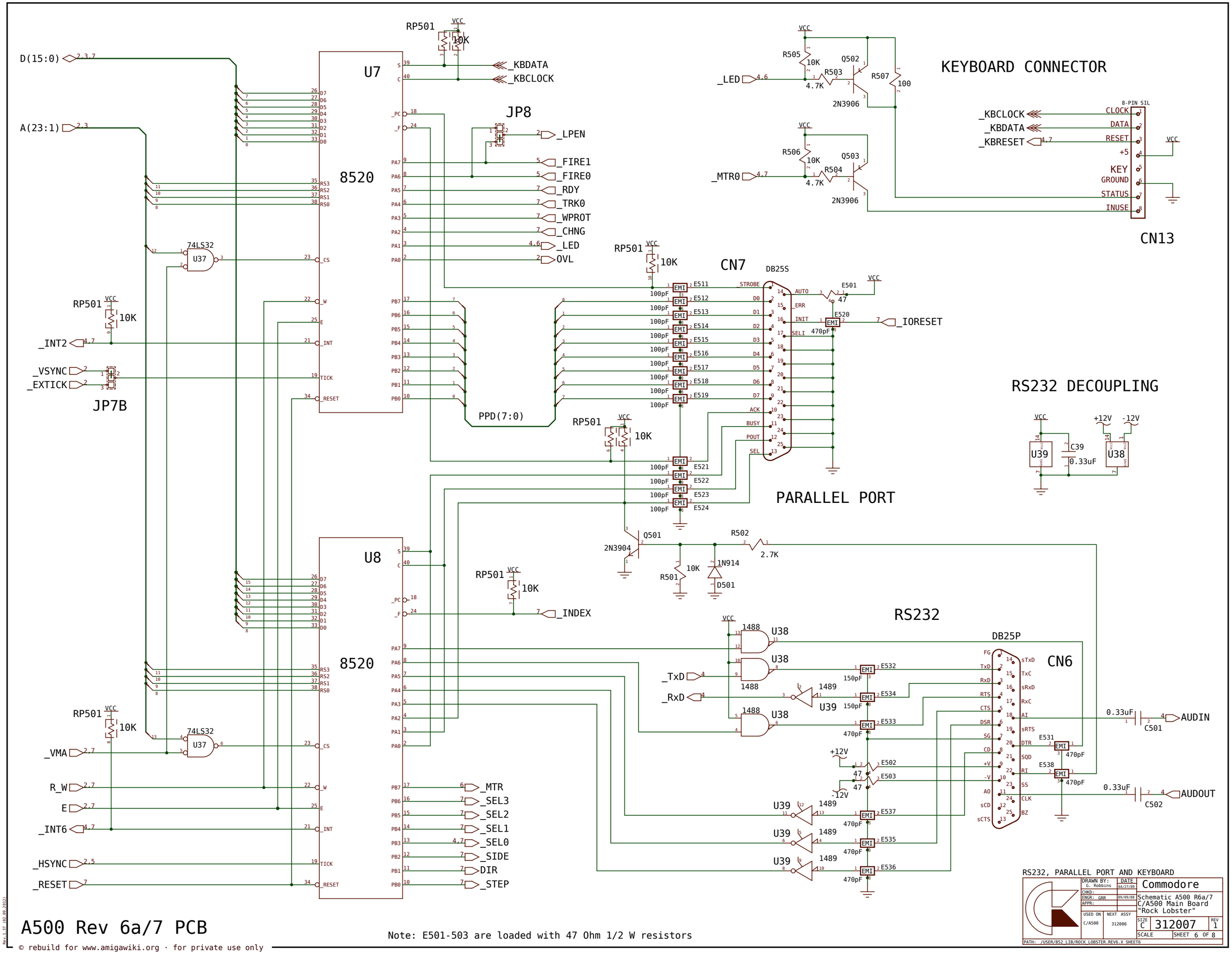
Note: Components designated as Exxx may be loaded with EMI fliters, ferrite beads or resistors!

Note: RP405 Not Used

Note: R409 Controls Composite output level for 390229-01 Hybrid.

DENISE IS PRETTY MUCH INTO VIDEO...

DRAWN BY: G. Robbins	DATE 04/27/89	Commodore
CHKD:		
ENGR: GRR	09/09/88	Schematic A500 R6a/7 C/A500 Main Board "Rock Lobster"
APPR:		
USED ON: C/A500	NEXT ASSY: 312006	SIZE C · 312007 · REV 1
PATH: ~b52_lib/rock_lobster.rev6_sheet5		SCALE · SHEET 5 OF 9



A500 Rev 6a/7 PCB

Note: E501-503 are loaded with 47 Ohm 1/2 W resistors

EXPANSION

P1

P1A P1B

JP6

7MHz 2

CDAC 2

_OVR 2

_INT2 4.6

A(23:1) 2,3,6

D(15:0) 2,3,6

0.01uF E702 VCC

0.01uF E703 -12V

0.01uF E704 +12V

_CONFIG

XC3 47pF

XC2 47pF

XC1 47pF

2 _CCKQ

2 _CCK

2 XRDY

4,6 _INT6

2 _FC(2:0)

2,4 _IPL(2:0)

2 _BEER

2 _VPA

2,6 E

2,6 _VMA

2,4,7 _RST

2 _HLT

2 _BR

2 _BGACK

2 _BG

2 _DTACK

2,6 R_W

2 _LDS

2 _UDS

2 _AS

EXTERNAL FLOPPY

CN5

DB23S

_RDY 6,7 — 100pF E611 — RDY

_DKRD 4,7 — 100pF E612 — RD

_MTRX 4 — 100pF E613 — MTRX

_SEL2 6 — 100pF E614 — SEL2

_IORESET 6,7 — 100pF E615 — RESET

_CHNG 6,7 — 100pF E616 — CHNG

SIDE E617 100pF 6,7 _SIDE

WPROT E618 100pF 6,7 _WPROT

TRK0 E619 100pF 6,7 _TRK0

WE E620 100pF 4,7 _DKWEB

WD E621 100pF 4,7 _DKWDB

STEP E622 100pF 6,7 _STEP

DIR E623 100pF 6,7 DIR

SEL3 E624 100pF 6 _SEL3

SEL1 E625 100pF 6,7 _SEL1

INDEX E626 100pF 6,7 _INDEX

+12V E602 0.01uF

VCC E601 0.01uF

CN11

CN11 CN11B

_CHNG 6,7 — 2 _CHNG — 1

4 _MTRON — 3

6 _INUSE — 5

_INDEX 6,7 — 8 _INDEX — 7

_SEL0 4,6,7 — 10 _SEL0 — 9

_SEL1 6,7 — 12 _SEL1 — 11

14 _SEL2 — 13

_MTR0 4 — 16 _MTRON — 15

DIR 6,7 — 18 DIR — 17

_STEP 6,7 — 20 _STEP — 19

_DKWDB 4,7 — 22 _WD — 21

_DKWEB 4,7 — 24 WE — 23

_TRK0 6,7 — 26 _TRK0 — 25

_WPROT 6,7 — 28 WPROT — 27

_DKRD 4,7 — 30 _RD — 29

_SIDE 6,7 — 32 _SIDE — 31

_RDY 6,7 — 34 _RDY — 33

INTERNAL FLOPPY

U37

_RST 2,4,7 — 74LS32 — 6 _RESET

74LS32 — 6,7 _IORESET

U37

JP1

Q711 2N3904

1K R713

4,6 _KBRESET

POWER UP RESET

VCC — C42 0.33uF — U42

R711 1M

R712 47K

C711 0.1uF

C712 10uF

U42 NE555 TRIG THRESH OUT DISCH VC RST

VCC — 0.01uF C713

FLOPPY DISK AND EXPANSION CONNECTORS

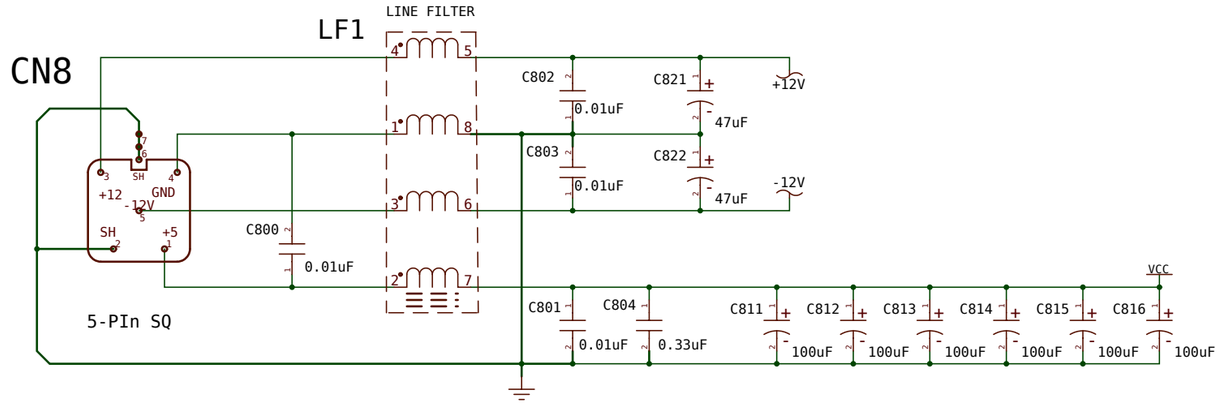
DRAWN BY: G. Robbins	DATE 04/27/89	Commodore
CHKD:		Schematic A500 R6a/7
ENGR: GRR	09/09/88	C/A500 Main Board
APPR:		"Rock Lobster"
USED ON: C/A500	NEXT ASSY: 312006	SIZE C 312007 REV 1
		SCALE SHEET 7 OF 8

PATH: /USER/BS2_LIB/ROCK_LOBSTER.REV6.X_SHEET7

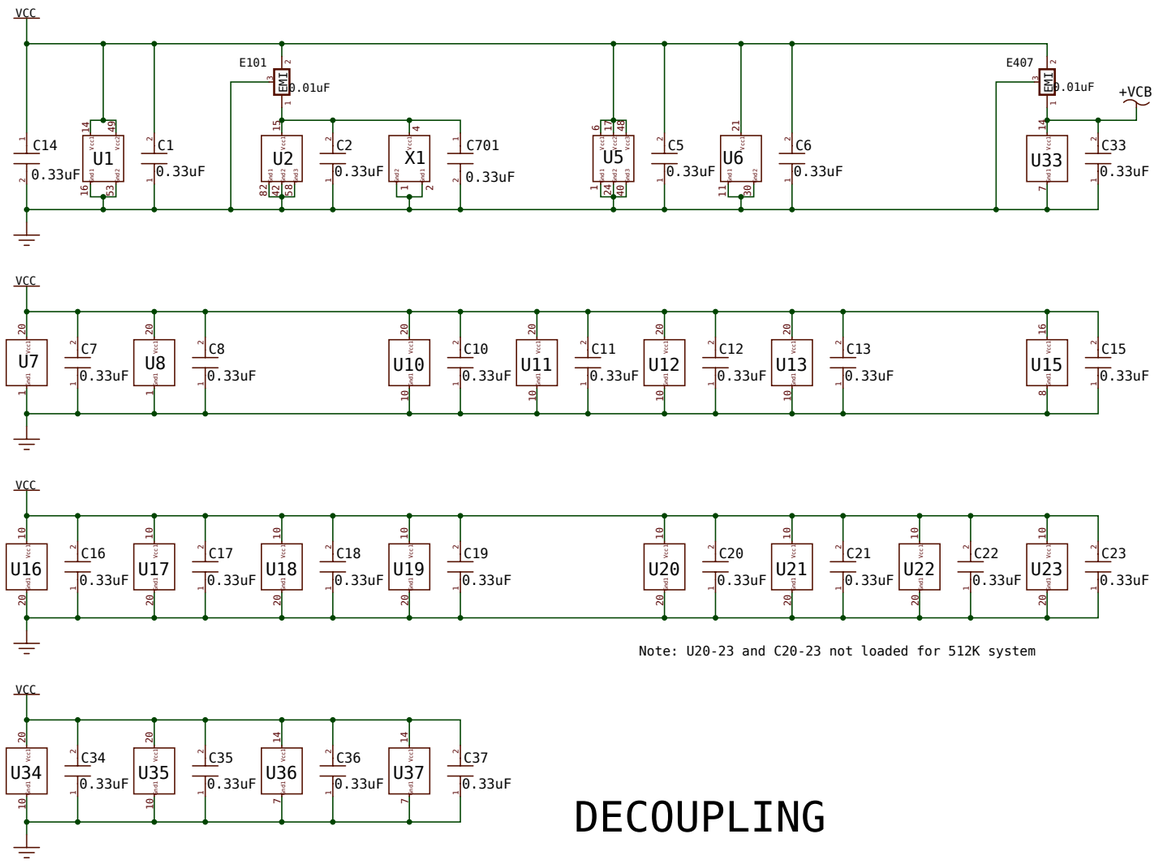
Rev:1.37 (03.09.2012)

A500 Rev 6a/7 PCB

POWER INPUT



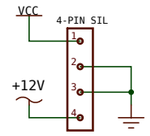
NOTE: HEAVY LINES INDICATE A
SINGLE POINT CONNECTION



Note: U20-23 and C20-23 not loaded for 512K system

DECOUPLING

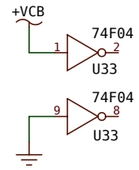
FLOPPY POWER



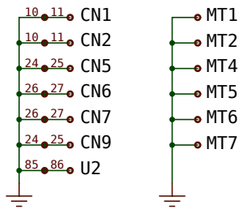
CN12

Note: Some drives are +5 only...

SPARES



GROUNDED HOLES, &c.



A500 Rev 6a/7 PCB

POWER DISTRIBUTION AND DECOUPLING

DRAWN BY: G. Robbins	DATE 04/27/89	Commodore	
CHKD:			
ENGR: GRR	09/09/88	Schematic A500 R6a/7 C/A500 Main Board "Rock Lobster"	
APPR:			
USED ON: C/A500	NEXT ASSY: 312006	SIZE C	312007 REV 1
		SCALE	SHEET 8 OF 8

PATH: /USER/B52_LIB/ROCK_LOBSTER.REV6.X SHEET6

Rev:1.37 (02.09.2012)

Cake

04/27/89

A501 Rev 6c PCB

Notes: Some configurations of this RAM expansion
require mods to rev 3 and 5 A500 boards
and/or use of the Agnus HR 2MB bond-out.

U1-U4 are generic 256K-bit x 4 120 nS DRAM
RP911,RP912 are optional DRD Termination
C10 is optional A8/RAS Setup Time Control
TP9 is Clock Calendar Frequency Test Point

Revision History

REV	DESCRIPTION	DATE	APRVL	MANAGER
1	Production	03/19/89	GRR	

ECO History

ECO NUMBER	DESCRIPTION	DATE

Configuration Options

	A	B
on-board	512K	2M
on A501	512K	-
U1-U4	256Kx4	1Mx4
Agnus	Fat/HR	HR (2M)
JP1	1-2	-
JP9	1-2,1-2	1-1,2-2

CNY

CNY CNY1 +5X

XDRD(15:0)

RP911 4.7Kx9* +5X

RP912 4.7Kx9* +5X

256Kx4 DRAM U1 XX4256-15

256Kx4 DRAM U2 XX4256-15

256Kx4 DRAM U3 XX4256-15

256Kx4 DRAM U4 XX4256-15

RP901 68

RP902 68

RP903 68

JP1 _XCLKCS _XOE _XCASL _XCASU _XRAS0 _XRAS1 _XWE

JP3

JP2

JP9 JP9A

XD(15:0)

XA(23:1)

_XCLKRD

_XCLKWR

+12X

74F27 74F86 U12 U13 47pF* C10

74LS163A U11

Refresh"Feature"

Real Time Clock

XD(15:0) XA(23:1) _XCLKRD _XCLKWR _XCLKCS

U9 MSM6242B STD.P

R912 10K TP9

R915 R914 10K

6.8-45pF TC9

Y9 32768Hz

C911 22pF

Real Time Power

BT9 3/60DK Ni-Cd 4.5V 100mAH

R911 470 D911 1N914 D912 1N914 R913 470

C913 4.7uF

C9 0.1uF

C902 C903 100uF

C1 C2 C3 C4 C11 C12 C13 0.33uF

Decoupling...

512K/2M-BYTE RAM EXPANSION AND CLOCK

DRAWN BY: G. Robbins	DATE 04/27/89	Commodore	
CHKD:			
ENGR: GRR	03/26/89	Schematic, A501 R6c	
APPR:		C/A501 512K Memory	
		1Mbit Flavor"Cake"	
USED ON C/A500	NEXT ASSY 312987	SIZE C	312988 REV 1
		SCALE	SHEET 1 OF 1

PATH: /USER/B52_LIB/CAKE.REV6.X_SHEET1

Rev1.27 (02.09.2021)