Digital System Design
Final Project

Objective

Design a system that find the maximum number in an array. The project includes the design of and finite state machine (FSM), and a Datapath.

Description

In this project, you will design a System that find the maximum number in a array; the project includes the design of FSM and the datapath. The following pseudo code describes the operation of the system:

```
int MAXIMUM (int startaddr, int n){

      int max = mem[startaddr];

      for (i = 0; i< n; i++){

            if(mem[startaddr + i] > max){
                  max = mem[startaddr + i];
            }
      }
}
```

Figure 0: Pseudocode of function MAXIMUM

The project implements the pseudo code of function MAXIMUM show in the Figure-0. In this code, *startaddr* and *n* are provided by an external source and remain stable through the calculation loop.

A *testbench* is necessary to validate your design, which is provided by the professor. The testbench provides the *mclk*, *reset*, *startaddr*, *n*, and *start* signals. After the start signal is provided, *startaddr* and *n* will remain constant. The testbench waits for the *done* signal. After the *done* signal the testbench waits 1 clock cycle and confirms the output signal is correct.

Operation

The FSM is responsible for active/deactive the signals to proper operation of the datapath. In addition to the pseudo code, the design includes hand shake pins "*start*" and "*done*". *Star*t tells the FSM to start a calculation loop. The FSM provides the *done* signal when it is IDLE. *Star*" and *done* are handle by the FSM.

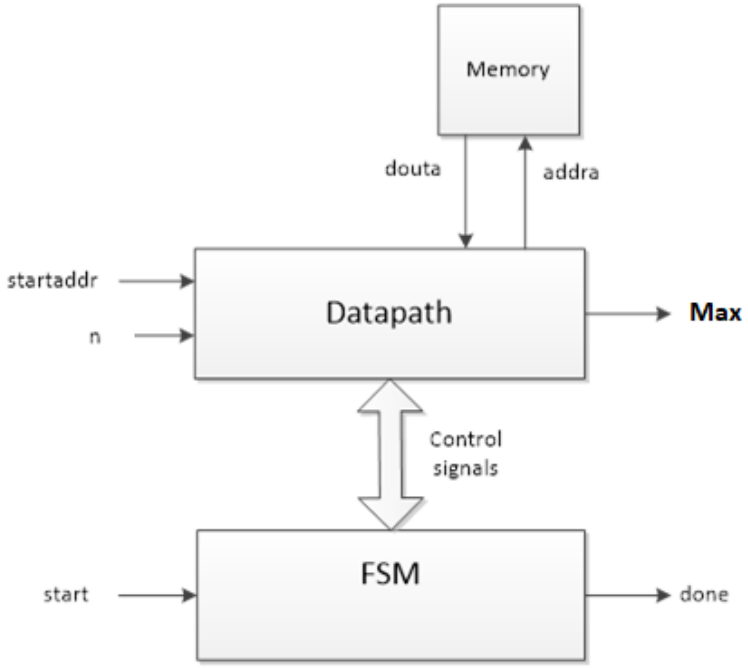

Figure 1: top view of system

The *mclk* and *reset* signals are not shown in the figure 1. Design your project in the following steps.

1. Datapath
    a. Diagram of the datapath
    b. List all blocks required for the datapath. Provide a short description of each.
    c. List the inputs and outputs of the data path. For each input list the source of the input. For each output list the destination.
    d. Implement your datapath in Verilog
2. FSM
    a. Draw a ASM chart
    b. List the inputs and outputs of the FSM. For each input list the source of the input. For each output list the destination

c. Implement the FSM using the ASM chart in Verilog.

3. Create a memory module called *mem.v* with depth = 256 and width = 16. Initialize the memory with the file provided (*ram.coe*)
4. Complete the top module provided (*top.v*) this module is incomplete you need to instances the FSM and Datapath module.
5. Validate your design using the testbench. For full credit your datapath should produce "0" ERROR messages in the simulation console window.

Report

Your report should be well-written in English or Spanish. This project has to be submitted via e-mail to the address: jyeckle@bayamon.inter.edu in the due date. A complete project consists of verilog files (*.v) and a report in word format. You have to zip all files to the single file, which has to be attached to the e-mail.

1) Datapath design:
    a. List all blocks required for the datapath . Provide a short description of each (why are necessary?).
    b. List the inputs and outputs of the data path. For each input list the source of the input. For each output list the destination
    c. List a set of verilog modules(*.v) used to implement the datapath with a short description.
    d. Draw a datapath diagram
2) FSM design:
    a. List of all ports. Include the port name, direction, vector width, *and* a 1-2 sentence description of each port.
    b. Include an ASM chart of your FSM.
3) Testing and Troubleshooting: Describe all major problems that you found
4) Conclusion:
    a. Analyze your design in terms of how the results met your expectations.
    b. Things you tried which did not work.
    c. Recommendations for future work (What might you do differently next time?)

Submission

In the deadline date you should submit the following:

1. An electronic copy to jyeckle@bayamon.inter.edu before class. In the email subject put: *'Digital systems project: YOUR LASTNAME'*. Attach a zip-file with format: *"lastname_project.zip"* that contains the following:
    a. Report in word format
    b. All Verilog files.
    c. README file where you should show a table with the files and description for each one.

ATTENTION: *It is very important that your code is your original work and not just a copy of your classmate's code (or Internet).*