8MP-LPDDR4-1A SOM (3V3/1V8 IO)

Table of Content

Revision History

Rev. Code	Date	By	Description
A	2019-10-25	Frank	Initial version
1A	2021-02-25	Andrew Bushuev	This respin is based on the initial design made by Frank @ 2019-10-25 © This respin includes: o) Build-time selectable IO voltages for various interfaces (incl. backward compatibility to the NXP SOM) o) I2C level shifter between the CPU and the PMIC o) 4 symmetrical SMD standoffs for the heatsink o) 0402 caps instead of 0201 around the DRAM and PMIC o) PCB stackup change from 6 layers to 8 o) PCB thickness change from 1.1mm to 1.6mm

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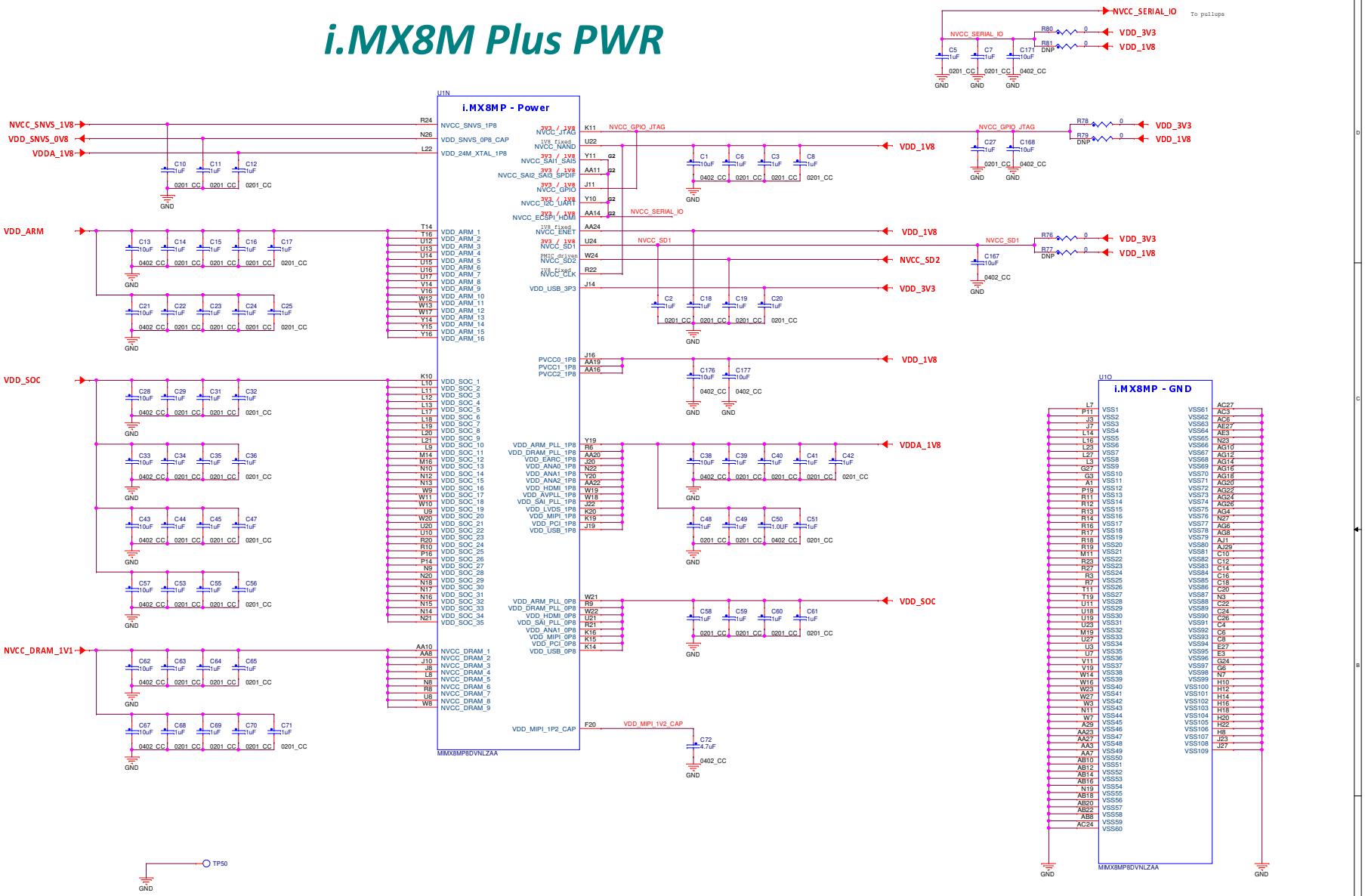
ICAP Classification: CP: IUO: PUBL

Designer: Andrew Bushuev	Drawing Title: 8MP-LPDDR4-1A	
Drawn by: Andrew Bushuev	Page Title: Title and Revision History	
Approved: Iain Galloway	Size: C	Document Number: 8MP-LPDDR4-1A — Rev: 1.0
	Date: Friday, February 25, 2022	Sheet 1 of 10

i.MX8M Plus PWR



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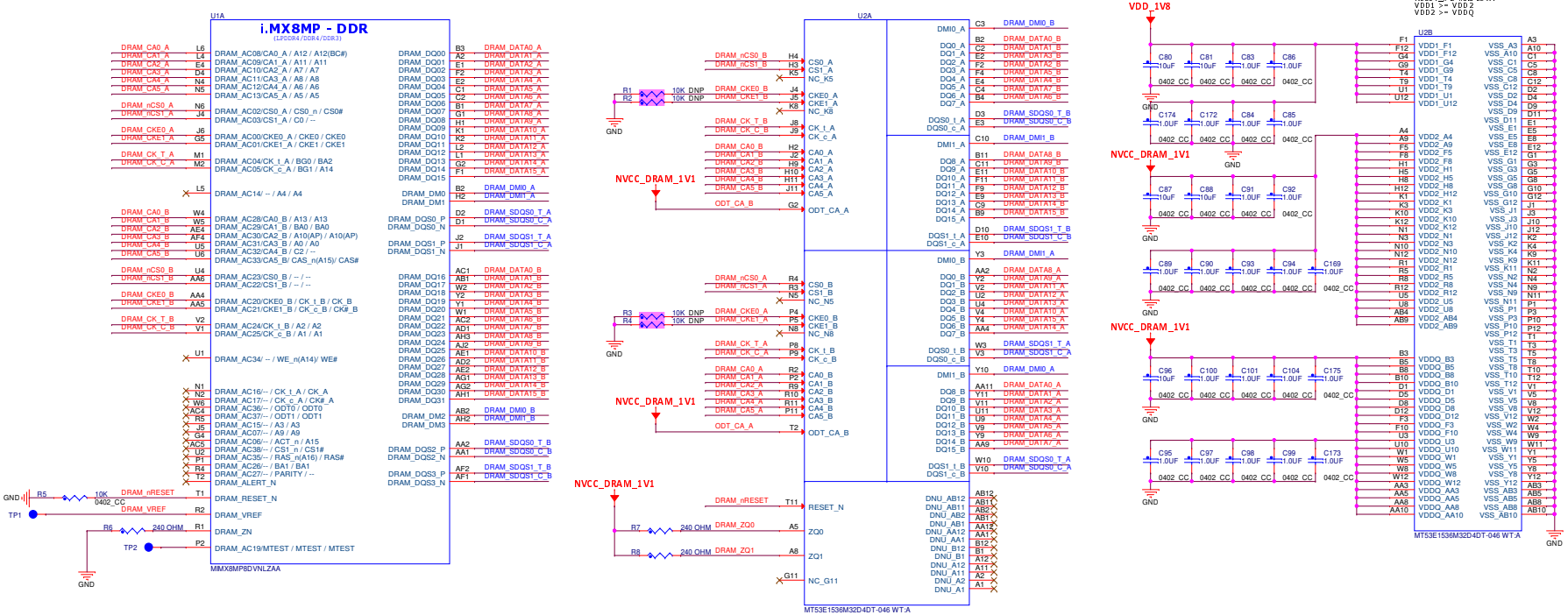
Designer: Andrew Bushuev	Drawing Title: **8MP-LPDDR4-1A**		
Drawn by: Andrew Bushuev	Page Title: **CPU PWR**		
Approved: Iain Galloway	Size: C	Document Number: 8MP-LPDDR4-1A	Rev: 1.0
	Date: Friday, February 25, 2022	Sheet 2 of 10	

LPDDR4 6GB



Data Bus

Pin Name	LPDDR4	DDR4
DRAM_DQS0_P	DQS0_t_A	DQS_t_A
DRAM_DQS0_N	DQS0_c_A	DQS_c_A
DRAM_DM0	DMI0_A	DM_n_A / DBI_n_A
DRAM_DQ00	DQ0_A	DQ0_A
DRAM_DQ01	DQ1_A	DQ1_A
DRAM_DQ02	DQ2_A	DQ2_A
DRAM_DQ03	DQ3_A	DQ3_A
DRAM_DQ04	DQ4_A	DQ4_A
DRAM_DQ05	DQ5_A	DQ5_A
DRAM_DQ06	DQ6_A	DQ6_A
DRAM_DQ07	DQ7_A	DQ7_A
DRAM_DQS1_P	DQS1_t_A	DQS_t_A
DRAM_DQS1_N	DQS1_c_A	DQS_c_A
DRAM_DM1	DMI1_A	DM_n_A / DBI_n_A
DRAM_DQ08	DQ8_A	DQ0_A
DRAM_DQ09	DQ9_A	DQ1_A
DRAM_DQ10	DQ10_A	DQ2_A
DRAM_DQ11	DQ11_A	DQ3_A
DRAM_DQ12	DQ12_A	DQ4_A
DRAM_DQ13	DQ13_A	DQ5_A
DRAM_DQ14	DQ14_A	DQ6_A
DRAM_DQ15	DQ15_A	DQ7_A
DRAM_DQS2_P	DQS0_t_B	DQS_t_B
DRAM_DQS2_N	DQS0_c_B	DQS_c_B
DRAM_DM2	DMI0_B	DM_n_B / DBI_n_B
DRAM_DQ16	DQ0_B	DQ0_B
DRAM_DQ17	DQ1_B	DQ1_B
DRAM_DQ18	DQ2_B	DQ2_B
DRAM_DQ19	DQ3_B	DQ3_B
DRAM_DQ20	DQ4_B	DQ4_B
DRAM_DQ21	DQ5_B	DQ5_B
DRAM_DQ22	DQ6_B	DQ6_B
DRAM_DQ23	DQ7_B	DQ7_B
DRAM_DQS3_P	DQS1_t_B	DQS_t_B
DRAM_DQS3_N	DQS1_c_B	DQS_c_B
DRAM_DM3	DMI1_B	DM_n_B / DBI_n_B
DRAM_DQ24	DQ8_B	DQ0_B
DRAM_DQ25	DQ9_B	DQ1_B
DRAM_DQ26	DQ10_B	DQ2_B
DRAM_DQ27	DQ11_B	DQ3_B
DRAM_DQ28	DQ12_B	DQ4_B
DRAM_DQ29	DQ13_B	DQ5_B
DRAM_DQ30	DQ14_B	DQ6_B
DRAM_DQ31	DQ15_B	DQ7_B

Command/Address

Pin Name	LPDDR4	DDR4
DRAM_RESET_N	RESET_N	RESET_n
DRAM_ALERT_N	MTEST1	ALERT_n / MTEST1
DRAM_AC00	CKE0_A	CKE0
DRAM_AC01	CKE1_A	CKE1
DRAM_AC02	CS0_A	CS0_n
DRAM_AC03	CS1_A	C0
DRAM_AC04	CK_t_A	BG0
DRAM_AC05	CK_c_A	BG1
DRAM_AC06	/	ACT_n
DRAM_AC07	/	A9
DRAM_AC08	CA0_A	A12
DRAM_AC09	CA1_A	A11
DRAM_AC10	CA2_A	A7
DRAM_AC11	CA3_A	A8
DRAM_AC12	CA4_A	A6
DRAM_AC13	CA5_A	A5
DRAM_AC14	/	A4
DRAM_AC15	/	A3
DRAM_AC16	/	CK_t_A
DRAM_AC17	/	CK_c_A
DRAM_AC19	MTEST	MTEST
DRAM_AC20	CKE0_B	CK_t_B
DRAM_AC21	CKE1_B	CK_c_B
DRAM_AC22	CS1_B	/
DRAM_AC23	CS0_B	/
DRAM_AC24	CK_t_B	A2
DRAM_AC25	CK_c_B	A1
DRAM_AC26	/	BA1
DRAM_AC27	/	PARITY
DRAM_AC28	CA0_B	A13
DRAM_AC29	CA1_B	BA0
DRAM_AC30	CA2_B	A10 / AP
DRAM_AC31	CA3_B	A0
DRAM_AC32	CA4_B	C2
DRAM_AC33	CA5_B	CAS_n / A15
DRAM_AC34	/	WE_n / A14
DRAM_AC35	/	RAS_n / A16
DRAM_AC36	/	ODT0
DRAM_AC37	/	ODT1
DRAM_AC38	/	CS1_n
DRAM_ZN	ZQ	ZQ
DRAM_VREF	VREF	VREF

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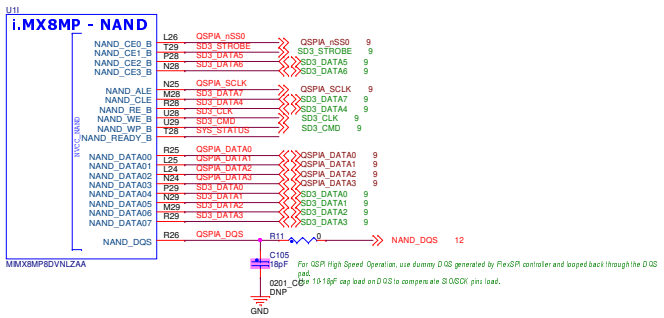
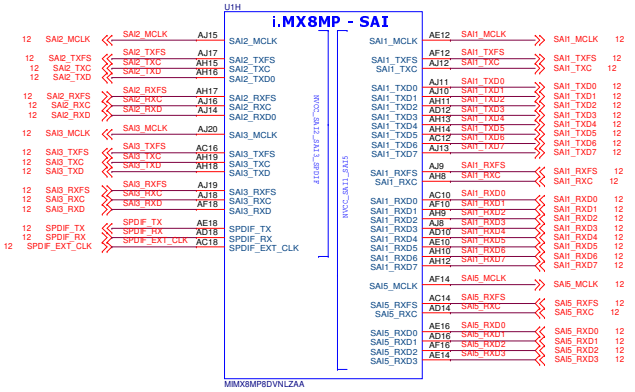
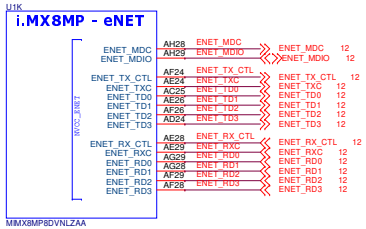
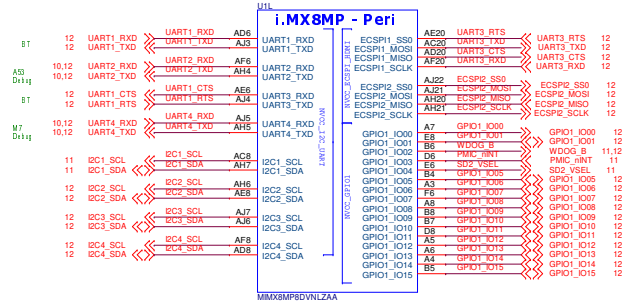
Drawn by: Andrew Bushuev	Page Title: CPU DRAM		
Approved: Iain Galloway	Size C	Document Number 8MP-LPDDR4-1A	Rev 1.0
	Date: Friday, February 25, 2022	Sheet 3 of 10	

i.MX8M Plus IO Interface

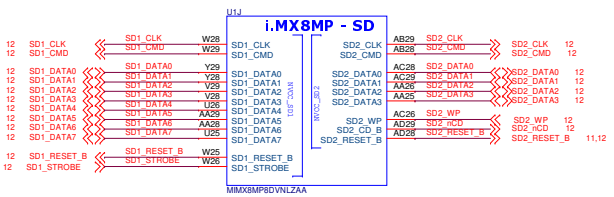


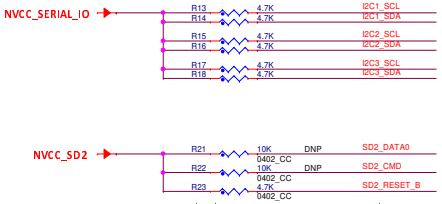




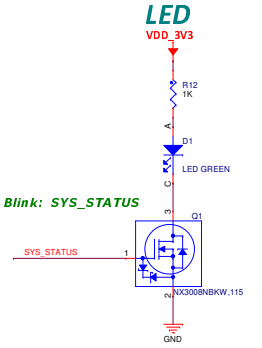


Configure Internal pull up at CPU side, open drain output
Configure Internal pull up at CPU side





External PU is necessary for SD2_RESET_B to enable SD card power as default!



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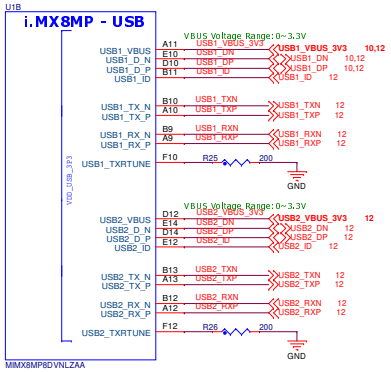
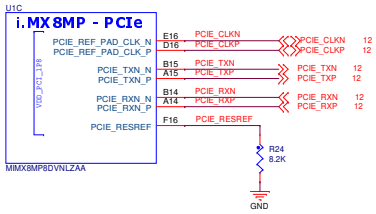
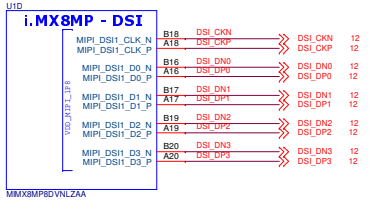
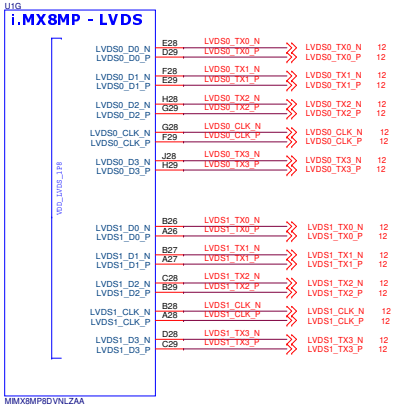
	Date: Friday, February 25, 2022	Sheet 4 of 10

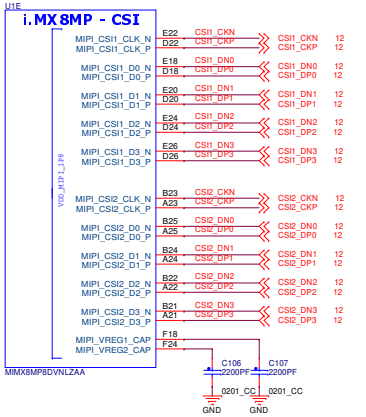
i.MX8M Plus PHYs

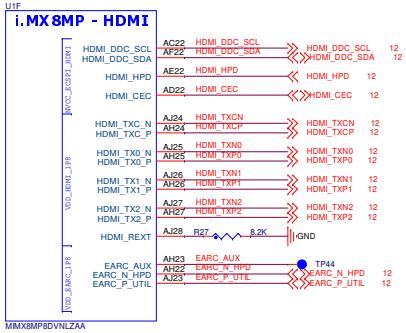












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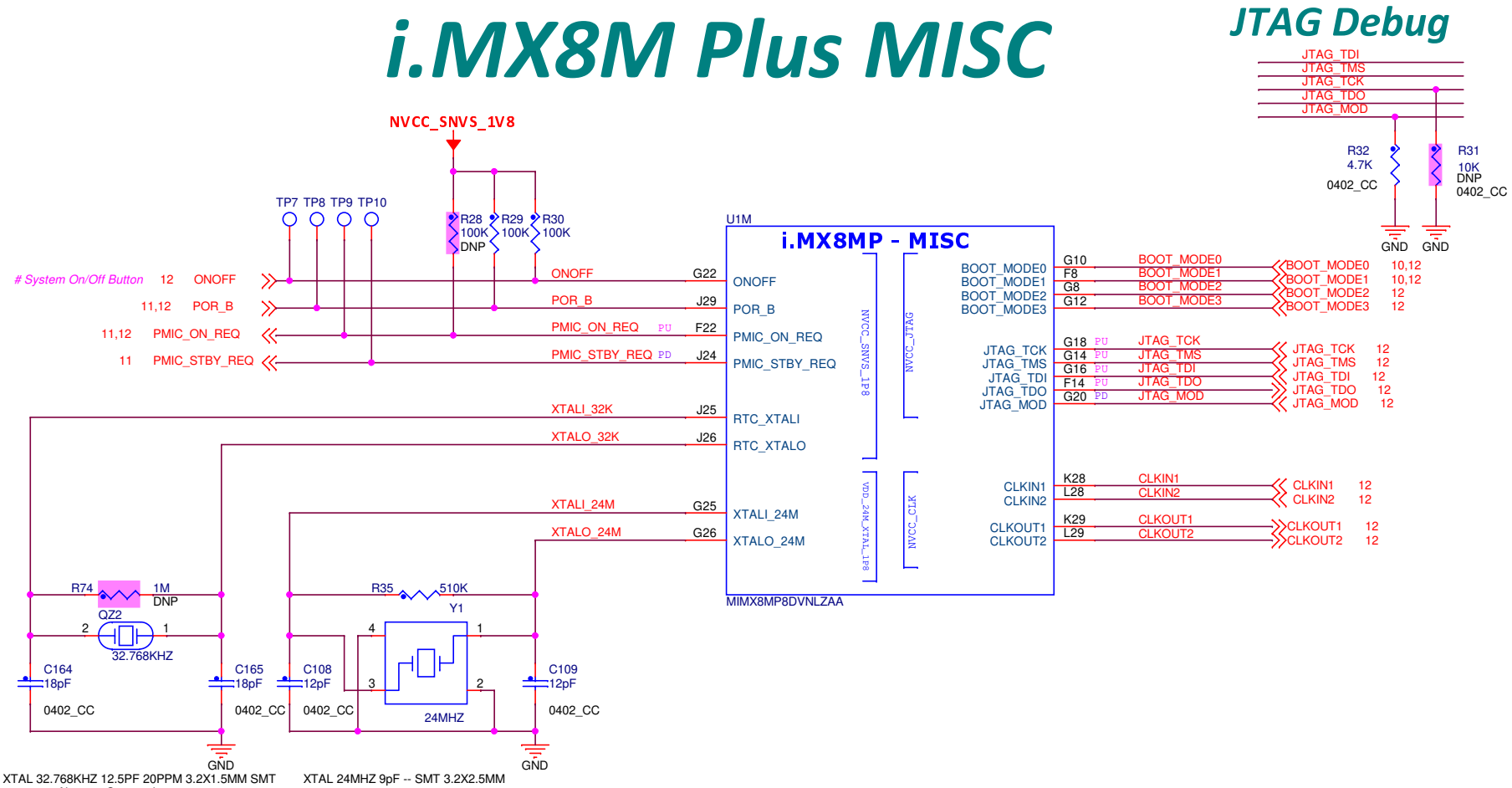
Drawn by: Andrew Bushuev	Page Title: **CPU PHYs**
Approved: Iain Galloway	Size: C; Document Number: 8MP-LPDDR4-1A; Rev: 1.0
	Date: Friday, February 25, 2022; Sheet 5 of 10

i.MX8M Plus MISC



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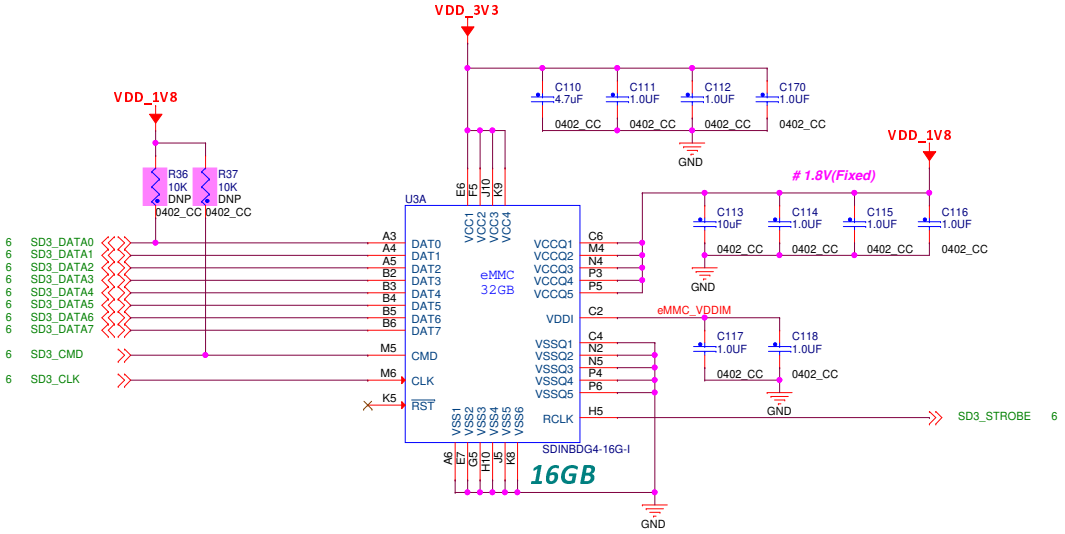
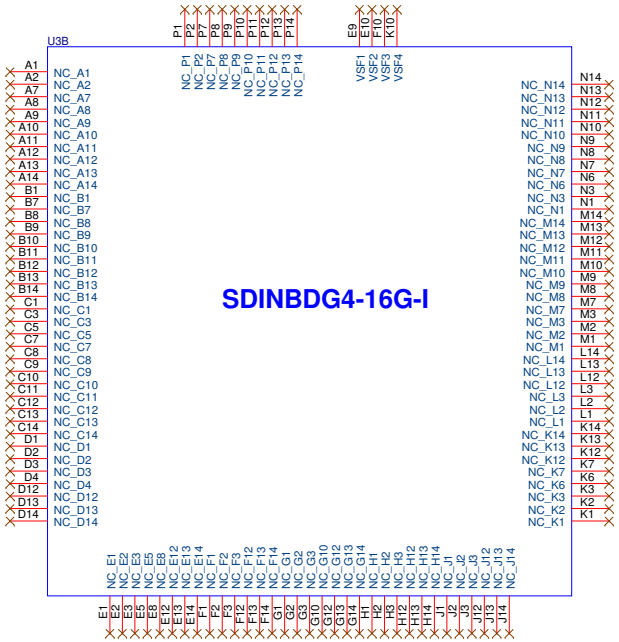
ICAP Classification: CP: ____ IUO: ____ PUBI: ____

Designer: Andrew Bushuev	Drawing Title: **8MP-LPDDR4-1A**		
Drawn by: Andrew Bushuev	Page Title: **CPU MISC**		
Approved: Iain Galloway	Size A4	Document Number 8MP-LPDDR4-1A	Rev 1.0
	Date: Friday, February 25, 2022	Sheet 6 of 10	

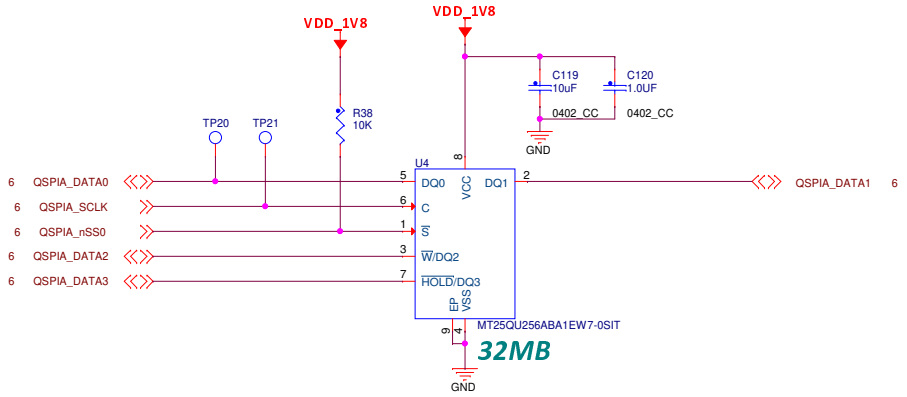
Storage

eMMC5.1





QSPI Flash



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Drawn by: Andrew Bushuev	Page Title: **eMMC/QSPI**	
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	Date: Friday, February 25, 2022	Sheet 7 of 10

Boot Mode

i.MX8M Plus ROM Fuse

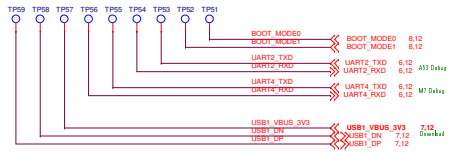
Full Line Address	Physical Address	7	6	5	4	3	2	1	0
0x470[15:0]	0x470[7:0]	OVERRIDE_NAND_PG_PER_BLK_VAL 00 - 32 pages 01 - 64 pages 10 - 128 pages 11 - 32 pages		OVERRIDE_FLEXSPI_BT_SEL 0 - Do not override 1 - Override	OVERRIDE_FLEXSPI_BT_SEL_VAL 00 - FlexSPI Hyperflash 1.8V) 01 - FlexSPI Flash with 4B READ)1x13 default supported) 10 - Default Octal mode (Micron, supported on BOXP 80 already) 11 - Default Octal mode (MXIC, Nice to have)		FLEXSPI_AUTO_PROBE_EN 0 - Disable 1 - Enable	FLEXSPI_AUTO_PROBE_TYPE 00 - Quad/Hi HSR 01 - MXIC Octal 10 - Micron Octal 11 - Adesto Octal	
0x480[15:0]	0x480[7:0]	Reserved	FLEXSPI_DUMMY_CYCLE_SEL				FLEXSPI_FREQ_SEL 000 - 100 MHz 001 - 133 MHz 010 - 166 MHz 011 - 200 MHz 100 - 80 MHz 101 - 20 MHz		
0x480[31:16]	0x480[23:16]	NOC_ID_REMAP_BYPASS	ROM_NO_LOG If blown, ROM will not log event to log buffer	SDP_DISABLE Disable USB serial download	FORCE_BT_FROM_FUSE Boot from programmed fuses, not Boot Mode Pins	FLEXSPI_HOLD_TIME_SEL 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		WDOG_TIMEOUT_SELECT 00 - 2.0s 01 - 1.5s 10 - 1.0s 11 - 0.5s	
0x490[15:0]	0x490[7:0]	USDHC_PWR_EN 0 - No power cycle 1 - Enabled via	EMMC_FAST_BT 0 - Regular 1 - Fast Boot	SDMMC_BUS_WIDTH 00 - 8-bit 01 - 4-bit 10 - 8-bit DDR (MMC 4.4) 11 - 4-bit DDR (MMC 4.4)		SD_SPEED: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104	EMMC_SPEED: 00 - Normal 01 - High	USDHC_VOL_SEL For Normal Boot Mode IO Voltage 0 - 3.3V 1 - 1.8V	USDHC_MFG_VOL_SEL For Mfg Mode IO Voltage 0 - 3.3V 1 - 1.8V
0x490[31:16]	0x490[23:16]	RECOVERY_SDMMC_BOOT_DIS 0 - Enable 1 - Disable	IMG_CNTN_SET1_OFFSET				USDHC_PAD_SION_EN 0 - Disable 1 - Enable	BT_RDC_DISABLE	USDHC_DLL_EN 0 - Disable DLL for SD/eMMC 1 - Enable DLL for SD/eMMC
0x4A0[15:0]	0x4A0[7:0]	SD_CALI_STEP '000' - 1 TBD	USDHC_PWR_INTERVAL 00 - 20ms 01 - 10ms 10 - 5ms 11 - 2.5ms			USDHC_PWR_DELAY 0 - 5ms 1 - 2.5ms	USDHC_PWR_POLARITY 0 - Low 1 - High	USDHC_OVRD_PAD_SETTING_UP1	EMMC_FAST_BT_ACK 0 - Boot Ack Disabled 1 - Boot Ack Enabled
0x4A0[31:16]	0x4A0[23:16]	Reserved							
0x4B0[15:0]	0x4B0[7:0]	Reserved	NAND_GPMI_DDR_DLL_VAL (GPMI Read DDR DLL Target Value) 0000 - 7 0001 - 1 0111 - 0 1111 - 15					USB_SS_ENABLE	NAND_CS_NUM (Nand Number Of Devices) 00 - 1 01 - 2 10 - 4 11 - Reserved
0x4B0[31:16]	0x4B0[23:16]	Reserved	FlexSPI NAND Busy Bit Offset Override			FlexSPI NAND CS Interval 00-100ns 01-200ns 10-400ns 11-50ns		FlexSPI NAND Column Address Width 00-12 01-13 10-14 11-15	

Full Line Address	Physical Address	7	6	5	4	3	2	1	0
0x470[15:0]	0x470[15:8]	BOOT_MODE_FUSES BootRom will retrieve boot mode from these fuses instead of BOOT_MODE pins if * BOOT_MODE_PINS = 0x0 or * BT_FUSE_SEL blown				OVERRIDE_USDHC_BT_SEL 0 - Do not override 1 - Override	OVERRIDE_USDHC_BT_SEL_VAL 00 - uSDHC1 SD 01 - uSDHC1 eMMC 10 - uSDHC2 eMMC 11 - uSDHC3 SD		OVERRIDE_NAND_PG_PER_BLK 0 - Do not override 1- Override
0x480[15:0]	0x480[15:8]	BT_LPB (Core/DDR/Bus) '00'/'01' - LPB Disable '10' - Div by 2 '11' - Div by 4		BT_LPB_POLARITY (G PIO polarity)	ICACHE_DIS L1 I-Cache DISABLE	TZASC_EN	WDOG_EN '0' - Disabled '1' - Enabled	BT_FREQ_SEL (ARM/DDR) 0 - 800 / 800 MHz 1 - 400 / 400 MHz	DCACHE_DIS Disable L1 and L2 D-Cache
0x480[31:16]	0x480[31:24]	ECSPI_PORT_SEL 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3		ECSPI_ADDR_SEL 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)	ECSPI_CS_SEL(SPI only) 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		RECOVER_ECSPI_BOOT_EN '0' - Disabled '1' - Enabled		DCACHE_BYPASS_DIS
0x490[15:0]	0x490[15:8]	USDHC_DLL_SEL 0 - DLL Slave Mode for 1 - DLL Override Mode	SDMMC_DLL_DLY[6:3] Delay target for USDHC DLL, it is applied to slave mode target delay or override mode target delay depends on DLL Override fuse bit value.						
0x490[31:16]	0x490[31:24]	USDHC_OVRD_PAD_SETTING_LOW8[7:0]							
0x4A0[15:0]	0x4A0[15:8]	BT_TOGGLE_MODE	NAND_RCB_SEARCH_COUNT 00 - 2 01 - 2 10 - 4 11 - 8		NAND_TG_PREAMBLE_RD_LATENCY (Toggle Mode 33MHz Preamble Delay, Read Latency) '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111' - 15 GPMICLK cycles			NAND_RST_TIME
0x4A0[31:16]	0x4A0[31:24]	NAND_OVERRIDE_PAD_SETTING[7:0]							
0x4B0[15:0]	0x4B0[15:8]	NAND_READ_RETRY_SEQ_ID[3:0] 0000 - Don't use read retry (RR) sequence embedded in ROM 0001 - Micron 20nm RR sequence 0010 - Toshiba A19nm RR sequence 0011 - Toshiba 19nm RR sequence 0100 - SanDisk 19nm RR sequence 0101 - SanDisk 1ynm RR sequence 0110 - Hynix 20nm A Die RR sequence 0111 - Hynix 26nm RR sequence 1000 - Hynix 20nm B Die RR sequence 1001 - Hynix 20nm C Die RR sequence Others - Reserved				NAND_ROW_ADDR_BYTES 00 - 3 01 - 2 10 - 4 11 - 5		Reserved	Reserved
0x4B0[31:16]	0x4B0[31:24]	RNG_TRIM[7:0]							

i.MX8M Plus Boot Mode

BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	Boot Modes
0	0	0	0	Boot From Internal Fuses
0	0	0	1	USB Serial Download
0	***0***	***1***	***0***	***USDHC3 (eMMC boot only, SD3 8-bit) Default***
0	0	1	1	USDHC2 (SD boot only, SD2)
0	1	0	0	NAND 8-bit single device 256 page
0	1	0	1	NAND 8-bit single device 512 page
0	1	1	0	QSPI 3B Read
0	1	1	1	QSPI Hyperflash 3.3V
1	0	0	0	ecSPI Boot
1	0	0	1	Reserved
1	0	1	0	FLEXSPI Serial NAND 2k page
1	0	1	1	FLEXSPI Serial NAND 4k page
1	1	0	0	Reserved (Boot on I2C connected to BOOT PIN[3:2])
1	1	0	1	Reserved
1	1	1	0	Infinite Loop Mode
1	1	1	1	Test Mode

Manufacturing Test



BOOT_MODE1	BOOT_MODE0	Boot Modes
1	***0***	***USDHC3 (eMMC boot only, SD3 8-bit)***
0	1	USB Serial Download

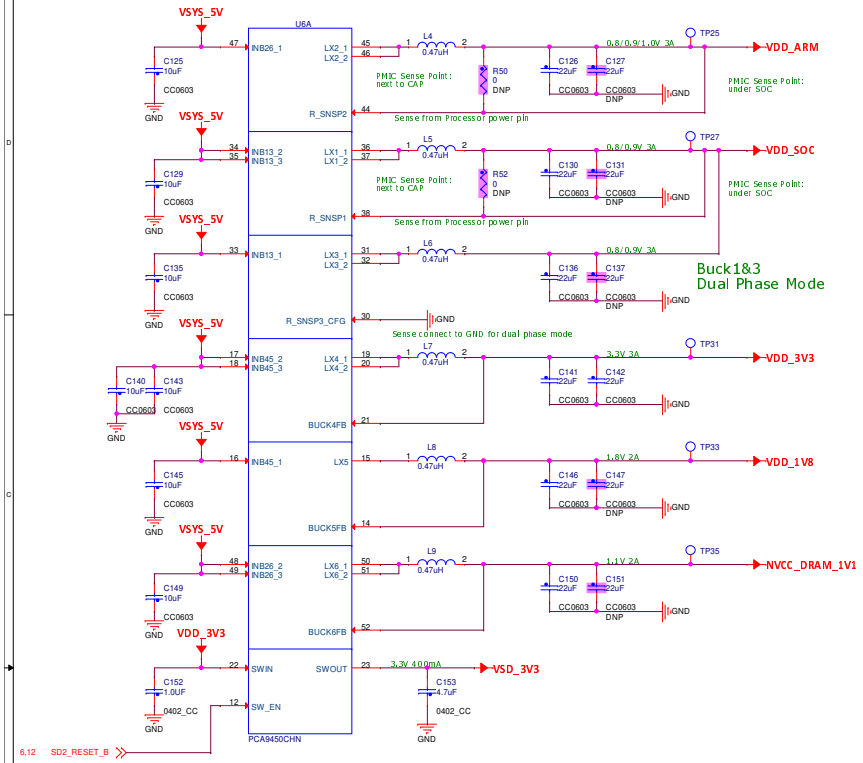
Software Cannery LLC
Electronics Design Accelerator

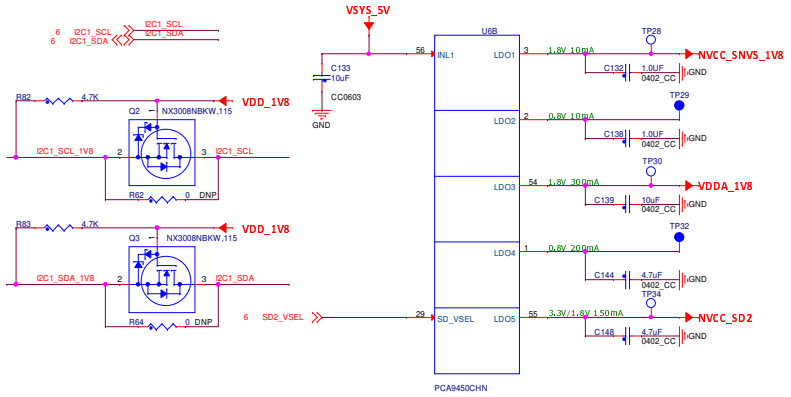
SOFTWARE CANNERY LLC
5651 Palmer Way, Suite B
Carlsbad, CA 92010

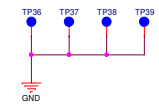
ICAP Classification: CP: IUO: PUBI:

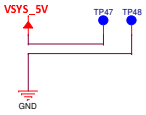
Designer: Andrew Bushuev	Drawing Title: 8MP-LPDDR4-1A		
Drawn by: Andrew Bushuev	Page Title: CPU BOOT MODE		
Approved: Iain Galloway	Size A2	Document Number 8MP-LPDDR4-1A	Rev 1.0
	Date: Friday, February 25, 2022	Sheet 8 of 10	

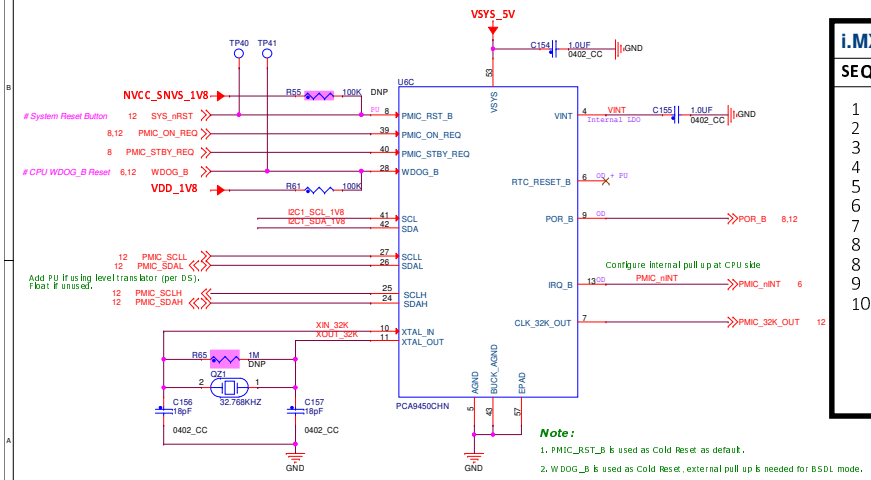
SYS PMIC











i.MX8M Plus LPDDR4 Power Sequence

SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNVS_1V8	LDO1	1.65	1.8	1.95	10
2	32K_INTERNAL	RTC_CLK	--	--	--	--
3	VDD_SOC	BUCK1/3	0.72/0.81	0.85/0.95	0.9/1.0	6000
4	VDD_ARM	BUCK2	0.72/0.81/0.9	0.85/0.95/1.0	0.9/1.0/1.025	3000
5	VDDA_1V8	LDO3	1.71	1.8	1.89	300
6	VDD_1V8/NVCC_xxx	BUCK5	1.65	1.8	1.95	2000
7	NVCC_DRAM_1V1	BUCK6	1.045	1.1	1.155	2000
8	VDD_3V3/NVCC_xxx	BUCK4	3	3.3	3.6	3000
8	VSD_3V3	MUXSW	3	3.3	3.6	400
9	NVCC_SD2	LDO5	3.0/1.65	3.3/1.8	3.6/1.95	150
10	POR_B	POR_B	--	--	--	--

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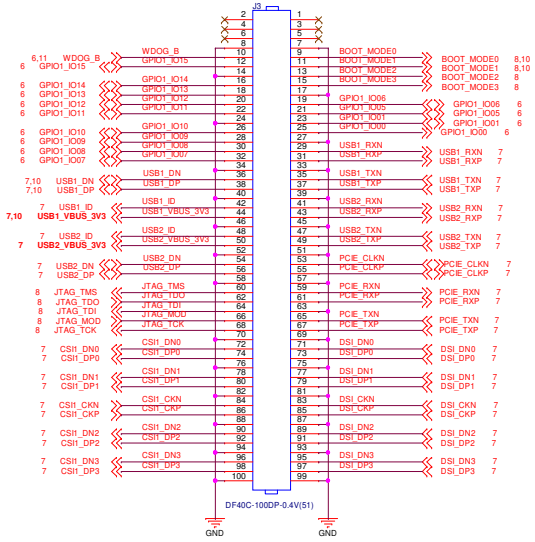
Approved: Iain Galloway	Size: C; Document Number: 8MP-LPDDR4-1A; Rev: 1.0
	Date: Friday, February 25, 2022; Sheet 9 of 10

B2B Connector for CPU Board

Header



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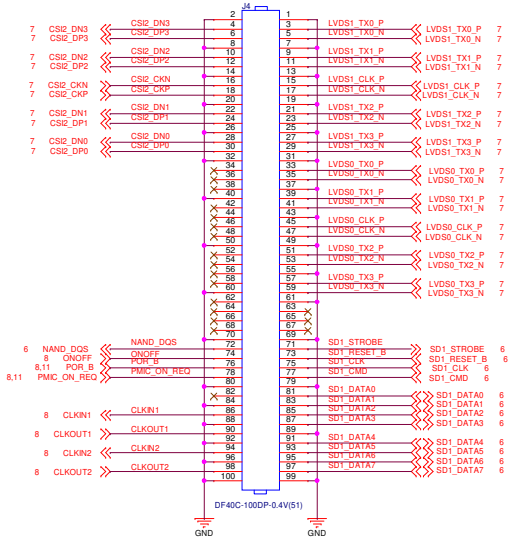

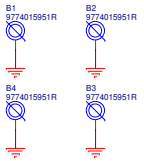

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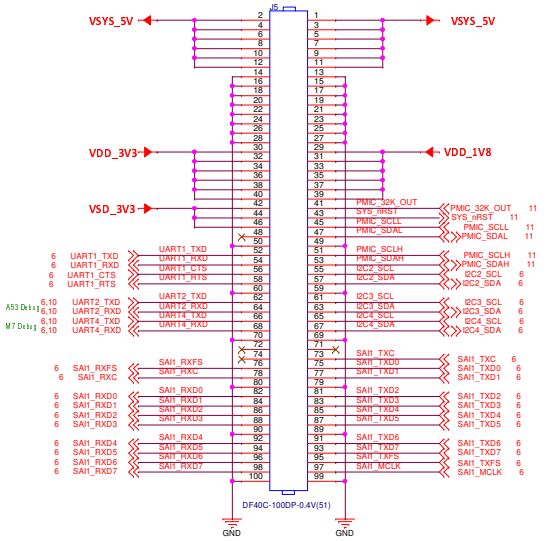

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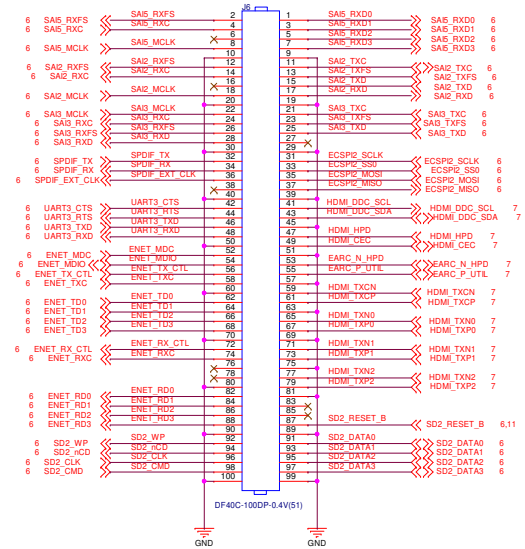

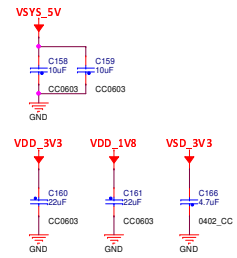

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Drawn by: Andrew Bushuev	Page Title: SOM IO	
Approved: Iain Galloway	Size C	Document Number 8MP-LPDDR4-1A — Rev 1.0
	Date: Friday, February 25, 2022	Sheet 10 of 10