2023

COMPUTER SCIENCE

Paper : CSMC-103

(Advanced Computer Architecture)

Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer ***question nos.*** **1, 2,** and ***any four*** from the rest.

1. Answer ***any five*** questions : 2×5

(a) What is ISA? What are the problem areas that cause a poorly designed instruction set to stall frequently in the pipelined processor?

(b) What is clock skewing? What are the different techniques to resolve clock skewing?

(c) What are the desirable properties of RISC architecture?

(d) What are the desirable properties of a processor to be a member of a multiprocessor system?

(e) What is virtual memory? How a virtual address is mapped into a real address?

(f) Discuss the alternative flow control strategies in any message-passing system.

(g) How many states are there in 4×4 switch including broadcasting and permutation? Comment on the control line format.

2. Answer ***any five*** questions : 4×5

(a) What are the different pipeline hazards? How do you avoid them?

(b) Let A be a $2^k \times 2^k$ matrix stored in row-major order in the main memory. Prove that the transposed matrix A^T can be obtained by performing k-perfect shuffles on A.

(c) Construct an example showing that the loss of a message can cause a deadlock among a set of communication processes.

(d) For a given latency cycle, split out the design steps to get a reservation table. Explain with an example of a latency cycle (2,3,2,5).

(e) Comment on the impact of branch instructions in pipelined architecture with an appropriate set of parameters and an example.

(f) What is memory interleaving? Briefly explain two interleaved memory organizations with suitable assumptions.

(g) A computer has a 16-way interleaved memory. We are required to access a 64 × 64 matrix. Compute the total time required for the access, if the elements are accessed by

(i) row-by-row

(ii) column-by-column.

3. (a) Given that 'c' is the number of 0s in the initial collision vector, show that for any static pipeline and any modified state diagram, the total number of states is no greater than 2^c. Can you make a similar statement for a dynamic pipeline? Justify.

   (b) Considering the following reservation table list all latencies and corresponding cross-collision matrices. Find the MAL for job type A only.

S 1	A	B		A	B
S 2		A		B	
S 3	B		AB		A

5+5

4. (a) Write an algorithm to test whether two input-output pairs of desired connections in an SE-MICN (8×8) will lead to conflicts or not.

   (b) Critically comment on XOR and destination tag routing schemes for MICN.

   (c) Critically comment on blocking inter-connection networks in terms of permutation mapping.

5+2+3

5. (a) Comment on the characteristic features of any systolic array or processors.

   (b) What is meant by systolization?

   (c) Identify all possible hazards for the following code segment with a three-stage pipeline architecture :

$R \leftarrow R + 1$
$ACC \leftarrow ACC + R$
$R1 \leftarrow ACC$
$ACC \leftarrow ACC + R$
$M \leftarrow ACC$

4+2+4

6. (a) Construct an example showing that the loss of a message can cause a deadlock among a set of communication processes.

   (b) Explain the following terms associated with a message-passing mechanism in the multi-computer network :

   (i) Store-and-forward routing at the packet level and wormhole routing at the flit level.

   (ii) Buffering flow control using virtual cut-through routing.

   (c) What is the difference between interrupts, function calls and message passing to transfer the execution flow controls?

4+4+2

7. (a) Critically comment on Data Flow Architecture in contrast to Control Flow Architecture. What are the alternatives to DFA? Compare and contrast them.

(b) Write an algorithm to multiply two matrices A_{nxn} and B_{nx1}. Modify the algorithm to incorporate the spatial locality and temporal locality so that the algorithm can be mapped to a suitable array of processors for systolic architecture. Make suitable assumptions.

(c) What are cache coherence resolution techniques? 4+4+2
