***Karnaugh Map***

1.    Design a 4-bit combinational circuit incremented (the circuit that adds one to a 4-bit binary number). The circuit can be designed using four half adders.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| a | b | c | d | W | X | Y | Z |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

W = ac’ + ab’ + ad’ + a’bcd

= a(b’+c’+d’) + a’bcd

= a(bcd)’ + a’bcd

= a⊕(bcd)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | cd |  |  |  |
| ab | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | 0 | 0 |
| 01 | 0 | 0 | 1 | 0 |
| 11 | 1 | 1 | 0 | 1 |
| 10 | 1 | 1 | 1 | 1 |

X = bc’ + bd’ + b’cd

= b(c’+d’) + b’cd

= b(cd)’ + b’(cd)

= b⊕(cd)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | cd |  |  |  |
| ab | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | 1 | 0 |
| 01 | 1 | 1 | 0 | 1 |
| 11 | 1 | 1 | 0 | 1 |
| 10 | 0 | 0 | 1 | 0 |

Y = c’d + cd’ = c⊕d

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | cd |  |  |  |
| ab | 00 | 01 | 11 | 10 |
| 00 | 0 | 1 | 0 | 1 |
| 01 | 0 | 1 | 0 | 1 |
| 11 | 0 | 1 | 0 | 1 |
| 10 | 0 | 1 | 0 | 1 |

Z = d’

= 1⊕d

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | cd |  |  |  |
| ab | 00 | 01 | 11 | 10 |
| 00 | 1 | 0 | 0 | 1 |
| 01 | 1 | 0 | 0 | 1 |
| 11 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 0 | 1 |