# 김형준 (Hyoungjoon "Paul" Kim)

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## Education

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|---|---|
| From Mar. 2018 | **BS in Electrical & Computer Engineering, Seoul National University**<br>Expected to graduate in Summer 2024<br>**Areas of Interest**: System Programming, Digital Systems Design, Deep Learning<br>**Graduation Project**: Optimising the CNN Architecture with Hardware Design |

## Experience

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| From Mar. 2023 | **FPGA Engineer Intern for NeuroRealityVision**<br>Dongtan, Republic of Korea<br>• Firmware, software development for MIPI-to-Ethernet integration<br>• Bare-metal, standalone FPGA application with interrupt-based workflow<br>• Custom IP development with Verilog-based RTL on Vivado |
| Jan. 2023 to Jun. 2023 | **Student Intern for Dept. of System Semiconductor Engineering**<br>**Seoul National University**, Seoul, Republic of Korea<br>• Worked on CNN Architecture and Hardware Design Optimisation |
| Dec. 2019 to Jul. 2021 | **KATUSA, Human Resources Specialist (42A)**<br>**94th Military Police Battalion**, Pyeongtaek, Republic of Korea<br>• Mandatory military service as a KATUSA Agent<br>(Korean Augmentation To the United States Army) |

## Skills

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| **Engineering** | • Experienced in embedded systems design on multi-purpose SoC FPGAs<br>• Capable of basic RTL hardware design using Verilog<br>• Capable of versatile development with C, C++ and Python<br>• Capable of maintaining HTML/CSS front-end projects<br>• Proficient in typesetting with LaTeX |
| **Languages** | • Korean: Native proficiency<br>• English: Fluent, professional working proficiency |

# Education

### Bachelor's Degree: ECE, SNU

- Expected to graduate in Summer 2024

- **Graduation Project**: Optimising the CNN Architecture with Hardware Design

  - RTL development with Verilog
  - Pipelined, streaming CNN architecture concurrently running multiple convolution layers
  - Improved performance in faster speed and less memory usage without affecting end results

- **Areas of Interest**: System Programming, Digital Systems Design, Deep Learning

  Key Courses Taken:

  - Computer Organisation, Digital Systems Design: Basic RTL simulation and synthesis on FPGAs
  - Operating Systems: System calls, tasks, multithreading and scheduling on the Linux kernel
  - Other Computer-related Courses: Introduction to Data Structures, Introduction to Algorithms

# Experience

### FPGA Engineer Intern: NeuroRealityVision

- Firmware, software development for MIPI-to-Ethernet integration

  - Extract MIPI data from normal camera (CIS) and **event camera** (DVS) sensors to FPGA main memory
  - **PS** (Processing System): Xilinx Gigabit Ethernet Controller (GEM) via embedded ARM Cortex A53 CPU
  - **PL** (Programmable Logic): Xilinx AXI 1G Ethernet Subsystem with multiple AXI DMA blocks
  - Experienced in hardware-firmware communication and interrupt handling mechanisms
  - Experienced in server-side software development for communication with attached FPGA boards
    *ex.* Ethernet packet parsing software to receive MIPI data and reconstruct image stream

- Custom IP development with Verilog-based RTL on Vivado

  - Receive parallel data from attached event camera (DVS) sensor and reorganise for AXI4-Stream
  - Created block designs including RTL blocks to generate IP
  - Basic experience with generating functioning IPs based on block designs in Vivado

### Student Intern: SSAI, SNU

- Research Interest: CNN Architecture and Hardware Design Optimisation

- In tandem with **graduation project** for bachelor's degree from ECE, SNU

### KATUSA Human Resources Specialist

- Mandatory military service as a KATUSA Agent (Korean Augmentation To the United States Army)

- Human Resources Specialist (42A) for RSO HHD, 94th Military Police Battalion at Camp Humphreys