Paul Kim (김형준)

Undergraduate at Electrical & Computer Engineering, Seoul National University

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Education

From Mar. 2018 — **BA in Electrical & Computer Engineering, Seoul National University**

Expected to graduate in Summer 2024

Areas of Interest: System Programming, Digital Systems Design, Deep Learning

Graduation Project: Optimising the CNN Architecture with Hardware Design

Experience

From Mar. 2023 — **FPGA Engineer Intern for NeuroRealityVision**

Dongtan, Republic of Korea

- Firmware, software development for MIPI-to-Ethernet integration
- Bare-metal, standalone FPGA application with interrupt-based workflow
- Custom IP development with Verilog-based RTL on Vivado

Jan. 2023 to Jun. 2023 — **Student Intern for Dept. of System Semiconductor Engineering**

Seoul National University, Seoul, Republic of Korea

- Worked on CNN Architecture and Hardware Design Optimisation

Dec. 2019 to Jul. 2021 — **KATUSA, Human Resources Specialist (42A)**

94th Military Police Battalion, Pyeongtaek, Republic of Korea

- Mandatory military service as a KATUSA Agent
  (Korean Augmentation To the United States Army)

Skills

Engineering

- Experienced in embedded systems design on multi-purpose SoC FPGAs
- Capable of basic RTL hardware design using Verilog
- Capable of versatile development with C, C++ and Python
- Capable of maintaining HTML/CSS front-end projects
- Proficient in typesetting with LaTeX

Languages

- Korean: Native proficiency
- English: Fluent, professional working proficiency

Education

Bachelor's Degree: ECE, SNU

- Expected to graduate in Summer 2024
- **Graduation Project**: Optimising the CNN Architecture with Hardware Design
  - RTL development with Verilog
  - Pipelined, streaming CNN architecture concurrently running multiple convolution layers
  - Improved performance in faster speed and less memory usage without affecting end results
- **Areas of Interest**: System Programming, Digital Systems Design, Deep Learning

  Key Courses Taken:
  - Computer Organisation, Digital Systems Design: Basic RTL simulation and synthesis on FPGAs
  - Operating Systems: System calls, tasks, multithreading and scheduling on the Linux kernel
  - Other Computer-related Courses: Introduction to Data Structures, Introduction to Algorithms

Experience

FPGA Engineer Intern: NeuroRealityVision

- Firmware, software development for MIPI-to-Ethernet integration
  - Extract MIPI data from normal camera (CIS) and **event camera** (DVS) sensors to FPGA main memory
  - **PS** (Processing System): Xilinx Gigabit Ethernet Controller (GEM) via embedded ARM Cortex A53 CPU
  - **PL** (Programmable Logic): Xilinx AXI 1G Ethernet Subsystem with multiple AXI DMA blocks
  - Experienced in hardware-firmware communication and interrupt handling mechanisms
  - Experienced in server-side software development for communication with attached FPGA boards *ex*. Ethernet packet parsing software to receive MIPI data and reconstruct image stream
- Custom IP development with Verilog-based RTL on Vivado
  - Receive parallel data from attached event camera (DVS) sensor and reorganise for AXI4-Stream
  - Created block designs including RTL blocks to generate IP
  - Basic experience with generating functioning IPs based on block designs in Vivado

Student Intern: SSAI, SNU

- Research Interest: CNN Architecture and Hardware Design Optimisation
- In tandem with **graduation project** for bachelor's degree from ECE, SNU

KATUSA Human Resources Specialist

- Mandatory military service as a KATUSA Agent (Korean Augmentation To the United States Army)
- Human Resources Specialist (42A) for RSO HHD, 94th Military Police Battalion at Camp Humphreys