김형준 (Hyoungjoon "Paul" Kim)

Combined Master's & Ph.D at Electrical & Computer Engineering, Seoul National University

Republic of Korea | jsvn7777@snu.ac.kr | thekpaul000@gmail.com

thekpaul | @thekpaul

Education

From Sep. 2024 — **MS & Ph.D in Electrical & Computer Engineering, Seoul National University**
Areas of Interest: Digital Systems Design, Deep Learning

Mar. 2018 to Aug. 2024 — **BS in Electrical & Computer Engineering, Seoul National University**
Areas of Interest: System Programming, Digital Systems Design, Deep Learning
Graduation Project: Optimising the CNN Architecture with Hardware Design

Experience

Mar. 2023 to Jun. 2024 — **FPGA Engineer Intern for NeuroRealityVision**
Dongtan, Republic of Korea

- Firmware, software development for MIPI-to-Ethernet integration
- Bare-metal, standalone FPGA application with interrupt-based workflow
- Real-time Ethernet packet capture and image rendering software development
  - Cross-platform development for Windows and Linux systems
  - Kernel-level optimisations in threading and system calls for faster processing speed
  - Direct modifications to system and network settings
- Custom IP development with Verilog-based RTL on Vivado

Jan. 2023 to Jun. 2023 — **Student Intern for Dept. of System Semiconductor Engineering**
Seoul National University, Seoul, Republic of Korea

- Worked on CNN Architecture and Hardware Design Optimisation

Dec. 2019 to Jul. 2021 — **KATUSA, Human Resources Specialist (42A)**
94th Military Police Battalion, Pyeongtaek, Republic of Korea

- Mandatory military service as a KATUSA Agent
  (Korean Augmentation To the United States Army)

Skills

Engineering

- Experienced in system software engineering for Windows and Linux
- Experienced in embedded systems design on multi-purpose SoC FPGAs
- Capable of versatile development with C, C++ and Python
- Capable of maintaining HTML/CSS front-end projects
- Proficient in typesetting with LaTeX

Languages

- Korean: Native proficiency
- English: Fluent, professional working proficiency

Education

Bachelor’s Degree: ECE, SNU

- Expected to graduate in Summer 2024
- **Graduation Project**: Optimising the CNN Architecture with Hardware Design
  - RTL development with Verilog
  - Pipelined, streaming CNN architecture concurrently running multiple convolution layers
  - Improved performance in faster speed and less memory usage without affecting end results
- **Areas of Interest**: System Programming, Digital Systems Design, Deep Learning
  Key Courses Taken:
  - Computer Organisation, Digital Systems Design: Basic RTL simulation and synthesis on FPGAs
  - Operating Systems: System calls, tasks, multithreading and scheduling on the Linux kernel
  - Other Computer-related Courses: Introduction to Data Structures, Introduction to Algorithms

Experience

FPGA Engineer Intern: NeuroRealityVision

- Firmware, software development for MIPI-to-Ethernet integration
  - Extract MIPI data from normal camera (CIS) and **event camera** (DVS) sensors to FPGA main memory
  - Experienced in hardware-firmware communication and interrupt handling mechanisms
    - **PS** (Processing System): Xilinx Gigabit Ethernet Controller (GEM) and ARM Cortex-A53 Processor
    - **PL** (Programmable Logic): Xilinx AXI 1G Ethernet Subsystem with multiple AXI DMA blocks
  - Experienced in server-side software development for communication with attached FPGA boards
    ex. Ethernet packet parsing software to receive MIPI data and reconstruct image stream
  - Experienced in system software engineering with multi-threaded applications optimised for speed
    - Cross-platform development for performance replications across multiple operating systems
    - Direct interactions with various kernel and OS-specific ABI for streamlined performance
    - Direct modifications to server system to enhance single-core and network performance
- Custom IP development with Verilog-based RTL on Vivado
  - Receive parallel data from attached event camera (DVS) sensor and reorganise for AXI4-Stream
  - Created block designs including RTL blocks to generate IP
  - Basic experience with generating functioning IPs based on block designs in Vivado
- Linux Server Management
  - Experienced in protocols such as VNC, SSH and RDP for remote work and automated services
  - System administration for wide range of hardware and software development toolkits

Student Intern: SSAI, SNU

- Research Interest: CNN Architecture and Hardware Design Optimisation
- In tandem with **graduation project** for bachelor’s degree from ECE, SNU

KATUSA Human Resources Specialist

- Mandatory military service as a KATUSA Agent (Korean Augmentation To the United States Army)
- Human Resources Specialist (42A) for RSO HHD, 94th Military Police Battalion at Camp Humphreys

Skills

System Software Engineering for Windows and Linux

- Designing and implementing multi-threaded applications for pseudo-real-time workloads
- Thread-safe access to global data structures such as lists, queues and custom `class`/`struct` objects
- Cross-platform programming with preprocessor conditions for different operating system ABIs

Embedded Systems Design on Multi-purpose SoC FPGAs

- Designing firmware for bare-metal systems with interrupt-based workflow on Vitis 2021.2
- Basic RTL hardware design using Verilog with partial support for AXI4-Stream standards
- Automated digital systems design and layout with Vivado 2021.2