LALIT ARORA

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With ~7 years of experience in VLSI, I specialize in Static Timing Analysis (STA) and Power Delivery Network (PDN). My innovative approach and technical expertise drive performance, quality signoff, and efficient design solutions. I leverage strong scripting skills to develop methodologies that optimize physical design, ensuring excellence in timing closure and PPA metrics.

EXPERIENCE

Intel Corporation, Bangalore, India

Lead Digital Design Engineer — June 2022 – Present

Nested Hyperscale based Multi Tech 3DIC Timing Methodology & Signoff

- Managed clocking for all SOC functional clocks including clock definition, clock groupings, defining uncertainties, and top-down die clock modeling.
- Defined and implemented CT guardbands, derates, margins, and PVT corners for cross-process 3DIC system timing signoff, ensuring accurate timing analysis across operating conditions.
- Managed constraints and timing exceptions for TAP/SSN/MBIST/BISR protocols and functional test architecture for 3DIC synchronous (3GHz+) and asynchronous interfaces.
- Delivered high-quality IO constraints to dies and managed the promotion of timing exceptions using Fishtail.
- Executed high-quality timing closure for 3DIC designs using nested Hyperscale and VIB parasitics (from STAR-RC).
- Conducted spice simulations for cross-die timing paths and complex multi-driver architectures, ensuring accurate timing and PVT modeling.

FCT: Full Chip Timing

- Delivered timing signoff for multiple designs with over 100 million cells, incorporating complex MI and high-voltage frequencies exceeding 3 GHz
- Led backend integration of SSN, MBIST, and BISR protocols, focusing on pipelining, constraints handling, data/clock flow, debugging, and achieving robust timing closure.
- Provided strategic guidance to sub-system teams on efficient floor planning and low-latency CTS, incorporating logic-flow-based floorplans, clock balancing, DOP placement, and skew group generation.
- Delivered high-quality ECOs by enabling quality constraints and context of MI partitions for accurate IO and constraints modeling, ensuring precise and efficient implementation.

Methodology

- Developed a machine learning-based algorithm to generate signoff-quality I/O constraints, ensuring precise and efficient timing. It helped the team to increase I/O constraints quality by 90 % & reduce manual intervention.
- Developed an RNN-based algorithm to analyze and predict synthesis optimizations on vanilla netlist, delivering valuable PPA (Power, Performance, Area) insights. It helped the team to provide early feedback to RTL owners for code optimizations.
- Directed and developed a machine learning-based algorithm for predicting crosstalk and generating ECOs targeting bigger low WNS timing violation buckets.

Qualcomm, Noida, India

Senior Engineer — July 2018 – June 2022

FCT: Full Chip Timing

- Delivered quality STA signoff for the Modem sub-system in a 7nm SoC, managing functional and test mode timing across multiple SOCs.
- Achieved optimized floorplan and low-latency CTS, providing feedback for module placement & clock balancing.
- Worked with the RTL team to enable and close skew checks for asynchronous interfaces.
- Managed clock balancing for all test clocks, delivering latency budgets to subsystems, and optimizing clock networks to achieve maximum shift mode frequency in Nom and HV modes.

- Enabled ECO generation flow for multiple SOCs using Tweaker.
- Facilitated VMIN evaluation flow for IR & non-IR aware timing models and Leakage Power reduction.
- Enabled IR-aware STA and delivered ECOs to meet performance specs after IR noise annotation.

PDN: Power Delivery Network

- Delivered PDN (Static/Dynamic IR, Power/Signal EM, ESD analysis, Grid resistance, Inrush Analysis) for multiple chips, working across tech nodes from 11nm to 5nm using Redhawk & Redhawk-SC.
- Lead end-to-end PDN signoff of 5G 5nm SOC with a team of 8 members.
- Collaborated with various stakeholders (package, system PDN, physical design, floorplan and partitioning, RDL and STA team) to decide on SOC Floorplan (Die size finalization), sub-system floorplan (location), pad placements, bump locations, bump assignment, die side cap placement, core PG grid finalization, package layout improvement, enablement of IR-aware STA and VMIN evaluation.
- Enabled SCAN mode dynamic IR simulations to replicate shift mode high-switching scenarios and assess their impact on the PG grid and Timing.
- Worked on VCD and VLESS-based IR simulations (DIE and CPA-based) for Func and test mode.

Methodology

- Developed a Python-based utility to extract and analyze ideal voltage, minimum droop, maximum droop, peak current, average current, and package parasitic of all design bumps. It helped the team in debugging the genuine package layout weakness.
- Developed a TCL utility to traverse through min violating paths and find the optimum points for hold buffering, having enough setup margin based on slack.
- Developed numerous utilities for the physical design team targeting feedthrough buffering, power routing, finding optimum power island locations, etc.

SKILLS

- Technical skills –STA (+DMSA), Clocking, Timing Constraints, PDN (IR + EM), PD (Basics), SPICE, ML (Basics)
- EDA tools – Primetime, Fusion compiler, Tempus, Tweaker, Fishtail, Redhawk, Redhawk-SC, HSPICE, Innovus
- Languages – TCL, Python, Perl, Shell (CSH/Bash), Verilog, Embedded C, VHDL
- Spoken languages – English, Hindi

EDUCATION

Jan 2023 – Dec 2024	MTech, Microelectronics & VLSI **Birla Institute of Technology and Sciences (BITS), University of Pilani, Rajasthan** Score: 10 CGPA
Aug 2014 – May 2018	BE, Electronics & Communication **Netaji Subhas Institute of Technology (NSIT), University of Delhi, Delhi** Score: 84.7 % Awarded Merit Scholarship twice for being amongst the top 10 students of the batch.
Apr 2013 – Mar 2014	Class XII **Bal Mandir Sr. Sec School, Delhi, Affiliated by CBSE** Score: 93.7 %
Apr 2011 – Mar 2012	Class X **Bal Mandir Sr. Sec School, Delhi, Affiliated by CBSE** Score: 9.8 CGPA

CONFERENCES & ACHIEVEMENTS

- Selected Paper on STML (ML Based Synthesis optimization) at VLSID, 2025
- Recognized by Best Presentation Award for delivering 3DIC Timing methodology at SNUG, 2024
- Recognized by Best Presentation Award for delivering ML-based Xtalk fixing algorithm at DAC, 2023
- Accepted 3 DTTC (Intel Internal) paper publications for 3DIC methodology, ML-based synthesis, and Auto PyRoute.
- Received many Qualstar (Qualcomm Internal recognition) awards for excellent performance.
- Received Merit scholarship (twice) for exceptional performance at NSIT
- 3rd position (Men's Doubles) in Table Tennis Tournament at Qualcomm
- Achieved 1st position in Tech Fest Hackathon at IGDTUW and 3rd position in Tech Week Hackathon by IEEE