LALIT ARORA

vlalitarora@gmail.com | +91 – 9910371459 | LinkedIn: www.linkedin.com/in/lalit-arora | Git: www.github.com/thelalitarora

VLSI engineer with ~7 years of experience, specializing in STA and PDN with a strong grasp of physical design flows. Proficient in developing methodologies and automation solutions to enhance design efficiency. Experienced in leveraging machine learning for VLSI design optimization.

SKILLS

- Technical skills –STA (+DMSA), Clocking, Timing Constraints, PDN (IR + EM), PD (Basics), SPICE, ML (Basics)
- EDA tools – Primetime, Fusion compiler, Tempus, Tweaker, Fishtail, Redhawk, Redhawk-SC, HSPICE, Innovus
- Languages – TCL, Python, Perl, Shell (CSH/Bash), Verilog, Embedded C, VHDL
- Spoken languages – English, Hindi

EXPERIENCE

Intel Corporation, Bangalore, India

Lead Digital Design Engineer — June 2022 – Present

Nested Hyperscale-based multi-Tech 3DIC Timing Methodology & Signoff

- Owned timing signoff for SoC, including clock definitions, clock groupings, uncertainty modeling, and top-down die-level clock modelling.
- Defined and implemented CT guardbands, PVT corners, and derates to enable accurate cross-process timing signoff across synchronous (3GHz+) and asynchronous 3DIC interfaces.
- Managed timing constraints and exceptions for TAP/SSN/MBIST/BISR, delivering high-quality IO constraints and driving exception promotion using Fishtail tools.
- Achieved timing closure for complex 3DIC designs using nested Hyperscale/VIB parasitics (STAR-RC) and SPICE simulations for cross-die timing and multi-driver paths, improving accuracy in PVT modeling.

FCT: Full Chip Timing

- Delivered timing signoff for SoCs exceeding 100M cells, managing complex multi-instance (MI) and high-frequency (>3 GHz) designs with robust timing closure across partitions.
- Led backend integration and constraints development for SSN, MBIST, and BISR, optimizing data/clock paths, pipelining, and exception handling to ensure closure in high-speed designs.
- Guided sub-system teams on floor planning and low-latency CTS, enabling quality ECOs and accurate IO/constraints modeling through logic-aware placement, DOP alignment, and skew optimization.

Methodology

- Built an ML-based algorithm to auto-generate signoff-quality I/O constraints, improving accuracy by 90% and significantly reducing manual effort.
- Designed an RNN model to predict synthesis outcomes on vanilla netlists, enabling early PPA insights and accelerating RTL optimization feedback loops.
- Led development of a crosstalk prediction model, automating ECO generation for large low-WNS violation buckets and enhancing timing closure efficiency

Qualcomm, Noida, India

Senior Engineer — July 2018 – June 2022

FCT: Full Chip Timing

- Delivered STA signoff for the Modem sub-system in a 7nm SoC, managing functional and test mode timing across multiple SoCs.
- Optimized floorplan and low-latency CTS, providing feedback on module placement and clock balancing to enhance timing efficiency.

- Managed clock balancing for all test clocks, optimizing clock networks, and achieving maximum shift mode frequency in NOM and HV modes.
- Streamlined ECO generation across multiple SoCs using Tweaker, improving design iteration efficiency and ensuring timing closure.
- Led VMIN evaluation for IR and non-IR aware timing models, driving leakage power reduction and delivering IR-aware STA to meet performance specs.

PDN: Power Delivery Network

- Led end-to-end PDN signoff for a 5G 5nm SoC, managing a team of 8 and delivering comprehensive analyses (Static/Dynamic IR, Power/Signal EM, ESD, Grid resistance, Inrush) across multiple tech nodes (11nm to 5nm) using Redhawk & Redhawk-SC.
- Collaborated across cross-functional teams (package, system PDN, physical design, and STA) to finalize SOC and sub-system floorplans, pad/bump placements, and core PG grid, optimizing layout, enabling IR-aware STA and VMIN evaluations.
- Enabled dynamic IR simulations in SCAN mode to replicate high-switching scenarios, assessing their impact on the PG grid and timing for improved power integrity.
- Performed VCD and VLESS-based IR simulations for functional and test modes, ensuring reliable power delivery and minimizing timing violations.

Methodology

- Developed a Python tool to analyze voltage droop, current, and parasitics across all bumps, identifying >90% of weak spots and accelerating package debug.
- Automated hold buffer insertion with a TCL utility, reducing manual analysis and improving hold closure time by ~40%.
- Created utilities for feedthrough buffering, power routing, and island placement, cutting physical design effort by ~30%.

EDUCATION

MTech, Microelectronics & VLSI
BITS Pilani, Rajasthan | Jan 2023 – Dec 2024 | **CGPA: 10.0**

B.E., Electronics & Communication Engineering

NSIT, University of Delhi | Aug 2014 – May 2018 | **84.7%**

Class XII – CBSE

Bal Mandir Sr. Sec School, Delhi | Apr 2013 – Mar 2014 | **93.7%**

Class X – CBSE

Bal Mandir Sr. Sec School, Delhi | Apr 2011 – Mar 2012 | **CGPA: 9.8**

PUBLICATIONS & CONFERENCES

- Published IEEE Paper on STML (ML Based Synthesis optimization), VLSID, 2025
- Recognized by Best Presentation Award for delivering 3DIC Timing methodology at SNUG, 2024
- Recognized by the Best Presentation Award for delivering an ML-based Xtalk fixing algorithm at DAC, 2023
- Accepted 3 DTTC (Intel Internal) paper publications for 3DIC methodology, ML-based synthesis, and Auto PyRoute.

AWARDS & ACHIEVEMENTS

- Received DRA Award at Intel for quality signoff of timing-critical design.
- Received many Qualstar (Qualcomm Internal recognition) awards for excellent performance.
- Received Merit scholarship (twice) for exceptional performance at NSIT
- 3rd position (Men's Doubles) in Table Tennis Tournament at Qualcomm
- Achieved 1st position in Tech Fest Hackathon at IGDTUW and 3rd position in Tech Week Hackathon by IEEE