VLS502: Analog IC Design, 2024-2025 Final Project

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Design of an Exernally Compensated Low Dropout Regulator(LDO)

1. Purpose of an LDO

Every electronics system requires a power supply to function. Portable systems are usually battery powered. For the circuits to function properly, the power supply has to be precise and stable. Hence, in between power source and circuit, voltage regulators are present. Broadly, there are two types of voltage regulators, linear regulators and switching regulators.
Even though efficiency of linear regulators is poor they provide high regulation compared to switching regulators. They occupy less area and are low cost.
Low Dropout Regulators (LDO) belongs to the class of linear regulators. The main advantage of LDO is that it can regulate voltage while having only a fraction of voltage drop across it to function.
LDO provides good suppression of noise generated from input.

Instructions: Discuss the role of an LDO in circuits, emphasizing its importance. Add 3-5 bullet points summarizing the purpose.

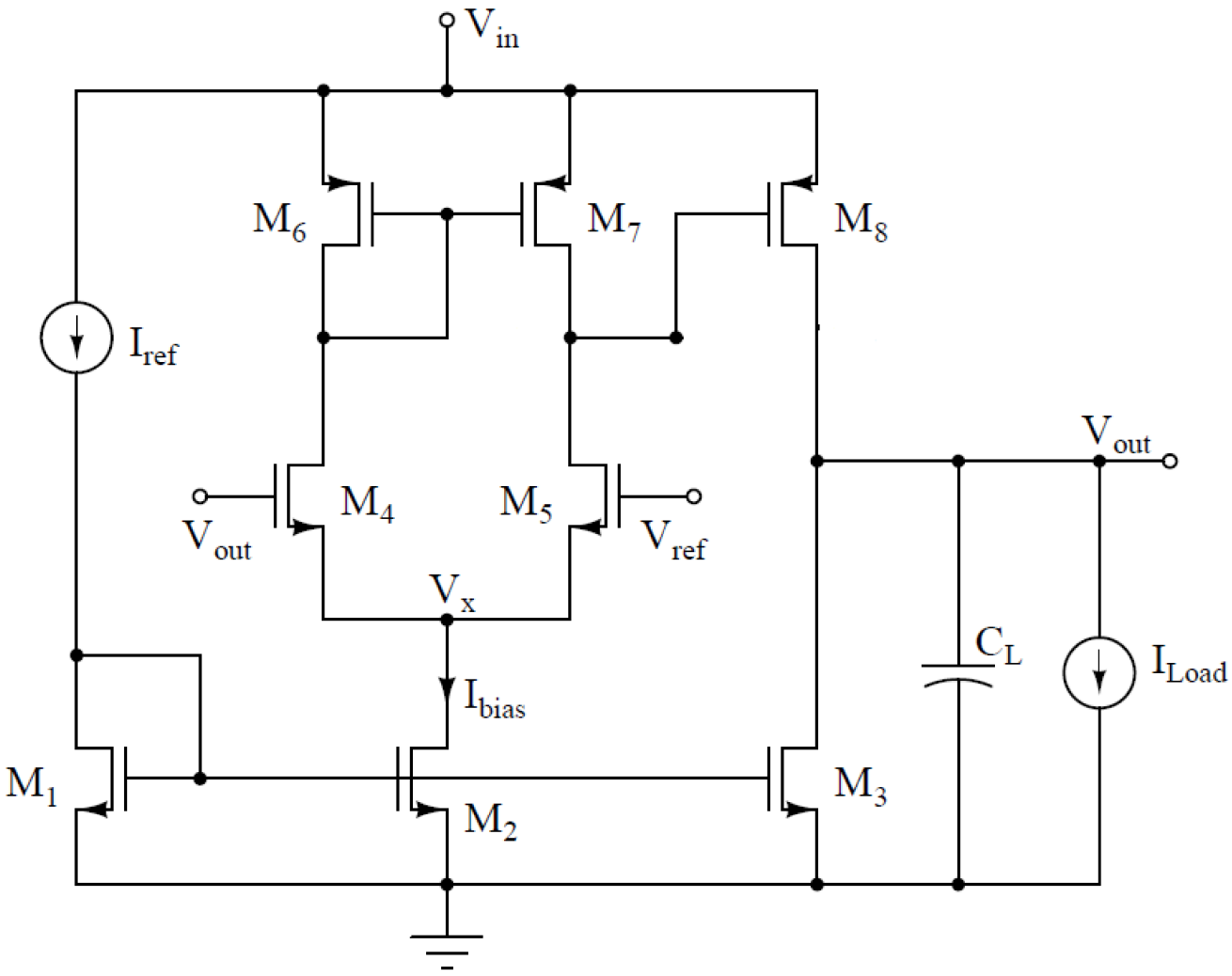


Figure 1: Externally Compensated Low Dropout Voltage Regulator

2. Specifications

This report provides the design of Externally compensated LDOs. The specifications allows dropout voltage of 0.4V, with load current ranging from 2mA to 10mA. Complete specifications for the design are summarized in following table.

Table 1: Specifications of Externally Compensated Low Dropout Voltage Regulator

Parameter	Value
Input Voltage (Vin)	1.4V
Output Voltage (Vout)	1V
Power Supply Rejection Ratio (PSRR) at heavy load	60dB
Minimum Load Current (Iload min)	2mA
Maximum Load Current (Iload max)	10mA
Load Capacitance (Cload)	1 µF
Quiescent Current (Iquiescent)	50 µA
Transient Duration	1 µs

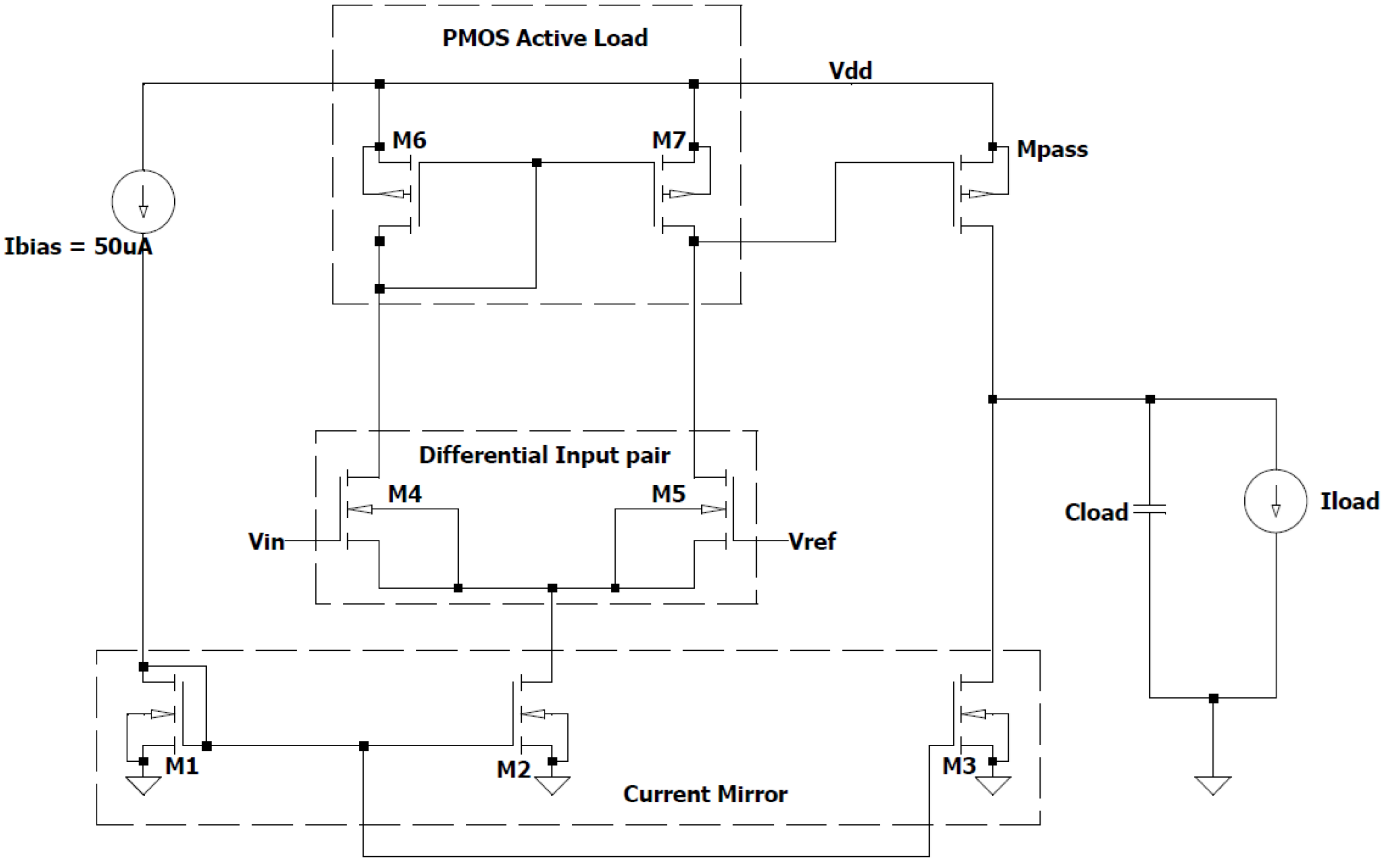


Figure 2: Schematic of Externally Compensated LDO

3. Relevance of Techplots

The main reason behind following the techplots based approach to design is to avoid the erroneous square law relation for mosfet which fails to correctly capture the relation between current through device and other parameters. This leads to multiple iterations in design before the specifications are met.
Techplots are generated for three quantities,

1. gm/ID Vs fT,
2. gm/ID Vs ID/W and
3. gm/ID Vs gmro.

Figure 3 shows the circuit used for generating tech plots where for fixed VD and Width(W), VGS is swept and ID, gm, ro, Cgg are stored. Length(L) is parameterized and takes values in step of 40nm.

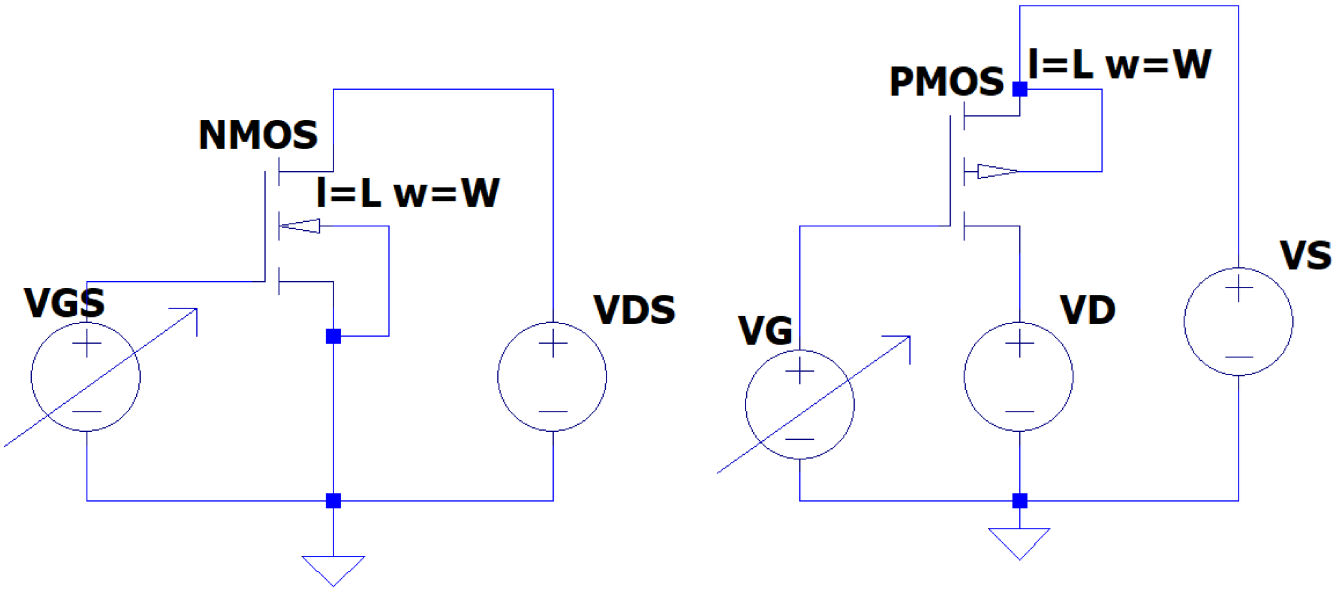


Figure 3: Schmatic to generate techplots

Github link to our techplots for technology node of 130nm :
Some of the important observations made by comparing techplots of 180nm technology node and 130nm technology node are as follows.

- f_T is inversely proportional to the square of length(L), hence as L reduces for 130nm node f_T improves, making circuits faster with with scaling.
- Example takeaway: f_T improves with shorter channel lengths, making circuits faster with scaling.
- In case of 130nm node, for same value of gm/ID, mosfet gives high values of intrinsic gain(gmro)
- VDS is chosen as 0.4V based on the design specifications, hence there will be negligible error.

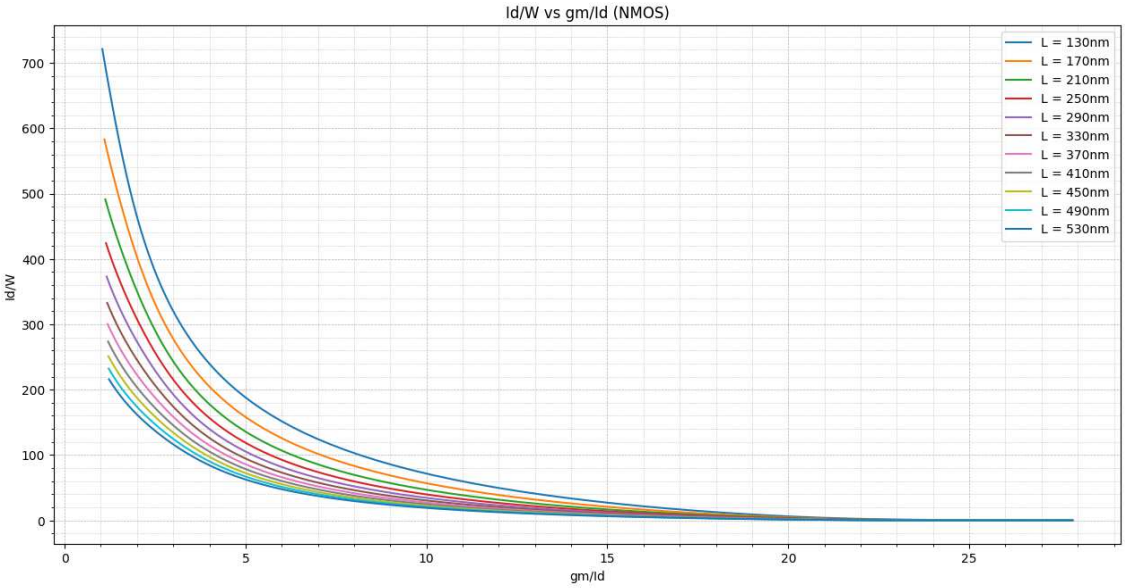


Figure 4: NMOS gm/Id Vs Id/W

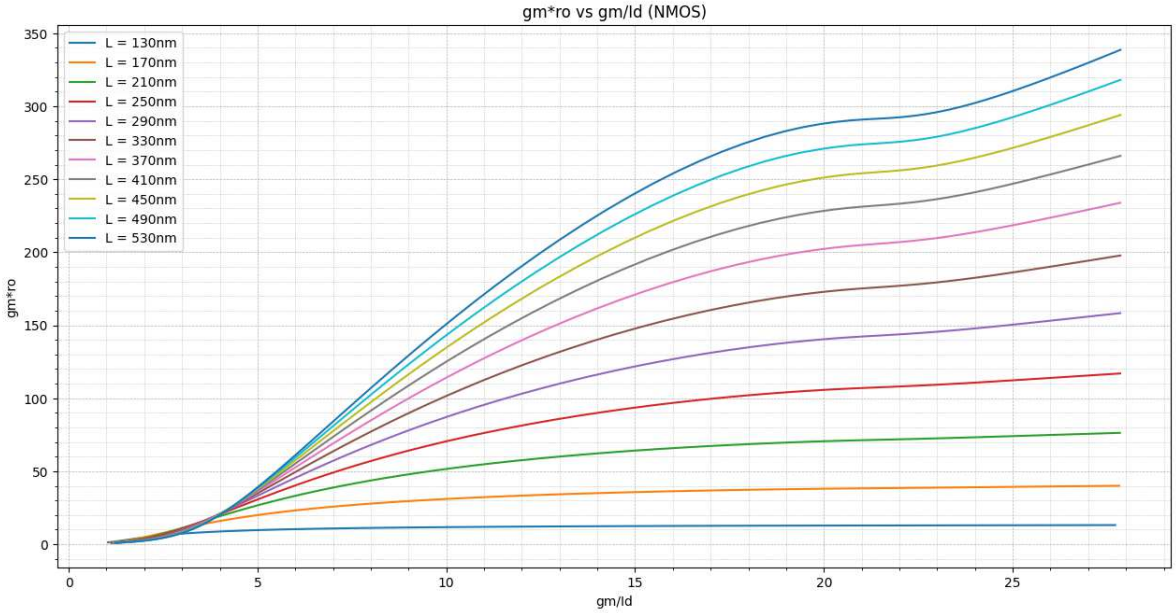


Figure 5: NMOS gm/Id Vs gmro

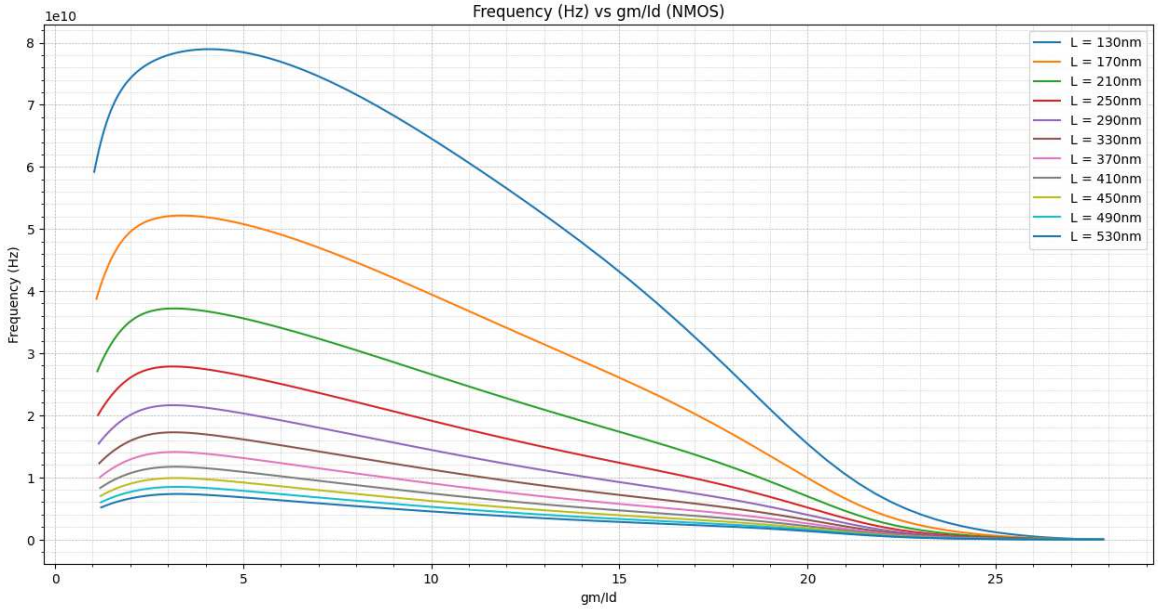


Figure 6: NMOS gm/Id Vs fT

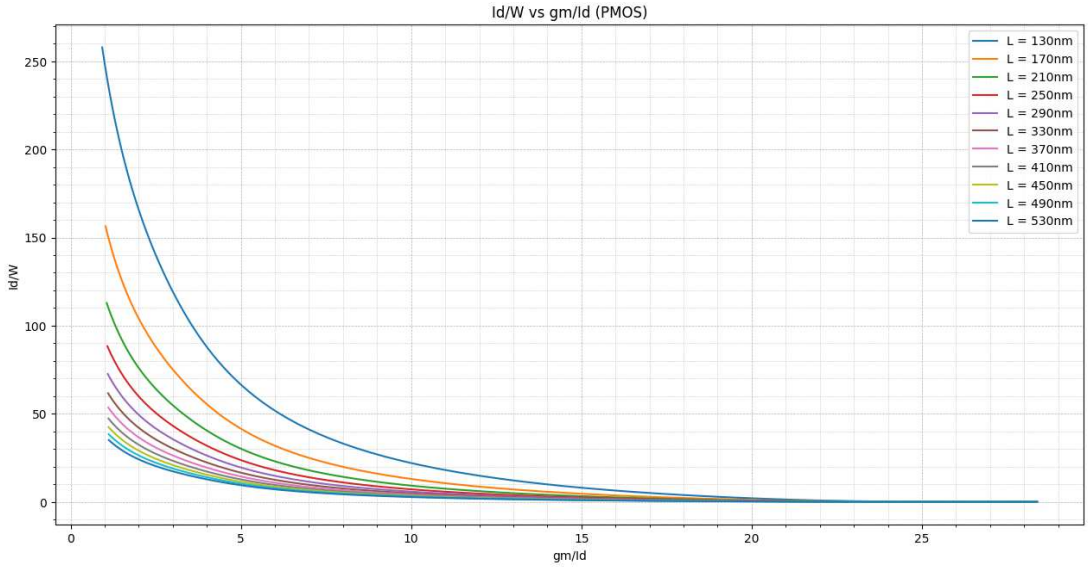


Figure 7: PMOS gm/Id Vs Id/W

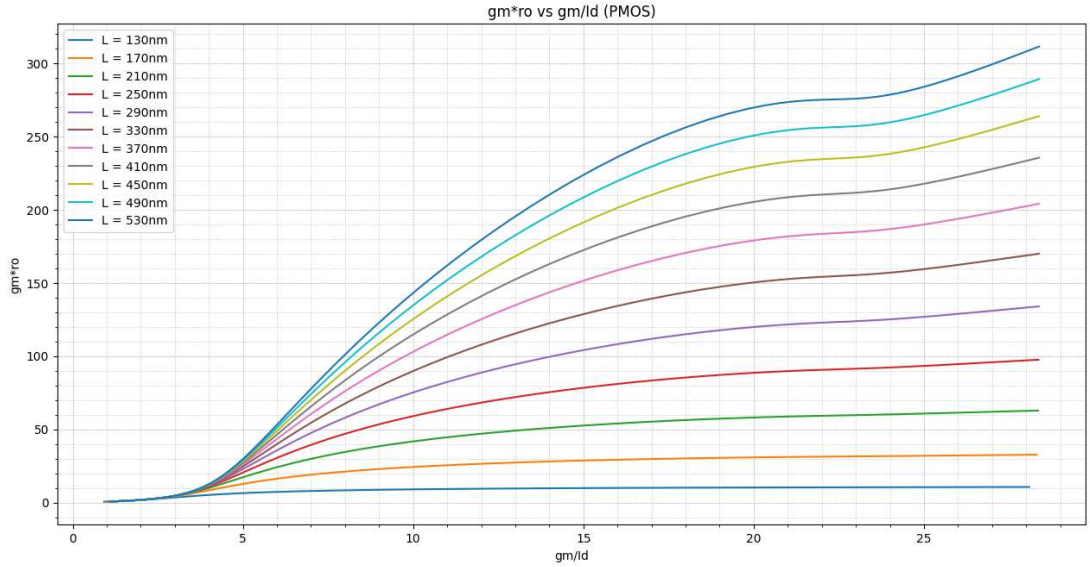


Figure 8: PMOS gm/Id Vs gmro

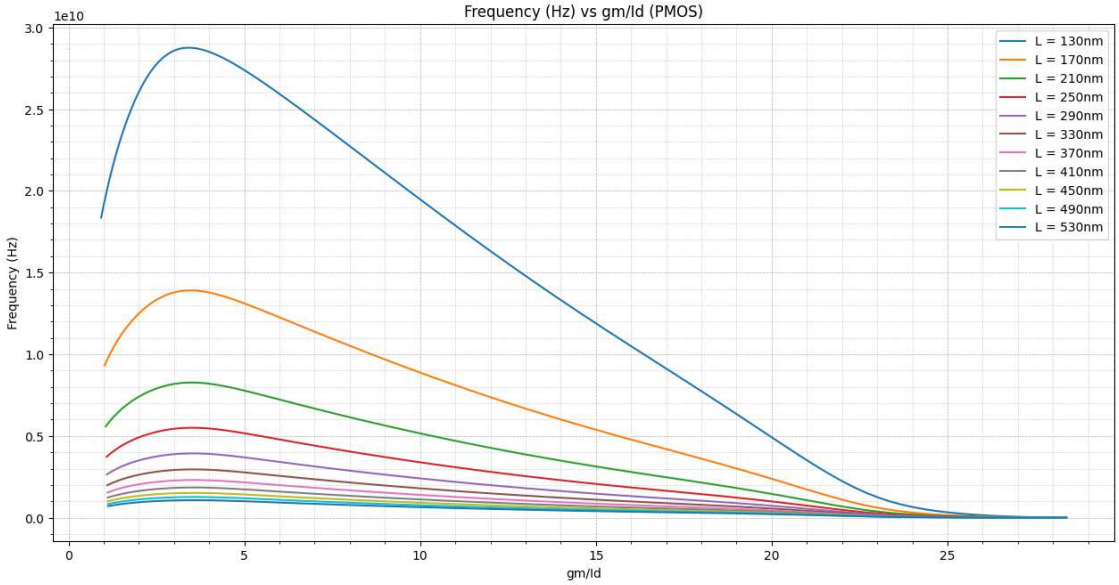


Figure 9: PMOS gm/Id Vs fT

4. FET Sizes

Table 3 gives the dimensions of all eight transistors in the circuit.

1. Bias Transistors NMOS - M1, M2, M3
2. Differential input pair NMOS - M4, M4
3. Active load PMOS - M6, M7
4. Series PassFET PMOS - Mpass

Transistors	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**	**M7**	**Mpass**
Length (nm)	530.00	530.00	530.00	250.00	250.00	290.00	290.00	170.00
Width (µm)	2.61	2.61	2.61	0.63	0.63	4.34	4.34	7.66

Table 2: Transistor Dimensions

Transistor	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**	**M7**	**Mpass**
Id (A)	5.00E-05	4.99E-05	5.10E-05	2.50E-05	2.50E-05	-2.50E-05	-2.50E-05	-1.01E-02
Vgs (V)	5.26E-01	5.26E-01	5.26E-01	4.97E-01	4.97E-01	-4.75E-01	-4.75E-01	-4.67E-01
Vds (V)	5.26E-01	5.03E-01	1.02E+00	4.22E-01	4.30E-01	-4.75E-01	-4.67E-01	-3.83E-01
Vth (V)	3.78E-01	3.78E-01	3.78E-01	3.76E-01	3.76E-01	-3.19E-01	-3.19E-01	-3.12E-01
Vdsat (V)	1.56E-01	1.56E-01	1.56E-01	1.29E-01	1.29E-01	-1.75E-01	-1.75E-01	-1.74E-01
Gm (S)	5.01E-04	5.00E-04	5.10E-04	2.67E-04	2.67E-04	2.55E-04	2.55E-04	1.00E-01
Gds (S)	2.49E-06	2.58E-06	1.84E-06	3.45E-06	3.41E-06	2.93E-06	2.96E-06	4.22E-03
Gmb (S)	1.19E-04	1.19E-04	1.22E-04	6.30E-05	6.30E-05	5.41E-05	5.40E-05	2.13E-02
Cbd (F)	1.14E-15	1.15E-15	1.04E-15	3.25E-16	3.24E-16	1.98E-15	1.98E-15	3.46E-13
Cbs (F)	2.10E-15	2.10E-15	2.10E-15	5.84E-16	5.84E-16	3.60E-15	3.60E-15	6.16E-13
Vov	1.48E-01	1.48E-01	1.48E-01	1.21E-01	1.21E-01	1.56E-01	1.56E-01	1.55E-01
Operating region	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation

Table 3: Transistor Parameters for Heavy Load (10mA)

Parameter	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**	**M7**	**Mpass**
Id (A)	5.00E-05	4.99E-05	5.10E-05	2.50E-05	2.50E-05	-2.50E-05	-2.50E-05	-2.05E-03
Vgs (V)	5.26E-01	5.26E-01	5.26E-01	4.97E-01	4.97E-01	-4.75E-01	-4.75E-01	-3.48E-01
Vds (V)	5.26E-01	5.03E-01	1.02E+00	4.22E-01	4.30E-01	-4.75E-01	-4.67E-01	-3.80E-01
Vth (V)	3.78E-01	3.78E-01	3.78E-01	3.76E-01	3.76E-01	-3.19E-01	-3.19E-01	-3.12E-01
Vdsat (V)	1.56E-01	1.56E-01	1.56E-01	1.29E-01	1.29E-01	-1.75E-01	-1.75E-01	-9.36E-02
Gm (S)	5.01E-04	5.00E-04	5.10E-04	2.67E-04	2.67E-04	2.55E-04	2.55E-04	3.54E-02
Gds (S)	2.49E-06	2.58E-06	1.84E-06	3.45E-06	3.41E-06	2.93E-06	2.96E-06	1.20E-03
Gmb (S)	1.19E-04	1.19E-04	1.22E-04	6.30E-05	6.30E-05	5.41E-05	5.40E-05	7.43E-03
Cbd (F)	1.14E-15	1.15E-15	1.04E-15	3.25E-16	3.24E-16	1.98E-15	1.98E-15	3.46E-13
Cbs (F)	2.10E-15	2.10E-15	2.10E-15	5.84E-16	5.84E-16	3.60E-15	3.60E-15	6.16E-13
Vov	1.48E-01	1.48E-01	1.48E-01	1.21E-01	1.21E-01	-1.56E-01	-1.56E-01	3.60E-02
Operating region	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation

Table 4: Transistor Parameters for Light Load (2mA) with New Values

5. Stability Analysis

Instructions: List pole locations and verify them from simulation. Explain their movement with respect to load. Discuss the worst-case phase margin.

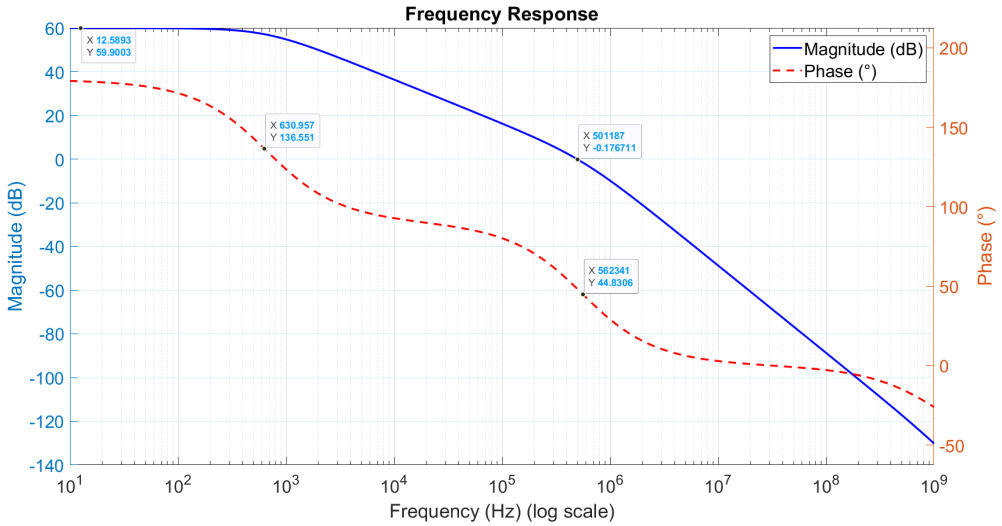


Figure 10: Loopgain for Heavy load

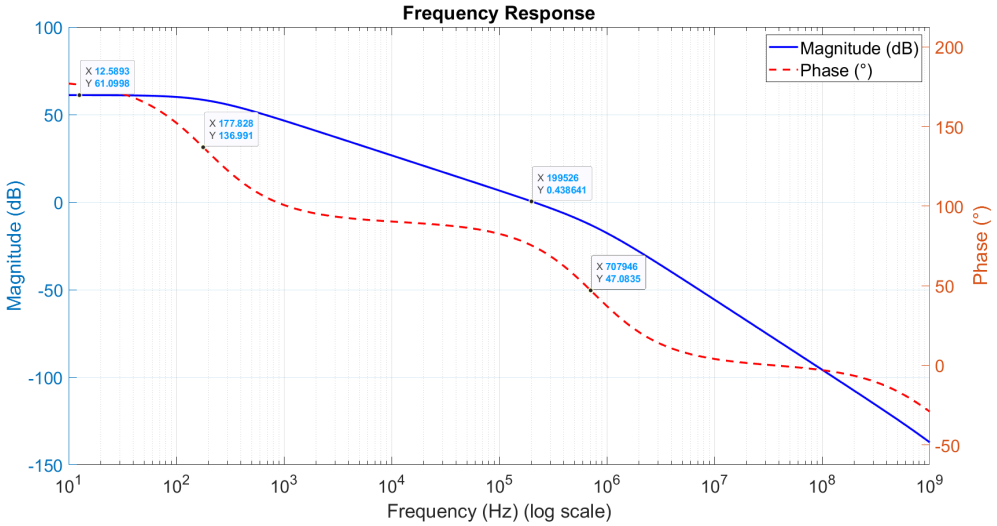


Figure 11: Loopgain for light load

Table 5: Key Metrics under Heavy and Light Load Conditions

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	59.47	61.09
Unity Gain Bandwidth (Hz)	541	203
Phase Margin (degrees)	48.6	75
Pole 1 (Hz)	658	131
Pole 2 (KHz)	541	203

6. PSRR Explanation

In the following figure we observe the signal paths for PSRR Calculations

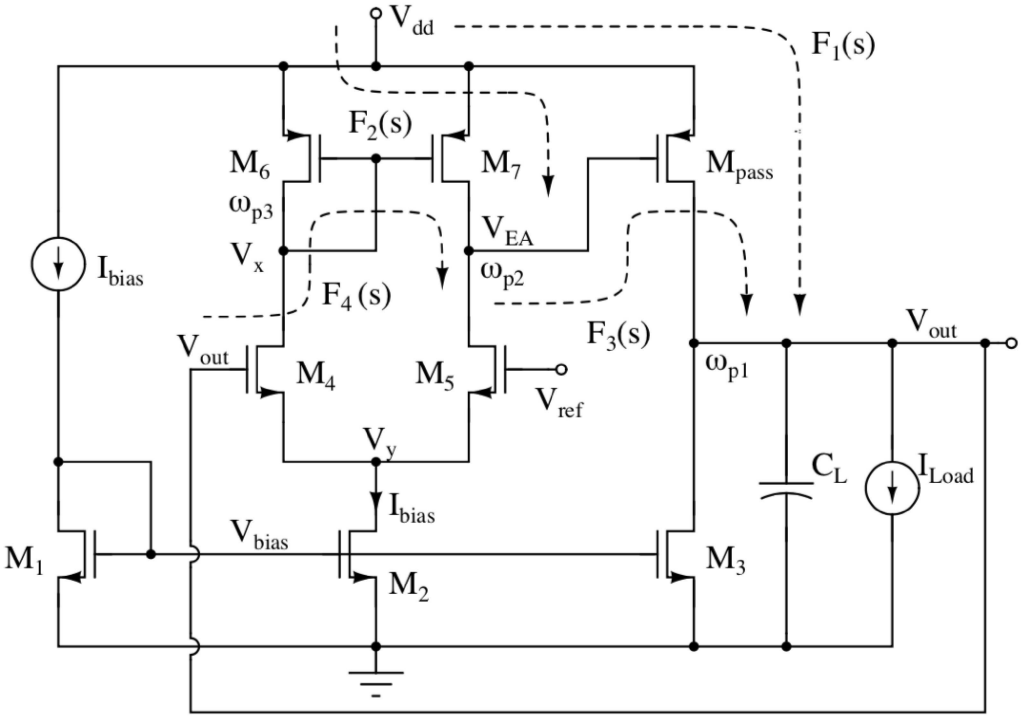


Figure 12: PSRR block diagram.

$$\text{PSRR}_{\text{OL}} = F_1(s) + F_2(s)F_3(s)$$

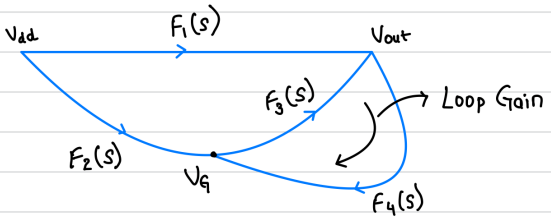
$$F_1(s) = \frac{1 + g_{mpass} r_{opass}}{\left(1 + \frac{s}{\omega_{p1}}\right)}, \qquad \omega_{p1} = \frac{1}{r_{opass} \cdot C_L}$$

$$F_2(s) = \frac{(r_{o5} \parallel r_{o7}) \cdot (1 + sC_{gspass}(r_{o7} \parallel r_{o4}))}{(r_{o4} \parallel r_{o7})\,[1 + s(C_{gspass} + C_{gdpass})(r_{o7} \parallel r_{o5})]}$$

$$F_3(s) = -\frac{g_{mpass} r_{opass}}{1 + \frac{s}{\omega_{p1}}}$$

$$A_{\text{LG}}(s) = \frac{A_{\text{diff}} \cdot A_{\text{pass}}}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

$$\text{PSRR}_{\text{CL}}(s) = \frac{\text{PSRR}_{\text{OL}}(s)}{1 + A_{\text{LG}}(s)}$$



$$\text{PSRR} = \frac{F_1(s) + F_2(s)\,F_3(s)}{1 + F_3(s)F_4(s)}$$

7. PSRR Simulation Results

PSRR simulation results at heavy and light load conditions.

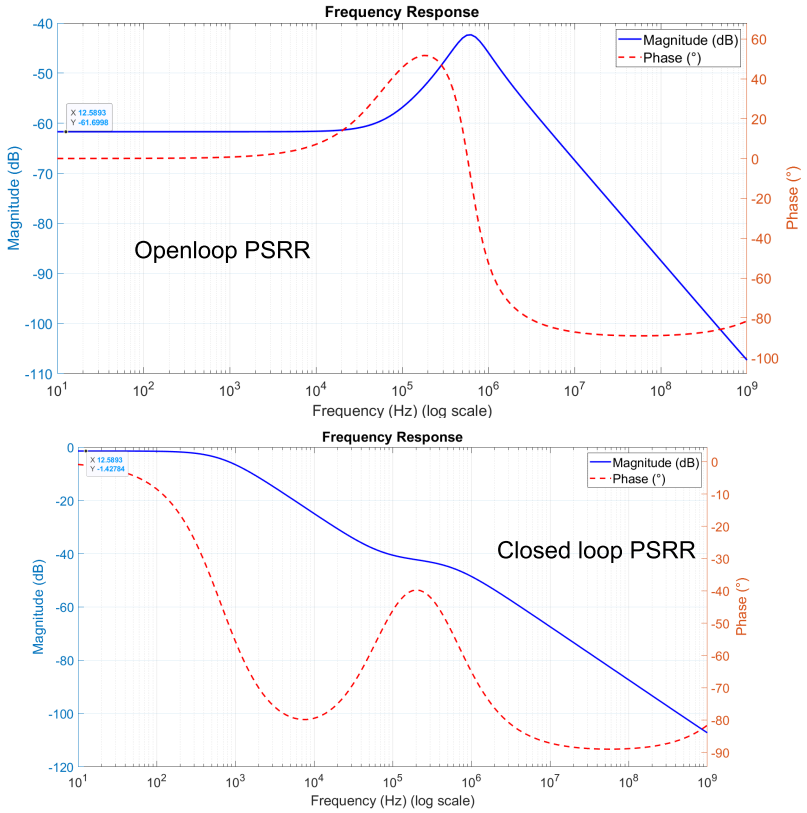


Figure 13: PSRR simulation results - heavy load.

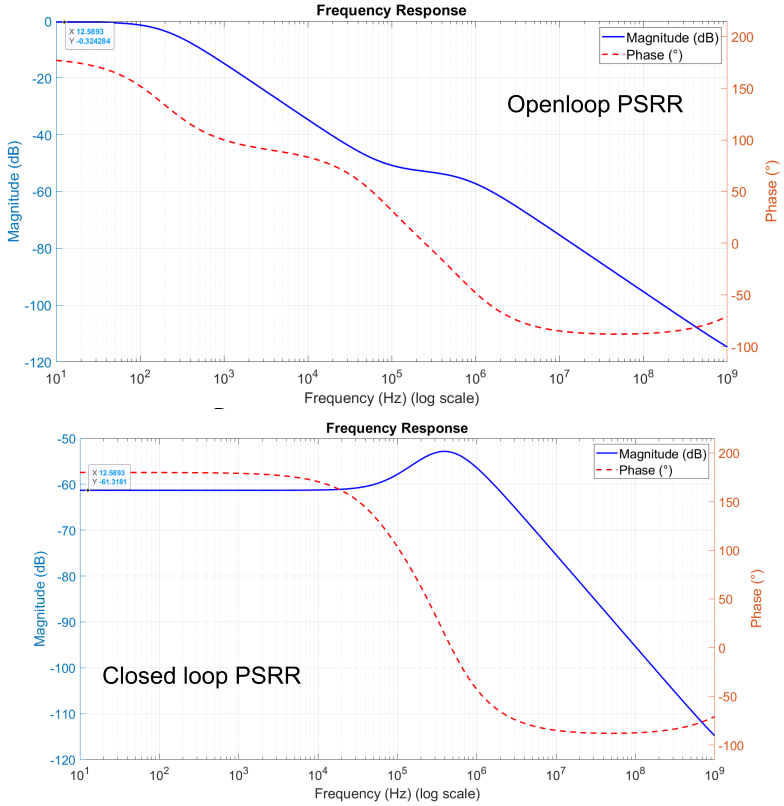


Figure 14: PSRR simulation results - light load.

Figure 14: PSRR simulation results - light load.

8. Transient Simulation Results

Step the load current from minimum to maximum. We can observe that during switching from light load to heavy load there is transient present.

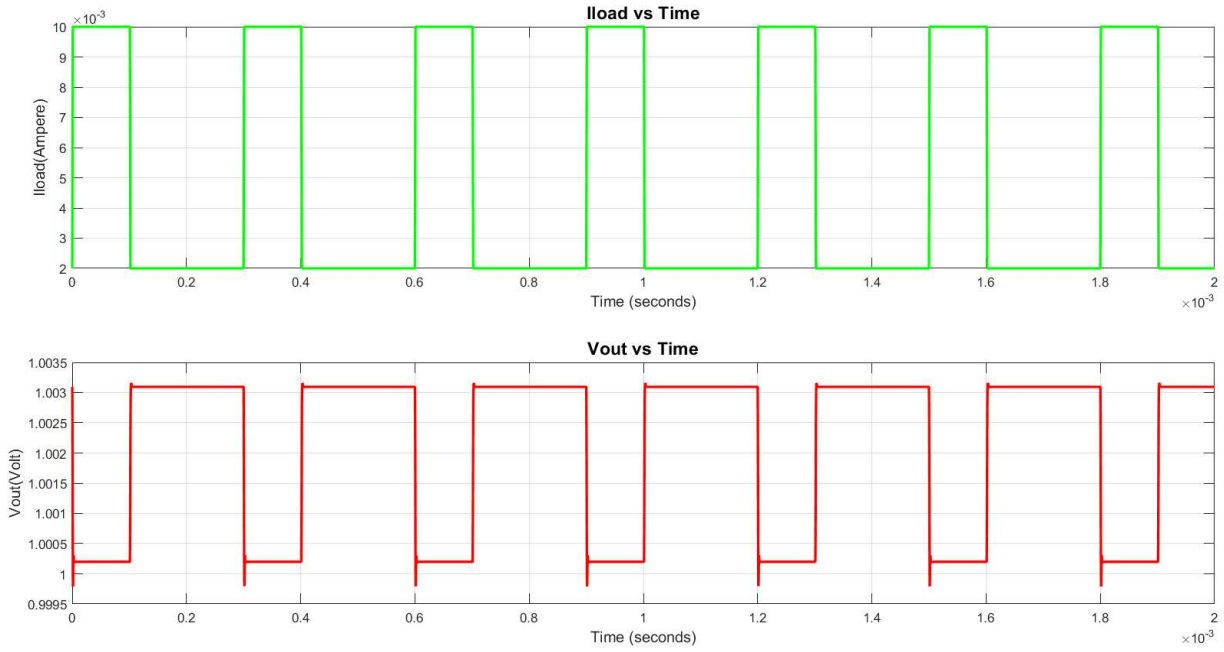


Figure 15: Transient simulation results.

9. Simulation vs. Hand Calculations

Table 6: Simulation vs. Hand Calculations with Percentage Error

Parameter	**Simulation**	**Hand-Calculation**	**% Error**
Heavy Load Loop Gain (dB)	59.9	60	0.16
Light Load Loop Gain (dB)	61.1	60	-0.01
Heavy Load Openloop PSRR (dB)	-1.43	0	0
Light Load Openloop PSRR (dB)	0	0	0
Heavy Load Closedloop PSRR (dB)	-61.7	-60	-2.8
Light Load Closedloop PSRR (dB)	-61.3	-60	-2.16
Heavy Load Phase Margin (degrees)	48.6	45	---
Light Load Phase Margin (degrees)	75	45	---
Heavy Load Unity Gain Bandwidth (kHz)	541	656	
Light Load Unity Gain Bandwidth (KHz)	203	131	---