An Approximate and Iterative Posit Multiplier

Group 33	
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Introduction:

Posit number system is an emerging number system which aims to be a competitor to the existing IEEE floating-point number system.

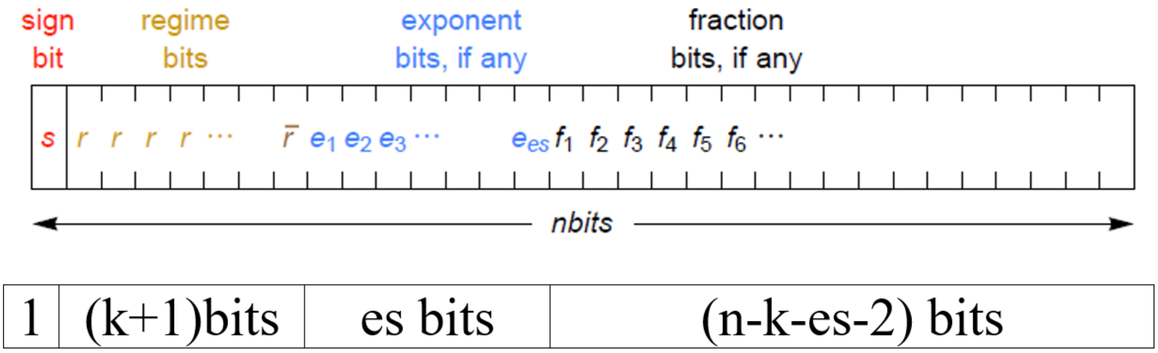


Figure 1. Generic posit format for an n-bit number

$$value = (-1)^s * (useed)^k * (2)^{exp} * (1 + frac)$$

$$useed = (2)\hat{}(2\hat{}es)$$

Methodology:

1) First, we extracted the sign, regime, exponent, and mantissa bits from the given 32-bit numbers. This step is referred to as *decoding*.
2) The decoding process was performed for both numbers that we need to multiply.
3) Using the sign, regime, and exponent of the two numbers, we calculated the sign, regime, and exponent of the result based on the reference paper.
4) Using the mantissas of the two numbers, we computed the mantissa of the result using an iterative approach, as described in the reference paper.
5) Finally, using the result's sign, regime, and exponent (from step 3) and the mantissa (from step 4), we reconstructed the final result. This step is called *encoding*.

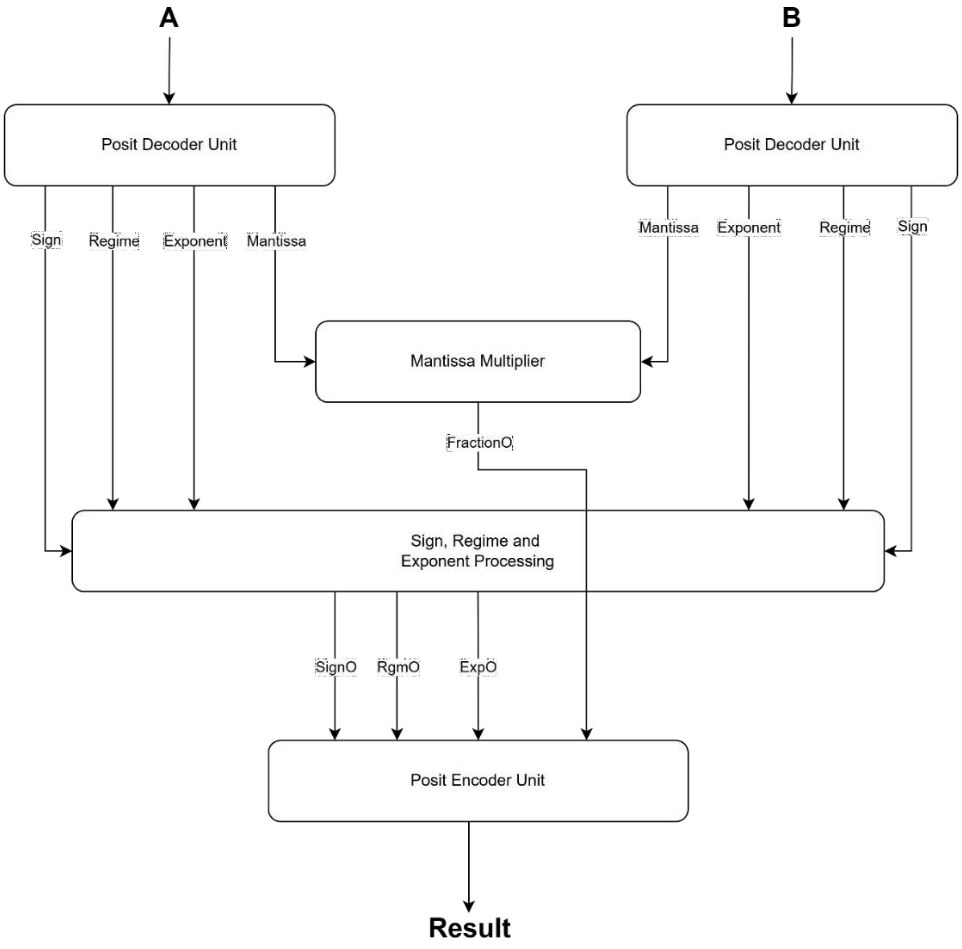
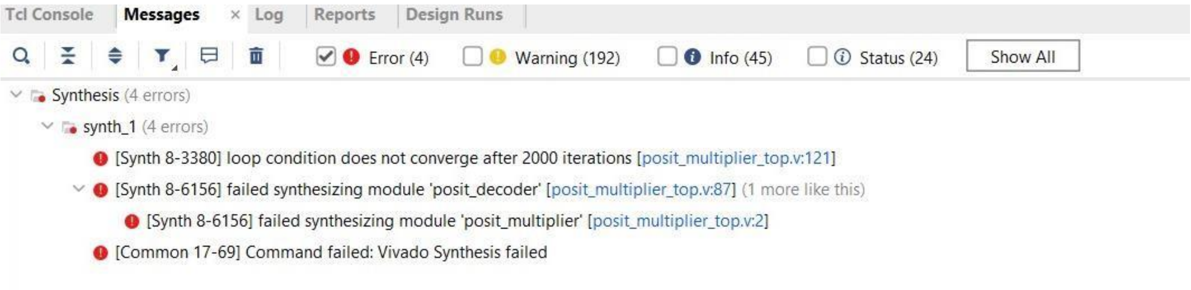


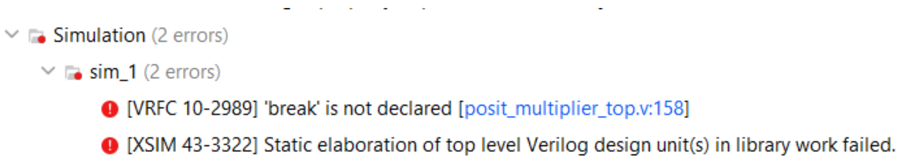
Figure 2: Datapath of the proposed multiplier circuit

Once we implemented the design in Verilog, we successfully simulated and verified the results. However, during synthesis, we encountered the following issues:

1. **Non-synthesizable loop variables**: To resolve this, we replaced the loop variable with its maximum value and used a conditional `if` statement within the loop to eliminate the error.
2. **Unsupported `break` statement in Verilog**: Since the `break` statement is not supported in Verilog, we replaced it with `i = -1;` which causes the loop to exit as intended.



```
Synthesis (4 errors)
  synth_1 (4 errors)
    [Synth 8-3380] loop condition does not converge after 2000 iterations [posit_multiplier_top.v:121]
    [Synth 8-6156] failed synthesizing module 'posit_decoder' [posit_multiplier_top.v:87] (1 more like this)
      [Synth 8-6156] failed synthesizing module 'posit_multiplier' [posit_multiplier_top.v:2]
    [Common 17-69] Command failed: Vivado Synthesis failed
```



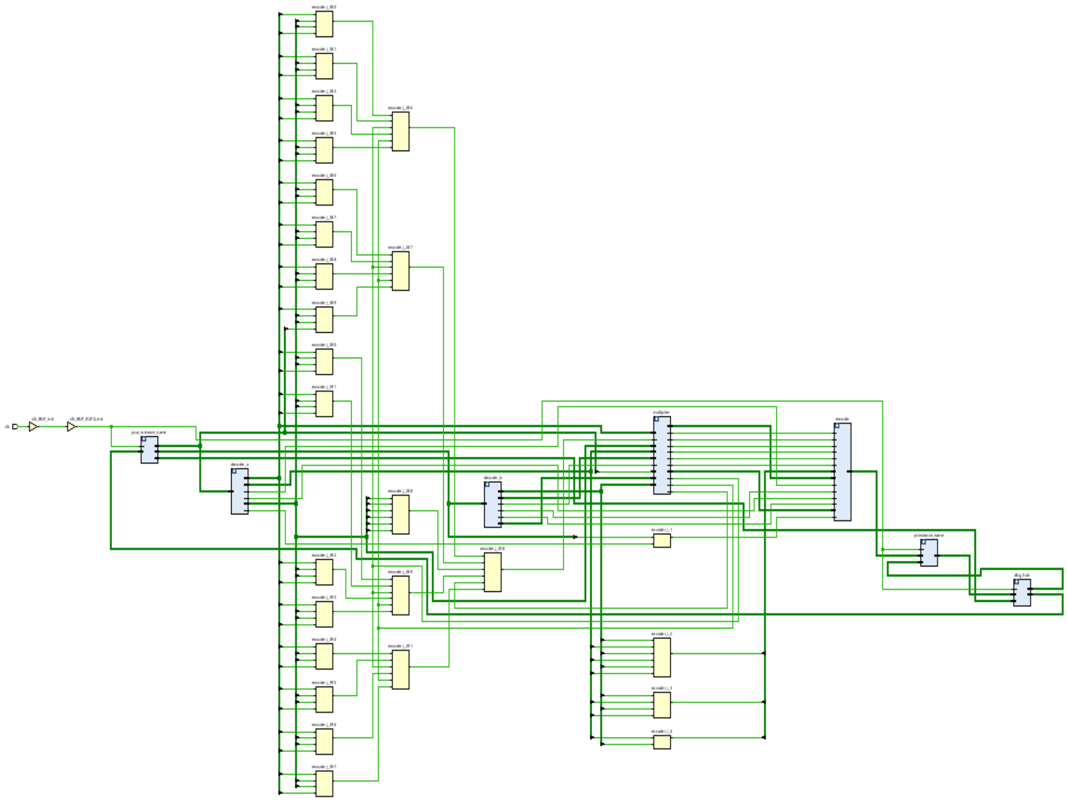
Simulation (2 errors)

sim_1 (2 errors)

[VRFC 10-2989] 'break' is not declared [posit_multiplier_top.v:158]

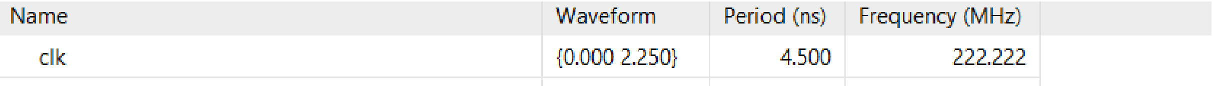
[XSIM 43-3322] Static elaboration of top level Verilog design unit(s) in library work failed.

Figure 3: Error screenshot during synthesis in Vivado

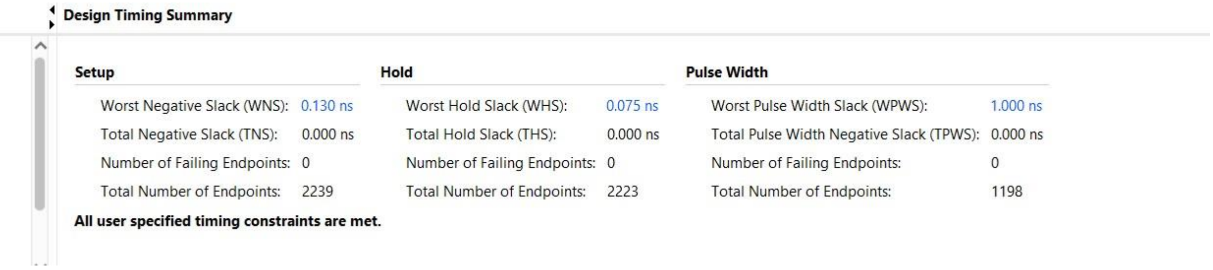


Results:

a) Max Clock Frequency Achieved:



Name	Waveform	Period (ns)	Frequency (MHz)
clk	{0.000 2.250}	4.500	222.222



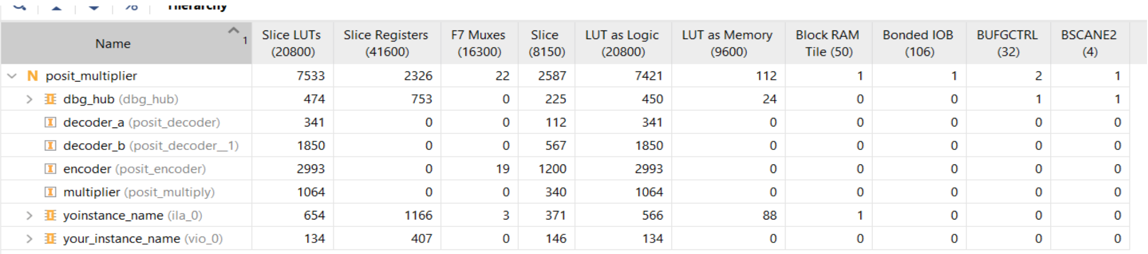
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.130 ns	Worst Hold Slack (WHS):	0.075 ns	Worst Pulse Width Slack (WPWS):	1.000 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	2239	Total Number of Endpoints:	2223	Total Number of Endpoints:	1198

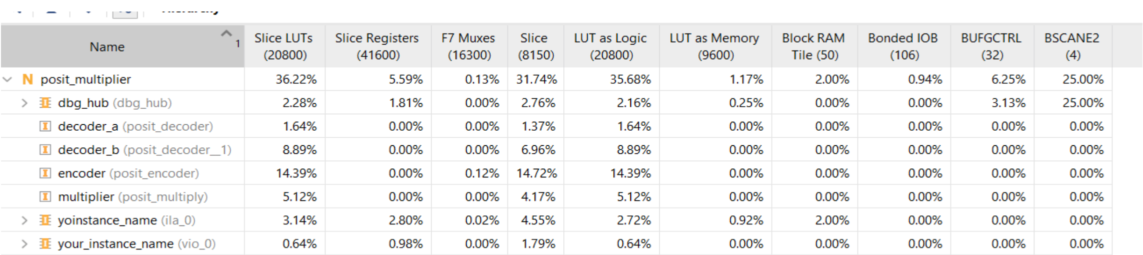
All user specified timing constraints are met.

$$Max\ Freq = \frac{1}{Tclk\ -\ WNS} = \frac{1}{(4.5 -\ 0.13)ns} = 228.23MHz$$

b) Resource Utilization:

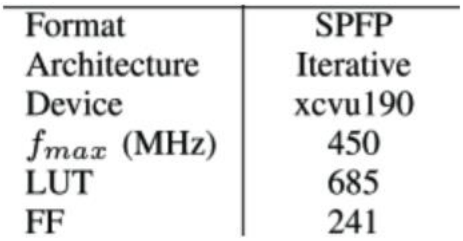


Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
posit_multiplier	7533	2326	22	2587	7421	112	1	1	2	1
dbg_hub (dbg_hub)	474	753	0	225	450	24	0	0	1	1
decoder_a (posit_decoder)	341	0	0	112	341	0	0	0	0	0
decoder_b (posit_decoder__1)	1850	0	0	567	1850	0	0	0	0	0
encoder (posit_encoder)	2993	0	19	1200	2993	0	0	0	0	0
multiplier (posit_multiply)	1064	0	0	340	1064	0	0	0	0	0
yoinstance_name (ila_0)	654	1166	3	371	566	88	1	0	0	0
your_instance_name (vio_0)	134	407	0	146	134	0	0	0	0	0



Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
posit_multiplier	36.22%	5.59%	0.13%	31.74%	35.68%	1.17%	2.00%	0.94%	6.25%	25.00%
dbg_hub (dbg_hub)	2.28%	1.81%	0.00%	2.76%	2.16%	0.25%	0.00%	0.00%	3.13%	25.00%
decoder_a (posit_decoder)	1.64%	0.00%	0.00%	1.37%	1.64%	0.00%	0.00%	0.00%	0.00%	0.00%
decoder_b (posit_decoder__1)	8.89%	0.00%	0.00%	6.96%	8.89%	0.00%	0.00%	0.00%	0.00%	0.00%
encoder (posit_encoder)	14.39%	0.00%	0.12%	14.72%	14.39%	0.00%	0.00%	0.00%	0.00%	0.00%
multiplier (posit_multiply)	5.12%	0.00%	0.00%	4.17%	5.12%	0.00%	0.00%	0.00%	0.00%	0.00%
yoinstance_name (ila_0)	3.14%	2.80%	0.02%	4.55%	2.72%	0.92%	2.00%	0.00%	0.00%	0.00%
your_instance_name (vio_0)	0.64%	0.98%	0.00%	1.79%	0.64%	0.00%	0.00%	0.00%	0.00%	0.00%

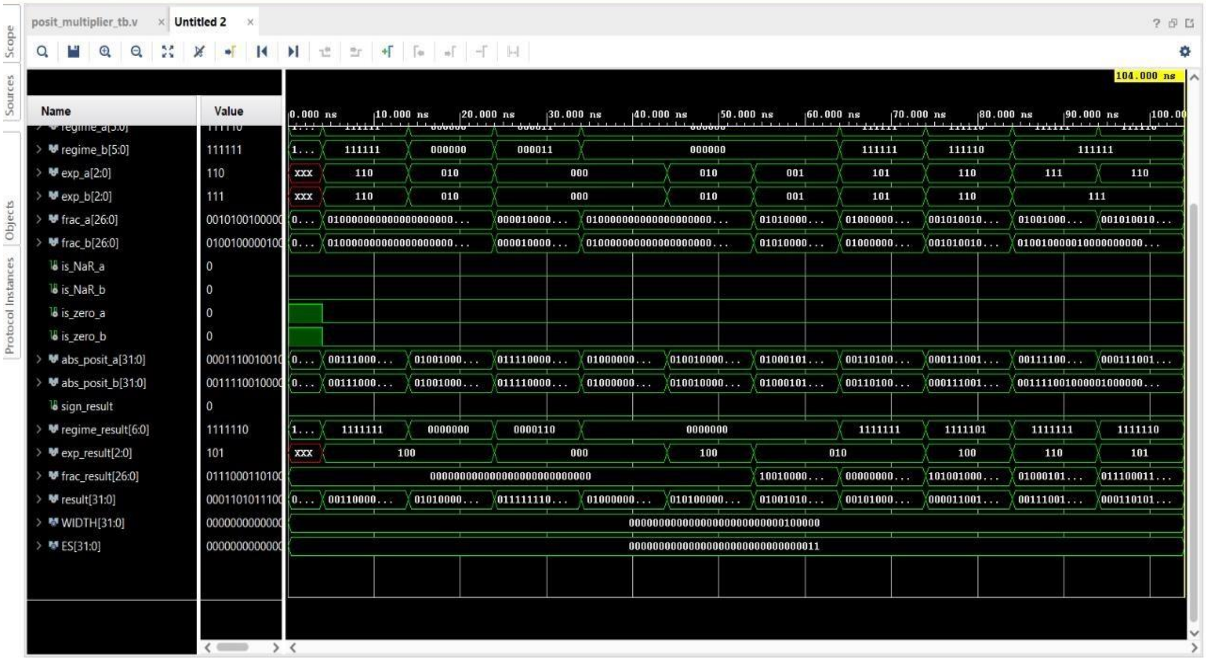
Comparison with floating point (from reference paper)



Format	SPFP
Architecture	Iterative
Device	xcvu190
f_{max} (MHz)	450
LUT	685
FF	241

c) Latency of Computation:

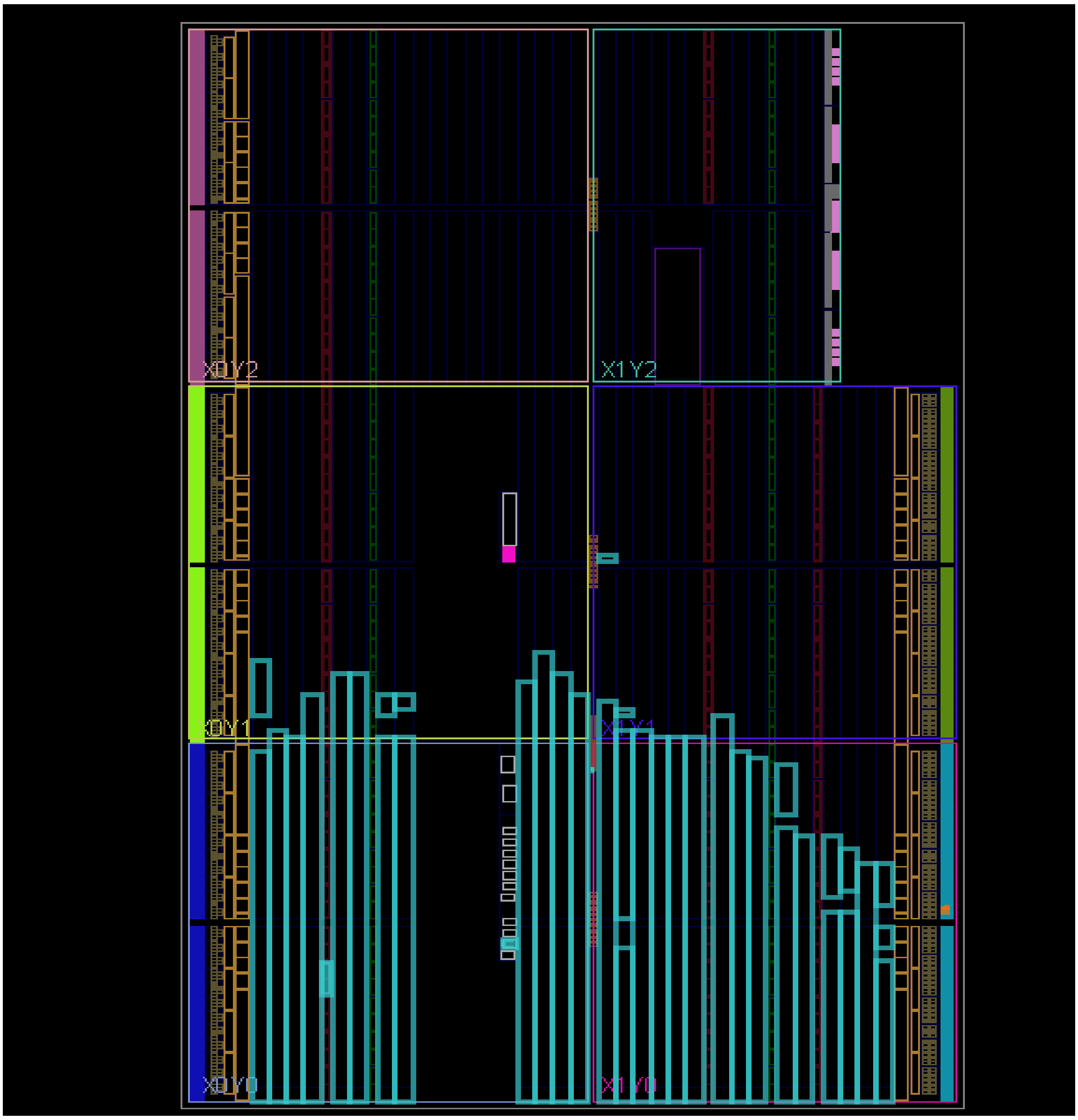
Behavioural and Post Implementation simulation Result

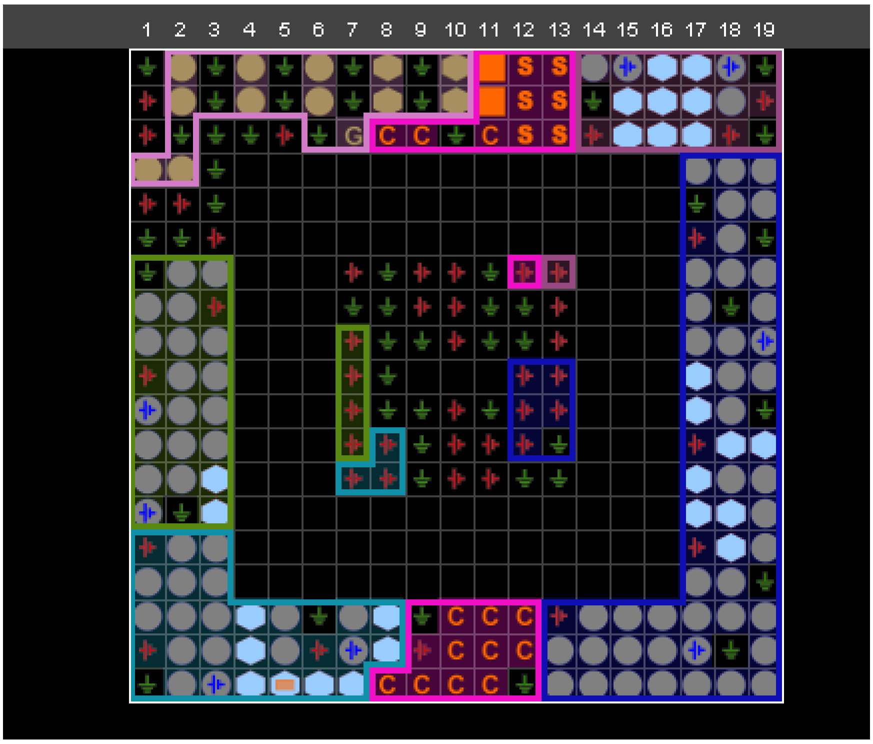


Name	Value
regime_a[5:0]	111110
regime_b[5:0]	111111
exp_a[2:0]	110
exp_b[2:0]	111
frac_a[26:0]	0010100100000
frac_b[26:0]	0100100000100
is_NaR_a	0
is_NaR_b	0
is_zero_a	0
is_zero_b	0
abs_posit_a[31:0]	0001110010010
abs_posit_b[31:0]	0011110010000
sign_result	0
regime_result[6:0]	1111110
exp_result[2:0]	101
frac_result[26:0]	0111000110100
result[31:0]	0001101011100
WIDTH[31:0]	0000000000000
ES[31:0]	0000000000000

No latency

d) Implemented Layout Diagram:





e) Max throughput achievable:

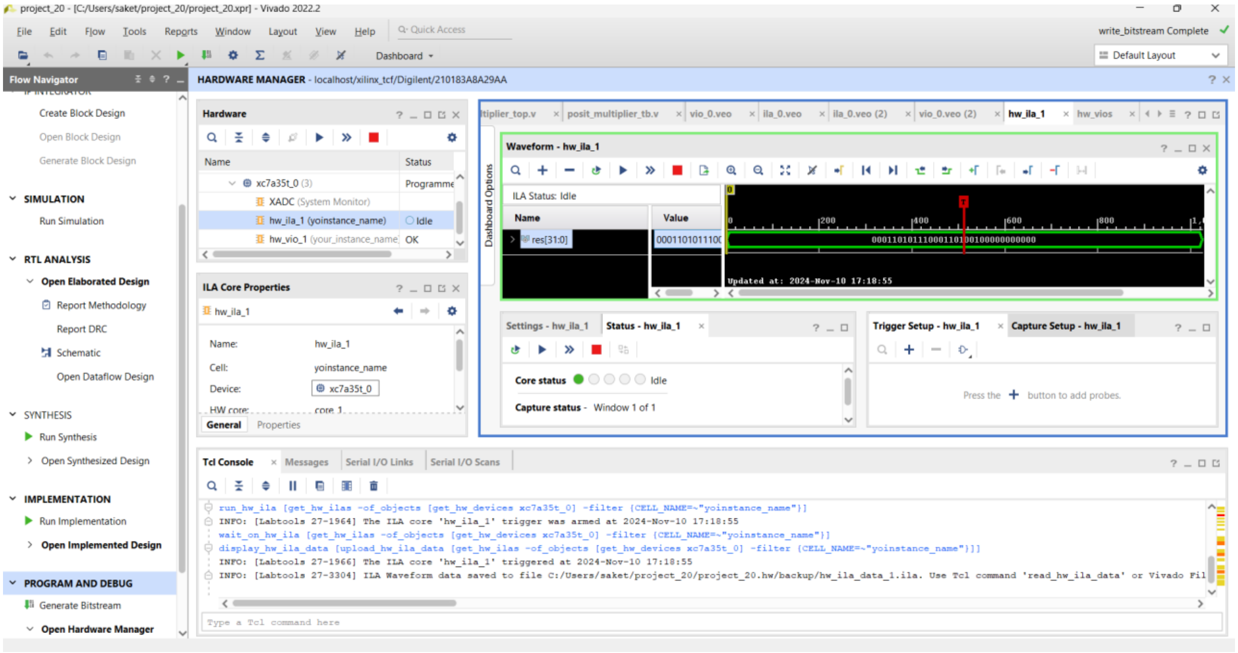
$$Max\ throughput = \frac{1}{Tclk * Max\ Utilization\ percentage}$$

$$Max\ throughput = \frac{1}{4.5ns * 3.8} * 100$$

$$Max\ throughput = 5.84 * 10^9 Hz$$

Maximum achievable throughput = 5.84GHz

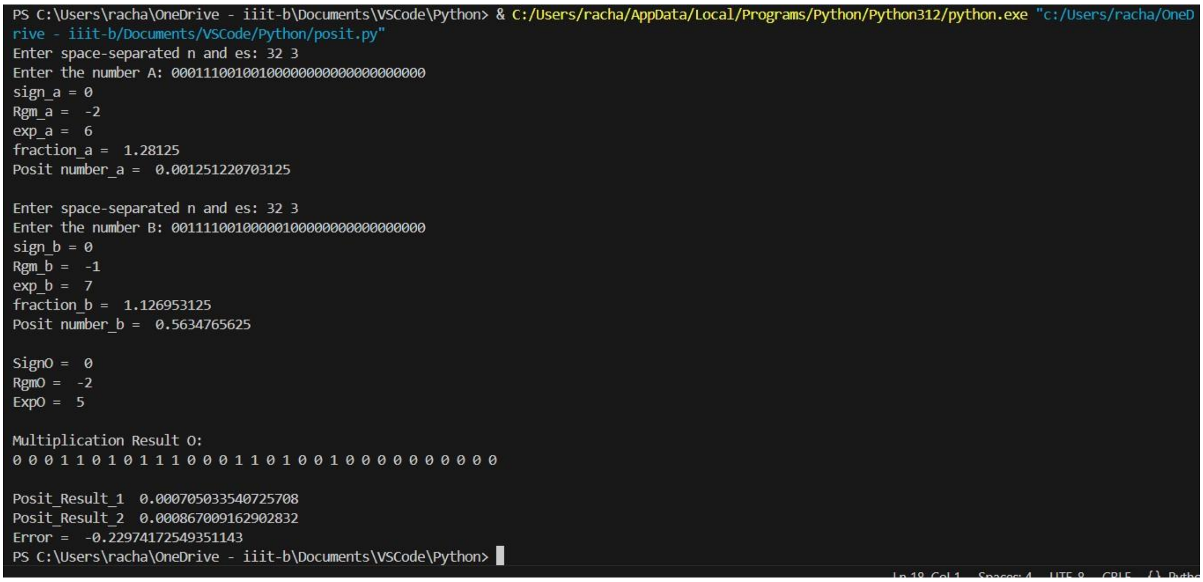
f) Bitstream Result on ILA



```
run_hw_ila [get_hw_ilas -of_objects [get_hw_devices xc7a35t_0] -filter {CELL_NAME=~"yoinstance_name"}]
INFO: [Labtools 27-1964] The ILA core 'hw_ila_1' trigger was armed at 2024-Nov-10 17:18:55
wait_on_hw_ila [get_hw_ilas -of_objects [get_hw_devices xc7a35t_0] -filter {CELL_NAME=~"yoinstance_name"}]
display_hw_ila_data [upload_hw_ila_data [get_hw_ilas -of_objects [get_hw_devices xc7a35t_0] -filter {CELL_NAME=~"yoinstance_name"}]]
INFO: [Labtools 27-1966] The ILA core 'hw_ila_1' triggered at 2024-Nov-10 17:18:55
INFO: [Labtools 27-3304] ILA Waveform data saved to file C:/Users/saket/project_20/project_20.hw/backup/hw_ila_data_1.ila. Use Tcl command 'read_hw_ila_data' or Vivado Fil
Type a Tcl command here
```

g) Error Calculation

Error calculation is performed using a Python program



```
PS C:\Users\racha\OneDrive - iiit-b\Documents\VSCode\Python> & C:/Users/racha/AppData/Local/Programs/Python/Python312/python.exe "c:/Users/racha/OneD
rive - iiit-b/Documents/VSCode/Python/posit.py"
Enter space-separated n and es: 32 3
Enter the number A: 00011100100100000000000000000000
sign_a = 0
Rgm_a =  -2
exp_a =  6
fraction_a =  1.28125
Posit number_a =  0.001251220703125

Enter space-separated n and es: 32 3
Enter the number B: 00111100100000100000000000000000
sign_b = 0
Rgm_b =  -1
exp_b =  7
fraction_b =  1.126953125
Posit number_b =  0.5634765625

Sign0 =  0
Rgm0 =  -2
Exp0 =  5

Multiplication Result O:
0 0 0 1 1 0 1 0 1 1 1 0 0 0 1 1 0 1 0 0 1 0 0 0 0 0 0 0 0 0 0 0

Posit_Result_1  0.000705033540725708
Posit_Result_2  0.000867009162902832
Error =  -0.22974172549351143
PS C:\Users\racha\OneDrive - iiit-b\Documents\VSCode\Python> ▌
```

- **GitHub Link**