International Institute of Information Technology Bangalore

Project

Performance Analysis of Full Adder using different CMOS technology

VLS 503: DCMOS VLSI DESIGN

Instructor: Dr. Madhav Rao

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Abstract:

This report summarizes the implementation of full adder at transistor level using two technology nodes, i.e. 45nm and 90nm. We present the design and their simulations in cadence and give the comparative analysis of designs from the viewpoint of delay and power. The conclusion we derive is that as the technology node reduces the performance parameter improves.

Introduction:

Any digital CMOS system has an adder as one of the central and important subsystems, for example in microprocessors, the main block is Arithmetic and Logic Unit, where in adder is main subblock, other arithmetic also has adder as part of operation, for example multiplier. Adder designs have many different types of architectures with each having its own advantage in terms of speed/power/area requirements. Some architecture improves speed at the cost of area, while others have smaller area but offer lower speed. The basic cell is a 1-bit full adder which adds two binary numbers with a carry input and gives the output.

$$Sum = A \oplus B \oplus C_{in}$$

$$Carry = AB + BC_{in} + AC_{in}$$

Input			Output	
A	*B*	*Cin*	*Sum*	*Cout*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Designs of Full Adder:

1. **Full adder using XOR gate and NAND gate**

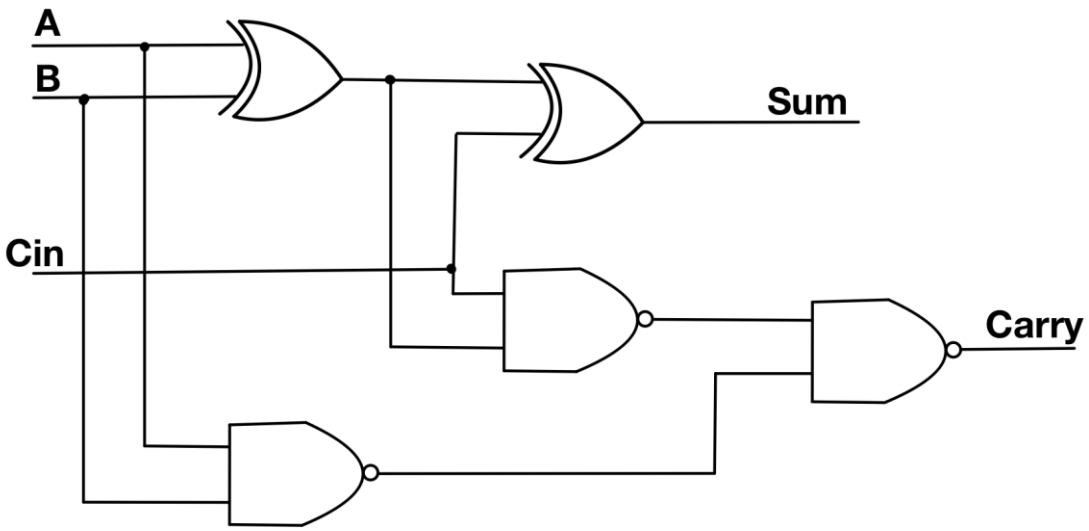
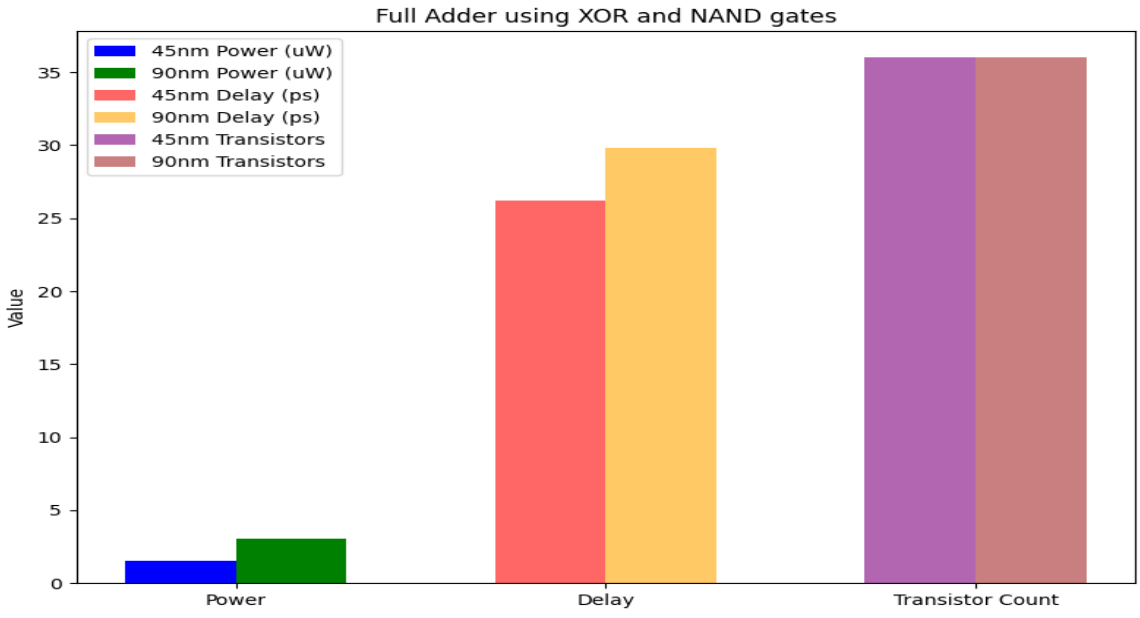


Fig 1 – Full adder using XOR and NAND gate

Design 1: Full Adder using XOR and NAND gates		
Technology Nodes	45nm	90nm
Average Power (uW)	1.52 uW	3.036 uW
Delay (ps)	26.2 ps	29.85 ps
Transistor Count	36	36



2. Full Adder using NAND gate

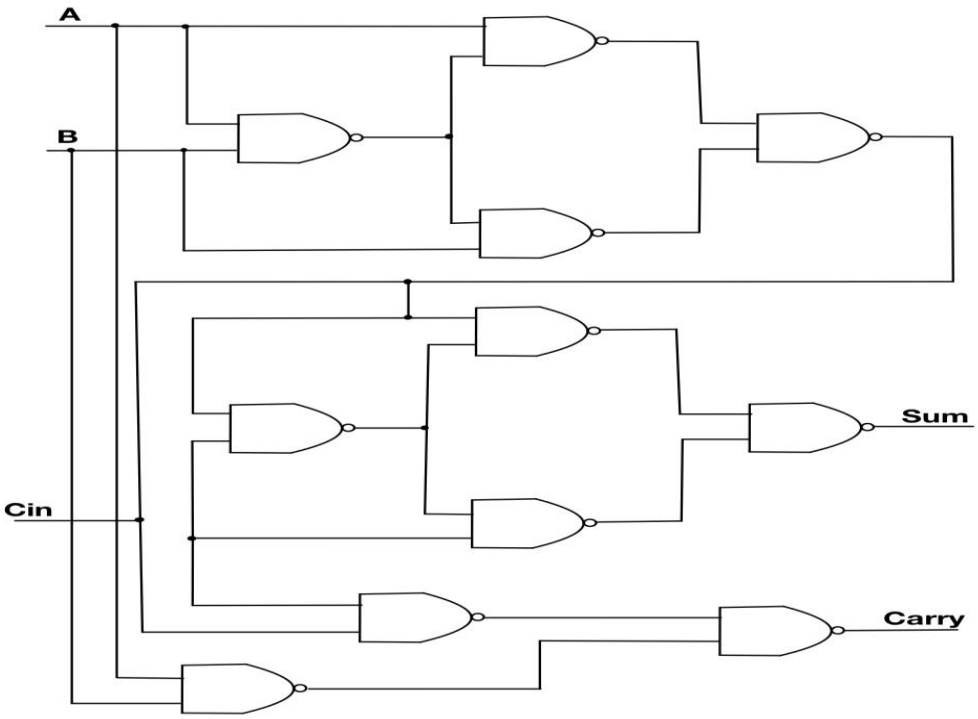
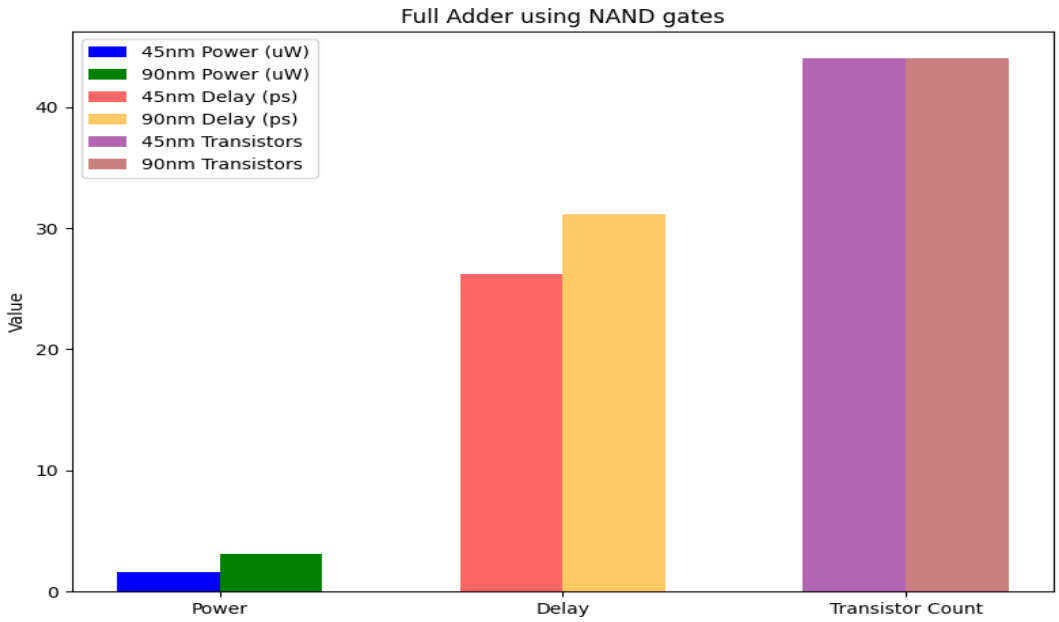


Fig 2 – Full adder using NAND gates only

Design 2: Full Adder using NAND gates		
Technology Nodes	45nm	90nm
Average Power (uW)	1.62 uW	3.12 uW
Delay (ps)	26.24 ps	31.13 ps
Transistor Count	44	44



3. Full Adder design with 28 Transistors

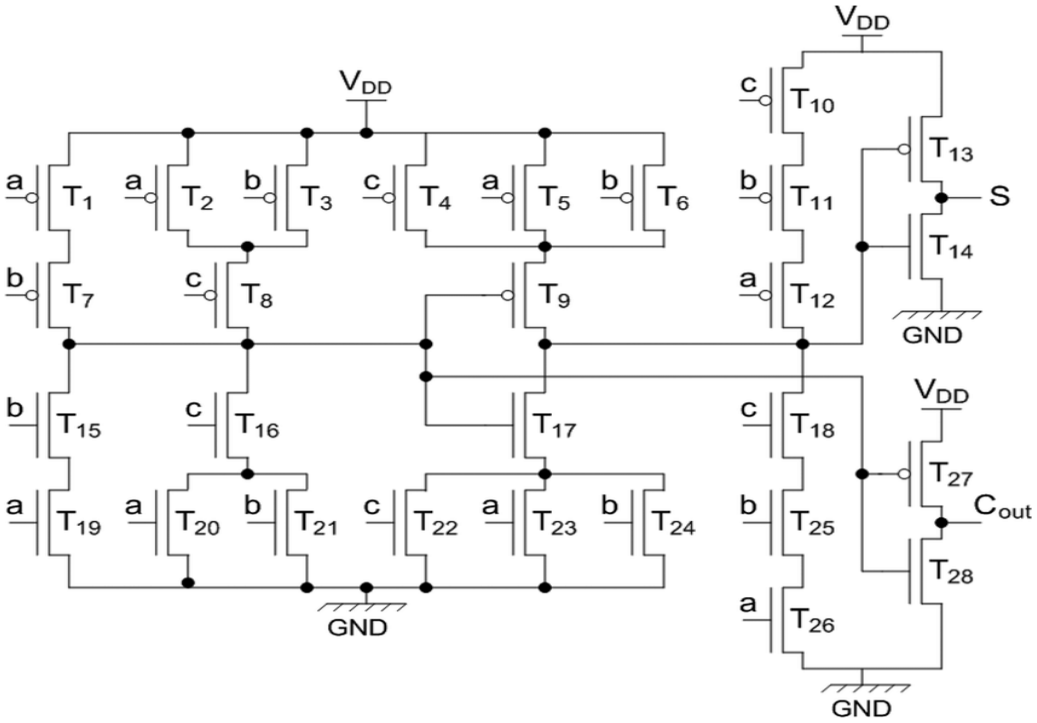
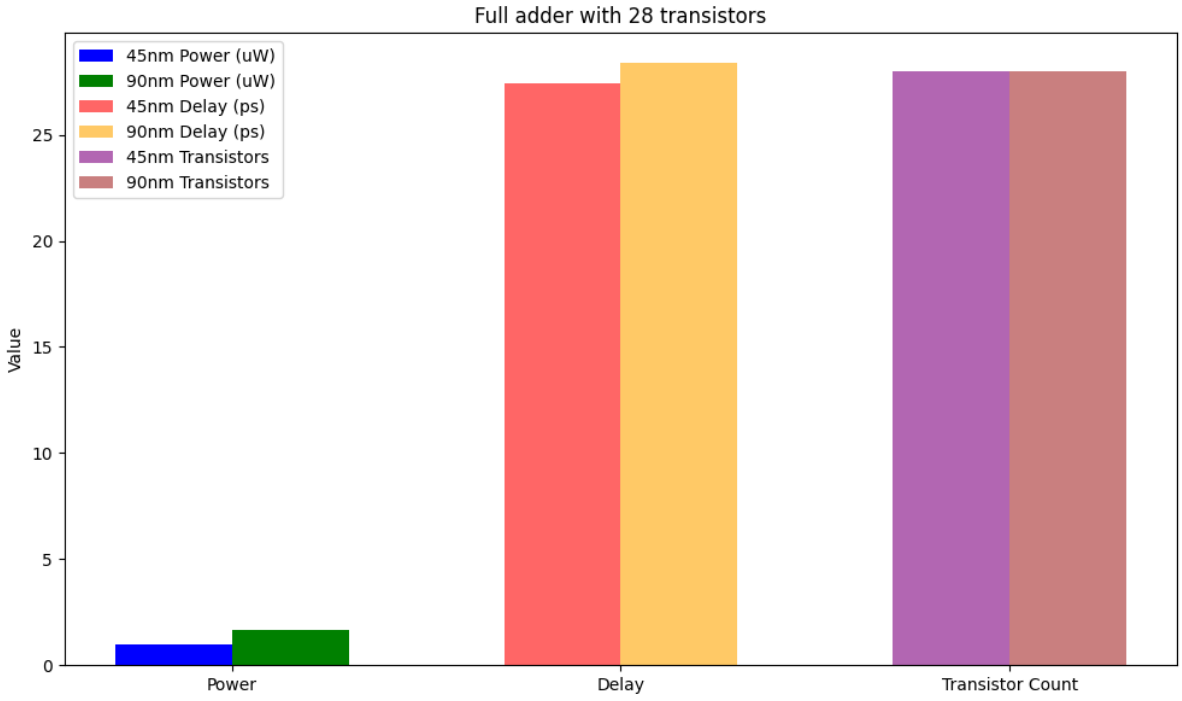


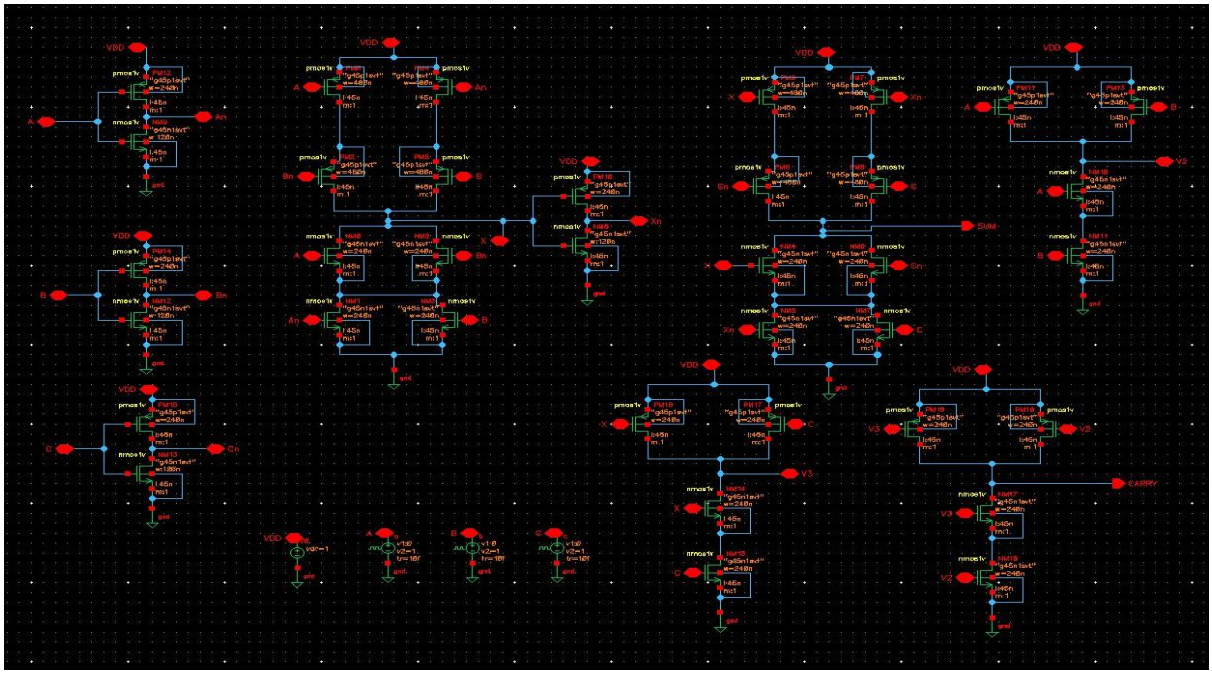
Fig 3 – Full adder with 28 transistors

Design 3: Full Adder with 28 transistors		
Technology Nodes	45nm	90nm
Average Power (uW)	1.01 uW	1.64 uW
Delay (ps)	27.42 ps	28.37 ps
Transistor Count	28	28

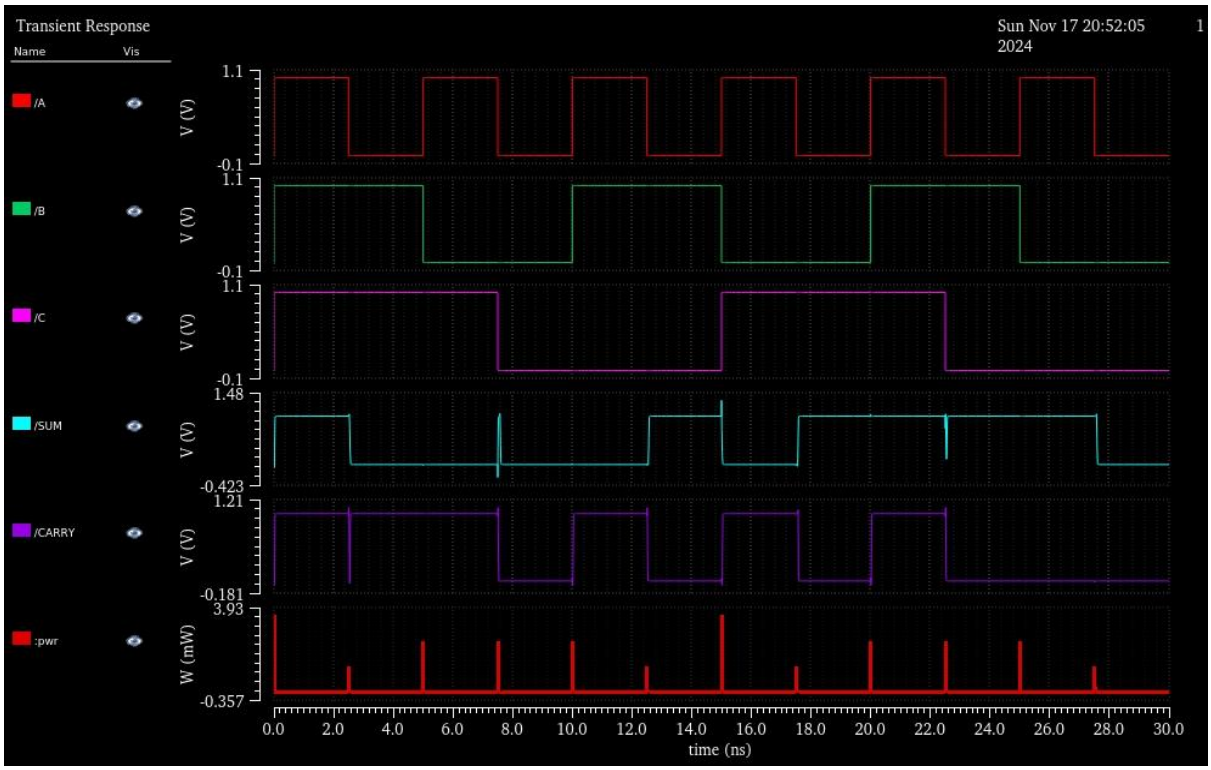


I. Full Adder Design with XOR and NAND Gate using 45 nm CMOS Technology

a) Schematic:

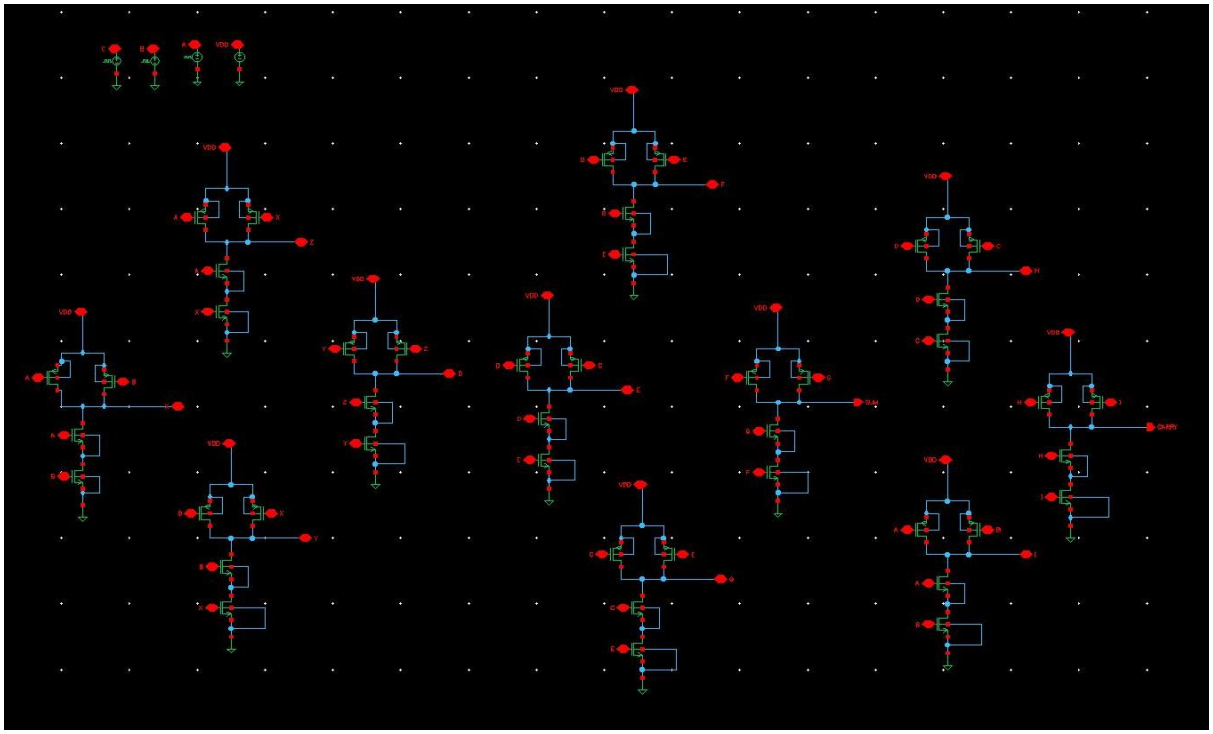


b) Waveforms:

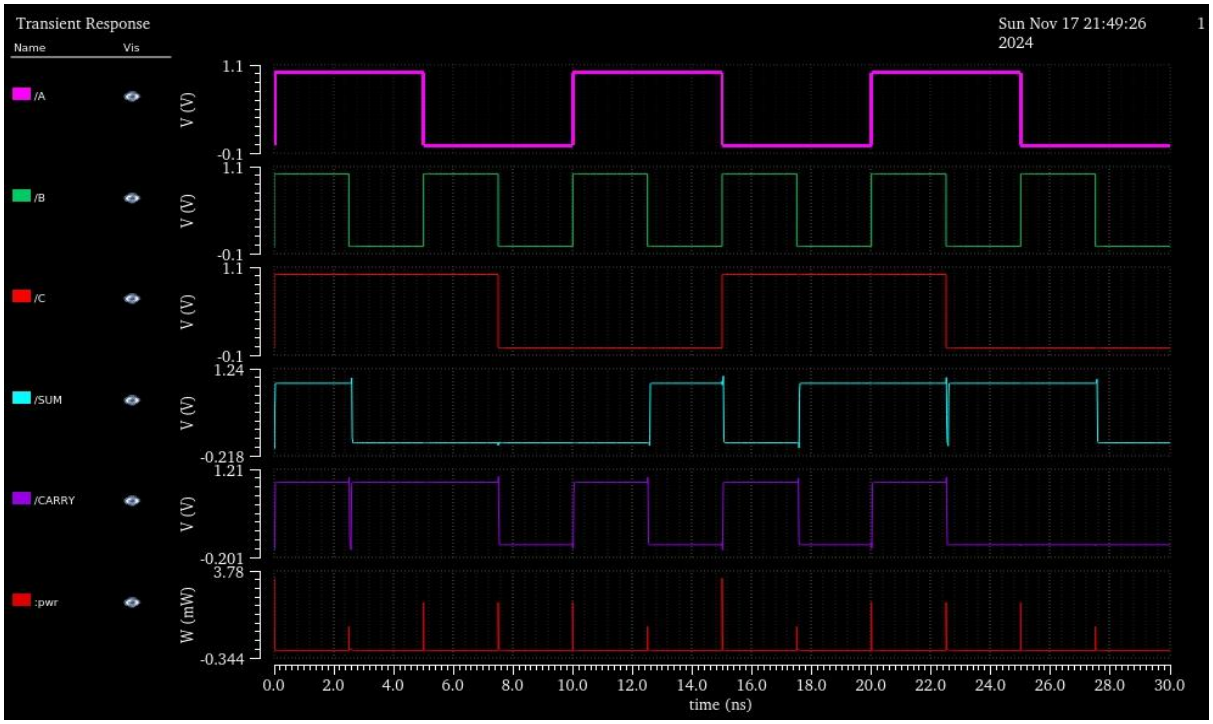


II. Full Adder Design with NAND Gate using 45 nm CMOS Technology

a) Schematic:

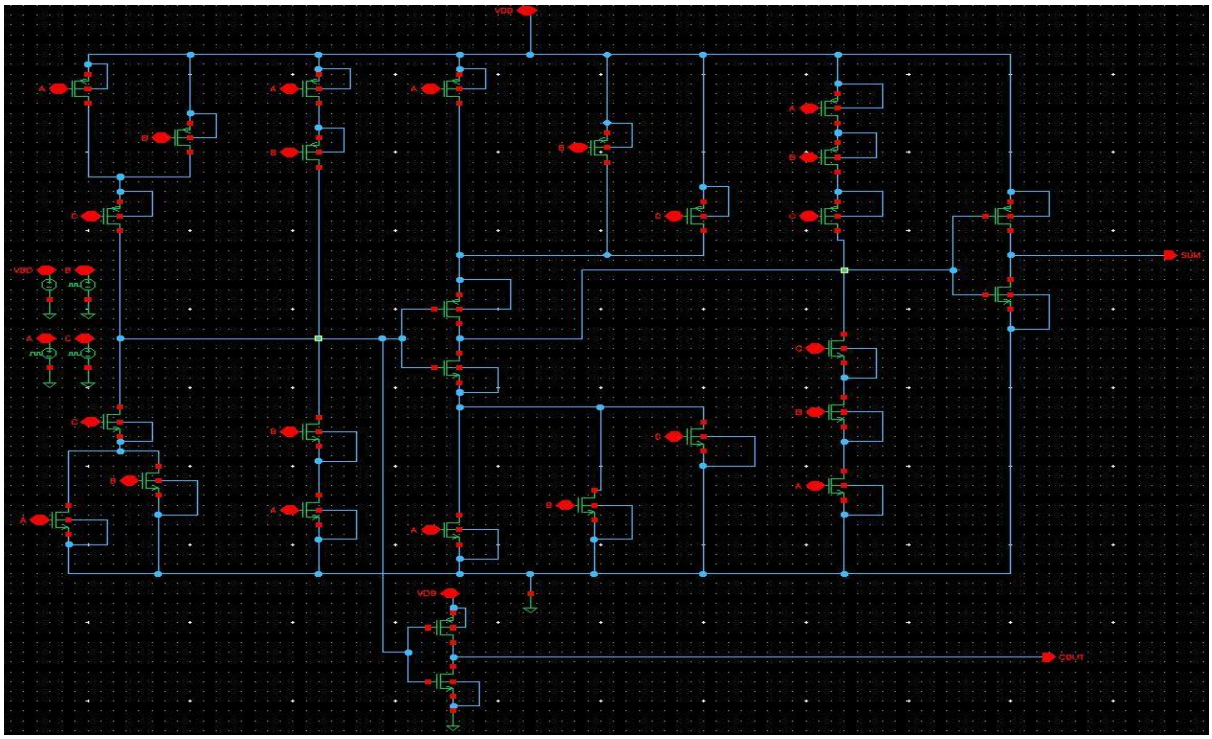


b) Waveforms:

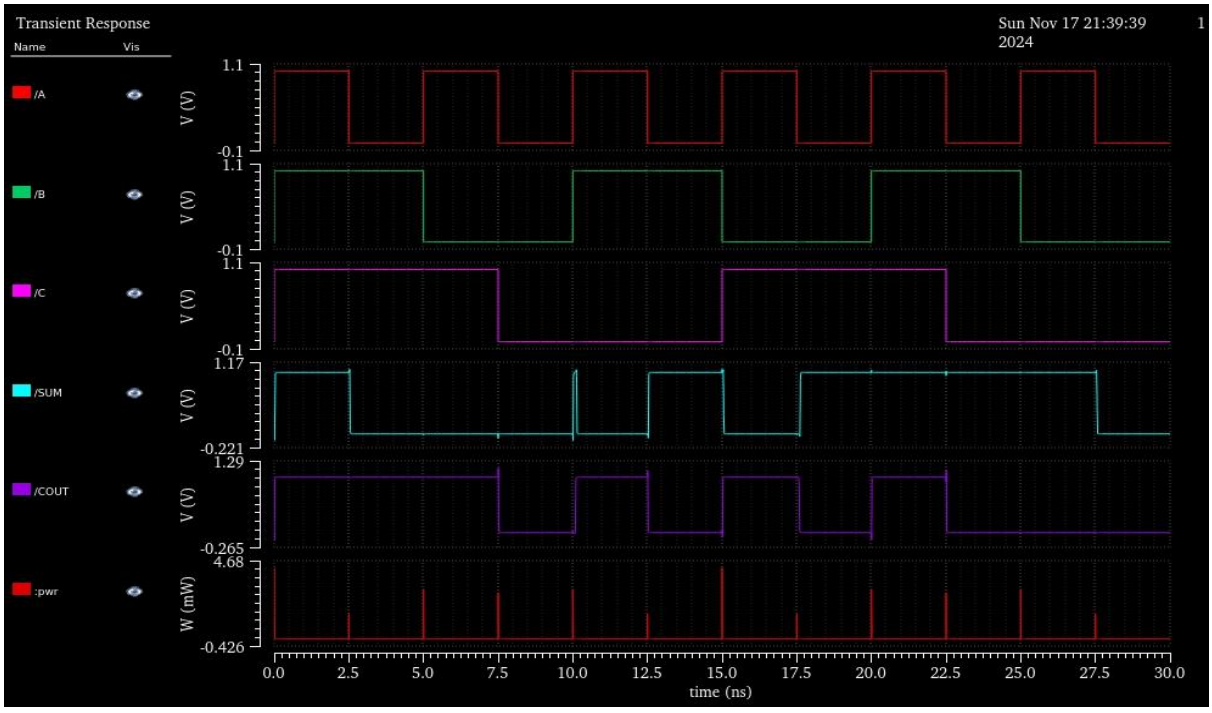


III. Full Adder Design with 28 Transistors using 45 nm CMOS Technology

a) Schematic:

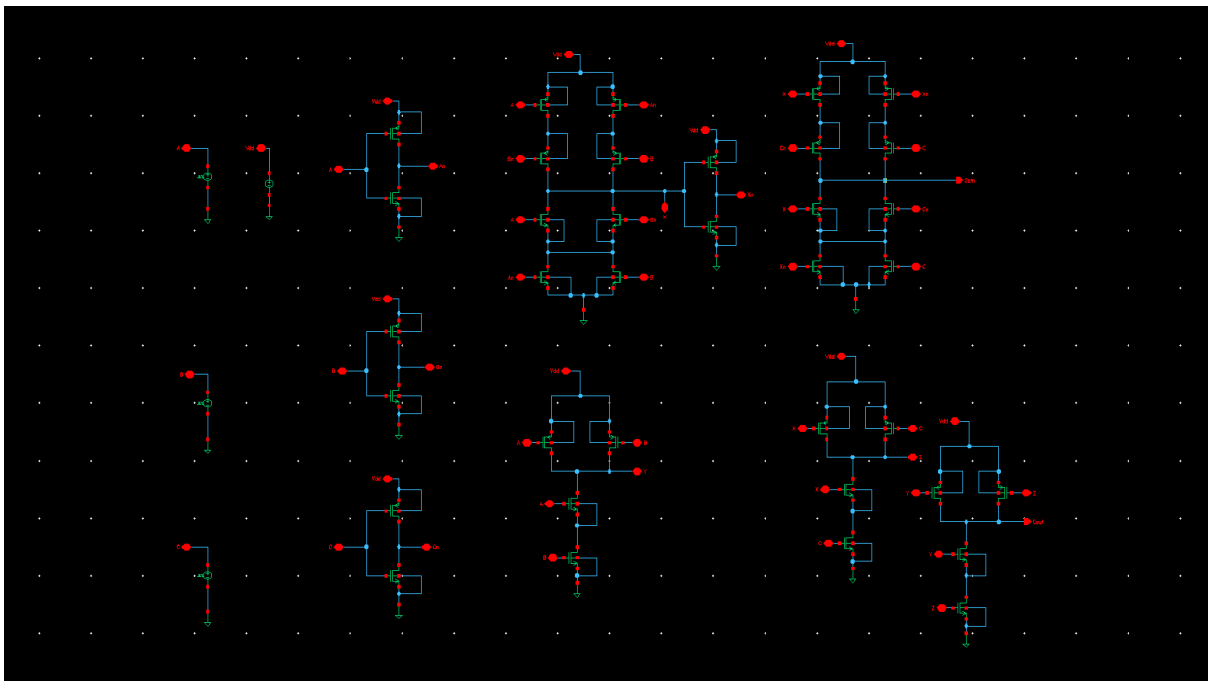


b) Waveforms:

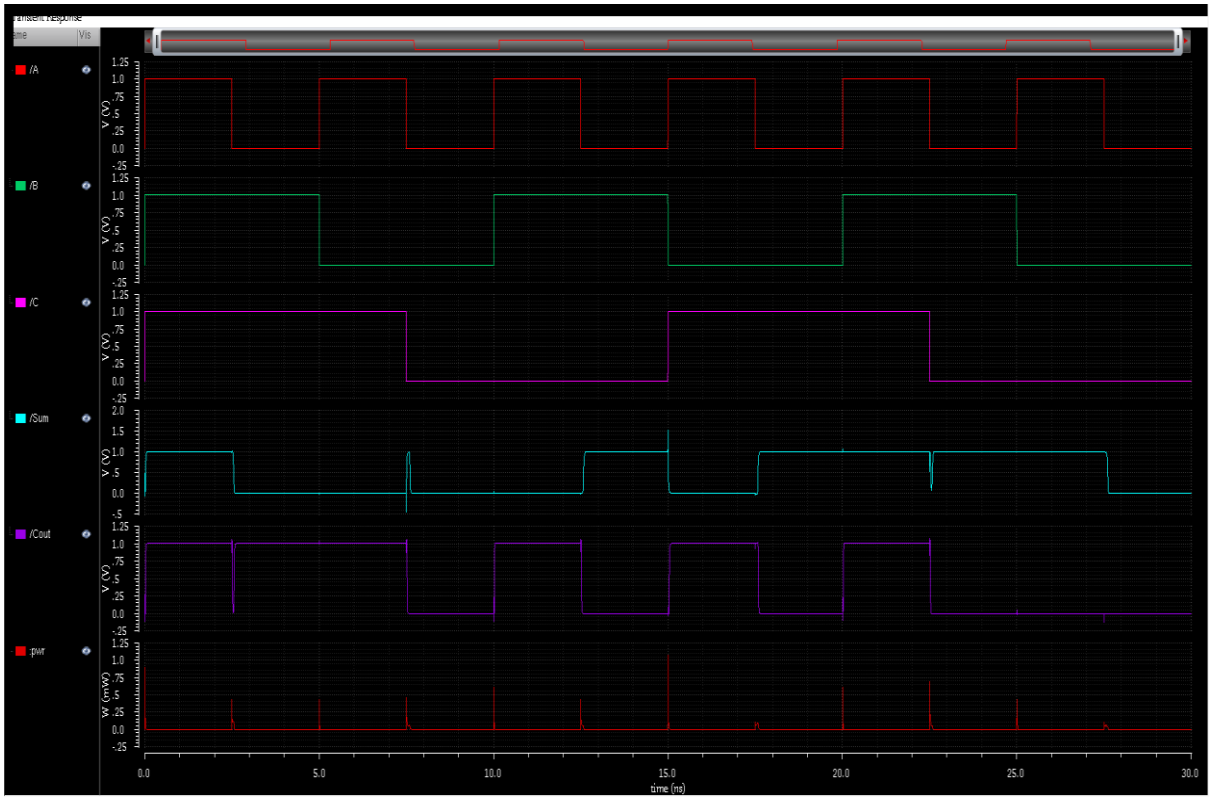


IV. Full Adder Design with XOR and NAND Gate using 90 nm Technology

a) Schematic:

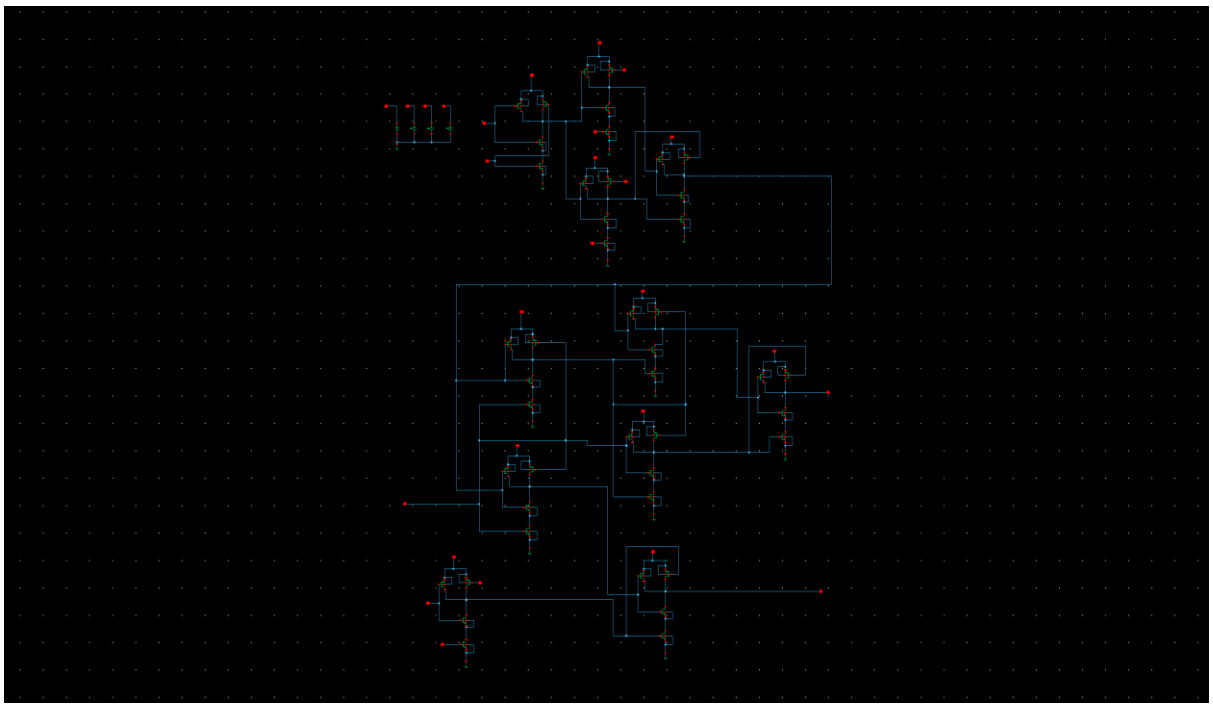


b) Waveforms:

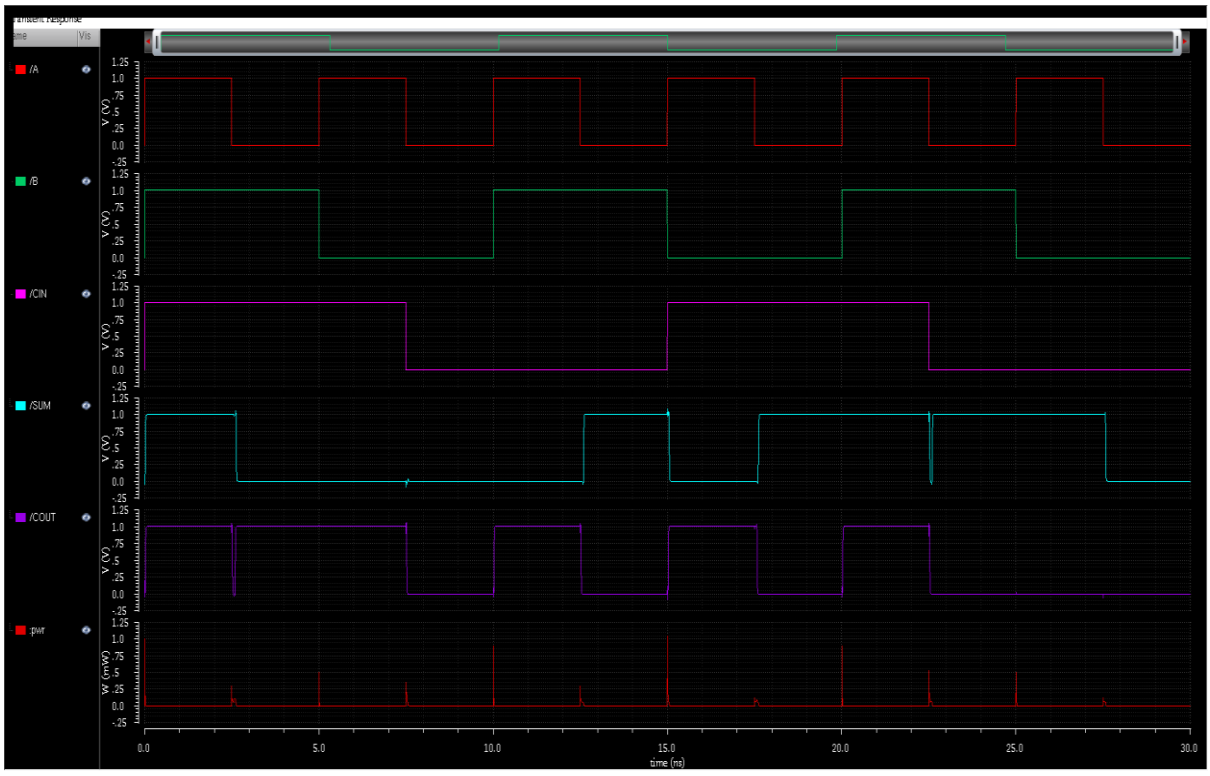


V. Full Adder Design with NAND Gate using 90 nm Technology

a) Schematic:

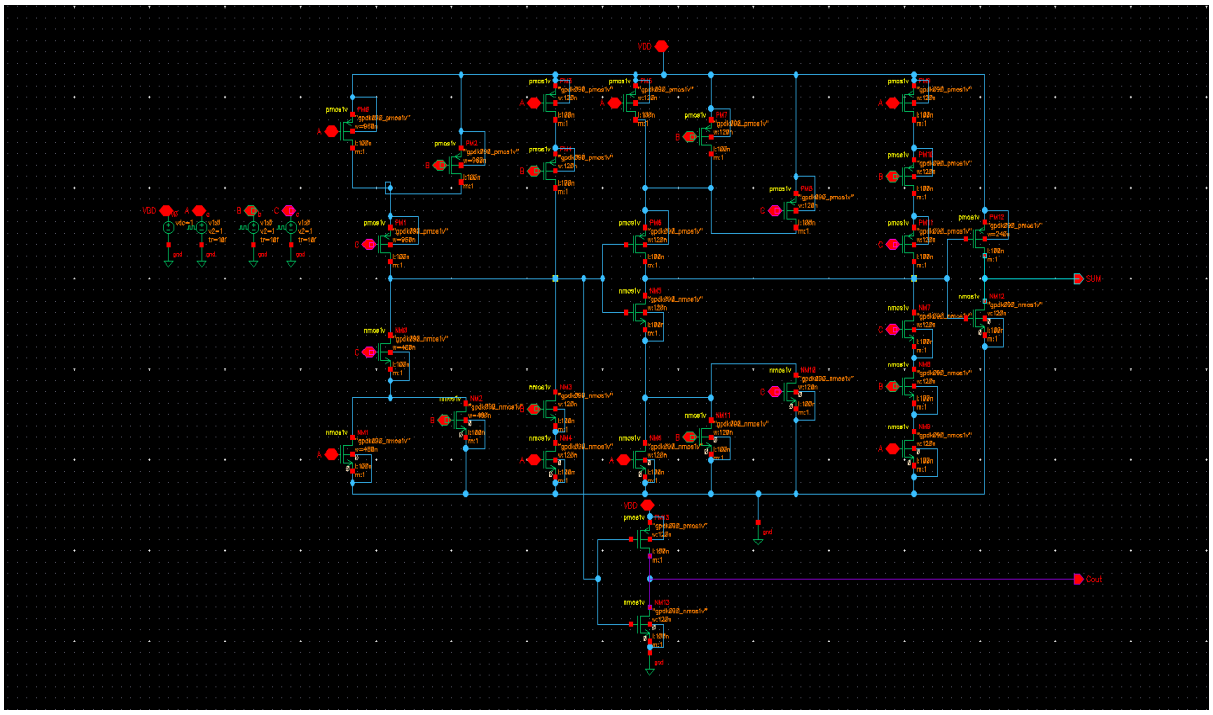


b) Waveforms:

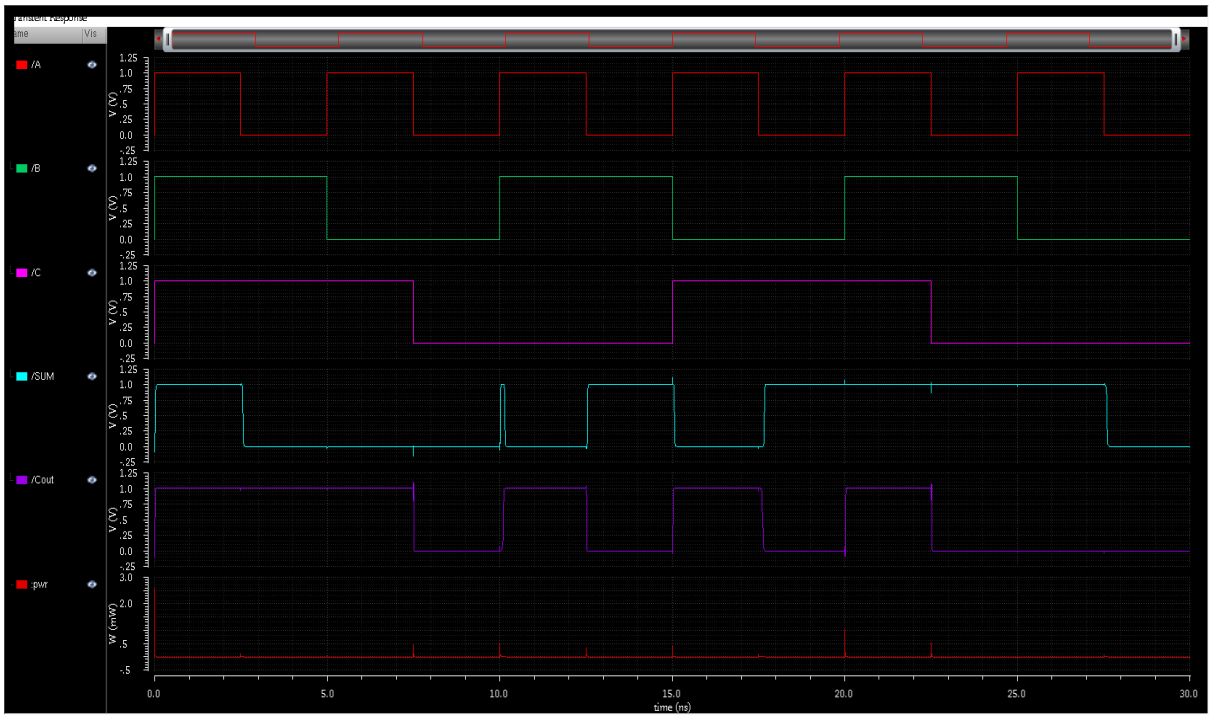


VI. Full Adder Design with 28 Transistors using 90 nm CMOS Technology

a) Schematic:



b) Waveforms:



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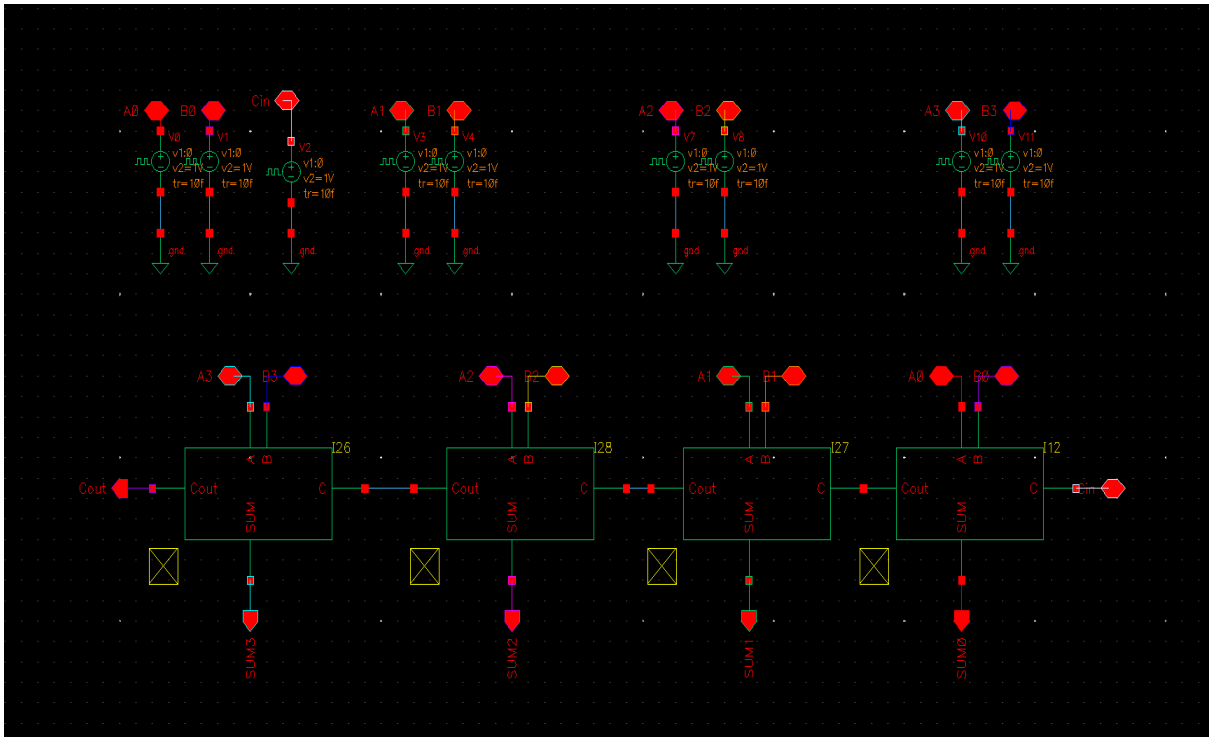
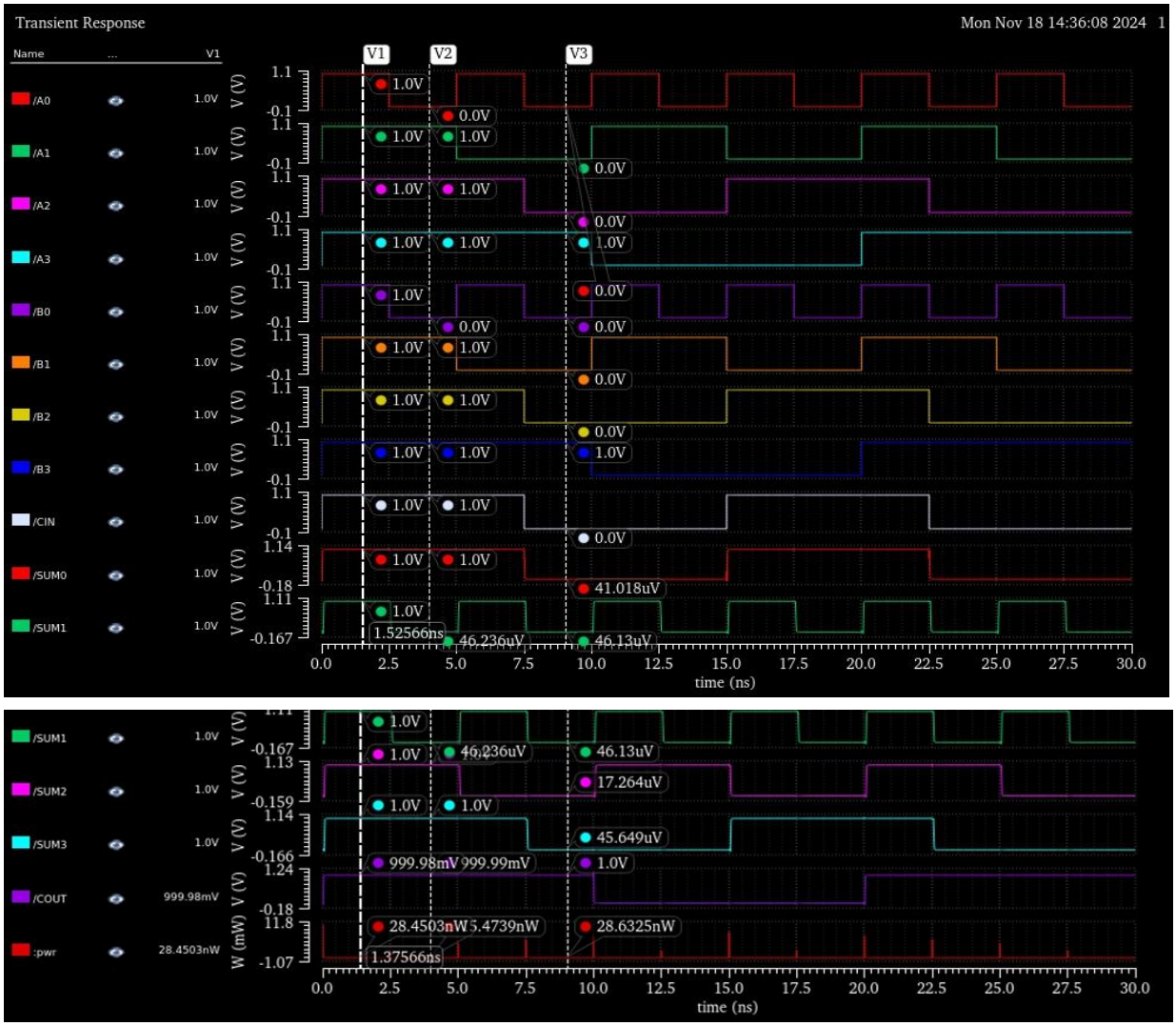
4-bit Parallel Adder

Schematic:



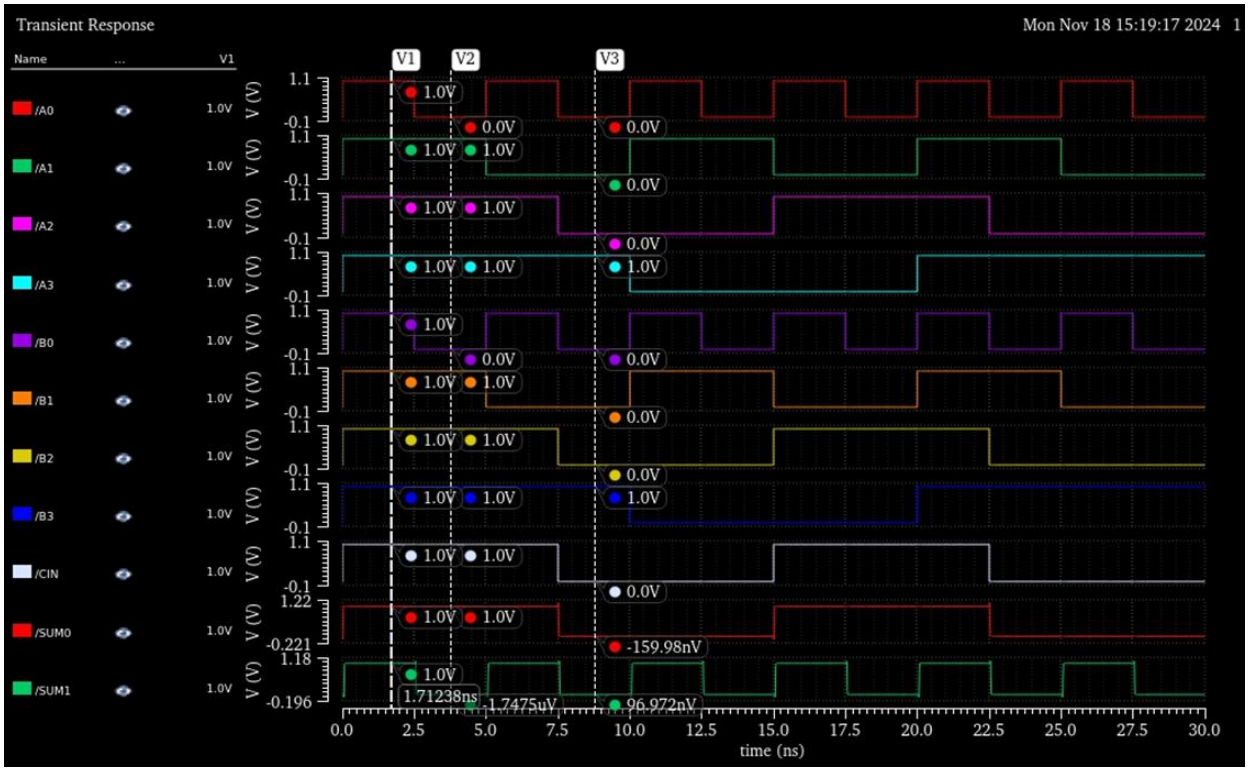
I. 4-Bit adder using XOR-NAND gates with 45nm technology

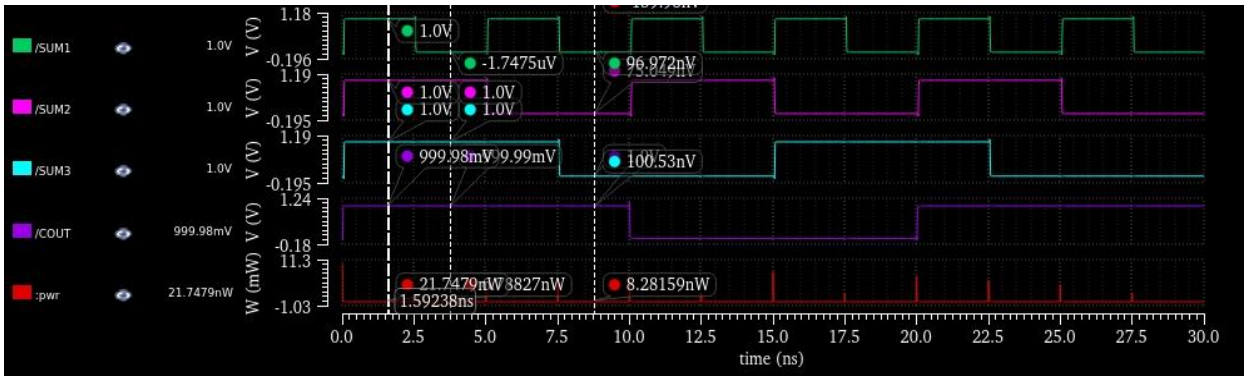
Waveforms:



II. 4-Bit adder using NAND gates 45nm technology

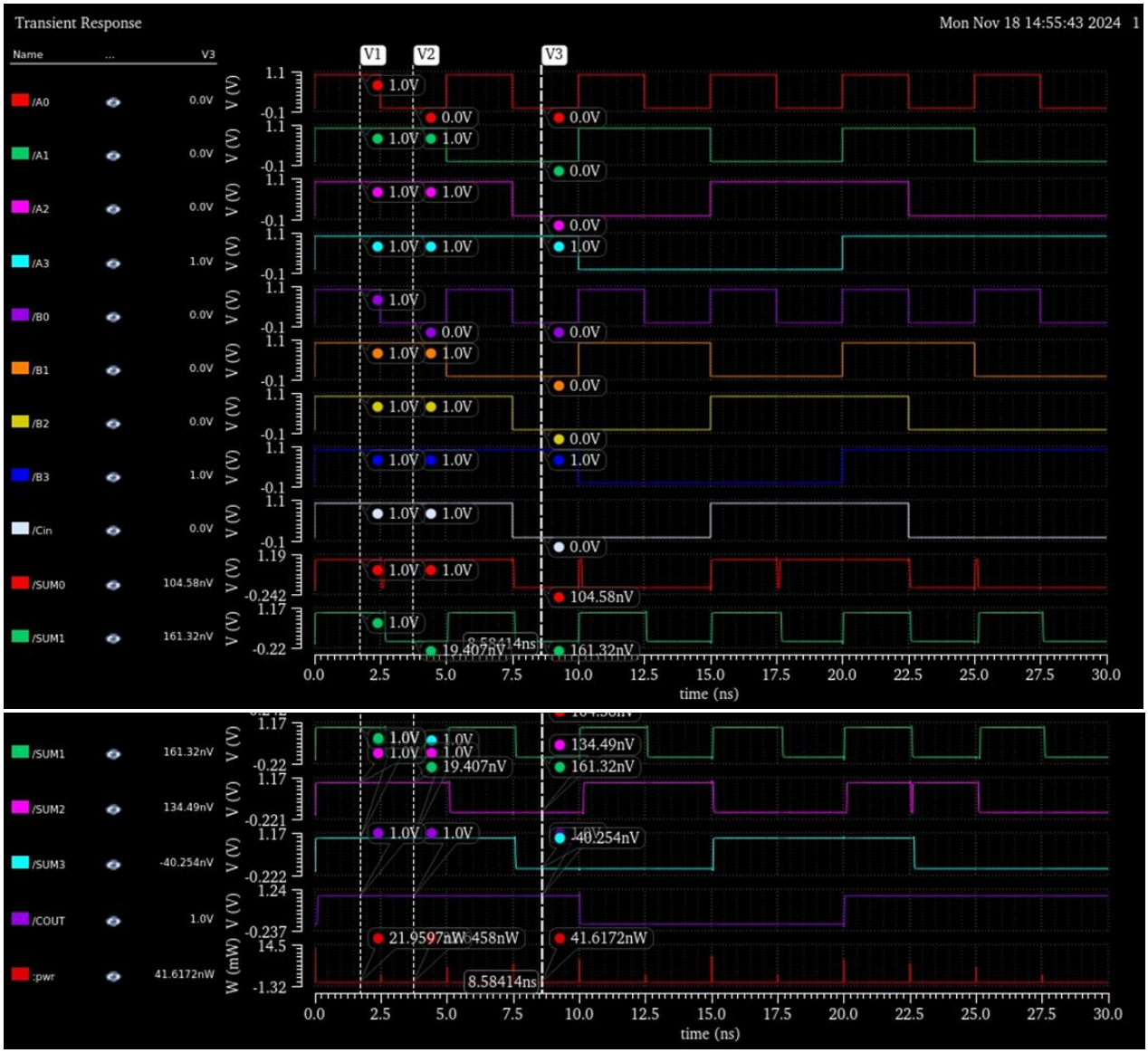
Waveforms:





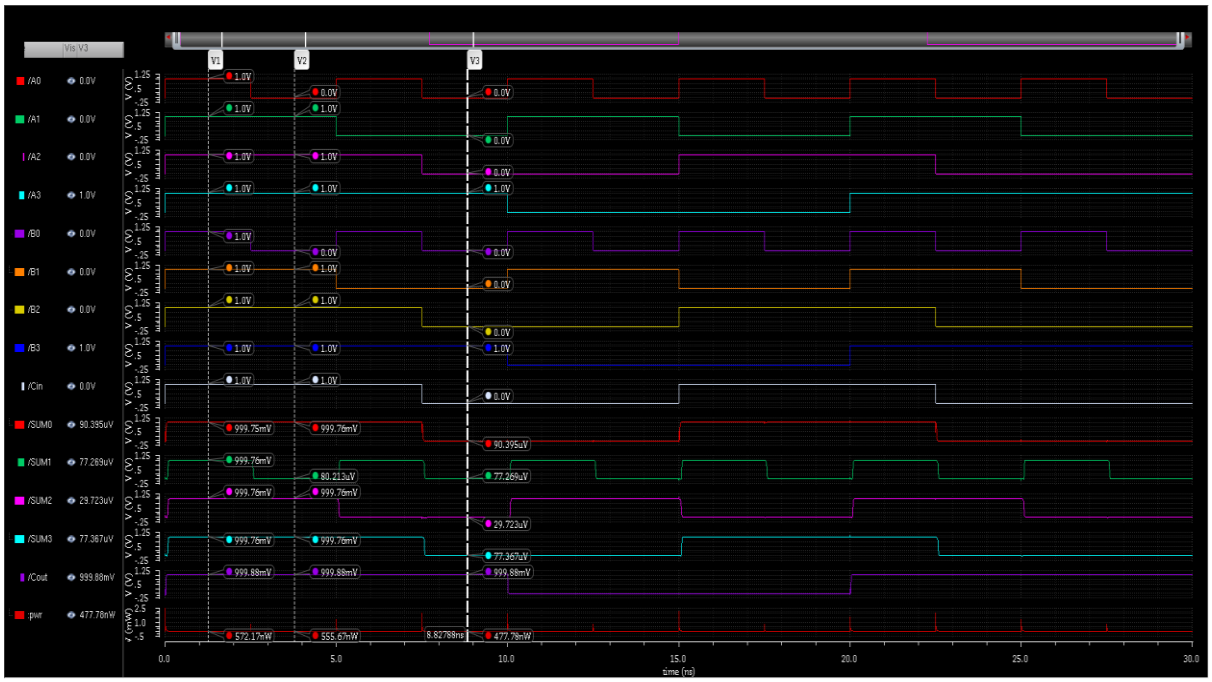
III. 4-Bit adder based on 28 Transistor 1-Bit adder 45nm technology

Waveforms:



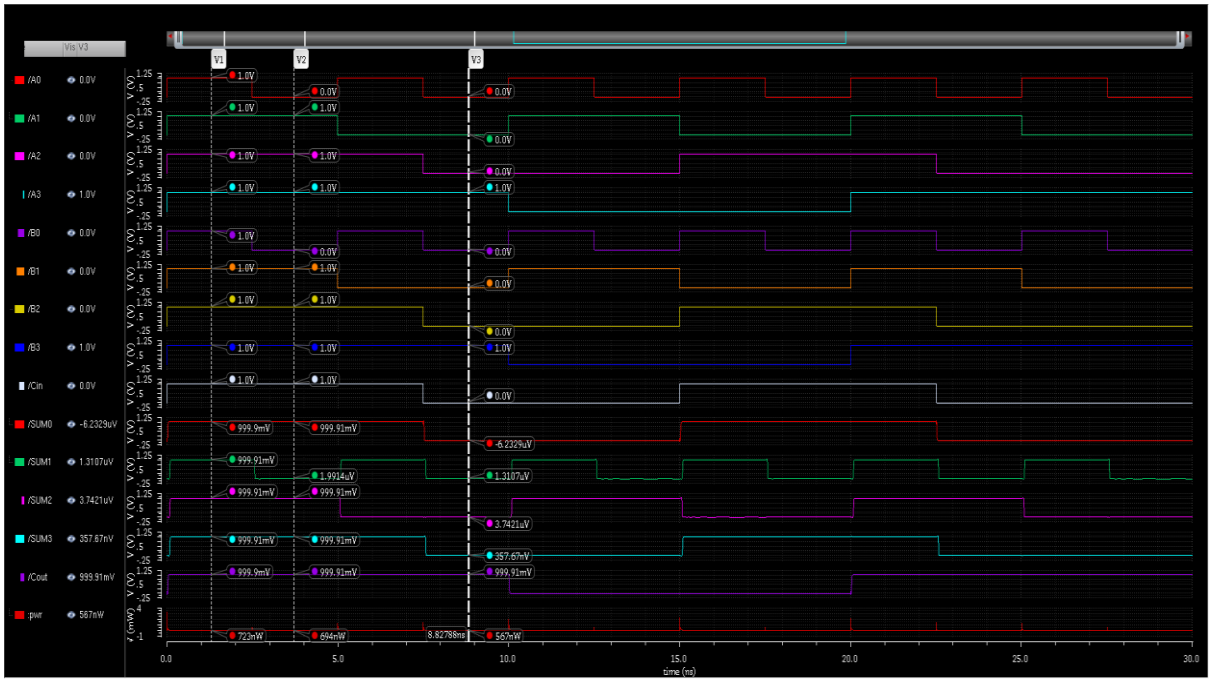
IV. 4-Bit adder using XOR-NAND gates with 90nm technology

Waveforms:



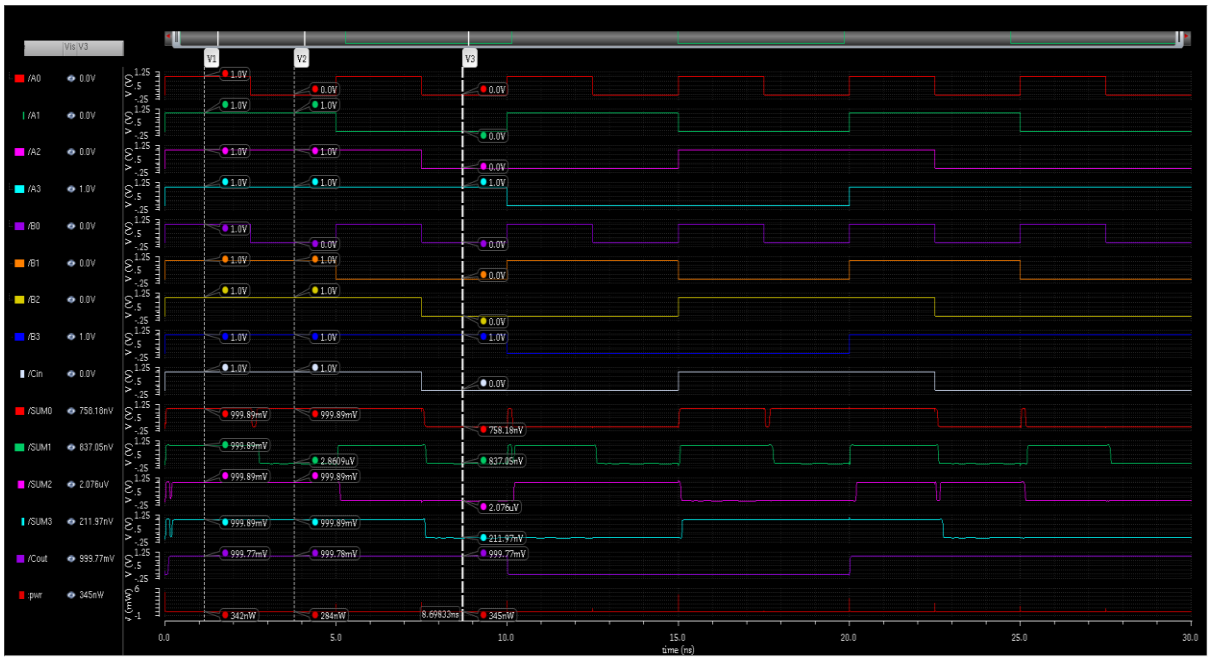
V. 4-Bit adder using NAND gates 90nm technology

Waveforms:



VI. 4-Bit adder based on 28 Transistor 1-Bit adder 90nm technology

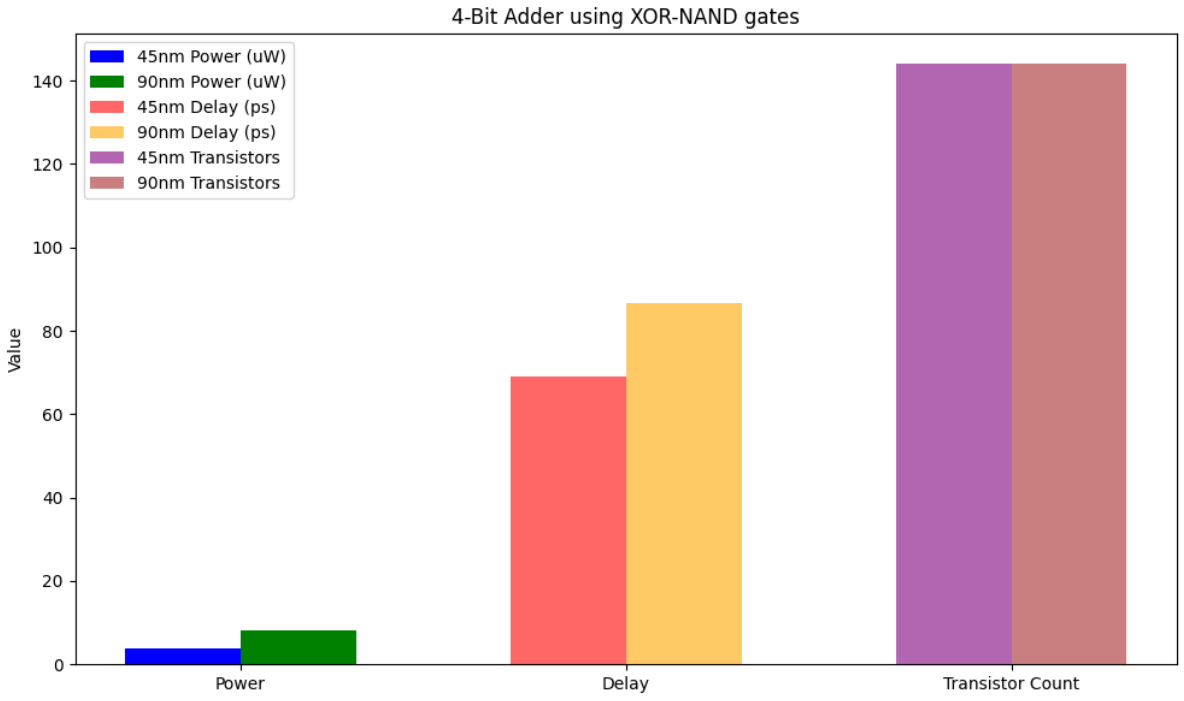
Waveforms:



4-bit Parallel Adder Trends:

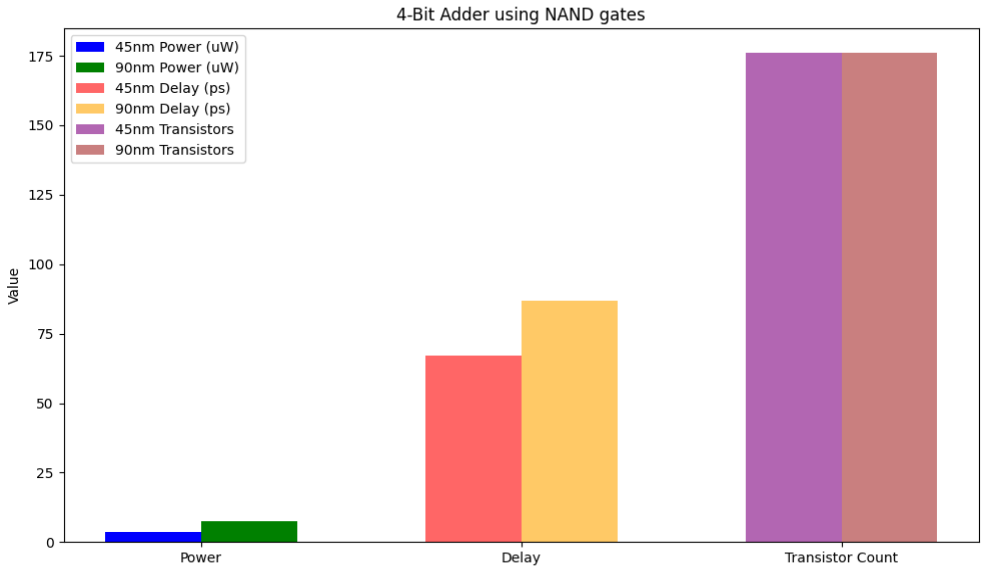
1. 4-Bit adder using XOR-NAND gates

4-Bit adder using XOR-NAND gates		
Technology Nodes	45nm	90nm
Average Power (uW)	3.889 uW	8.167uW
Delay (ps)	69.16 ps	86.7ps
Transistor Count	144	144



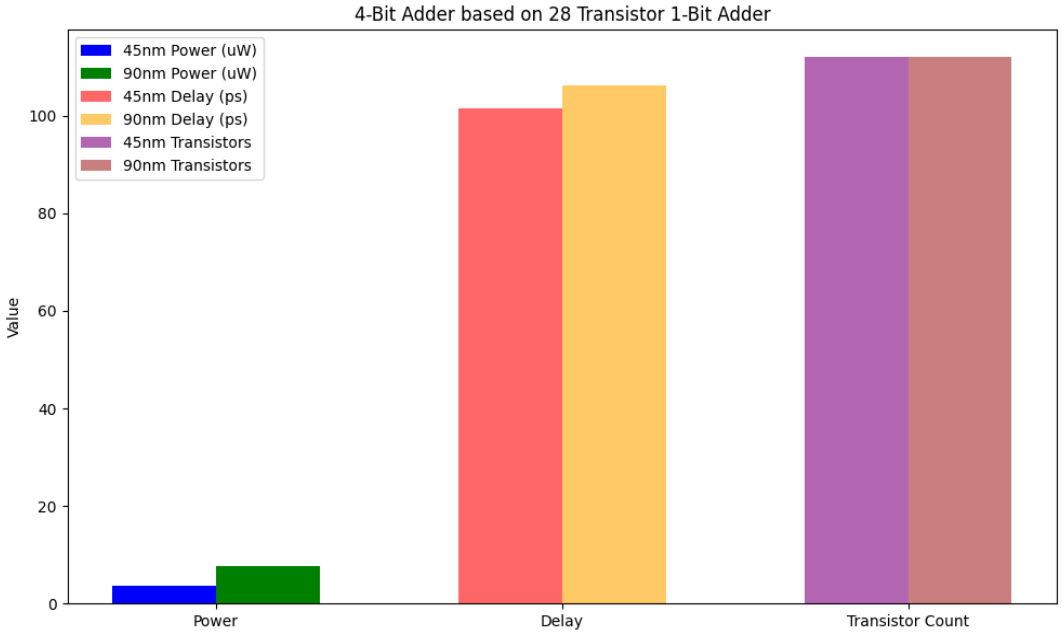
2. 4-Bit adder using NAND gates

4-Bit adder using NAND gates		
Technology Nodes	45nm	90nm
Average Power (uW)	3.734 uW	7.636 uW
Delay (ps)	66.95 ps	86.87 ps
Transistor Count	176	176



3. 4-Bit adder based on 28 Transistor 1-Bit adder

4-Bit adder based on 28 Transistor 1-Bit adder		
Technology Nodes	45nm	90nm
Average Power (uW)	3.742 uW	7.804uW
Delay (ps)	101.5 ps	106.3ps
Transistor Count	112	112



Conclusion:

In this report, we did a comparative analysis of three different designs of adders for 1-bit adders in two different technology nodes, 45nm and 90nm. The percentage improvement in propagation delay for 45nm node over 90nm for design with 28 transistors is 3.35%, 15.70% in case of design with 44 transistors based on NAND gates and 12.06% in case of 36 transistors based on XNOR-NAND based design.

For 4-bit adders using above 1-bit adder designs is around 4.51% for design with 28 transistors, 22.93% for design with 44 transistors based on NAND gates and 20.23 % for 36 transistors based on XNOR-NAND based design.

References:

[1] H. N. Y. Pwint and T. T. Hla, "Performance Analysis of Full Adder Using Different CMOS Technology," 2024 IEEE Conference on Computer Applications (ICCA), Yangon, Myanmar, 2024, pp. 1-5, doi: 10.1109/ICCA62361.2024.10532847.

[2] V. Rajput, A. P. Singh, S. Tirkey and S. Nakhate, "Design of Full Adder Circuits with Optimized Power and Speed Using CMOS Technique," 2024 IEEE International Students' Conference on Electrical, Electronics and Computer Science (SCEECS), Bhopal, India, 2024, pp. 1-5, doi: 10.1109/SCEECS61402.2024.10482060.

[3] S. -K. Chang and C. -L. Wey, "A Fast 64-bit hybrid adder design in 90nm CMOS process," 2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS), Boise, ID, USA, 2012, pp. 414-417, doi: 10.1109/MWSCAS.2012.6292045.