XN297 Data Sheet (EN)

2.4GHz single chip high-speed wireless transceiver chip

Functional Description:

Frequency range 2400 ~ 2483MHz
Wireless speed: 1 or 2Mbps
SPI interface speed: 0 ~ 8Mbps
General-purpose communication and enhanced communication
GFSK monolithic transceiver chip
Ultra-low power consumption
Built-in hardware link layer
Automatic response and automatic retransmission
Fast channel switching, can be applied to frequency hopping algorithm
20-pin QFN 4mm × 4mm package

Low-cost crystal ± 60ppm
The use of simple low-cost peripheral components
Low operating voltage: 2.0 ~ 3.6V
Can support double-sided PCB board program

Applications:

Wireless mouse and wireless keyboard
Wireless gaming devices
Wireless data communication

Smart TV remote control
Wireless tags
Wireless access
Security system
Remote control device

Remote sensing survey
Intelligent sports equipment
Industrial sensors and wireless industrial equipment
Wireless toys

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1. Overview

XN297 is a single-chip wireless transceiver in the world-wide 2.4 ~ 2.483GHz ISM band chip. The chip integrates RF transceiver, frequency generator, multi-communication mode controller, crystal oscillator, modulator, demodulator and other functional modules. It can be flexibly configured via SPI interface for output power, channel selection, protocol settings and other purposes.

XN297 chip advantages:

Low power consumption

- The current consumption is 15mA when the transmit power is 0dBm in the transmit mode
- The current consumption is 14mA when operating in receive mode
- The current consumption is 2uA when operating in Sleep mode

Low cost

- Low cost system solution
- Less than 15 external components
- With double-layer PCB, you can use printed circuit board antenna
- Provides complete MCU solutions for customers

High performance

- Operating frequency 2400MHz ~ 2483MHz
- Maximum data rate of 2Mbps
- The maximum output power is 11dBm
- Sensitivity up to -88dBm

2. Pin definition

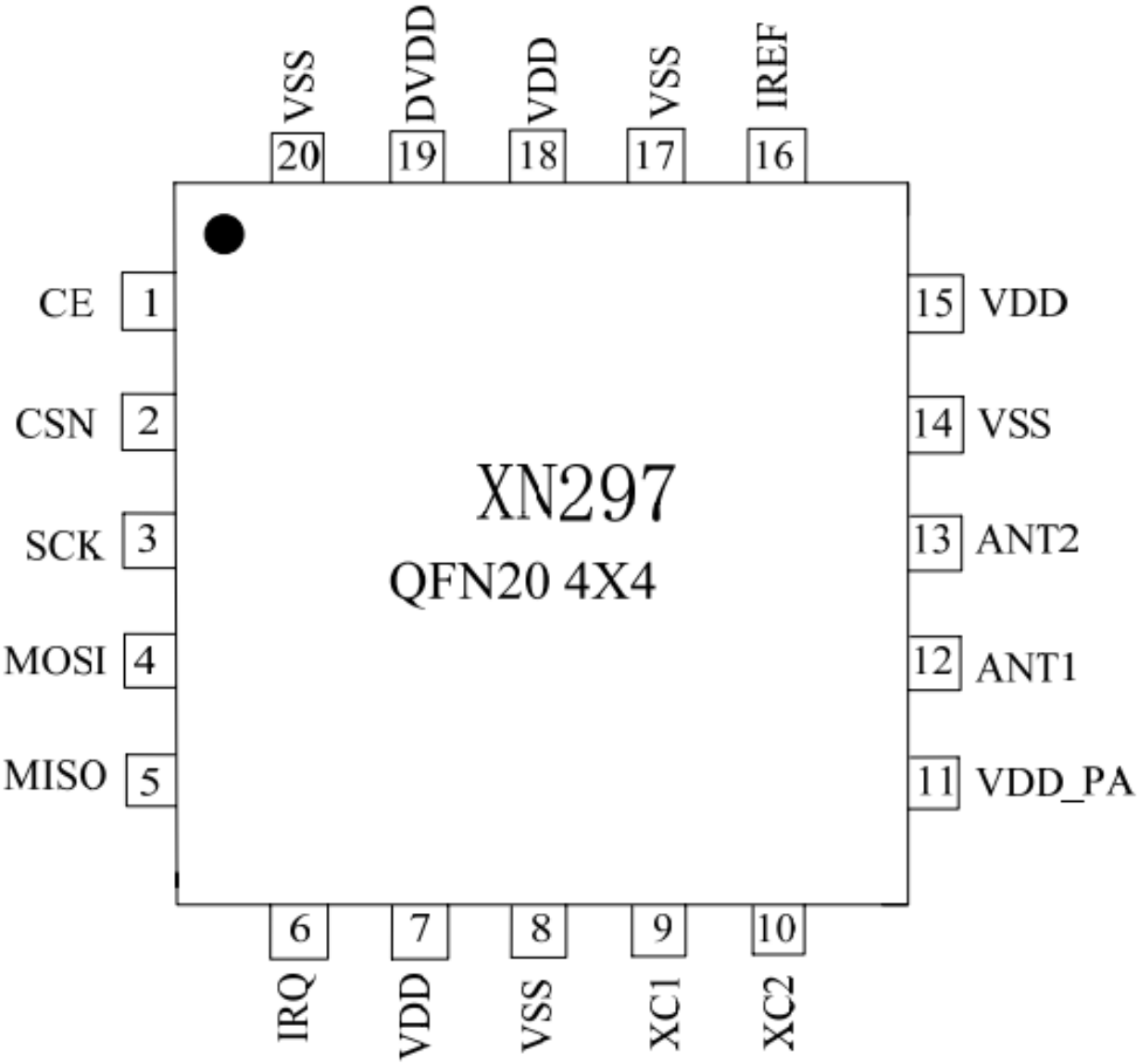

Figure 1 - Pin definition

PIN Number	Name	Description	PIN Number	Name	Description
1	CE	Mode chip select signal	11	VDD_PA	Power output
2	CSN	SPI chip select signal	12	ANT1	Antenna port 1
3	SCK	SPI clock signal	13	ANT2	Antenna port 2
4	MOSI	SPI data input signal	14	VSS	Ground (GND)
5	MISO	SPI data output signal	15	VDD	Power input
6	IRQ	Interrupt signal	16	IREF	Reference current
7	VDD	Power input	17	VSS	Ground (GND)
8	VSS	Ground (GND)	18	VDD	Power input
9	XC1	Crystal input	19	DVDD	Power output
10	XC2	Crystal output	20	VSS	Ground (GND)

Table 1 - PIN definition

3. Chip control description

This chapter describes the various operating modes of the XN297, as well as the parameter usage definitions used to control the XN297 operating mode. XN297 internal state machine is used to control the chip operating mode, the state machine controlled by the value of the register configuration and internal signals.

3.1 Operating modes

The XN297 has five operating modes, which are described in this section.

3.1.1 State diagram

Figure 2 is a XN297 state diagram showing transitions five operating modes, as well as five operating modes. The XN297 begins to operate at VDD> 2.0V. Even entering the sleep mode, MCU can still control the chip through the SPI and CE pins into the other four states.

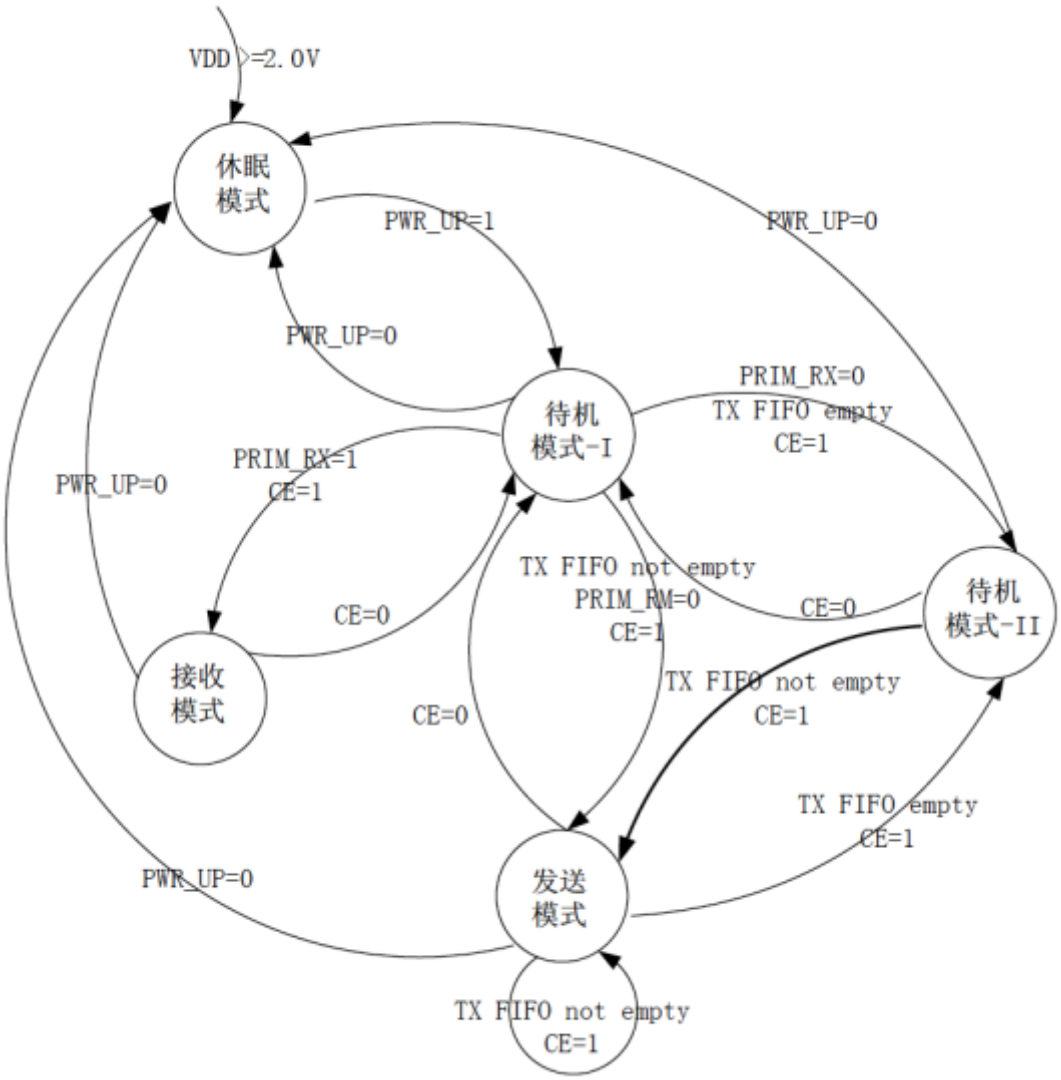

Figure 2 - State diagram

Table 2 shows the XN297 five main modes corresponding to the control register parameter level and the FIFO register state

Mode	PWR_UP	PRIM_RX	CE	FIFO register status
Receive Mode	1	1	1	-
Transmission Mode	1	0	1	The data is in the TX FIFO register
Standby Mode I	1	-	0	No data transfer
Standby Mode II	1	0	1	TX FIFO is empty
Sleep mode	0	-	-	-

Table 2 - XN297 5 operating modes corresponding to the control parameter configuration and FIFO register status

3.1.2 Sleep Mode

In Sleep mode, all functions of the XN297 are turned off, keeping current consumption to a minimum. After entering Sleep mode, the XN297 stops operating, but the register contents remain unchanged. Sleep mode is controlled by the PWR_UP bit in the register.

3.1.3 Standby Mode-I

In the standby mode-I, the chip to maintain crystal work while the rest of the functional modules are closed, and can be restarted in a relatively short period. Standby Mode -I consumes less average current. In Sleep mode, the chip enters standby mode -I by setting the PWR_UP value of the configuration register high. While in the transmit or receive mode, if the CE is set to low chip will return to standby mode-I.

3.1.4 Standby Mode-II

Standby Mode II is entered when the TX FIFO register is empty and CE is high (standby mode-II is usually understood as a ready-to-transmit mode). At this point, the crystal buffer and power management module is turned on. During the standby mode-II, the register configuration remains unchanged. If a packet is sent to the TX FIFO, the PLL immediately starts its operation and waits for its frequency to lock, and the transmitter transmits the packet.

3.1.5 Receive Mode

Receive mode is XN297 communication part of the receiver is in working condition, when the PWR_UP, PRIM-RX, CE is set to high when the receive mode.
In the RX mode, the RF section receives the signal from the antenna and amplifies and down converts it. The demodulator converts the analog modulation signal into digital information, and determines whether the message is valid per the protocol (by matching the address), the complete valid message Will be uploaded. The valid information

carried by this packet is placed in the empty position of the RX FIFO. If the RX FIFO is full, the received packet will be lost.

3.1.6 Transmit Mode

Transmit mode is XN297 send data packets when the transmitter is in working condition, when the PWR_UP and CE is high, PRIM-RX is low, there is valid data in the transmit FIFO.

XN297 will remain in transmit mode until the packet is sent. If CE = 0, XN297 returns to standby mode -I. If CE = 1, the transmit FIFO will determine the next active state. If the XN297 TX FIFO in transmit mode is not empty, then it will send the next packet. If the TX FIFO is empty, the XN297 will enter Standby mode-II. When operating in transmit data mode, the XN297 transmit part of the PLL operates in the open-loop state.

3.2 Different modes and PIN states

The XN297 different modes of I/O and their corresponding pin states are shown in Table 3.

Pin Name	Direction	Transmission mode	Receive mode	Standby mode	Sleep mode
CE	Input	High level	High level	Low level	-
CSN	Input	SPI chip select enable, low enable			
SCK	Input	SPI clock			
MOSI	Input	SPI serial input			
MISO	Three-state output	SPI serial output			
IRQ	Output	Interrupt, low enable			

Table 3 - PIN States in different modes

3.3 Packet handling

XN297 has the following data packet processing methods.

3.3.1 General purpose communication mode

General-purpose communication mode, XN297 can be connected with the general low-speed MCU to complete the communication. High-speed signal processing is done by the chip's internal protocol. XN297 provides SPI interface, the data rate depends on the MCU interface speed. XN297 and MCU low-speed communication, and high-speed signal processing part of the chip, reducing the overall program of current consumption. Therefore, the average current consumption in the general-purpose communication mode is reduced.

In the general-purpose communication reception mode, the IRQ notifies the MCU when a valid address and data are received, and then the MCU can read the received data from the RX FIFO register.

The XN297 automatically generates the preamble in the general purpose communication mode. After the data is sent, the IRQ notifies the MCU, which reduces the MCU's coordination and reduces the software development cycle. The XN297 has two different RX FIFO registers (six channels share this register) and two different TX FIFO registers. In Sleep mode, the MCU can access the FIFO registers at any time during standby and during data transfer. Allows the SPI interface to transfer data at low speed, and can use the MCU's general-purpose I / O port as the SPI interface.

3.3.2 Enhanced communication mode

The enhanced communication mode makes it easier and more efficient to implement the bidirectional link protocol. A typical two-way link is: the sender requires the terminal device to receive data in response to the signal, so that the sender to detect the existence of data loss. Once the data is lost, through the retransmission function will be lost data recovery. Enhanced communication mode can control the response and retransmission functions without increasing the MCU workload.

XN297 in receive mode can receive 6 different channels of data, as shown in Figure 4. Each data channel uses a different address, but shares the same channel. That is, six different XN297 can be set to send mode with the same set to receive mode XN297 to communicate, and set to receive mode XN297 can identify these six senders. Data channel 0 is the only data channel that can be configured as a 40-bit self-address. 1 to 5 data channels are 8-bit self-address and 32-bit public address. All data channels can be configured for enhanced communication mode.

The XN297 records the address of the sender after confirming that the data has been received, and sends an acknowledge signal with the address as the destination address. On the transmit side, data channel 0 is used as the receive acknowledge signal, so the receive address of data channel 0 is equal to the sender address to ensure that the correct acknowledge signal is received. Figure 5 shows an example of how PTX and PRX addresses are configured.

When the XN297 is configured for enhanced communication mode, the XN297 initiates the enhanced mode to send data as long as the MCU has data to transmit. After sending the data, the XN297 transitions to the receive mode and waits for the acknowledge signal from the terminal. If the correct answer is not received within the specified time, the XN297 will retransmit the same packet until it receives an acknowledge signal or the number of transfers exceeds the value set in the SETUP_RETR_ARC register. If the number of transmissions exceeds the set value, MAX_RT interrupt.

As soon as the acknowledgment is received, XN297 asserts that the last packet of data has been successfully transmitted (the receiver has received the data), clears the data in the TX FIFO and generates a TX_DS interrupt (IRQ pin high). In the enhanced communication mode, XN297 has the following characteristics:

- Low power consumption, fast start automatically air transmission, greatly reducing the current consumption.

- With few external controls, the XN297 integrates all high-speed link-layer operations, such as retransmitting lost packets and generating auto-answer signals. SPI interface can use the MCU general-purpose I / O port for communication.

- Fast transmission, air transmission time is short, greatly reducing the wireless transmission of the signal collision phenomenon.

- Development cycle is short, the chip link layer completely internal integration, very easy to hardware and software development.

3.3.3 Enhanced transmission mode

1. The configuration register bit PRIM_RX is low
2. When the MCU has data to send, the receive node address (TX_ADDR) and valid data (TX_PLD) are written to the XN297 through the SPI interface. The length of the transmit data is written to the TX FIFO from the MCU in byte counts. When CSN is low, data is continuously written. After the transmitter sends data, it sets the channel 0 to the receive mode to receive the acknowledge. The receive address (RX_ADDR_P0) is the same as the receiver address (TX_ADDR). For example, in Figure 5, the transmitter (PTX5) and the receiver (RX) of data channel 5 are set as follows:

   TX5: TX_ADDR = 0XC2C3C4C5C1
   TX5: RX_ADDR_P0 = 0xC2C3C4C5C1
   RX: RX_ADDR_P5 = 0XC2C3C4C5C

3. Set CE high to start the transmission
4. Enhanced communication mode Features:
   - Automatic switching mode;
   - Start the internal 16MHz clock;
   - Automatic data package and send;
   - High transmission data rate (set by the MCU to 1Mbps or 2Mbps)
5. If auto-answer mode is enabled (auto-transfer counter does not equal 0, ENAA_P0 = 1), XN297 immediately goes into receive mode. If the acknowledge signal is received within the valid response time range, the data is considered to have been successfully transmitted to the receiver. The TX_DS bit in the status register is set high and the data is cleared from the TX FIFO. If an acknowledge signal is not received within the set time range, the data is retransmitted. If the automatic transfer counter (ARC_CNT) overflows (exceeding the programmed value), the MAX_RT bit in the status register is set high and the data in the TX FIFO is not cleared. The IRQ pin generates an interrupt when MAX_RT or TX_DS is high. The IRQ interrupt is reset by writing to the status register. If the number of transmissions has not yet received an Acknowledge when the maximum number of transmissions is reached, the packet will not be retransmitted until the MAX_RX interrupt is cleared. The packet loss counter (PLOS_CNT) is incremented by one each time the MAX_RT interrupt is generated. That is, the retransmission counter ARC_CNT calculates the number of retransmitted packets, and PLOS_CNT calculates the number of packets that have not yet been successfully transmitted when the maximum permissible number of transmissions is reached.
6. If the CE is low, the system enters the standby mode-I. If CE is not set low, the system sends the next packet of data in the TX FIFO register. If the TX FIFO register is empty and CE is high, the system enters Standby Mode II.

7. If the system is in Standby Mode II, the system goes into Standby Mode-I immediately after CE is set low.

3.3.4 Enhanced communication reception mode

1. The enhanced communication reception mode is selected by setting the PRIM_RX bit in the register high. The channel ready to receive data must be enabled (EN_RXADDR register), and the auto-acknowledge function for all data channels operating in enhanced communication mode is enabled by the EN_AA register, the effective data width being set by the RX_PW_PX register
2. The receive mode is set by CE to high start
3. After the preset wait time, the XN297 begins to detect the radio signal
4. After a valid packet is received (address match), the data is stored in RX_FIFO with the RX_DR bit high and an interrupt is generated. The RX_P_NO bit in the status register indicates which channel the data is received from
5. If the auto acknowledge signal is enabled, an acknowledge signal is sent
6. MCU sets CE pin low, enter standby mode -I
7. The MCU reads the data through the SPI port at the appropriate rate
8. The chip is ready to enter transmit mode, receive mode, or sleep mode

3.3.5 two-way data communication

If data is required for bidirectional communication, the PRIM_RX register must be changed as the chip operates. The processor must ensure synchronization of PTX and PRX. Data may be stored in the RX_FIFO and TX_FIFO registers at the same time.

1 Auto answer (RX):
Auto-answer feature can be through the SPI port on the different data channels are configured. When a valid packet is received, the system enters transmit mode and sends an acknowledgment. After sending the acknowledgment signal, the system enters the normal working mode (working mode is decided by PRIM_RX bit and CE pin).

2 Automatic transmission function (ART), (TX):
The automatic transmission function is for the sender of the automatic answering system. SETUP_RETR register setting: The length of time to start retransmission of data.
At the end of each transmission, the system enters the receive mode and waits for a response within the set time range. After receiving the response signal, the system goes into the normal send mode. If there is no data to be transmitted in the TX FIFO and the CE pin is low, the system goes into standby mode. If no acknowledge signal is received, the system returns to transmit mode and retransmits data until an acknowledgment signal is received or the retransmission count exceeds the set value (maximum retransmission times) New data is sent or the PRIM_RX register is configured to lose packets and counter is reset

3.3.6 Packet Identification in Enhanced Communication Mode

Each packet data includes a two-bit PID (packet identification) to identify whether the received data is a new packet or a retransmitted packet. PID identification can prevent the same data packets sent into the MCU multiple times. Each time the sender gets a packet of new data from the MCU, the PID value is incremented by one. The PID application determines whether the received data is a retransmitted data packet or a new data packet on the receiving side. If some of the data in the link is lost, the PID value is the same as the PID value of the previous packet.

1. Receiver:
   The receiving party compares the PID value of the newly received packet with the previous packet. If the PID values are different, the received packet is considered as a new packet. If the PID value is the same as the previous packet, the newly received packet may be the same as the previous packet.
2. Sender:
   The sender's PID value is incremented by one each time a new packet is sent

3.4 Data Channels

When XN297 is configured in receive mode, it can receive data on 6 different channels at the same frequency. Each data channel has its own address and can be individually configured via registers

The data channel is set by register EN_RXADDR. By default, only data channel 0 and data channel 1 are on.
The address of each data channel is configured via the register RX_ADDR_PX. Normally, different data channels are not allowed to set the exact same address. Table 5 shows an example of each channel address configuration

	BYTE 4	BYTE 3	BYTE 2	BYTE 1	BYTE 0
Data Pipe 0 (RX_ADDR_P0)	0xF1	0xD2	0xE6	0xA2	0x33
	↓	↓	↓	↓	↓
Data Pipe 1 (RX_ADDR_P1)	0xD3	0xD3	0xD3	0xD3	0xD3
	↓	↓	↓	↓	↓
Data Pipe 2 (RX_ADDR_P2)	0xD3	0xD3	0xD3	0xD3	0xD4
	↓	↓	↓	↓	↓
Data Pipe 3 (RX_ADDR_P3)	0xD3	0xD3	0xD3	0xD3	0xD5
	↓	↓	↓	↓	↓
Data Pipe 4 (RX_ADDR_P4)	0xD3	0xD3	0xD3	0xD3	0xD6

	↓	↓	↓	↓	↓
Data Pipe 5 (RX_ADDR_P5)	0xD3	0xD3	0xD3	0xD3	0xD7

Table 4 - Multi-Channel Address Settings

It can be seen from Table 4 that a total of 40 bits of data are available for data channel (0 to 5 byte). Addresses of data channels 1 to 5 are configured as 32-bit shared addresses + respective addresses (least significant bytes).
The address of channel 0 ~ 5 of the above table is set. When receiving data from a data channel, and this data channel is set to answer mode, the XN297 generates an acknowledge signal after receiving the data, the destination address of which is the receiving channel address.

4. Data and control interfaces

All configuration of XN297 are stored in the register, and the register can be read/write through SPI.

4.1 SPI Interface

SPI interface is a standard SPI interface, the maximum data transfer rate of 8Mbps. Most registers have read and write functions

4.2 SPI Instruction set

The instructions used by the SPI interface are described in 4.3. When CSN is low, XN297 waits for instructions to be executed. The execution of each instruction must go through a high to low CSN change.

4.3 SPI Instruction Format

<Command word: from high to low (per byte)>
<Data Byte: Low Byte to High Byte, High Byte for Each Byte>

Command name	Command word (binary)	Data byte	Operation
R_REGISTER	000A AAAA	1 to 5 first low bits	Read command and status registers AAAAA = 5bit register address
W_REGISTER	001A AAAA	1 to 5 first low bits	Write Command Register and Status Register AAAAA = 5bit Register Address Write only in power_down and standby mode Executable
R_RX_PAYLOAD	0110 0001	1 to 64 first low bits	Read the receive data, the read operation usually starts from the 0th byte. The data will be deleted from the FIFO after reading. Receive mode is available
W_TX_PAYLOAD	1010 0000	1 to 64 first low bits	Write transmit data, the write operation is usually started by 0 bytes. Emission mode
FLUSH_TX	1110 0001	0	Clear Tx_FIFO, Tx mode is available
FLUSH_RX	1110 0010	0	Cleared in Rx_FIFO, Rx mode is available. It can not be executed when the response is returned. Otherwise, the response data will be incomplete
REUSE_TX_PL	1110 0011	0	Used in the PTX mode chip to reuse the last transmitted data. When CE is high, the data will be used repeatedly. The reuse Tx data is available after the W_REGISTER, FLUSH_TX command is executed. This command can not be executed during data transfer
ACTIVATE	0101 0000	1	Using the command followed by data 0x73 activates the following functions • R_RX_PL_WID • W_ACK_PAYLOAD • W_TX_PAYLOAD_NOACK Using this command again with the same data will turn off the above functions. This command is only executable in power_down and standby mode.
R_RX_PL_WID	0110 0000		Read Rx_FIFO The topmost RX-payload data width

W_ACK_PAYLOAD	1010 1PPP	1 to 64 first low bits	Rx mode is available Write PIPE PPP (PPP value from 000 to 101) in response to ACK while the data is returned. Up to 3 ACK packets can be set. The data with the PIPE will be sent on a first-in-first-out basis. The write operation is normally started from 0 bytes.
W_TX_PAYLOAD_NOACK	1011 0000	1 to 64 first low bits	Tx mode Using this command to send data will make AUTOACK unavailable
NOP	1111 1111	0	No operation. Can be used to read the status register

Table 5 - SPI Instruction Format

The R_REGISTER and W_REGISTER registers may operate on single-byte or multi-byte registers. When accessing the multi-byte register, the first byte to be read / written is the most significant bit of the least significant byte. The write SPI operation can be ended before all multi-byte registers are written, in which case the unwritten high byte remains unchanged. For example, the lowest byte of the RX_ADDR_P0 register can be changed by writing a byte to the register RX_ADDR_P0. After the CSN state changes from high to low, the contents of the status register can be read by MISO.

4.4 Interrupts

The interrupt pin (IRQ) of the XN297 is a low-level trigger that is triggered when TX_DS, RX_DR, or MAX_RT are high in the status register. When the MCU writes a '1' to the interrupt source, the interrupt pin is disabled. Maskable interrupts can be masked by IRQ interrupts. By setting the maskable interrupt bit high, the interrupt response is disabled. By default, all interrupt sources are disabled.

4.5 SPI timing

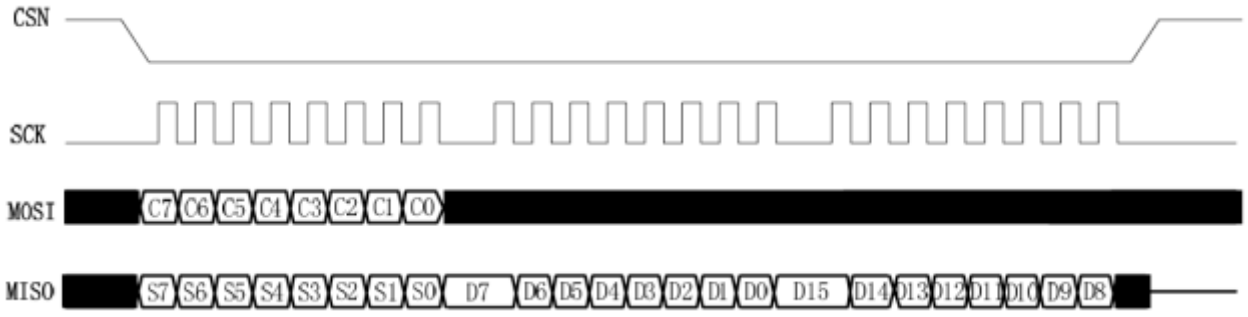

Figure 3 - SPI read operation

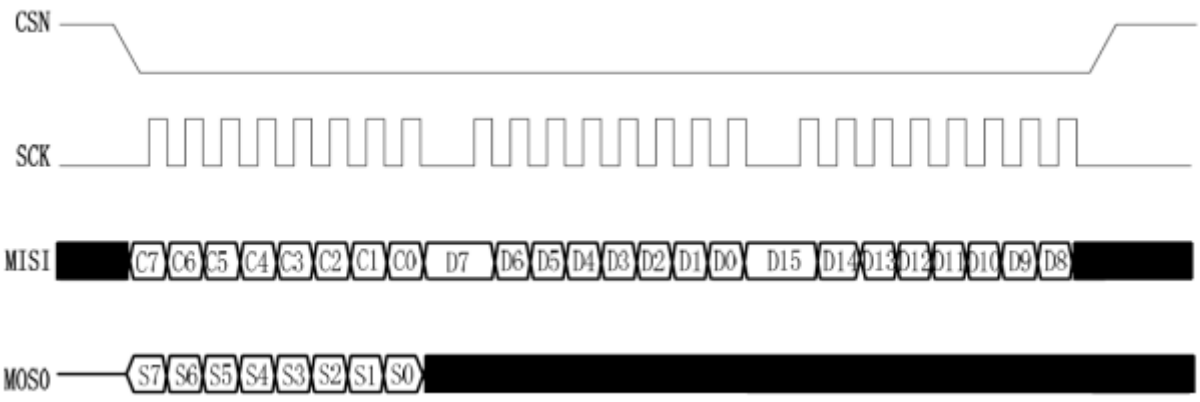

Figure 4 - SPI write operation

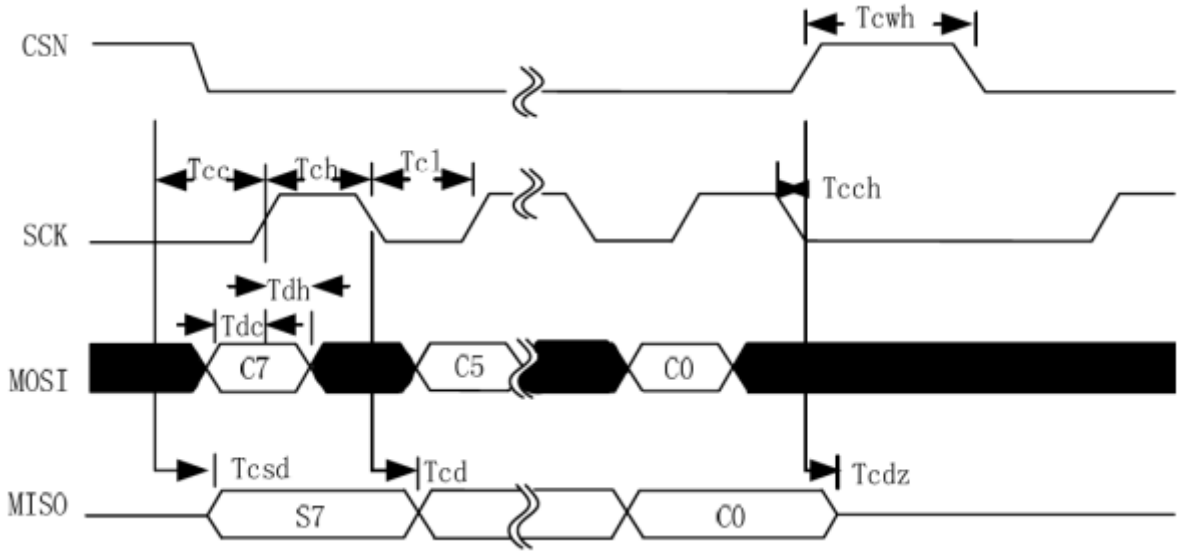

Figure 5 - SPI, NOP operation timing diagram

SYMBOL	PARAMETERS	MIN	MAX	UNITS
Tdc	Data Settling Time	15		ns
Tdh	Data hold time	2		ns
Tcsd	CSN signal valid time		40	ns
Tcd	SCK signal valid time		51	ns
Tcl	SCK signal low time	38		ns
Tch	SCK signal high time	38		ns
Fsck	SCK Signal frequency	0	8	MHz
Tr, Tf	SCK signal rise and fall time		110	ns
Tcc	CSN signal setup time	2		ns
Tcch	CSN signal hold time	2		ns
Tcwh	CSN Invalid Time	49		ns

Tcdz	CSN signal high impedance		40	ns

Table 6 - SPI reference time

Note: The parameters in Table 6 can be adjusted per the selected MCU
Figure Figure 3Figure 4Figure 5 and Table 6 show SPI operation and timing. Be sure to enter Standby or Sleep mode before writing to the register.
The following symbols are used in the diagram:

- C_i-SPI instruction bit
- S_i - Status Register bits
- D_i - Data bit (Remark: low byte to high byte, high byte in each byte)

Note: i = 1,2,3 ... n.

4.6 Control register

The XN297 can be configured and controlled by SPI using the registers defined in Table 7. In this table, unused registers are not defined and set to "0".

Address (HEX)	Memory	BIT	Default value (19 / 1E / 1F register is the recommended value)	Read and write	Description
00	**CONFIG**				**Working register**
	DATAOUT_SEL	7	0	R/W	Data Read Select bit 1: Causes bit7: 1 of address 0X09 to output bit 6: 0 of Analog_data 0: The output of bit 7: 0 of address 0X09 is the 4-bit RSSI data given by the receiver in real time + the receiver 4-bit RSSI data in packet synchronization
	MASK_RX_DR	6	0	R/W	The interrupt enable bit for the receive data is successful 1: The interrupt is not reflected to the IRQ pin 0: The RX_DR interrupt is reflected to the IRQ pin
	MASK_TX_DS	5	0	R/W	Transmit Data Successful interrupt escalation enable bit 1: The interrupt is not reflected to the IRQ pin 0: TX_DS interrupt is reflected to the IRQ pin
	MASK_MAX_RT	4	0	R/W	The interrupt enable bit for the maximum number of transfers is reached

					1: The interrupt is not reflected to the IRQ pin 0: The MAX_RT interrupt is reflected to the IRQ pin
	EN_CRC	3	1	R/W	CRC enable bit 1: CRC enable, 2byte 0: CRC is disabled, and CRC check is not performed
	N/A	2	0	R/W	Reserved
	PWR_UP	1	0	R/W	Chip enable bit 1: POWER_UP 0: POWER_DOWN
	PRIM_RX	0	0	R/W	RX / TX control 1: PRX 0: PTX
01	**EN_AA Enhanced Burst**				**Auto Answer Enable**
	Reserved	7:6	00	R/W	Only 00 allowed
	ENAA_P5	5	0	R/W	Enable the pipe5 auto-answer
	ENAA_P4	4	0	R/W	Enable the pipe 4 auto-answer
	ENAA_P3	3	0	R/W	Enable the pipe 3 auto-answer
	ENAA_P2	2	0	R/W	Enable the pipe 2 auto-answer
	ENAA_P1	1	0	R/W	Enable the pipe 1 auto-answer
	ENAA_P0	0	0	R/W	Enable the pipe 0 auto-answer
02	**EN_RXADDR**				**RX address is enabled**
	Reserved	7:2	00	R/W	Only 000000 allowed
	AW	1:0	11	R/W	RX / TX address width 00: Invalid 01: 3 bytes 10: 4 bytes 11: 5 bytes If the address width is set to less than 5 bytes, the receive address will use the low byte
03	**SETUP_AW**				**Automatic retransmission settings**
	Reserved	7:2	000000	R/W	Only 000000 allowed
	AW	1:0	11	R/W	RX / TX address width 00: Invalid 01: 3 bytes 10: 4 bytes 11: 5 bytes If the address width is set to less than 5 bytes, the

					receive address will use the low byte
04	**SETUP_RETR**				**Automatic retransmission settings**
	ARD	7:4	0000	R/W	Automatic retransmission delay 0000 :250μs 0001 :500μs 0010 :750μs …… 1111: 4000μs
	ARC	3:0	0011	R/W	The number of retransmissions is set automatically 0000: Normal communication mode 0001: Enhanced mode 1 transmission ... 1111: Enhanced mode 15 transmissions
05	**RF_CH**				**Communication channel settings**
	Reserved	7	0	R/W	Only 0 allowed
	RF_CH	6:0	0000010	R/W	Set the usage channel to Channel = RF_CH + 2400
06	**RF_SETUP**				**Communication channel configuration**
	RSSI_EN	7	0	R/W	RSSI enable bit 1: RSSI enabled 0: RSSI is disabled
	Reserved	6	0	R/W	Only 0 allowed
	RSSI_SEL	5	0	R/W	RSSI data selection method 1: sampled signal data through the filter 0: The sampled signal data does not pass through the filter
	Reserved	4	0	R/W	Only 0 allowed
	RF_DR	3	1	R/W	Data rate 0: 1 Mbps 1: 2 Mbps
	RF_PWR	2:1	11 (Recommended value 10)	R/W	Set the RF output power 00: -10 dBm 01: 0 dBm 10: 8 dBm 11: The maximum output power of 10dBm
	LNA_HCURR	0	1	R/W	Set LNA high current enable 1: High current 0: Low current
07	**STATUS**				**Status register**

	Reserved	7	0	R/W	Only 0 reserved
	RX_DR	6	0	R/W	The RX FIFO receives a data interrupt and generates an interrupt when new data is received into the RX FIFO. Write 1 clear interrupt
	TX_DS	5	0	R/W	TX FIFO send data interrupt, after the completion of data transmission interrupt. When AUTO_ACK is enabled, this bit is set high only after the ACK signal is received. Write 1 clear interrupt
	MAX_RT	4	0	R/W	An interrupt is generated when the maximum number of transfers is reached. Write 1 clear interrupt If this interrupt is generated, communication must be resumed after the interrupt is cleared
	RX_P_NO	3:1	111	R	The pipe number that can be read from RX_FIFO 000-101: pipe number 110: Not Used 111: RX_FIFO is empty
	TX_FULL	0	0	R	TX FIFO full flag 1: TX FIFO is full 0: TX FIFO is not full
08	**OBSERVE_TX**				**Transmission status register**
	PLOS_CNT	7:4	0000	R	Packet loss counter When the counter reaches the maximum value of 15, it stops counting until reset, and communication continues without resetting the value. The counter is reset when writing RF_CH

	ARC_CNT	3:0	0000	R	The number of retransmission times counter for enhanced communications. Used in conjunction with ARC registers. Each time the retransmission limit value is reached, the packet loss is considered and PLOS_CNT is incremented. The counter is reset when new data is written to the TX FIFO. Number of retransmissions = number of transmissions - 1
09	**DATAOUT**	**7:0**	**00000000**	**R**	**Data read register When DATAOUT_SEL is 1, The output of bit7: 1 is the Analog_data register Bit6: 0 When DATAOUT_SEL is 0, The output of bit 7: 0 is the 4-bit RSSI data real-time given by the receiver + the receiver 4-bit RSSI data for packet synchronization Used in conjunction with the DATAOUT_SEL bit**
0A	RX_ADDR_P0	39:0	0xE7E7E7E7E7	R/W	Data pipe 0 address, up to 5 bytes. (Written by low word Start address length defined by SETUP_AW)
0B	RX_ADDR_P1	39:0	0xC2C2C2C2C2	R/W	Data pipe 1 address, up to 5 bytes. (Written by low word Start address length defined by SETUP_AW)
0C	RX_ADDR_P2	7:0	0xC3	R/W	Data pipe 2 receive address, only the least significant bit, high bit equal to RX_ADDR_P1 [39: 8]
0D	RX_ADDR_P3	7:0	0xC4	R/W	Data pipe 3 receive address, only the least significant bit, the high bit is equal to RX_ADDR_P1 [39: 8]
0E	RX_ADDR_P4	7:0	0xC5	R/W	Data pipe 4 receive address, only the least significant bit, the high bit is equal to RX_ADDR_P1 [39: 8]

0F	RX_ADDR_P5	7:0	0xC6	R/W	Data pipe 5 receive address, only the least significant bit, the high bit is equal to RX_ADDR_P1 [39: 8]
10	TX_ADDR	39:0	0xE7E7E7E7E7	R/W	The sender address. (Written by low word) can only be used in a chip configured for PTX mode, it is necessary to set RX_ADDR_P0 equal to this address to receive automatic answer in enhanced communication mode.
11	**RX_PW_P0**				**Data length of RX payload in data pipe 0**
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P0	6:0	0000000	R/W	Data length of RX payload in data pipe 0 (1 to 64 bytes) 0: The pipe is not used 1 = 1 byte ... 64 = 64 bytes
12	**RX_PW_P1**				**Data length of RX payload in data pipe 1**
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P1	6:0	0000000	R/W	Data length of RX payload in data pipe 1 (1 to 64 bytes) 0: The pipe is not used 1 = 1 byte ... 64 = 64 bytes
13	**RX_PW_P2**				**Data length of RX payload in data pipe 2**
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P2	6:0	0000000	R/W	Data length of RX payload in data pipe 2 (1 to 64 bytes) 0: The pipe is not used 1 = 1 byte ... 64 = 64 bytes
14	**RX_PW_P3**				**Data length of RX payload in data pipe 3**
	Reserved	7	0	R/W	Only 0 allowed

	RX_PW_P3	6:0	0000000	R/W	Data length of RX payload in data pipe 3 (1 to 64 bytes) 0: The pipe is not used 1 = 1 byte ... 64 = 64 bytes
15	**RX_PW_P4**				**Data length of RX payload in data pipe 4**
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P4	6:0	0000000	R/W	Data length of RX payload in data pipe 4 (1 to 64 bytes) 0: The pipe is not used 1 = 1 byte ... 64 = 64 bytes
16	**RX_PW_P5**				**Data length of RX payload in data pipe 5**
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P5	6:0	0000000	R/W	Data length of RX payload in data pipe 5 (1 to 64 bytes) 0: The pipe is not used 1 = 1 byte ... 64 = 64 bytes
17	**FIFO_STATUS**				**FIFO status register**
	Analog_data	7	0	R/W	Bit9
	TX_REUSE	6	0	R	When high, retransmits the data transmitted from the last frame in the last transmission, and retransmits when the CE pin is high. TX_REUSE is configured by the SPI command REUSE_TX_PL and is reset by the SPI command W_TX_PAYLOAD or FLUSH TX. This bit is 1 in enhanced mode MAX_RT and REUSE_TX_PL is disabled.
	TX_FULL	5	0	R	TX FIFO full flag 1: TX FIFO is full 0: TX FIFO is available
	TX_EMPTY	4	1	R	TX FIFO empty flag bit 1: TX FIFO empty 0: TX FIFO has data
	Analog_data	3:2	00	R/W	Bit8:7

	RX_FULL	1	0	R	RX FIFO full flag 1: RX FIFO is full 0: RX FIFO is available
	RX_EMPTY	0	1	R	RX FIFO empty flag bit 1: RX FIFO empty. 0: RX FIFO has data
N/A	ACK_PLD	255:0	X	W	By SPI write, the corresponding data pipe ACK number written by the SPI command. Valid only in RX mode
N/A	TX_PLD	255:0	X	W	By writing TX data to the SPI, the data is stored in either Level 2, Level 32, or Level 1, 64-byte FIFOs Only used in TX mode
N/A	RX_PLD	255:0	X	R	Read the RX data by SPI command, the data is stored in two 32-byte or 1 64-byte FIFO, all RX PIPE share the same FIFO
19	DEMOD_CAL	39:0	03 A7 00 DF 0B	R/W	Demodulator Parameters (Debug Register)
1C	DYNPD				The dynamic PAYLOAD length is enabled
	Reserved	7:6	0	R/W	Only 00 allowed
	DPL_P5	5	0	R/W	Enable PIPE 5 Dynamic PAYLOAD length (Requires EN_DPL and ENAA_P5)
	DPL_P4	4	0	R/W	Enable PIPE 4 Dynamic PAYLOAD length (Requires EN_DPL and ENAA_P4)
	DPL_P3	3	0	R/W	Enable PIPE 3 Dynamic PAYLOAD length (Requires EN_DPL and ENAA_P3)
	DPL_P2	2	0	R/W	Enable PIPE 2 Dynamic PAYLOAD length (Requires EN_DPL and ENAA_P2)
	DPL_P1	1	0	R/W	Enable PIPE 1 Dynamic PAYLOAD length (Requires EN_DPL and ENAA_P1)
	DPL_P0	0	0	R/W	Enable PIPE 0 Dynamic PAYLOAD length (Requires EN_DPL and ENAA_P0)
1D	FEATURE				Feature register
	Reserved	7:5	000	R/W	Only 000 allowed

	DATA_LEN_SEL	4:3	00	R/W	Data length selection 11: 64byte (512bit) mode 00: 32byte (256bit) mode
	EN_DPL	2	0	R/W	Enable dynamic PAYLOAD length
	EN_ACK_PAY	1	0	R/W	Enable ACK with payload
	EN_DYN_ACK	0	0	R/W	The W_TX_PAYLOAD_NOACK command is enabled
1E	RF_CAL	55:0	0x95 0x2B 0x83 0x61 0xB0 0x9A 0xCA	R/W	RF parameters (debug registers)
1F	BB_CAL	39:0	0x20 0x9C 0x67 0x84 0x7F	R/W	Baseband parameter (debug register)

Table 7 - Control Register

4.6 Packet format description

4.6.1 Enhanced mode

Preamble (3 bytes)	Address (3 to 5 bytes)	Identification (10 bits)	Data (0 to 64 bytes)	CRC check (0/2 bytes)

Table 8 - Packet format in enhanced communication mode

In this table the address bits, the identification bits, and the data bits can be either scrambled or not scrambled. The identification bits consist of 10 bits and the composition format is shown in following table.

Data Length Identifier (7 bits)	PID flag (2 bits)	The NO_ACK flag (1 bit)

Table 9 - Identification bit format for enhanced communication mode

4.6.2 General-purpose mode

Preamble (3 bytes)	Address (3 to 5 bytes)	Data (1 to 64 bytes)	CRC check (0/2 bytes)

Table 10 - Packet format in General-Purpose Mode of communication