Design and Simulation of a 6T SRAM Cell Using Verilog, DSCH2, and Microwind

**Rakesh Suramoni |Kamalvignesh|jaya krishna***B.Tech – Electronics and Communication Engineering*

**Abstract**

In this project, a 6-transistor (6T) Static Random Access Memory (SRAM) cell is designed, modeled, and simulated using Verilog Hardware Description Language (HDL), DSCH2 for schematic design, and Microwind for layout and timing simulation. The project highlights the full workflow of digital memory cell design starting from behavioral coding to post-layout verification. The resulting design is tested and validated with both functional and physical parameters, making it suitable for integration into low-power memory blocks commonly used in embedded systems.

**1. Introduction**

Static Random Access Memory (SRAM) is widely used in digital electronics due to its fast access time and simple cell structure. Each SRAM bitcell typically uses six transistors (4 NMOS, 2 PMOS) to store one bit of data. Compared to dynamic RAM (DRAM), SRAM does not require refreshing, making it ideal for cache memories and register files.  
The purpose of this project is to understand and implement a 6T SRAM cell using industry-recognized design tools and simulation environments. The project serves as a foundational exercise for memory design, layout creation, and signal timing analysis. Through this design, key concepts like memory access, stability, and layout efficiency are studied.

**2. Tools Used**

• Verilog HDL – for behavioral modeling and RTL simulation

• DSCH2 – for logic-level circuit schematic

• Microwind – for CMOS layout, design rule checks (DRC), and transient simulation

• ModelSim/Vivado – for waveform simulation and functional verification

**3. Design Methodology**

**3.1 Verilog Design**

The 6T SRAM cell was first described using Verilog HDL to simulate its behavior during read and write operations. Registers, access transistors, and bit-lines were coded to reflect the working of a single SRAM cell. The testbench was written to simulate storing and retrieving data from the cell.

**3.2 Schematic in DSCH2**

DSCH2 was used to construct the actual circuit diagram of the SRAM using NMOS and PMOS elements. The schematic includes two cross-coupled inverters and two NMOS access transistors connected to a wordline.

**3.3 Layout using Microwind**

The Verilog netlist from DSCH2 was exported to Microwind, where the CMOS layout was automatically generated. The layout was verified for design rules, and a transient simulation was carried out to evaluate timing parameters, signal integrity, and noise margins.

**3.4 Functional and Timing Simulation**

Using both ModelSim and Microwind, the waveforms of SRAM cell operation were verified. Timing delays, access time, and signal stability were examined. Successful read/write operations were observed in simulation outputs.

**4. Output Screenshots**

• Schematic Design (DSCH2): A screenshot showing the 6T cell arrangement

• Layout Design (Microwind): Automatically generated layout based on netlist

• Simulation Waveform: Output graph showing bit-line response over time

**5. Results and Analysis**

The simulation outputs confirmed the correct functioning of the 6T SRAM cell. The read and write cycles were clearly visible in the waveforms. The physical layout also adhered to design constraints and passed all design rule checks. The project validated the theoretical understanding of memory cells with practical simulation, giving insight into real-world VLSI design challenges.

**6. Conclusion**

This project successfully implemented a 6T SRAM cell from RTL description to physical layout. Using Verilog, DSCH2, and Microwind, the complete design and validation cycle of a memory cell was demonstrated. The experience bridges the gap between academic concepts and industry practices, laying a strong foundation for future VLSI design and memory architecture development.

**7. References**

• Rabaey, Jan M. – Digital Integrated Circuits

• DSCH2 and Microwind Official Documentation

• NPTEL VLSI Design Course

• IEEE Journal on Low-Power SRAM Design Techniques