Ivan Oliveras:

1. Lab Assignment Pages

• CDA3201 • Intro to Logic Design • **Lab Assignment** **1**

Name: Ivan Oliveras **Z#:** 23466357 **Grade:** /100

1. [100] To get your lab points you need to get your lab grader by the Teaching Assistnat (TA) and submit under Canvas > Assignment > Lab 1 a **portfolio** consisting of one pdf file that includes:

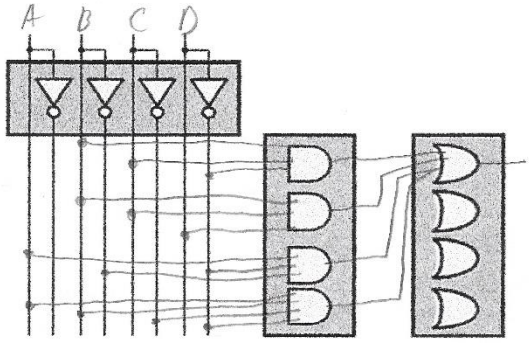
- your handwork in this lab,
- a capture of your schematic done in Quartus – must include comment with your name and Z#
- a capture of your waveform simulation done in Quartus for all 3 circuits resulting from lab 1
- a picture of your breadboard
- a picture of your gradesheet containing the grade and signature of TA

1.1 [10] Given the following Boolean Algebra Equation, complete the Truth Table

$$X = BC\overline{D} + BCD + A\overline{B}\,\overline{D} + AB\overline{C}\,\overline{D}$$

ABCD	BCD'	BCD	AB'D'	ABC'D'	X
0000	0	0	0	0	0
0001	0	0	0	0	0
0010	0	0	0	0	0
0011	0	0	0	0	0
0100	0	0	0	0	0
0101	0	0	0	0	0
0110	1	0	0	0	1
0111	0	1	0	0	1
1000	0	0	1	0	1
1001	0	0	0	0	0
1010	0	0	1	0	1
1011	0	0	0	0	0
1100	0	0	0	1	1
1101	0	0	0	0	0
1110	1	0	0	0	1
1111	0	1	0	0	1

1.2 [10] Utilizing the NOT AND OR gates provided below, label the input that you need to put through NOT, determine how many inputs are needed for each gate and use the number of gates you need (there may be extras). Draw the circuit connections to implement X exactly as specified.



$$X = BC\overline{D} + BCD + A\overline{B}\,\overline{D} + AB\overline{C}\,\overline{D}$$

1.3 [10] Create a project in Altera Quartus called **lab1-PETRIE-yourlastname** following Dr. Petrie's step by step guide and verify the circuit you designed in 1.2 works according to 1.1 Truth Table. If it does not work as specified by the Truth Table, then determine if error is in the Truth Table or your design. Create with same name a Block Diagram/Schematics (.bdf) of your design in 1.3. Is there a 4-input OR gate available? If there is not then figure out how you will change the design using 2 input OR gates. Generate with same name a Waveform file (.vwf), group the inputs and set the counter to step through all the values, Compile, and Simulate. Make sure to save the project, the .bdf and .vwf files often. Check the .vwf to verify it produces same results as the Truth Table 1.1. Keep the project and files to expand the Block Diagram to include the other 2 circuits in the rest of lab 1.

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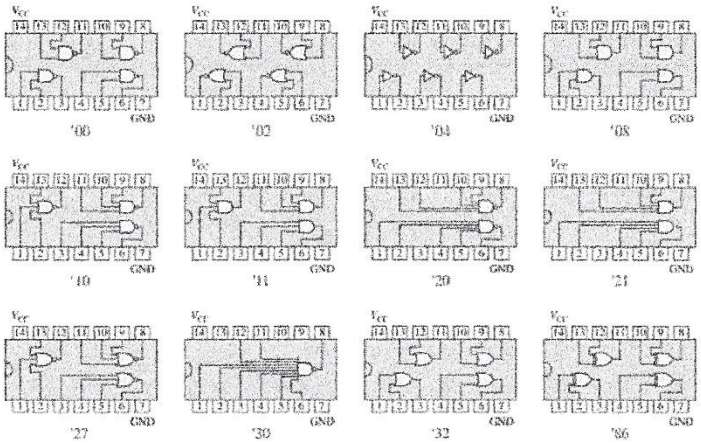
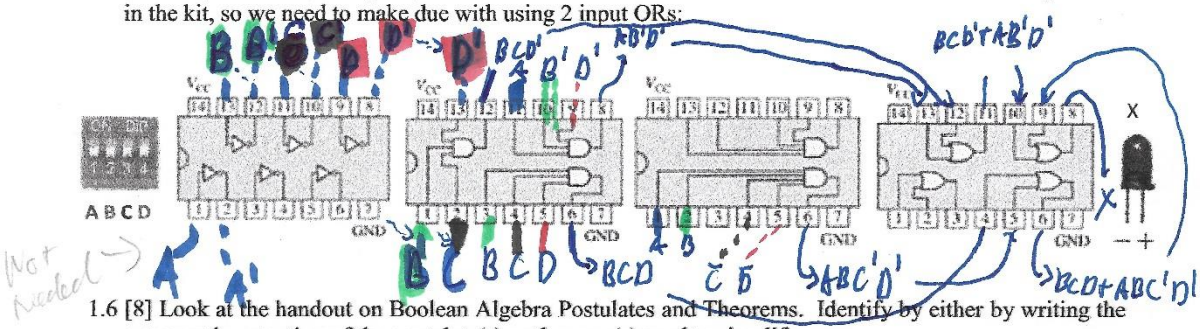
The 7400 Series Family of Integrated Circuits (ICs)

1.4 [5] Gates are packaged in ICs. Determine which and how many ICs from the 7400 Series family at right you will need to implement the circuit as you specified in 1.3 (Note there are no 4 input ORs in your kit so use 2 input OR ICs instead:

Quantity needed?	7400 Series IC #
1	09
1	11
1	21
1	32



1.5 [10] Plan out the layout by labeling inputs and outputs of the gates or drawing the wiring use blue-A, Green-B, Brown-C, Orange-D, use the same color dashed wire for NOT. Note we don't have 4 input ORs in the kit, so we need to make due with using 2 input ORs:



1.6 [8] Look at the handout on Boolean Algebra Postulates and Theorems. Identify by either by writing the name or the equation of the postulate(s) or theorem(s) used to simplify.

$$X = B C \overline{D} + B C D + A \overline{B} \overline{D} + A B \overline{C} \overline{D}$$

Factoring

$$= B C (\overline{D} + D) + (\overline{B} + B \overline{C}) A \overline{D}$$

Additive Complement

Absorption

$$= B C (1) + (\overline{B} + \overline{C}) A \overline{D} = B C + A \overline{B} \overline{D} + A \overline{C} \overline{D}$$

Multiplicative Identity

Or

Distributive

$$= B C + (\overline{B C}) A \overline{D} = B C + A \overline{D}$$

De Morgan's Law

Absorption

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As you verified in 1.a.6, the following Boolean function is algebraically reduced to two different forms denoted as X1 and X2 as follows.

$X = BC\bar{D} + BCD + A\bar{B}\bar{D} + AB\bar{C}\bar{D}$

$= BC(\bar{D}+D) + (\bar{B}+B\bar{C})A\bar{D}$

$= BC + (\bar{B}+\bar{C})A\bar{D} = \underline{\underline{BC + A\bar{B}\bar{D} + A\bar{C}\bar{D} = X1}}$

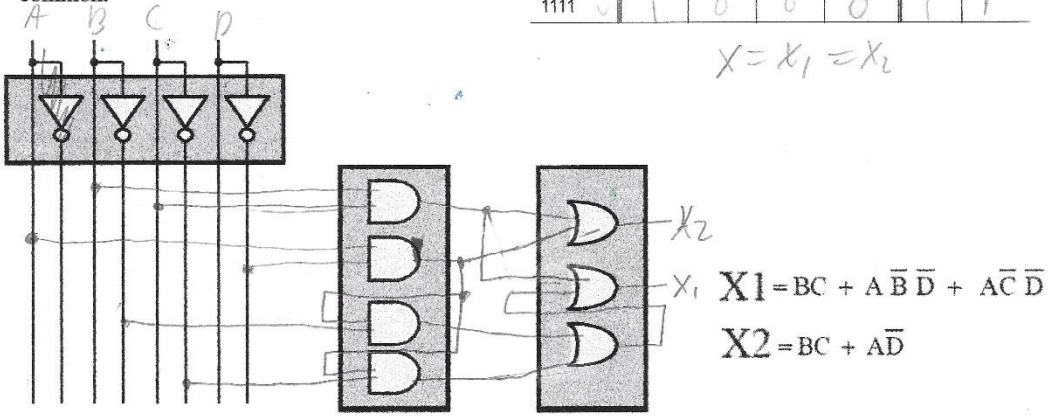
or $= BC + \overline{(BC)}A\bar{D} = \underline{\underline{BC + A\bar{D} = X2}}$

ABCD	BC	$A\bar{B}\bar{D}$	$A\bar{C}\bar{D}$	$A\bar{D}$	X1	X2
0000	0	0	0	0	0	0
0001	0	0	0	0	0	0
0010	0	0	0	0	0	0
0011	0	0	0	0	0	0
0100	0	0	0	0	0	0
0101	0	0	0	0	0	0
0110	1	0	0	0	1	1
0111	1	0	0	0	1	1
1000	0	1	1	1	1	1
1001	0	0	0	0	0	0
1010	0	1	0	1	1	1
1011	0	0	0	0	0	0
1100	0	0	1	1	1	1
1101	0	0	0	0	0	0
1110	1	0	0	1	1	1
1111	1	0	0	0	1	1

$X = X_1 = X_2$

1.7) [5] Verify the equivalence of X1 and X2 using the following truth table:

1.8) [7] Design the circuit for the above two reduced functions, X1 and X2, using exactly 3 NOT gates, 4 2-input AND gates, 3 2-input OR gates. Note, there will not enough gates unless you are able to reuse by finding things both equations have in common.



1.9) [10] Verify the circuit design/behavior by implementing the circuit using Quartus before you actually build the circuit on the breadboard. Open the Quartus project you build in 1.a.3 and add the X1 and X2 circuits to the X circuit Block Diagram / Schematics. Add the X1 and X2 inputs to the Waveform File and Compile and Simulate, check if all X = X1 = X2. You will show the TA you have these files and submit the .bdf and .vwf to the Lab 1 together with the scan of this completed Lab with all your work. Dr. Petrie will adjust your grade – these 2 points will be converted to 20 points total for this section and 1.a.3.

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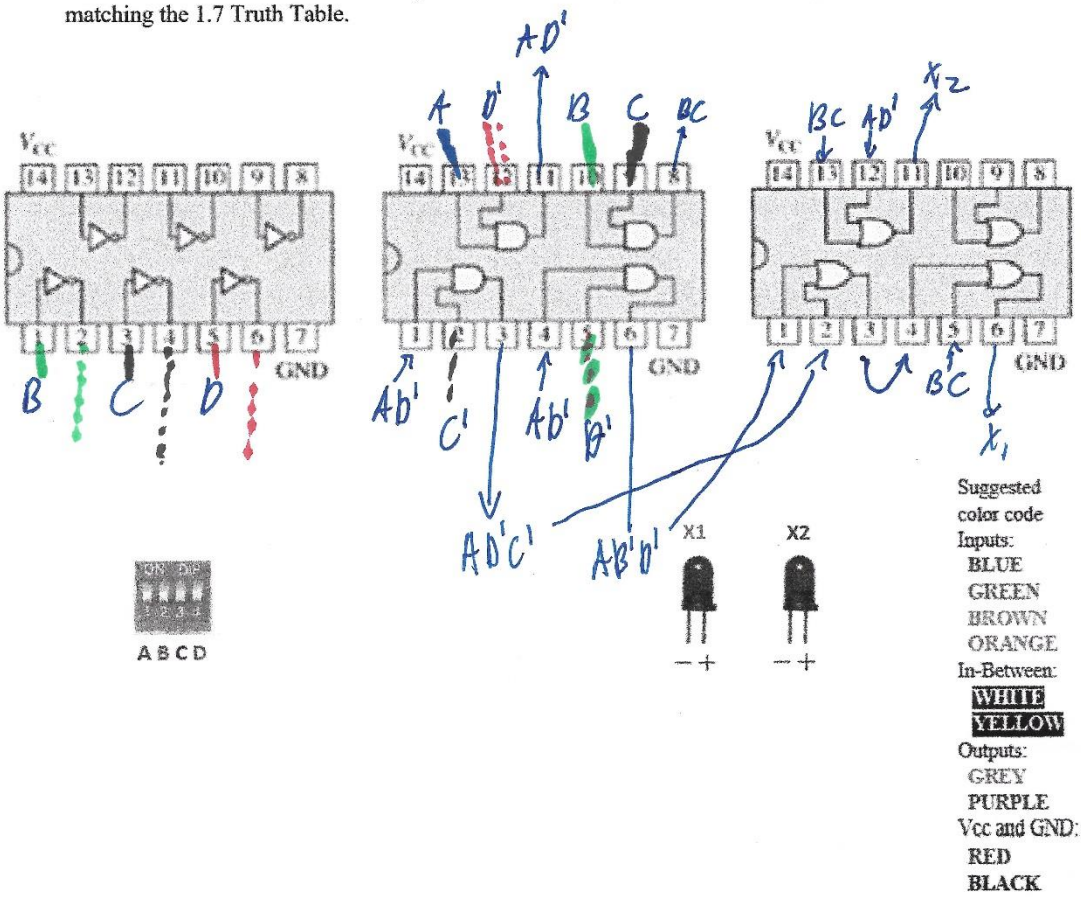
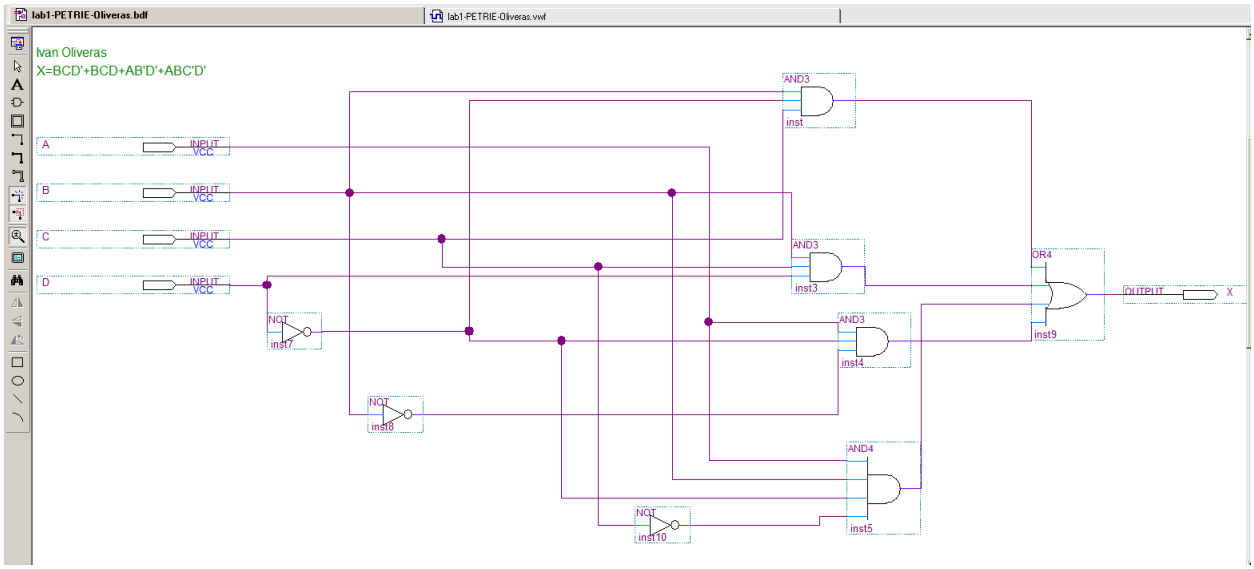
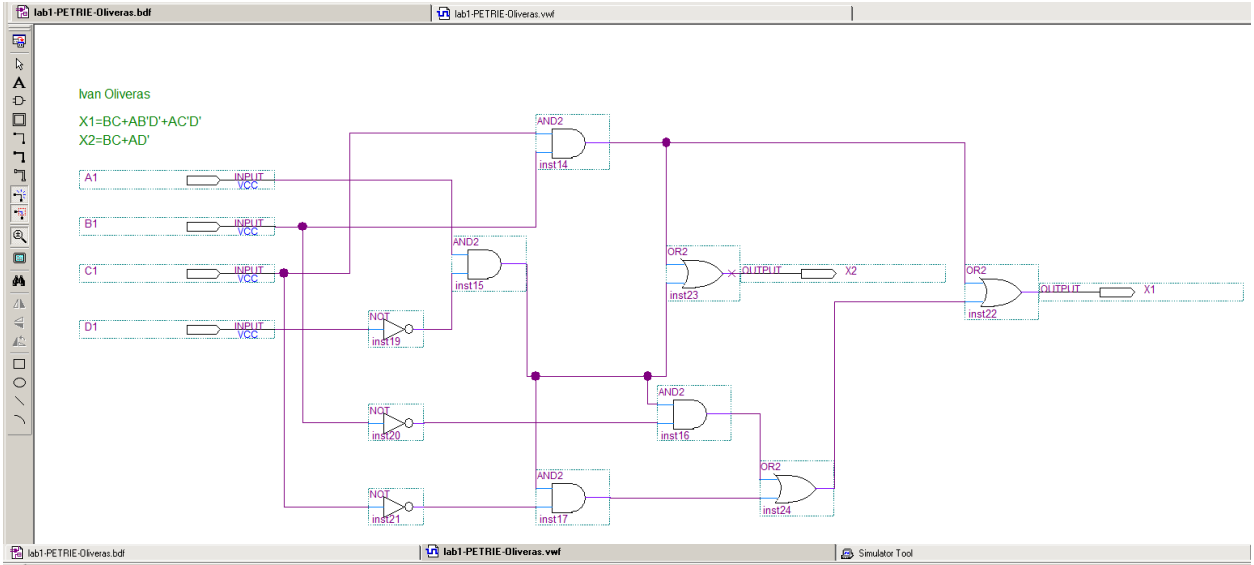
1.10) [20] Use the following chip pin-out to conveniently plan your wiring to build the above 2-output circuit for X1 and X2 on your breadboard using exactly 1/2 7404, 1 7408 and 3/4 7432 chips on your breadboard and then connect inputs ABCD to 4 DIP switched and the outputs X1 X2 to two LED indicators. Test all the 16 different input combinations and observe the two outputs to be equivalent and matching the 1.7 Truth Table.

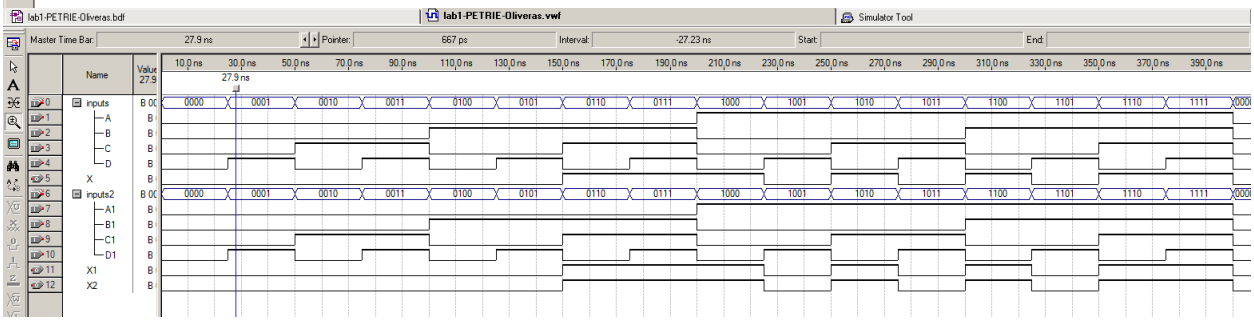


After you get it to work but before the TA grades it, take a picture of your breadboard to submit as part of Lab 1 documentation. After it is graded take a picture of the gradesheet, then, except for the ground and power wires, pull the wires attached to the three the three ICs on the upper breadboard you used for this experiment (Do NOT pull the lab platform wires just the ones in the upper breadboard), leaving the three ICs plugged into your board with power and ground connected. **KEEP THE WIRE TO REUSE FOR NEXT LAB.** Upload the portfolio of your labwork to Canvas to validate your lab grade.

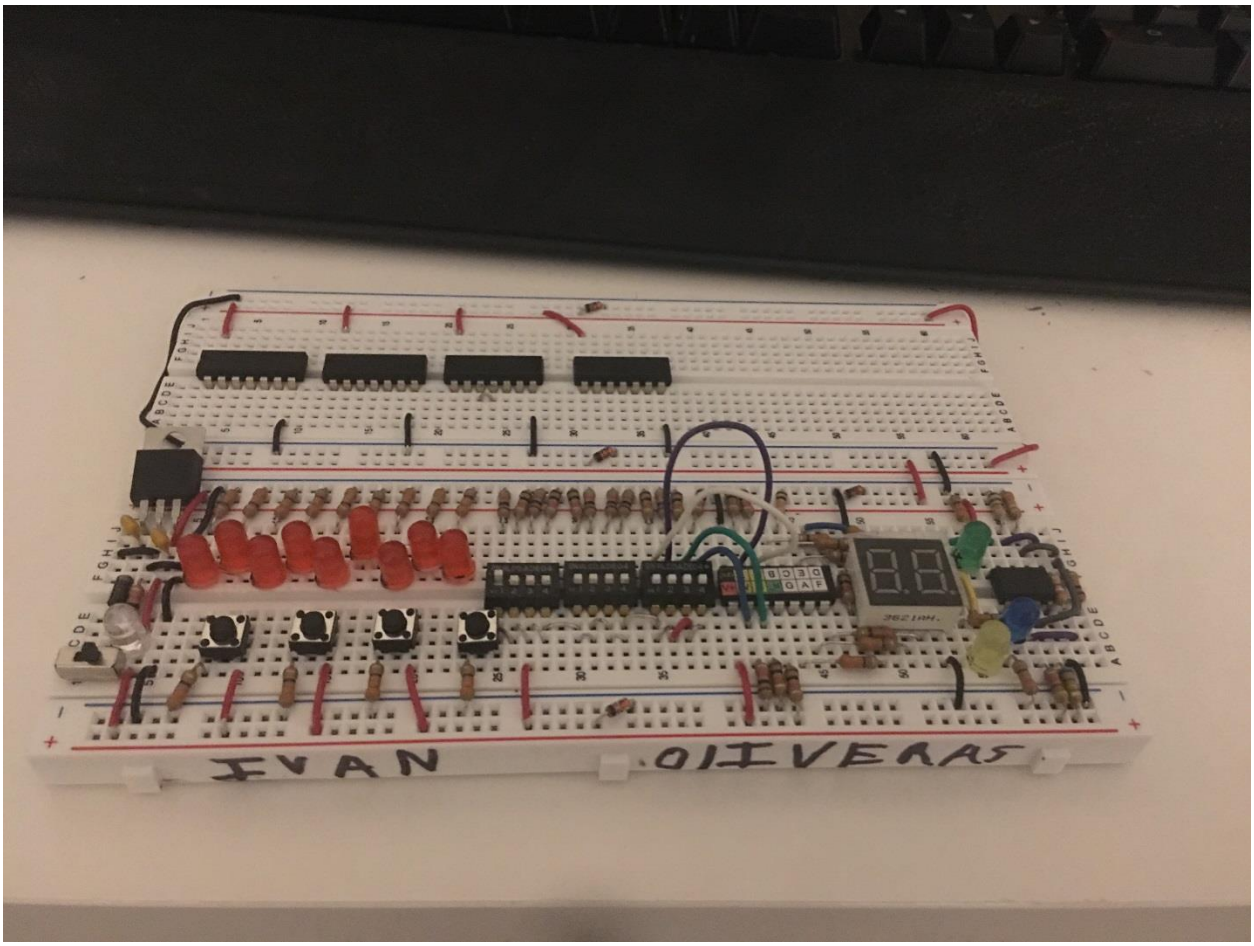
Altera Quartus Logic and Waveform Diagrams







Graded Circuit and Proof




Energizer
9V
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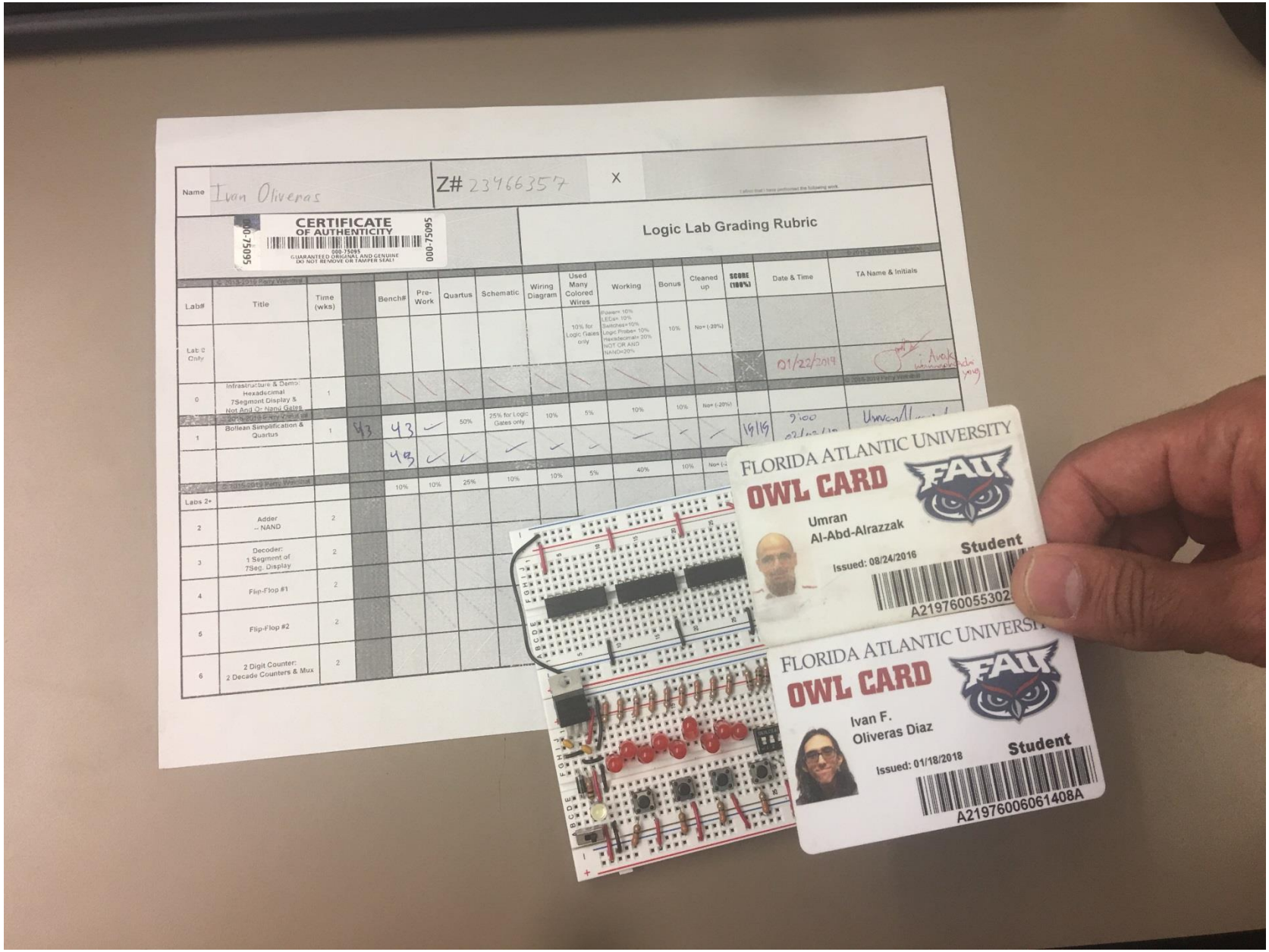
Name Ivan Oliveras
Z# 23466357
CERTIFICATE OF AUTHENTICITY
000-75095
GUARANTEED ORIGINAL AND GENUINE
DO NOT REMOVE OR TAMPER SEAL!
Logic Lab Grading Rubric
Lab#
Title
Time (wks)
Bench#
Pre-Work
Quartus
Schematic
Wiring Diagram
Used Many Colored Wires
Working
Bonus
Cleaned up
SCORE (100%)
Date & Time
TA Name & Initials
Lab 0 Only
01/22/2019
0
Infrastructure & Demo: Hexadecimal 7Segment Display & Not And Or Nand Gates
1
1
Boolean Simplification & Quartus
1
43
50%
25% for Logic Gates only
10%
5%
10%
10%
Labs 2+
10%
10%
25%
10%
10%
5%
40%
10%
2
Adder -- NAND
2
3
Decoder: 1 Segment of 7Seg. Display
2
4
Flip-Flop #1
2
5
Flip-Flop #2
2
6
2 Digit Counter: 2 Decade Counters & Mux
2
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