• CDA3201 • Intro to Logic Design • **Lab Assignment** **0**

Name: Ivan Oliveras **Grade:** /5

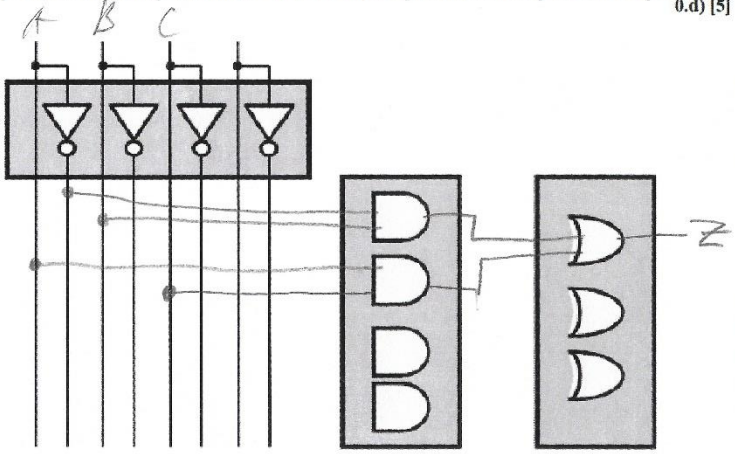
0) [5] This lab experiment is used for the lab orientation where TAs will walk you through practical steps to build the experiment circuit and test it. You will use the following simple function:

$$Z = A'B + AC$$

0.a) [0] Fill the truth table for the above function

	A B C	A' B	A C	Z
1	000	0	0	0
1	001	0	0	0
1	010	1	0	1
1	011	1	0	1
0	100	0	0	0
0	101	0	1	1
0	110	0	0	0
0	111	0	1	1

0.b) [0] Draw the switching function (**Z = A' B + A C**) using Inverters, AND gates, and OR gate



0.c) [0] Using the three logic chips below, draw the wires to make the needed connections between the various gates. Note that not all gates in all chips are used.

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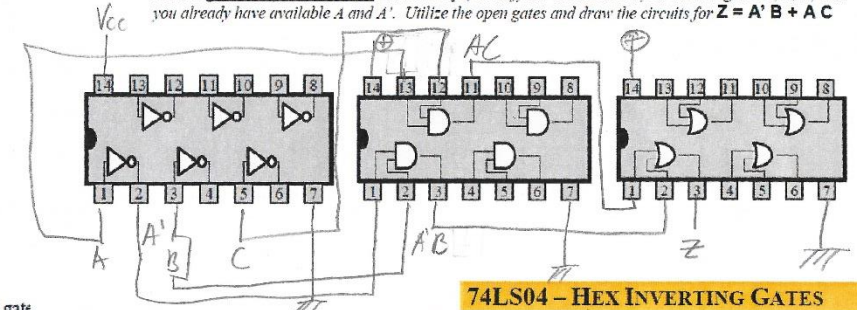
NOTE FROM DR. PETRIE *– Do not remove NOT, AND, OR, and NAND chips and wires from 1st part. Look at gates that you did not use in those chips, identify the switches that you will designate A, B, C, note you already have available A and A'. Utilize the open gates and draw the circuits for* **Z = A' B + A C**



0.d) [5] With the wiring diagram above, you are ready to implement the circuit on the breadboard. For inputs ABC, use three DIP switches (most left) with all in off position (ABC= logic 000).

Note from Dr. Petrie: *Decide which bank of switches you want to use or reuse the inputs you had before.*

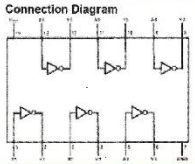
For output Z, use one of the LED indicators (most right). If output Z is logic 0, the LED should be off and when Z is logic 1, the LED should be on. Note that all switches and LED indicators are active high.

Next use the 3 DIP switches to try all binary combinations of inputs ABC and observe the output Z if it turns on and off according to the truth table above. If you have a perfect match, it means you wired the circuit correctly, and you completed lab 0.

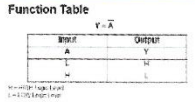
To check the logic level of any pin on any chip, use the probe wire

74LS04 – HEX INVERTING GATES

Connection Diagram

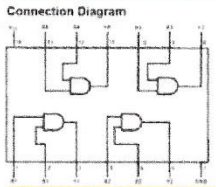


Function Table

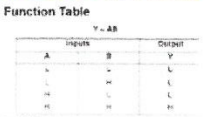


74LS08 – QUAD 2-INPUT AND

Connection Diagram

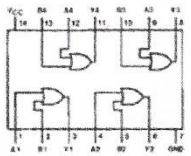


Function Table

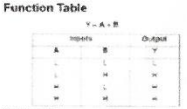


74LS32 – QUAD 2-INPUT OR

Connection Diagram

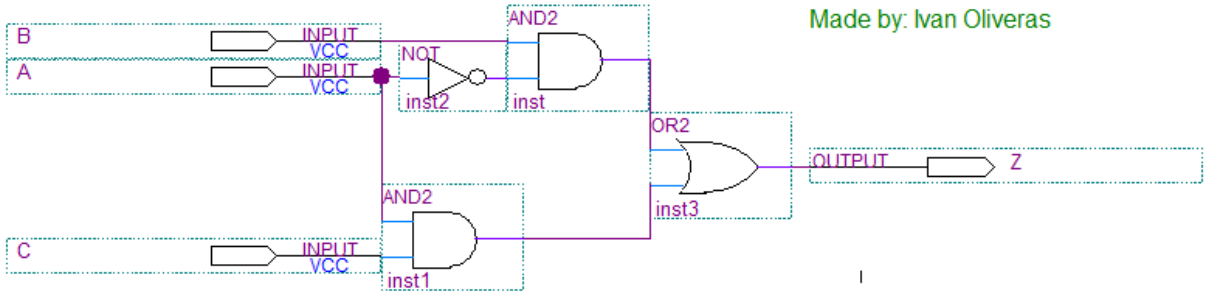


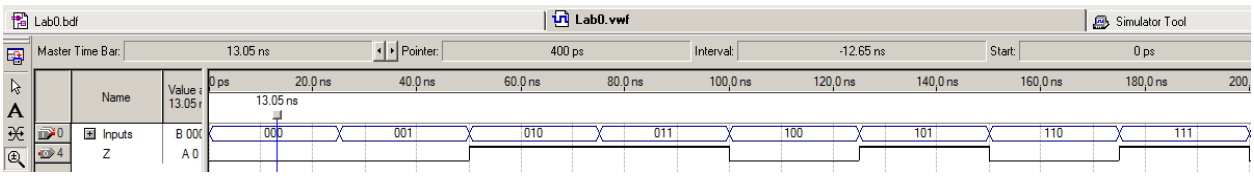
Function Table

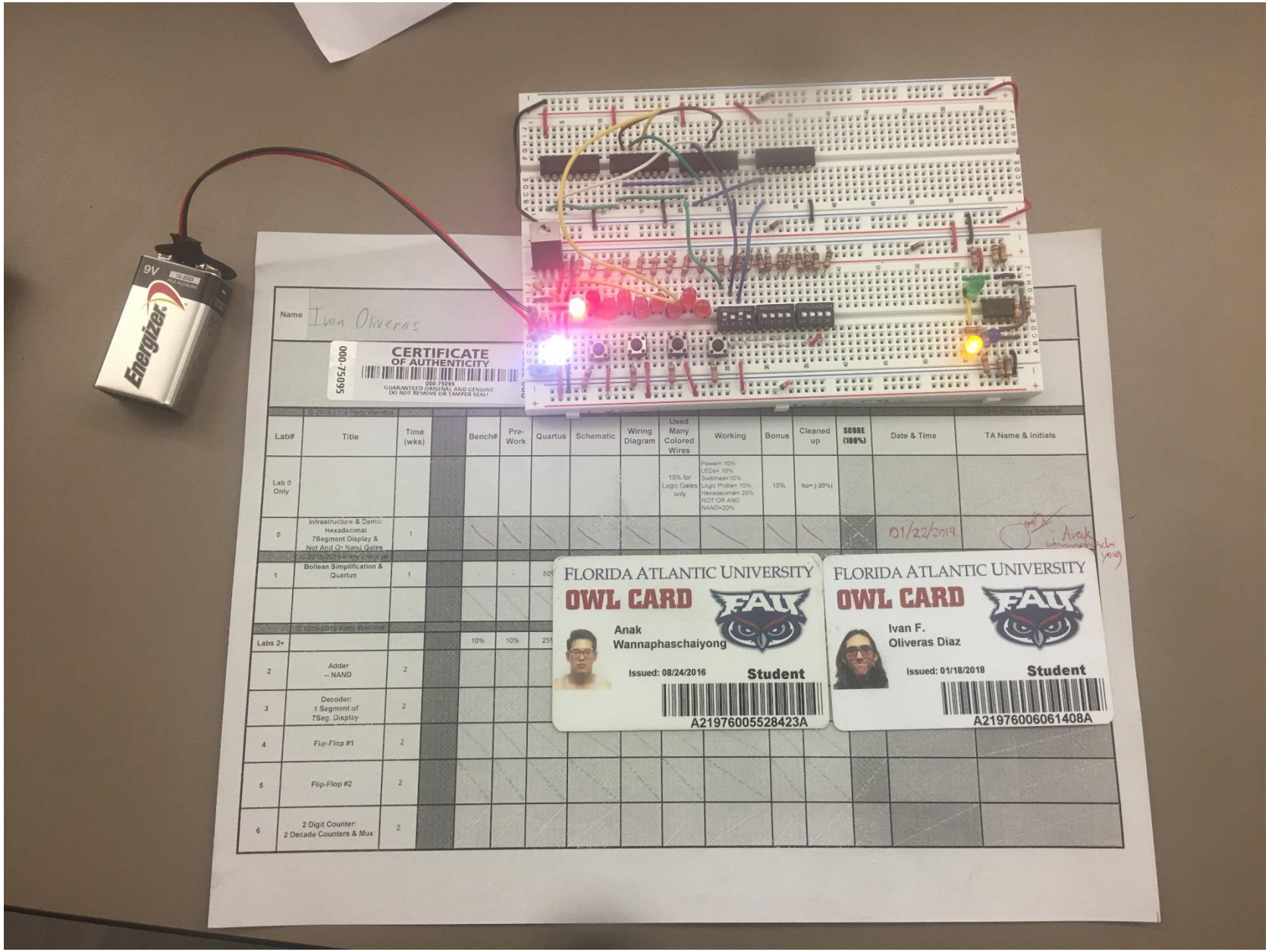


/AB+AC=Z

Made by: Ivan Oliveras







Lab#	Title	Time (wks)	Bench#	Pre-Work	Quartus	Schematic	Wiring Diagram	Used Many Colored Wires	Working	Bonus	Cleaned up	SCORE (100%)	Date & Time	TA Name & Initials
Lab 0 Only								10% for Logic Gates only	Power= 10% LEDs= 10% Switches=10% Logic Probe= 10% Hexadecimal= 20% NOT OR AND NAND=20%	10%	No= (-20%)			
0	Infrastructure & Demo: Hexadecimal 7Segment Display & Not And Or Nand Gates	1											01/22/2019	
1	Boolean Simplification & Quartus	1												
Labs 2+				10%	10%	25%								
2	Adder -- NAND	2												
3	Decoder: 1 Segment of 7Seg. Display	2												
4	Flip-Flop #1	2												
5	Flip-Flop #2	2												
6	2 Digit Counter: 2 Decade Counters & Mux	2												