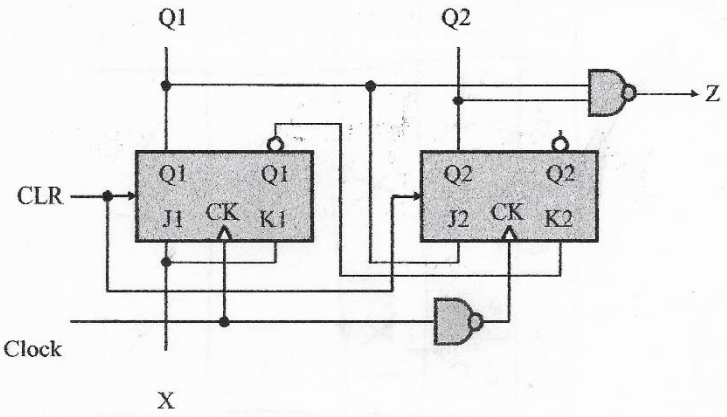
Lab 4 Portfolio

Lab manual

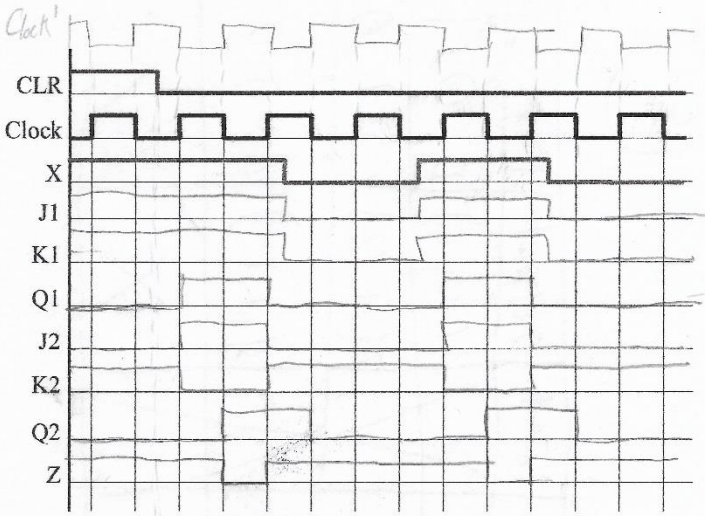
• CDA3201 • Intro to Logic Design •	Lab Assignment	4
Name: Ivan Olveras	Grade:	/100

4) [40] Consider the following sequential circuit with two positive-edge-triggered JK flip-flops.



4.a) [4] Trace the timing diagram for the above circuit by hand.

J2 = Q1
K2 = $\overline{Q1}$



J -> 1
K -> 1
Flip

J -> 1
K -> 0
Set

J -> 0
K -> 1
Reset

J -> 0
K -> 0
Hold

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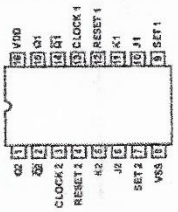
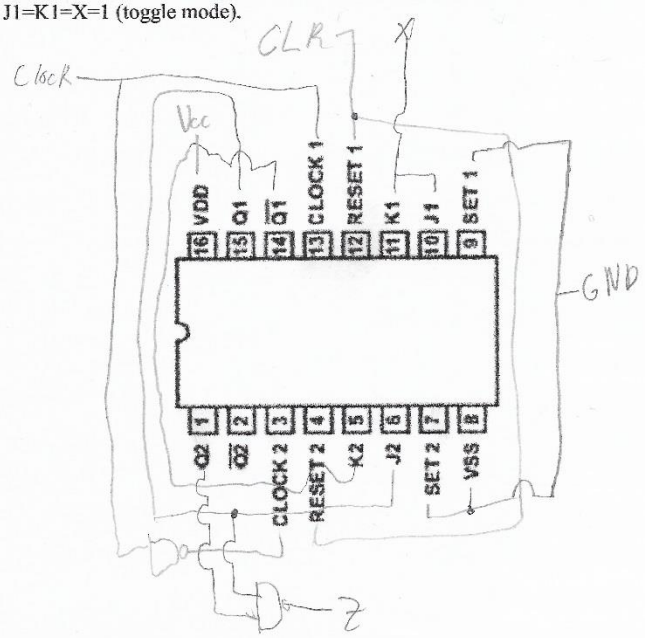


4.c) [8] Verify the circuit design/behavior by implementing the circuit using Quartus and the CD4027BE J-K Flip Flop. Review the PowerPoint in this section know how set the value of CLR and X to a value within a time period. SET1 and SET2 are active high so disable them by connecting permanently to low so see how to set a constant (0) throughout the time period, and how to set the fluctuating value of the clock. Turn in a picture of your Schematic and a picture of the VectorWaveForm generated to match the given timing diagram

4.b) [16] Build the above circuit using the CD4027BE dual JK flip-flop logic chip on your breadboard and then connect it to your test platform to test it. Use the chip block diagram below to plan for your wiring. Use 2 logic switches for inputs X and CLR (Reset), and one pulse switch for the Clock. Use 4 LEDs to observe X=J1= K1, Q1=J2=K2*, Q2, and Z=Q1*+Q2*. Tie the SET inputs to low as they are active high. Plan your circuit below.

Observation: If X is kept high, Q1 will toggle at every positive Clock transition because J1=K1=X=1 (toggle mode).



Q2 Not Used

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4.d) [12] From the analysis of the circuit above, draw the State Table and the State Diagram.

State Diagram:

Check Back

Present State		Input	Output	Next State	Flip Flop Transition
State	Q	i	Z	Q+	

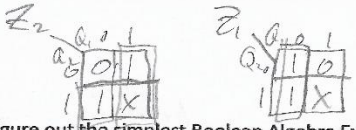
4.e) [60] Build a "Waltz Counter", the Waltz is a dance where you keep time by counting 1, 2, 3, 1, 2, 3, 1, 2, 3, 1...

[10] Draw the State Diagram and Table

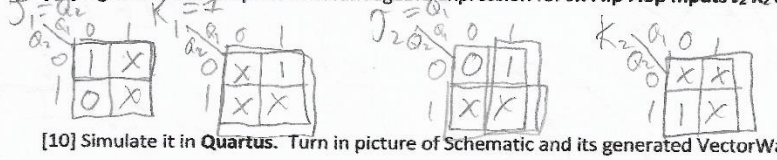
State Diagram: Check p2. back

Present State		Input	Output	Next State	Flip Flop Transition
State	Q	i	Z	Q+	

[10] Figure out the simplest Boolean Algebra Expression for 2 **Output bits Z_2 and Z_1**

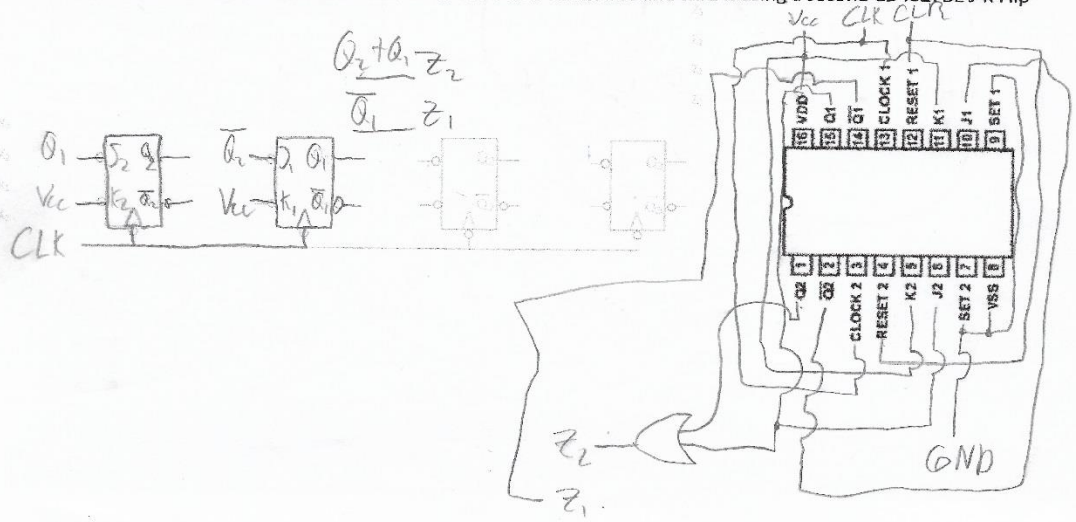


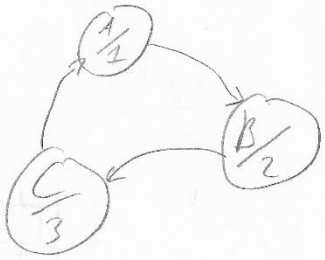
[10] Figure out the simplest Boolean Algebra Expression for **JK Flip Flop Inputs J_2 K_2 and J_1 K_1**



[10] Simulate it in **Quartus.** Turn in picture of Schematic and its generated VectorWaveForm

[20] Plan your wiring below using template below as a guide and wire it using a second CD4027BE J-K Flip



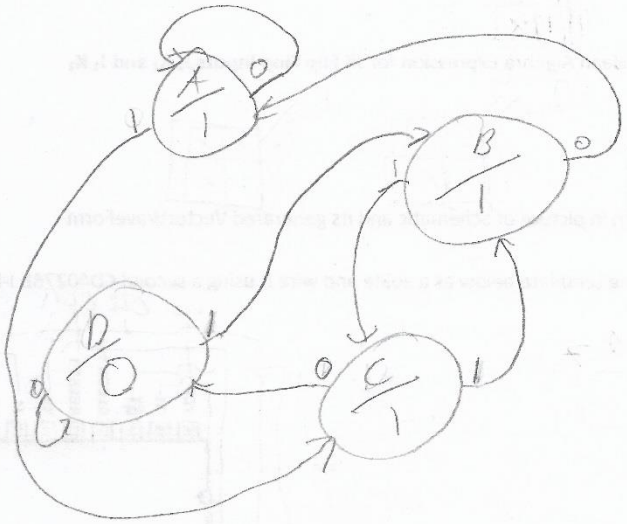


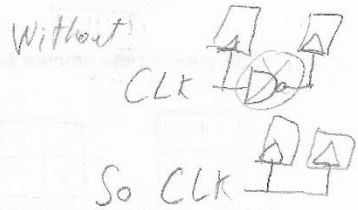
Present State Q_2 Q_1		inPut	Output Z_2 Z_1	Next State Q_2^+ Q_1^+		F. F. Transition J_2 K_2		J_1 K_1	
A	0 0		1 (0 1)	B	0 1	0	X	1	X
B	0 1		2 (1 0)	C	1 0	1	X	X	1
C	1 0		3 (1 1)	A	0 0	X	1	0	X
X	1 1		X	X	X X	X	X	X	X

$Q \to Q^+$	J	K	
0 → 0	0	0	0X
	0	1	
0 → 1	1	0	1X
	1	1	
1 → 0	0	1	X1
	1	0	
1 → 1	1	0	X0
	0	0	

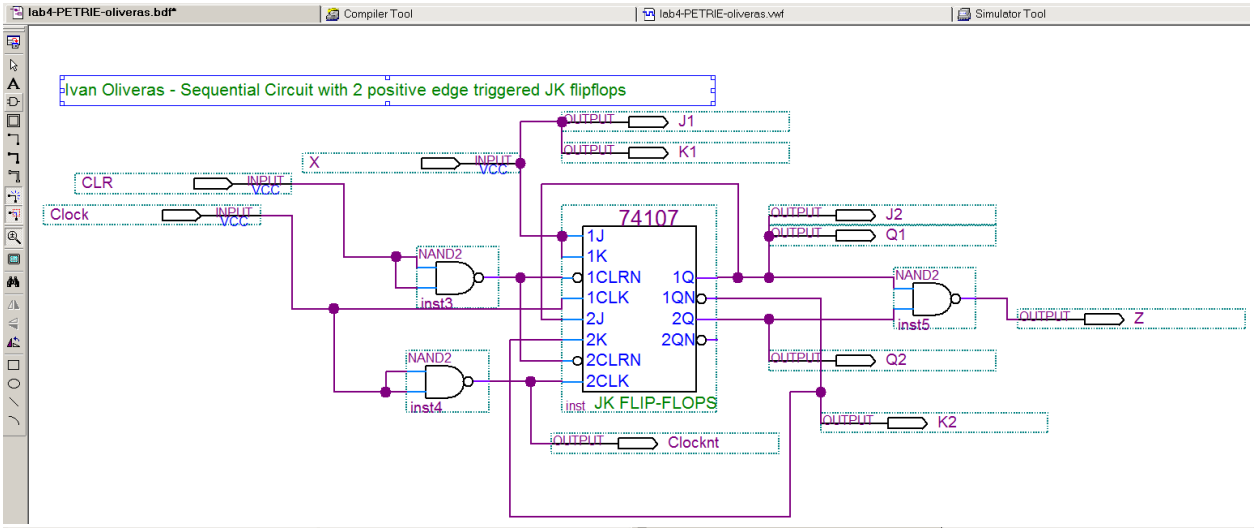
$\overline{Q_1 Q_2}$ Z $\overline{Q_1 Q_2}$

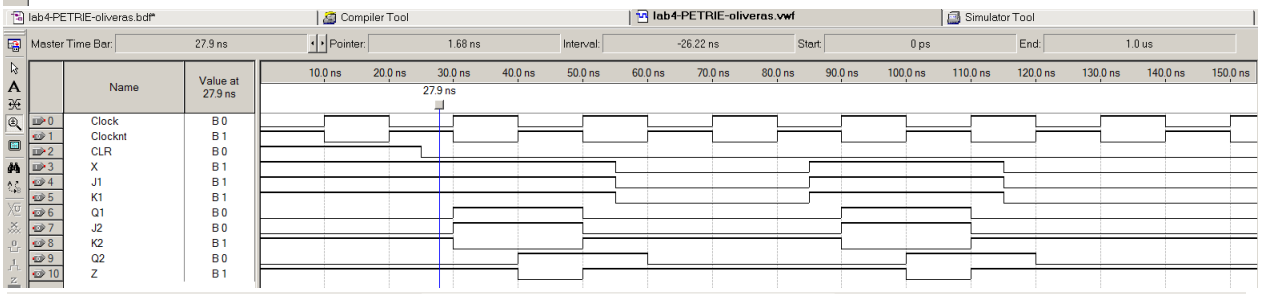
Present State	Input	Output	Next state	F.F. Transition	
Name $Q_1 Q_2$	X	Z	Name $Q_1^+ Q_2^+$	J_1 J_2 K_1 K_2	
A 0 0	0	1	A 0 / C 1 0	0 0 OH / 1 0 1T	Reset
B 0 1	0	1	A 0 / C 1 0	0 0 OH / 1 1 1T	
C 1 0	0	1	D 1 / B 0	0 1 OH / 1 1 1T 0	Set
D 1 1	0	0	D 1 / B 0	0 1 OH / 1 1 1T 0	
	1				

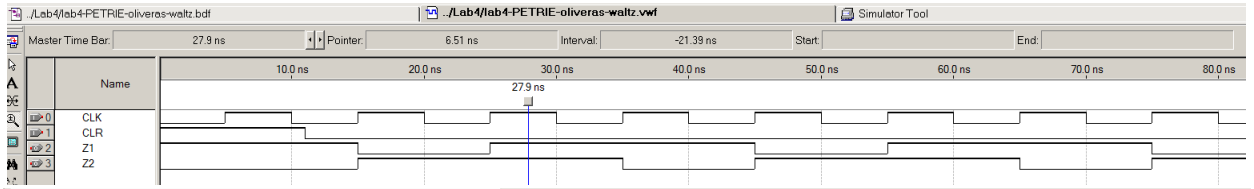


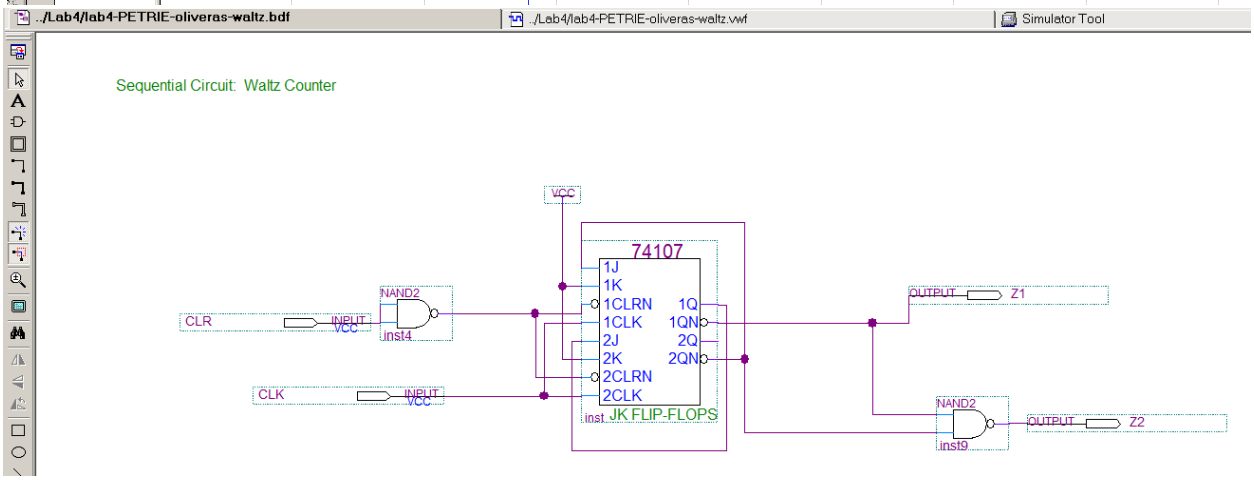


Quartus Schematics and Waveform

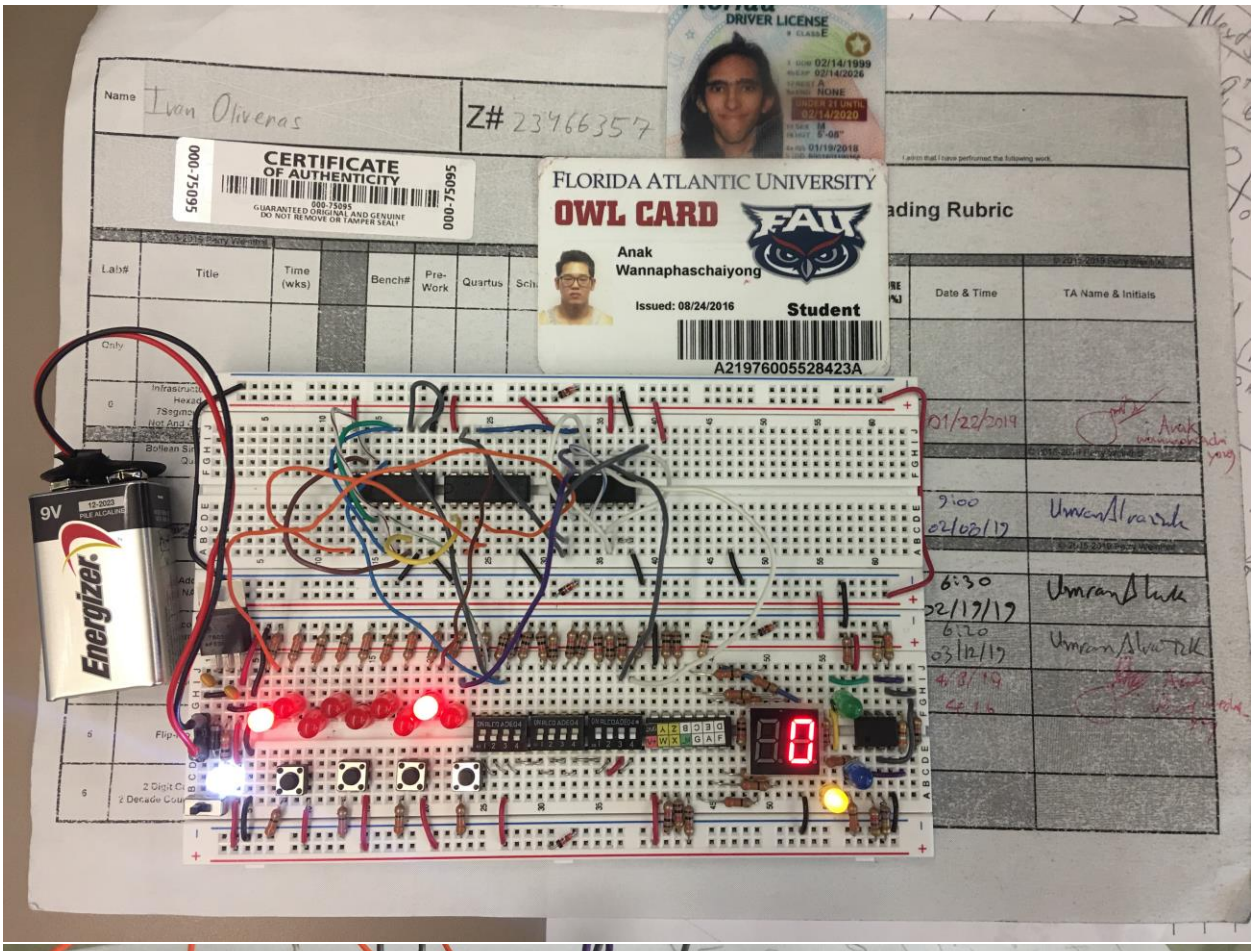


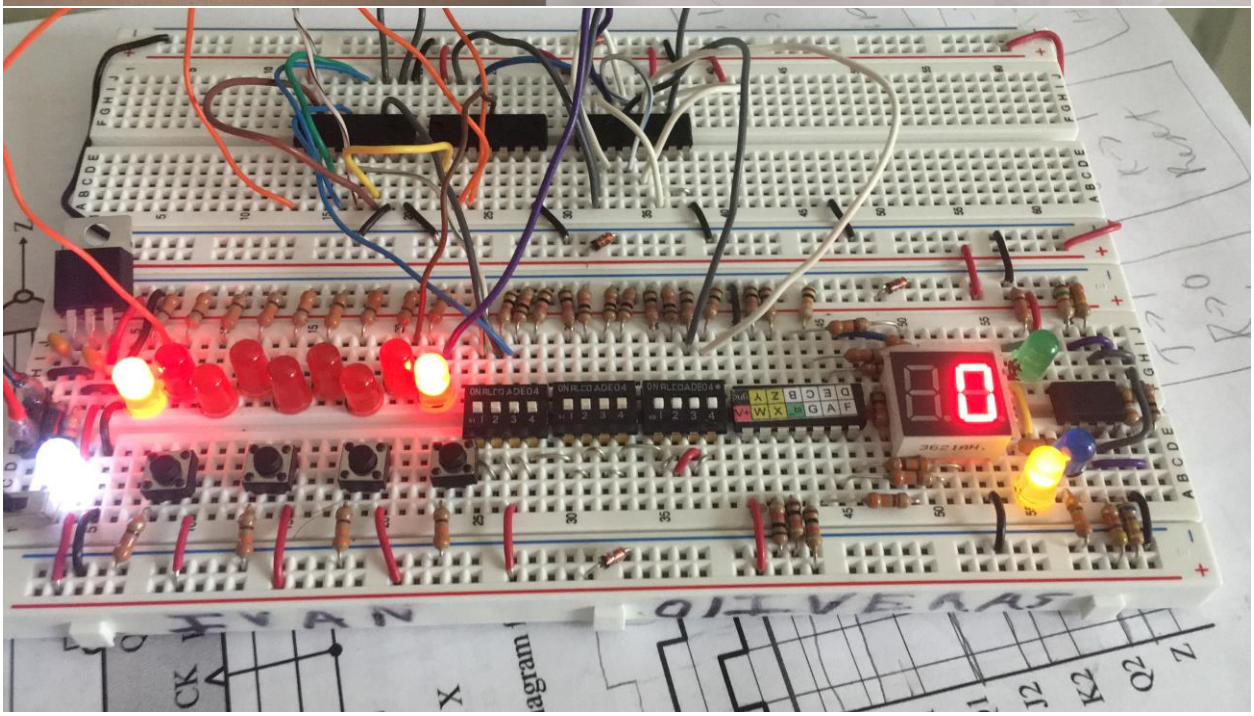


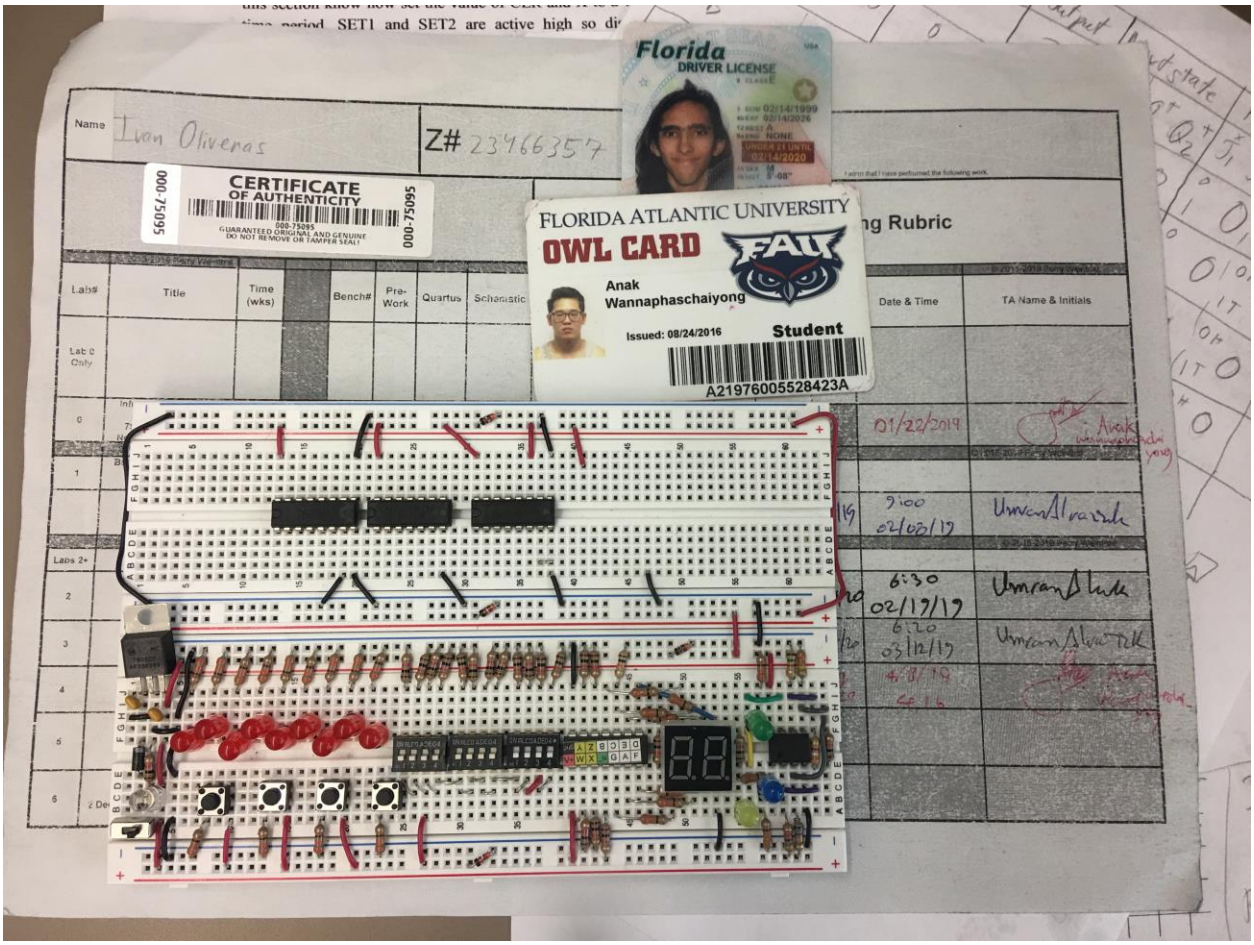




Photos of Lab 4 done in infrastructure



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