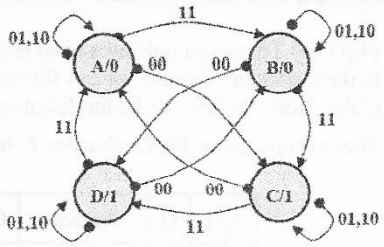
Lab 5 Lab Manual

• CDA3201 • Intro to Logic Design • **Lab Assignment** **5**

Name: Ivan Oliveras **Grade:** /20

5) [20] At right is the state diagram for a Moore sequential circuit which monitors two inputs X_1X_0. When the two inputs X_1X_0 are 00, the output Z toggles at every clock. When the two inputs X_1X_0 are 11, the output Z toggles at every other clock. When the two inputs X_1X_0 are different, the output Z holds its state and does not change until the inputs are equal again.



Use the following table with the gray code assigned (easier to fill in the K-Map if use gray code)

Present State (Q)		Input (X)	Output (Z)	Next State (Q+)		Flip Flop Transition	
State Name	Q_1 Q_0	X_1 X_0	Z	State Name	Q_1^+ Q_0^+	J_1 K_1	J_0 K_0
A	0 0	0 0	0	C	1 1	1 X	1 X
		0 1		A	0 0	0 X	0 X
		1 1		B	0 1	0 X	1 X
		1 0		A	0 0	0 X	0 X
B	0 1	0 0	0	D	1 0	1 X	X 1
		0 1		B	0 1	0 X	X 0
		1 1		C	1 1	1 X	X 0
		1 0		B	0 1	0 X	X 0
C	1 1	0 0	1	A	0 0	X 1	X 1
		0 1		C	1 1	X 0	X 0
		1 1		D	1 0	X 0	X 1
		1 0		C	1 1	X 0	X 0
D	1 0	0 0	1	B	0 1	X 1	1 X
		0 1		D	1 0	X 0	0 X
		1 1		A	0 0	X 1	0 X
		1 0		D	1 0	X 0	0 X

5.a) [TA-4] Fill in the **output** and the **next state** columns of the table

5.b) [TA-4] Fill in the the next state columns of the table

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Flip Flop Transition indicates what is the input needed for J and K to cause the change from the present state to the next state. Before we can fill the Flip Flop Transition columns of the table, complete the JK truth table. Note: Action can be the following H = Hold (don't change), S=Set, R=Reset, T=Toggle (change). Then complete the **JK Excitation Table** that permits the Flip Flop to change from **Q** to **Q⁺**

J	K	Q	Action	Q+
0	0	0	Holds	0
		1		1
0	1	0	Reset	0
		1		0
1	0	0	Set	1
		1		1
1	1	0	Toggle	1
		1		0

Q → Q⁺ Action J K

0 → 0 H 0 0 / R 0 1 — 0 X

0 → 1 T 1 1 / S 1 0 — 1 X

1 → 0 T 1 1 / R 0 1 — X 1

1 → 1 H 0 0 / S 1 0 — X 0

In the table on the first page highlight the values of Q_1, Q_1^+ and area under J_1 K_1 in one color, use a different highlight for Q_0, Q_0^+ and J_0 K_0. Using the Excitation table compare the same color **Q → Q⁺** to fill the value under corresponding **J K** to complete the JK Transition table

5.c) [2] Fill the JK input maps for each of the two flip-flops. Note how easy it is to fill in from the table because we are using the gray code for numbering.

5.d) [2] Write the JK inputs and Z output expressions in a minimized form:

J_1 (rows Q_1Q_0, columns X_1X_0 in 00 01 11 10):

Q_1Q_0 \ X_1X_0	00	01	11	10
00	1	0	0	0
01	1	0	1	0
11	X	X	X	X
10	X	X	X	X

K_1 (rows Q_1Q_0, columns X_1X_0 in 00 01 11 10):

Q_1Q_0 \ X_1X_0	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	1	0	0	0
10	1	0	1	0

J_0 (rows Q_1Q_0, columns X_1X_0 in 00 01 11 10):

Q_1Q_0 \ X_1X_0	00	01	11	10
00	1	0	1	0
01	X	X	X	X
11	X	X	X	X
10	1	0	0	0

K_0 (rows Q_1Q_0, columns X_1X_0 in 00 01 11 10):

Q_1Q_0 \ X_1X_0	00	01	11	10
00	X	X	X	X
01	1	0	0	0
11	1	0	1	0
10	X	X	X	X

Z_0 (rows Q_1, columns Q_0 in 0 1):

Q_1 \ Q_0	0	1
0	0	0
1	1	1

$J_1 = \bar{X}_1\bar{X}_0 + Q_0X_1X_0$ $\quad K_1 = \bar{X}_1\bar{X}_0 + \bar{Q}_0X_1X_0$

$J_0 = \bar{X}_1\bar{X}_0 + X_1X_0\bar{Q}_1$ $\quad K_0 = \bar{X}_1\bar{X}_0 + Q_1X_1X_0$

$Z = Q_1$

$\overline{AD} = \bar{A} + \bar{B}$

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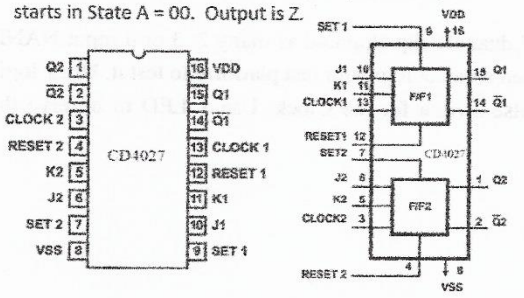
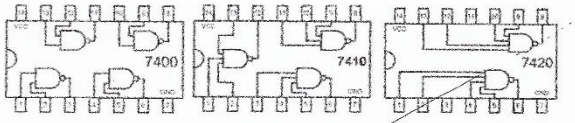
5.e [Petrie - 80] Design the circuit above using the **CD4027BE dual JK flip-flop** in your kit and as many 2, 3, or 4 input NAND gates as needed. Inputs are X1 and X2, Clock and Reset. Reset should reset both Flip Flops so the system starts in State A = 00. Output is Z.

Note for the CD4027: the clocks are activated on the rising edge (going from 0 to 1 – when pushing down the pulse switch to turn on). If the pulse switch does not work well as the clock, use a toggle switch, sometimes the switches "bounce". Note that the CD4027 has a SET and a RESET. These are used to clear to 0 or set the values to the first state of the state diagram. Note both SET and RESET are active high. If you assigned State A as 00 then to start we need to RESET both Flip Flops, so link them together and connect to one of the switches. So you will have the two Xs, and the RESET for the circuit linked to the Switches. You will not be using SET, so tie it to ground so it won't be activated, note it is active high. VDD is equivalent to VCC and VSS is equivalent to GND

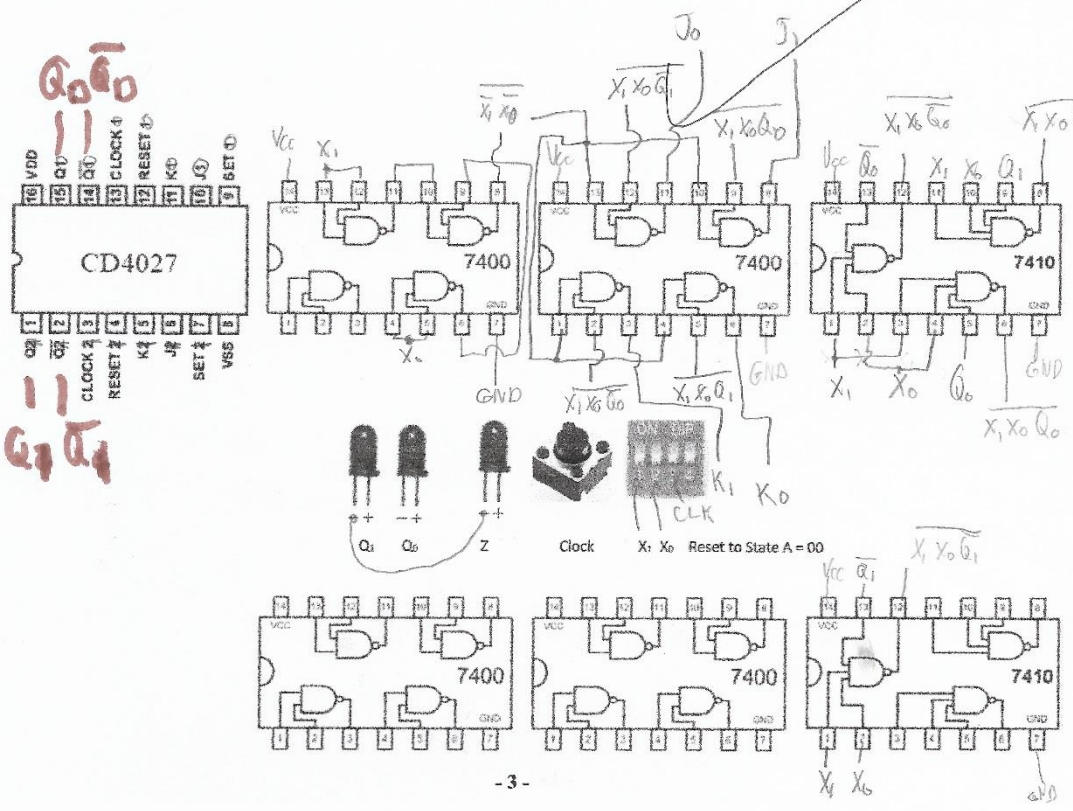


(a) Pinout (b) Functional Diagram

CD4027BE dual JK flip-flop



Determine how many NAND Chips you need



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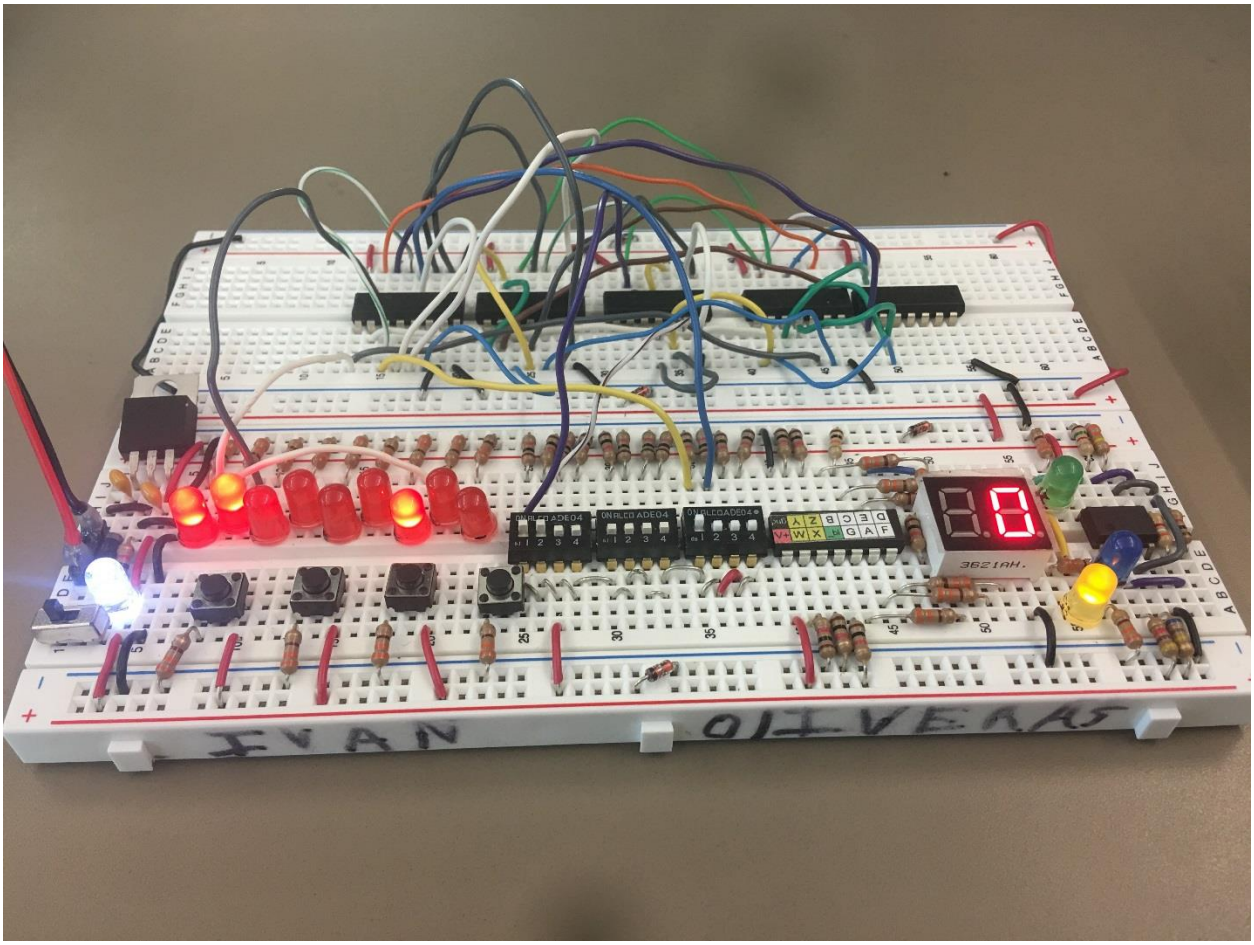
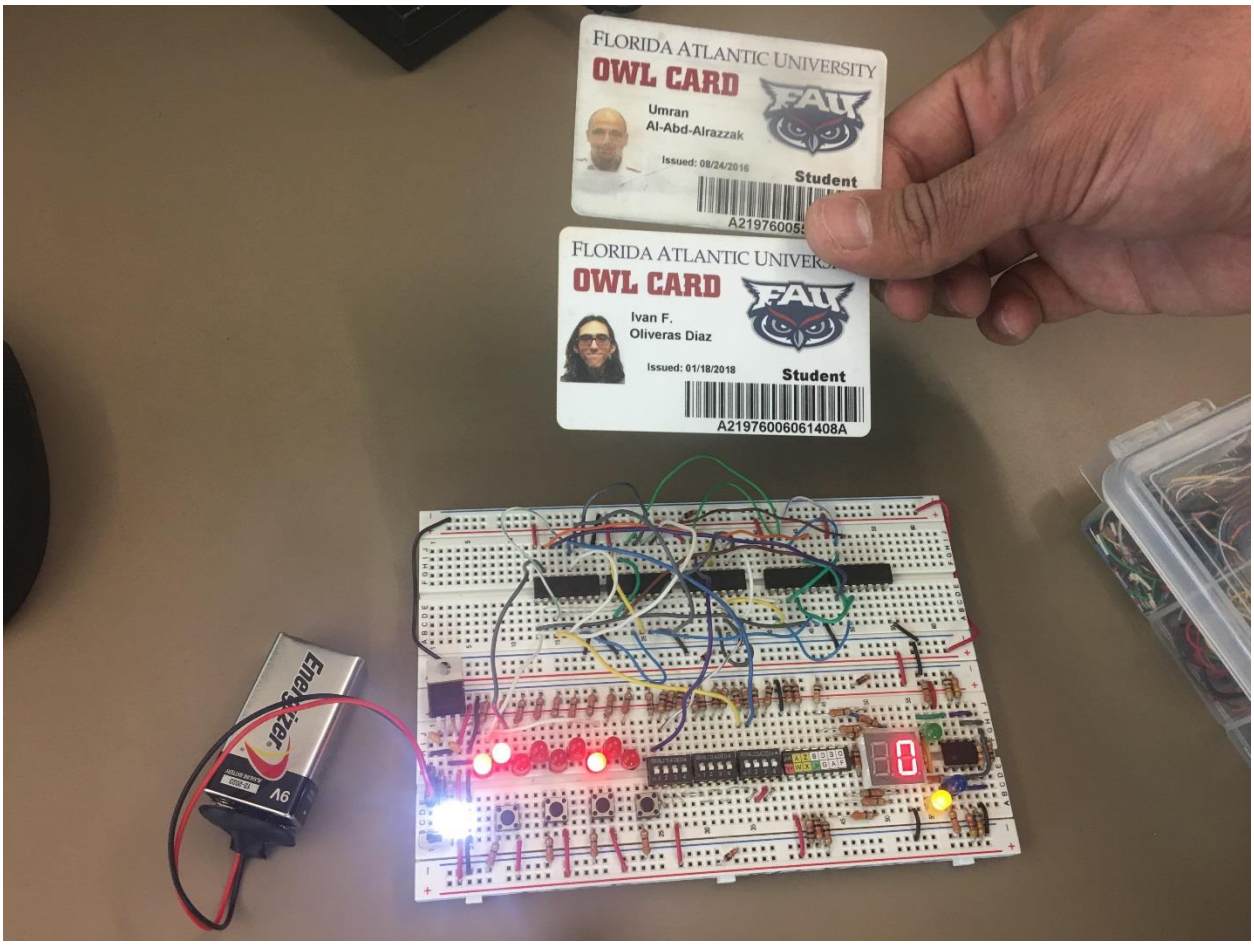
YOU DO NOT NEED TO DO QUARTUS FOR LAB 5

5.f) [4] Verify the circuit design/behavior by implementing the circuit using Quartus. In Quartus you can group inputs X1 and X2 to count, the Clock is set using the same interface as you select to produce binary count but select Clock instead. You will need to set other parameters of the clock, such as the period and the duty cycle. Set to Use 1 LED to observe the behavior of output Z. It is highly recommended that you use

5.e) [8] Build the above circuit using the CD4027 dual JK flip-flop and as many 2, 3 or 4 input NAND gates as needed on your breadboard and then connect it to your test platform to test it. Use 2 logic switches for inputs X1 and X2 and 1 pulse switch for the Clock. Use 1 LED to observe the behavior of output Z.

Lab 5 in infrastructure

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Issued: 08/24/2016
Lab# Title Time (wks) Bench# Pre-Work
Lab 0 Only
0 Infrastructure & Demo: Hexadecimal 7Segment Display & Nor And Or Nand Gates 1
1 Boolean Simplification & Quartus 1
Labs 2+
2 Adder -- NAND 2
3 Decoder: 1 Segment of 7Seg. Display 2
4 Flip-Flop #1 2
5 Flip-Flop #2 2
6 2 Digit Counter: 2 Decade Counters 1 Mux 2
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