Digital Logic Design

Computer Assignment 4

Report sheet

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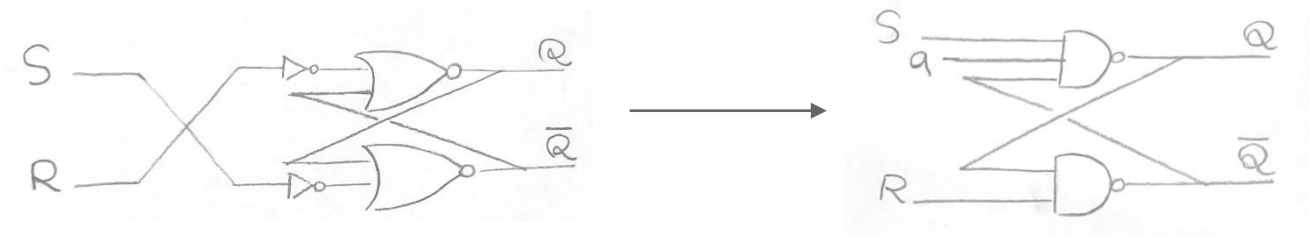
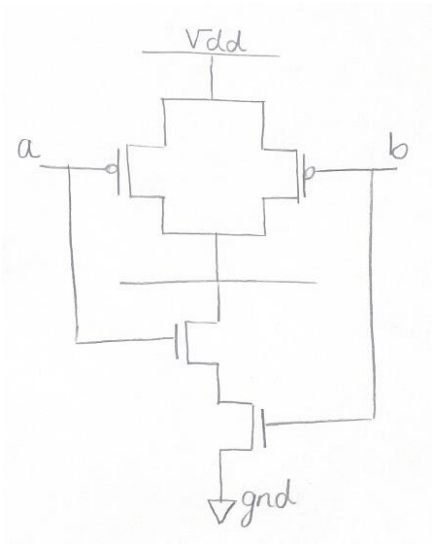
Q1) a) First we design a simple NOR SR-latch and to do that we invert the inputs using invertors cause the inputs are active low. Then we use extra bubbles to simplify the latch and make it with all NAND gates like shown below:

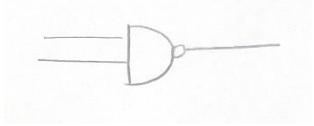


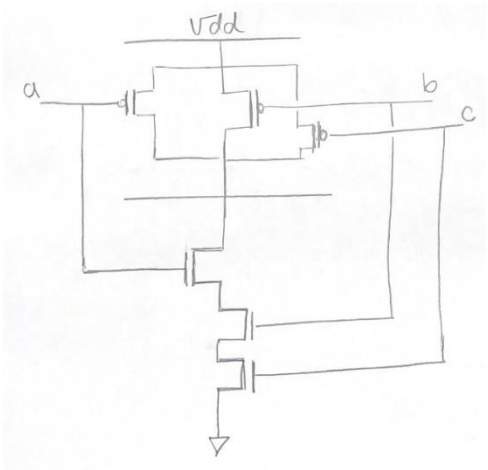
As the question said we put a 3-input NAND on the top for probable use and if we don't need in we would put a = 1 .

b) We build the switch level for both 2 and 3 input NAND gates and calculate the delays:

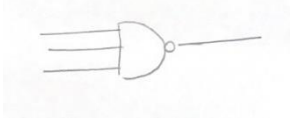


Delay = max (6, 4 + 4) = 8 ns

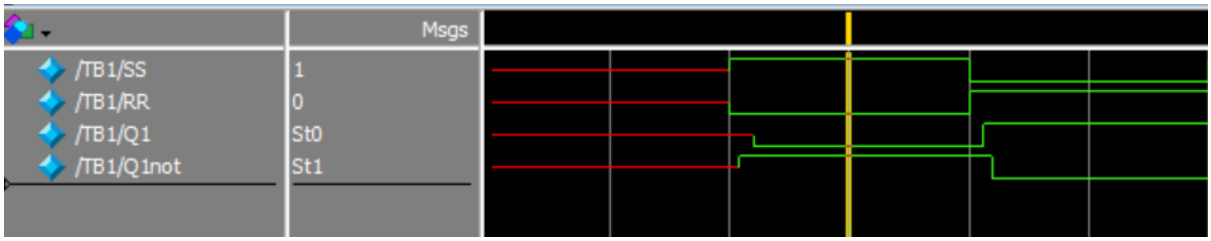




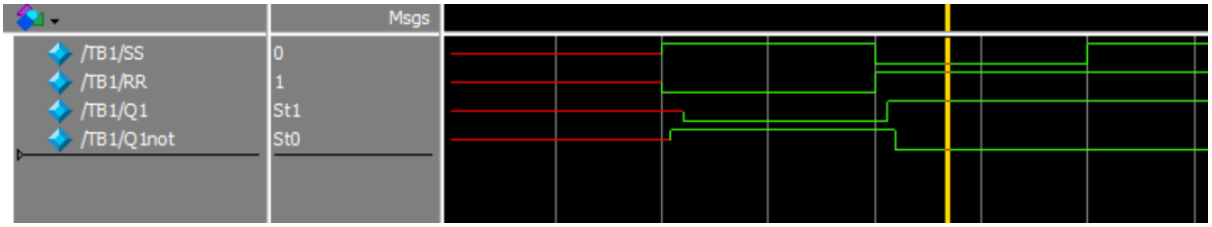
Delay = max (6, 4 + 4 + 4) = 12 ns



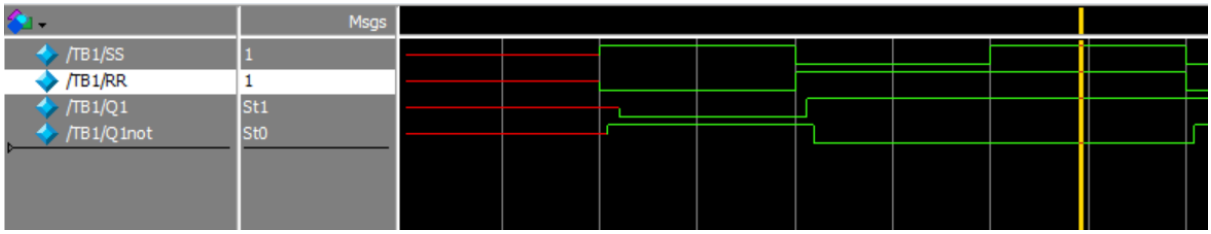
c) Wrote a testbench for the mentioned latch and the waveforms would be like:



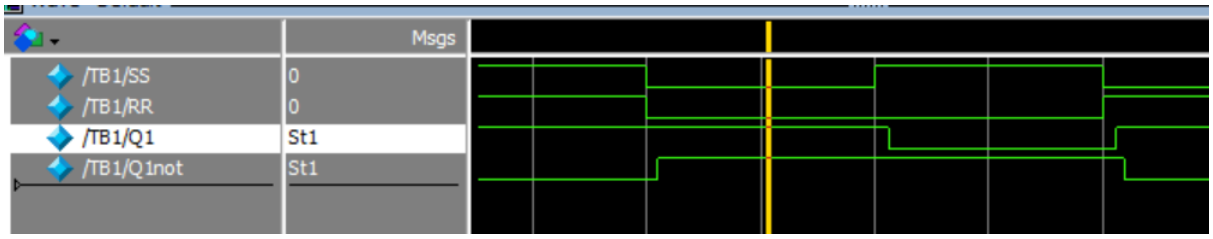
1. S = 1 , R = 0 , Q = 0



2. S = 0 , R = 1, Q = 1



3. S = 1 , R = 1 , Q = same state

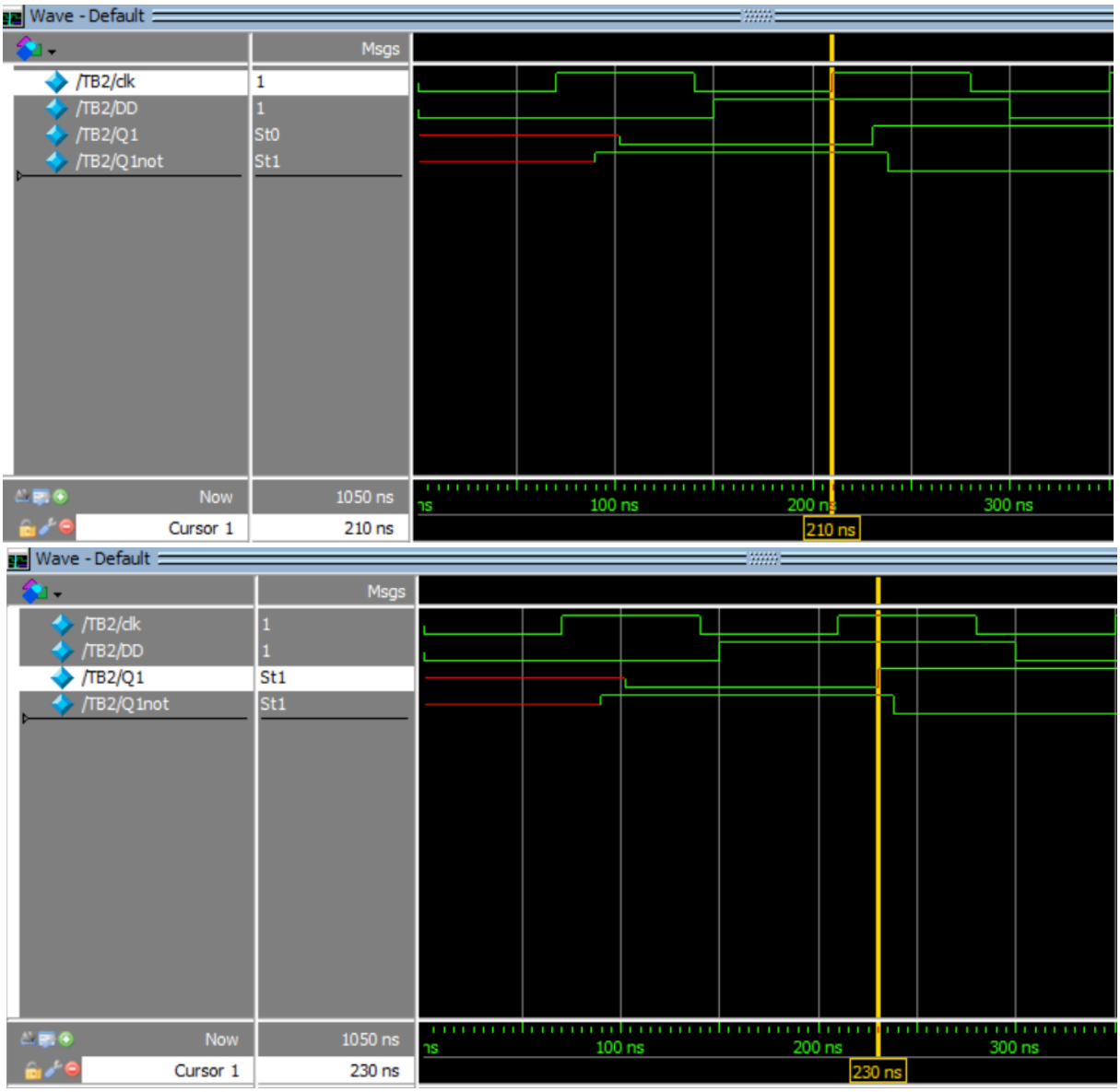


4. S = 0 , R = 0 , Q = 1 & ~Q = 1

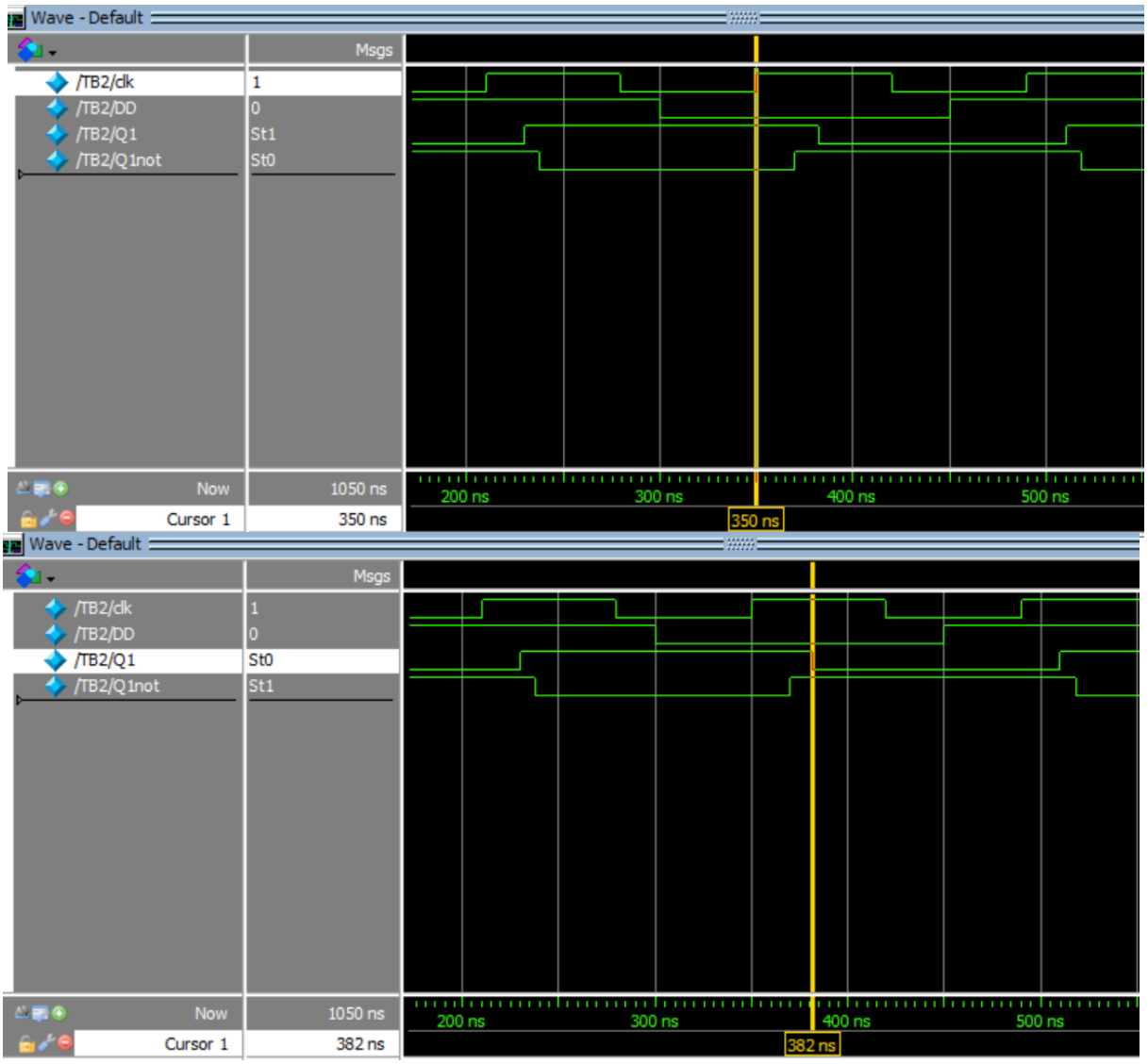
We observe having memory loss In this case.

Q2) a) To build this flip-flop we use a 3-input NAND in the upper gate to have similar delays so we put a = 1 in 2 of 3 of the 3-input NANDs.
Then we use the Q1 module (the SR-latch) 3 times to build the requested flip-flop.

b) In the waveform below when the clock is rising from 0 to 1 and our D input is 1, so we expect Q to change to 1 like our input D is. The to-1 delay is appears to be 20 ns as we can see in the waveforms.

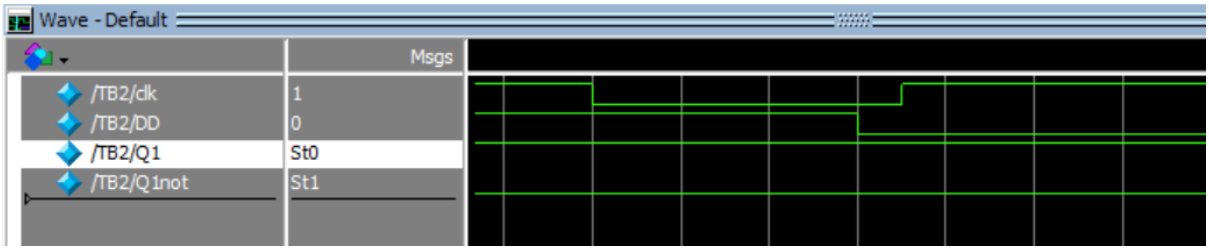


In the same way, Q to-0 delay appears to be 382-350 = 32 ns.

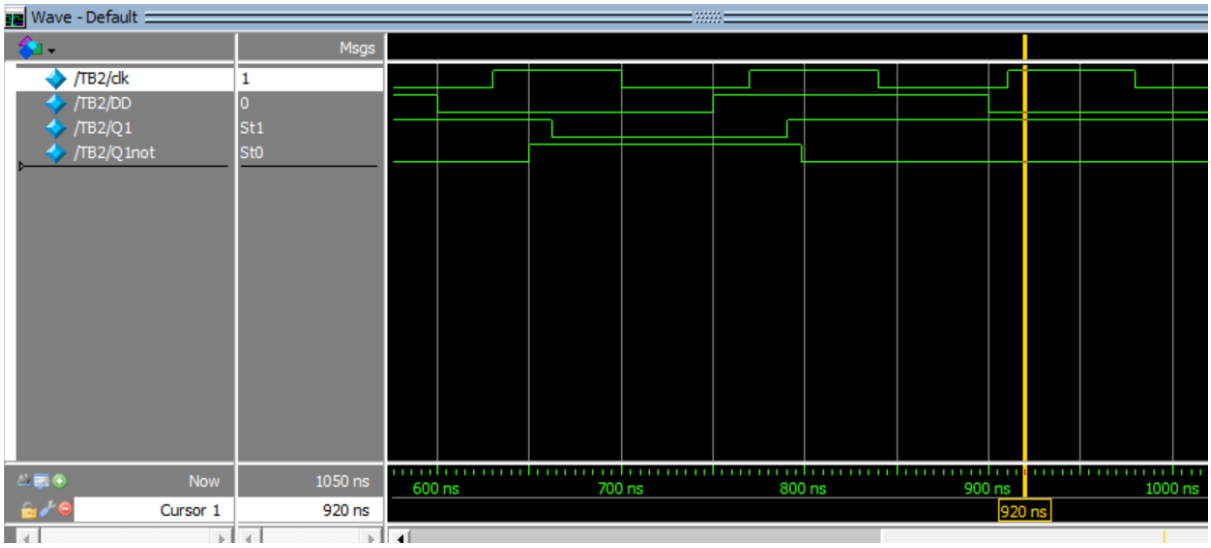


As we know, Q output depends on D value only if our clock is in rising edge, otherwise Q does not change.

For example in the waveform from Q2 testbench shown below, when D input changes within the setup time), the Q value would not change because clock would get ahead of it and ignore it.

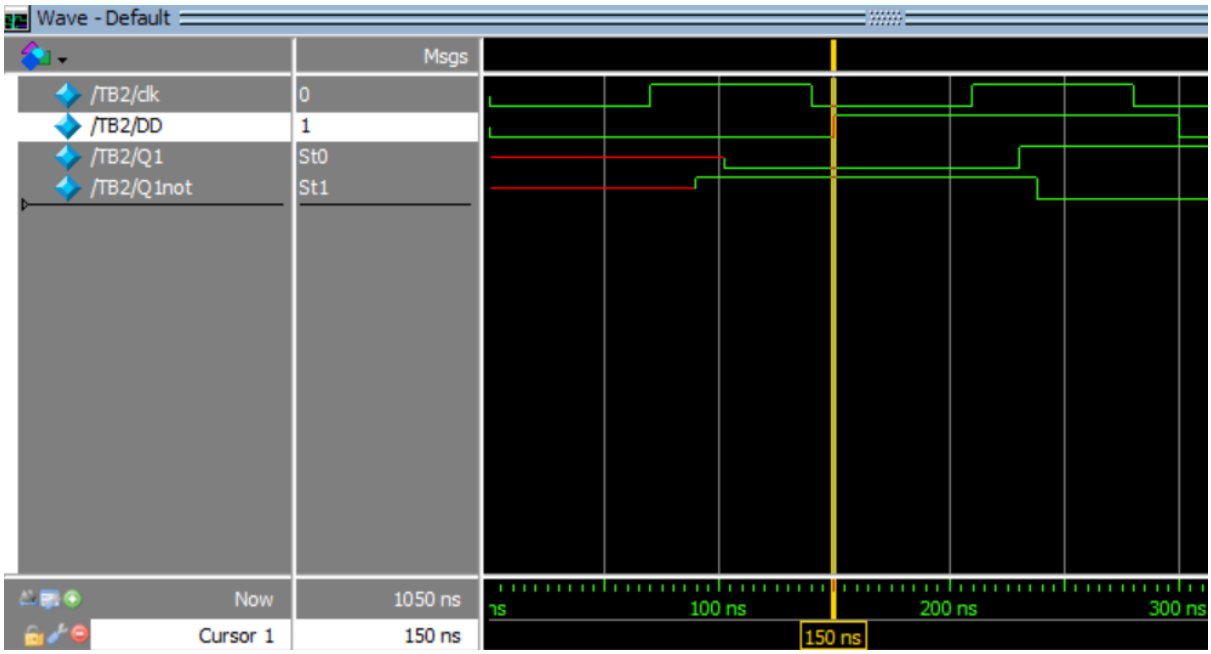


c) to examine the t-setup time as we observe the waveform, we can say that the output does not change if D changes 10ns before clocking but it does change if D changes 20ns before it. So we can say that the t-setup time would be a number between 10 - 20 ns for sure.



d) the t-hold time also appears to be smaller that 20 ns because as we can see in the waveform below its going all fine.

Its also visible that the t-hold time can be even lower like about 10 ns:



Q3) e) We have 3 NAND gates in this flip-flop and all of those are 3-inputs so we should just call the 3-input NAND module 3 times to build this one.

You should also notice that preset and clear value are both active low here.

g) While preset being active the Q output would not change even if we clock as we can see in the waves.

h) Preset and clear simultaneously active would cause a memory loss because both Q and ~Q would get 1.