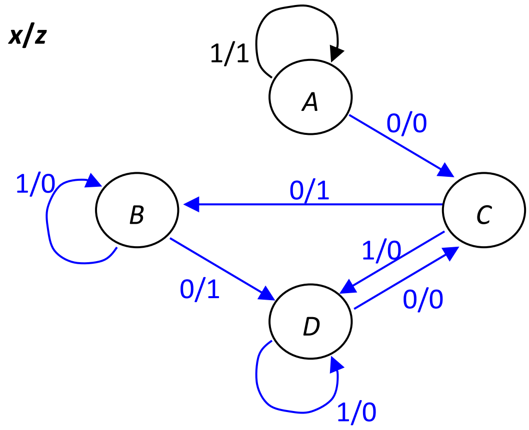
CS2100 Computer Organisation
Tutorial #9: Sequential Circuits
(Week 11: 1 – 5 April 2024)
Answers

Discussion Questions:

D1. The state table on the right describes the state transition of a circuit with 4 states *A*, *B*, *C* and *D*, an input *x*, and an output *z*. For example, if the circuit is in state *A* and its input *x* is 0, then it moves into state *C* and generates the output 0 for *z*.

	x	
	0	1
A	*C*/0	*A*/1
B	*D*/1	*B*/0
C	*B*/1	*D*/0
D	*C*/0	*D*/0

(a) Complete the state diagram below. The label of the arc indicates input/output, hence 1/1 means *x*=1 and *z*=1.

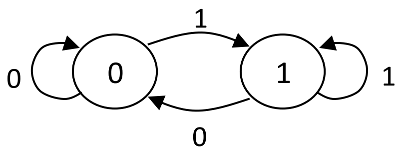


(b) Assuming that the circuit starts in state *A*, find the output sequence and state sequence for the input sequence *x* = 100010 (read from left to right). (*x* = 100010 means that initially *x* is 1, then in the next clock *x* is 0, and so on.)

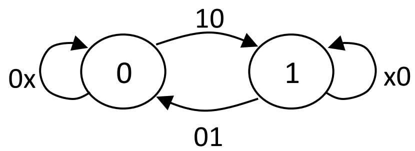
State *Q*:	*A*	*A*	*C*	*B*	*D*	*D*	
Input *x*:	1	0	0	0	1	0	
Next state Q^+:	***A***	***C***	***B***	***D***	***D***	***C***	← required answer
Output *z*:	**1**	**0**	**1**	**1**	**0**	**0**	← required answer

D2. Match the following state diagrams to the 4 flip-flops: *JK* flip-flop, *D* flip-flop, *RS* flip-flop, and *T* flip-flop. Don't-care value is indicated by "x".

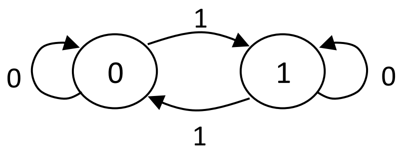
(a) *D* flip-flop



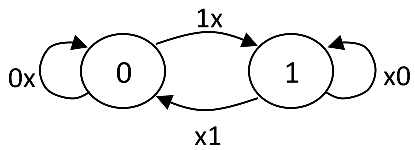
(b) *SR* flip-flop



(c) *T* flip-flop

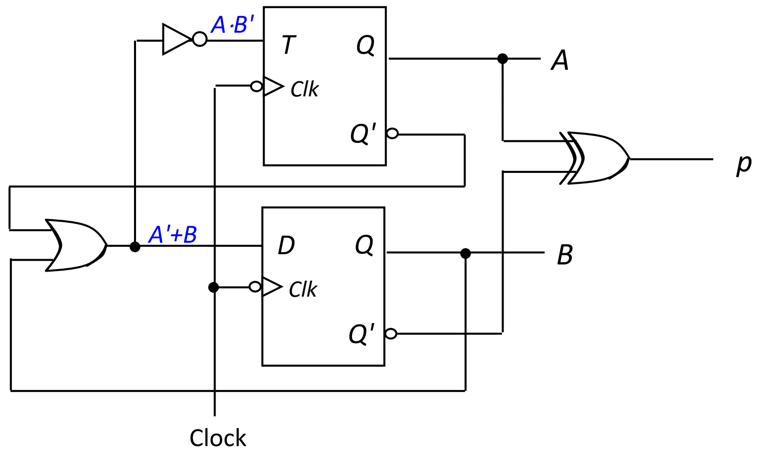


(d) *JK* flip-flop



Tutorial Questions

1. A four-state sequential circuit below consists of a ***T* flip-flop** and a ***D* flip-flop**. Analyze the circuit.



   (a) Complete the state table and hence draw the state diagram.
   (b) Assuming that the circuit is initially at state 0, what is the final state and the outputs generated after 3 clock cycles?

   A state is called a ***sink*** if once the circuit enters this state, it never moves out of that state.

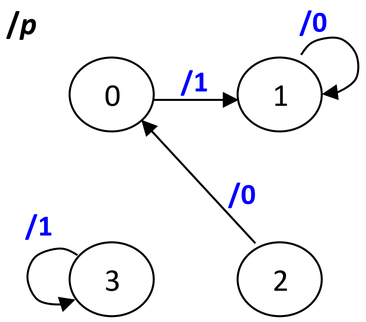
   (c) How many sinks are there for this circuit?
   (d) Which is likely to be an unused state in this circuit?

Answers:

(a)

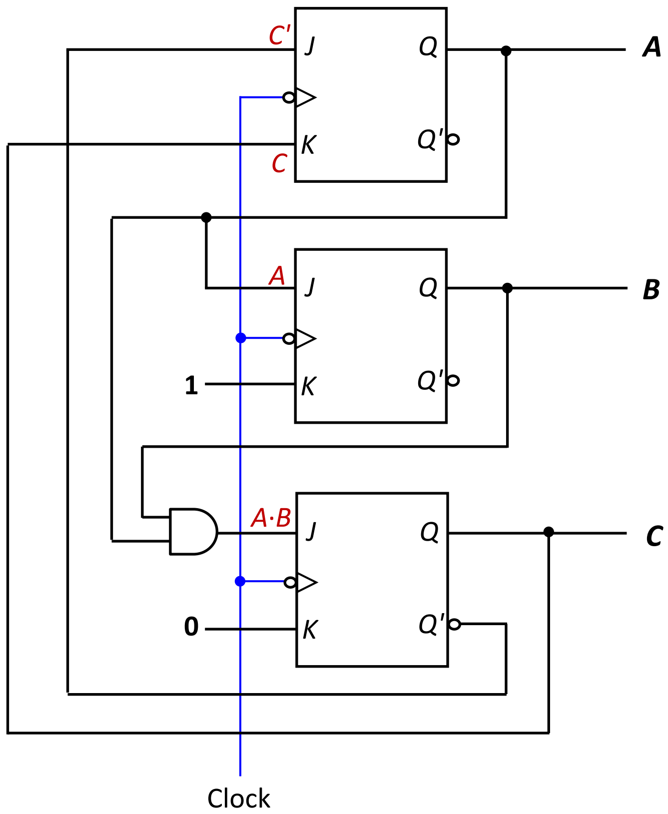
$p = A \cdot B + A' \cdot B'$
$TA = A \cdot B'$
$DB = A' + B$

Present state		Output	Flip-flop inputs		Next state	
A	***B***	***p***	***TA***	***DB***	***A+***	***B+***
0	0	**1**	**0**	**1**	**0**	**1**
0	1	**0**	**0**	**1**	**0**	**1**
1	0	**0**	**1**	**0**	**0**	**0**
1	1	**1**	**0**	**1**	**1**	**1**

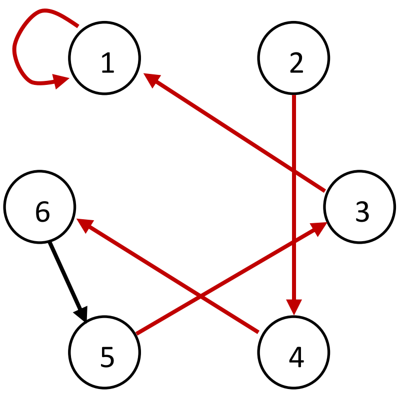


(b) After 3 clock cycles, the circuit is in state 1, and it generated 100 as output.
(c) There are 2 sinks: states 1 and 3.
(d) State 3 is likely to be an unused state.

2. [AY2021/22 Semester 2 Exam]
A sequential circuit with 6 states: state 1 (ABC=001_2) through state 6 (ABC=110_2) is implemented using three *JK* flip-flops as shown below.



(a) Complete the state diagram below. One of the transitions has been drawn for you.



(b) A circuit is **self-correcting** if for some reason the circuit enters into any unused (invalid) state, it is able to transit to a valid state after a finite number of transitions.
Is this circuit self-correcting? Explain.

Answer: Yes, it is self-correcting. State 0 transits to state 4 and state 7 transits to state 1.

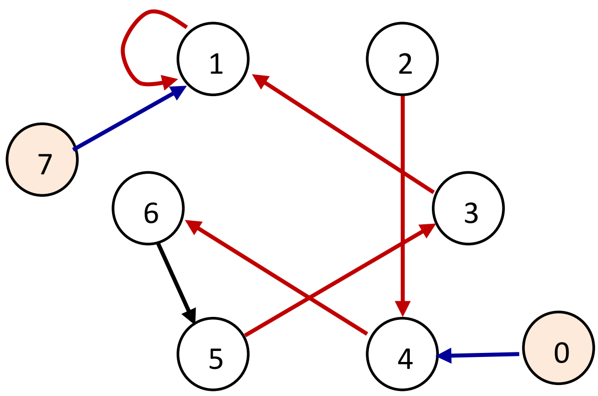
Working:

(a) $JA = C'$; $KA = C$; $JB = A$; $KB = 1$; $JC = A \cdot B$; $KC = 0$.

Fill in the flip-flop inputs in the state table using the above expressions, then find the values of A^+, B^+, and C^+.

Present state			Next state			Flip-flop inputs					
A	B	C	A^+	B^+	C^+	$JA=C'$	$KA=C$	$JB=A$	$KB=1$	$JC=A \cdot B$	$KC=0$
0	0	0	1	0	0	1	0	0	1	0	0
0	0	1	0	0	1	0	1	0	1	0	0
0	1	0	1	0	0	1	0	0	1	0	0
0	1	1	0	0	1	0	1	0	1	0	0
1	0	0	1	1	0	1	0	1	1	0	0
1	0	1	0	1	1	0	1	1	1	0	0
1	1	0	1	0	1	1	0	1	1	1	0
1	1	1	0	0	1	0	1	1	1	1	0

State diagram with unused states 0 and 7.



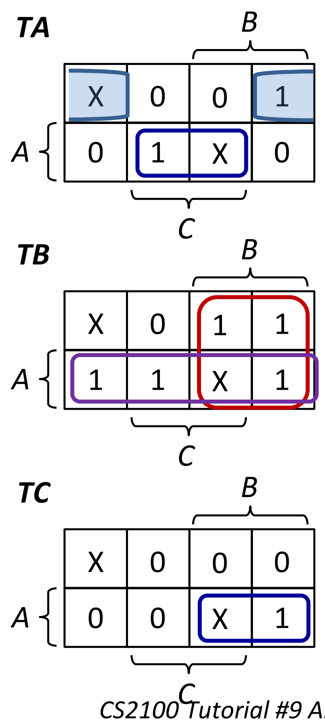
3. [AY2021/22 Semester 2 Exam]
Redesign the circuit in question 2 by using only ***T* flip-flops**. You do not have to follow where the unused states transit to in question 2. Write out the flip-flop input functions TA, TB and TC so that your new design can be implemented with the fewest number of logic gates other than the flip-flops.

Answers: 3 logic gates (XNOR, OR, AND)

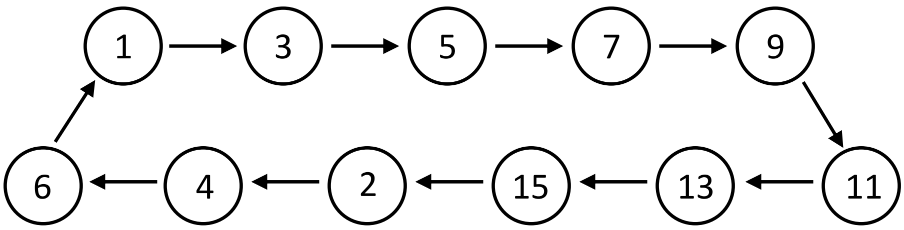
$TA = A \cdot C + A' \cdot C' = A \odot C$
$TB = A + B$
$TC = A \cdot B$

Working:

Present state			Next state			Flip-flop inputs		
A	B	C	A^+	B^+	C^+	TA	TB	TC
0	0	0	X	X	X	X	X	X
0	0	1	0	0	1	0	0	0
0	1	0	1	0	0	1	1	0
0	1	1	0	0	1	0	1	0
1	0	0	1	1	0	0	1	0
1	0	1	0	1	1	1	1	0
1	1	0	1	0	1	0	1	1
1	1	1	X	X	X	X	X	X



4. [AY2018/19 Semester 2 exam]
A sequential circuit goes through the following states, whose state values are shown in decimal:

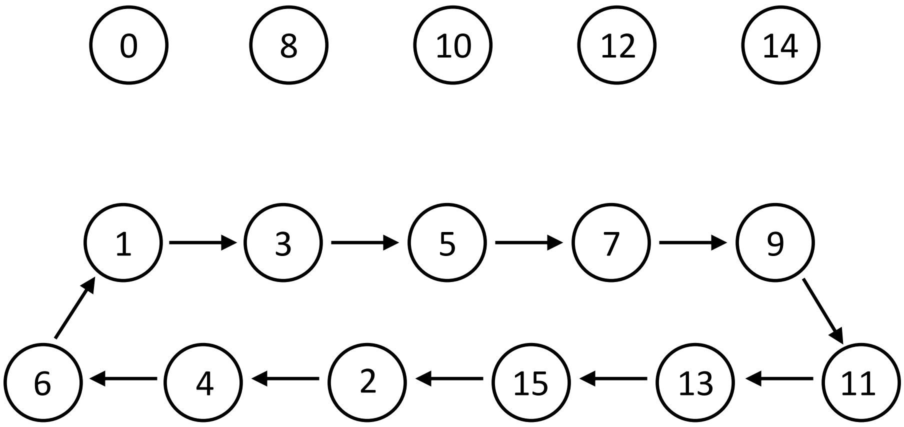


The states are represented by 4-bit values *ABCD*. Implement the sequential circuit using a *D* flip-flop for *A*, *T* flip-flops for *B* and *C*, and a *JK* flip-flop for *D*.

(a) Write out the **simplified SOP expressions** for all the flip-flop inputs.

(b) Implement your circuit according to your simplified SOP expressions obtained in part (a). Complete the given state diagram, by indicating the next state for each of the five unused states.

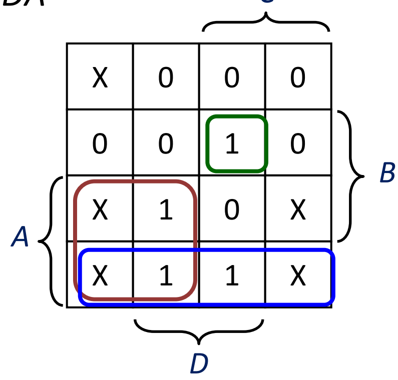
(c) Is your circuit self-correcting? Why?



Answers:

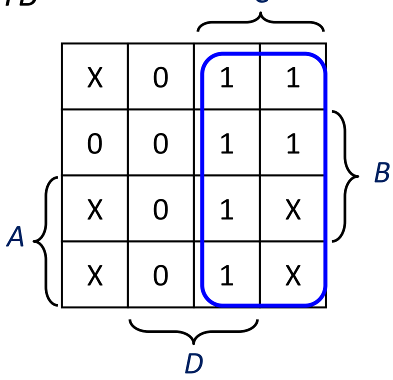
Current state				Next state							
A	*B*	*C*	*D*	*DA*=*A*⁺	*B*⁺	*C*⁺	*D*⁺	*TB*	*TC*	*JD*	*KD*
0	0	0	0	X(0)	X(0)	X(1)	X(0)	X(0)	X(1)	X(0)	X(0)
0	0	0	1	0	0	1	1	0	1	X	0
0	0	1	0	0	1	0	0	1	1	0	X
0	0	1	1	0	1	0	1	1	1	X	0
0	1	0	0	0	1	1	0	0	1	0	X
0	1	0	1	0	1	1	1	0	1	X	0
0	1	1	0	0	0	0	1	1	1	1	X
0	1	1	1	1	0	0	1	1	1	X	0
1	0	0	0	X(1)	X(0)	X(1)	X(0)	X(0)	X(1)	X(0)	X(0)
1	0	0	1	1	0	1	1	0	1	X	0
1	0	1	0	X(1)	X(1)	X(0)	X(0)	X(1)	X(1)	X(0)	X(0)
1	0	1	1	1	1	0	1	1	1	X	0
1	1	0	0	X(1)	X(1)	X(1)	X(0)	X(0)	X(1)	X(0)	X(0)
1	1	0	1	1	1	1	1	0	1	X	0
1	1	1	0	X(0)	X(0)	X(1)	X(1)	X(1)	X(0)	X(1)	X(1)
1	1	1	1	0	0	1	0	1	0	X	1

DA



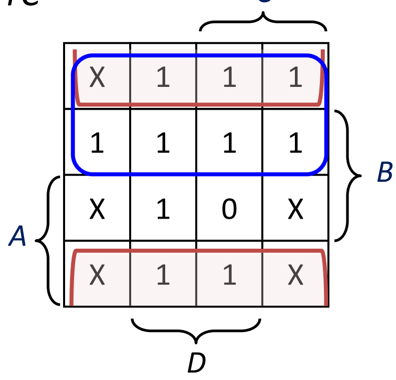
DA = *A*·*B*' + *A*·*C*' +*A*'·*B*·*C*·*D*

TB



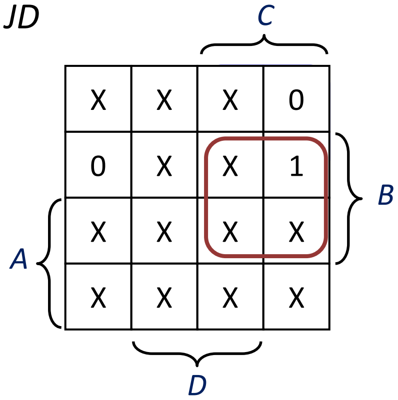
TB = *C*

TC



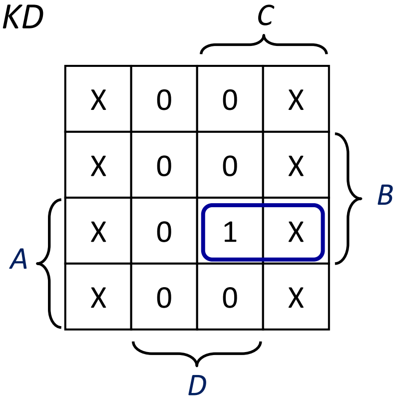
TC = *A*' + *B*' + *C*'

JD



JD = *B*·*C*

KD



KD = *A*·*B*·*C*

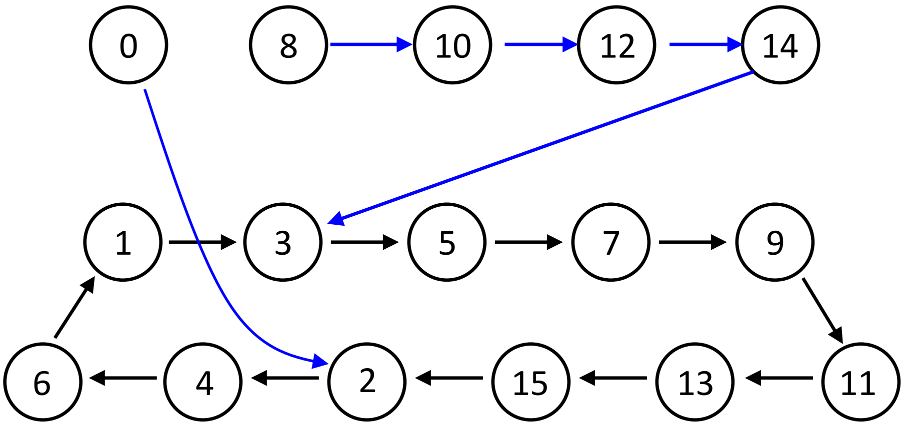
$DA = A \cdot B' + A \cdot C' + A' \cdot B \cdot C \cdot D$

$TB = C$

$TC = A' + B' + C'$

$JD = B \cdot C$

$KD = A \cdot B \cdot C$



The circuit is self-correcting as any unused state can transit to a used state after a finite number of cycles.