

CS2100 Tutorial 8

MSI Components

Recap

- Decoders and Encoders
- Multiplexers and Demultiplexers
- Half adders, Full-adders, Multi-bit adders

Overview

Q1) Using multiplexers

Q2) Implementing boolean functions with decoders

Q3) [Past paper] Block-level design

Q4) [Past paper] Equivalent gate

Q5) [Past paper] Finding boolean function from diagram

Q1) Using multiplexers

<i>X</i>	<i>Y</i>	<i>Z</i>	<i>F</i>
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	<i>d</i>
1	0	1	0
1	1	0	0
1	1	1	1

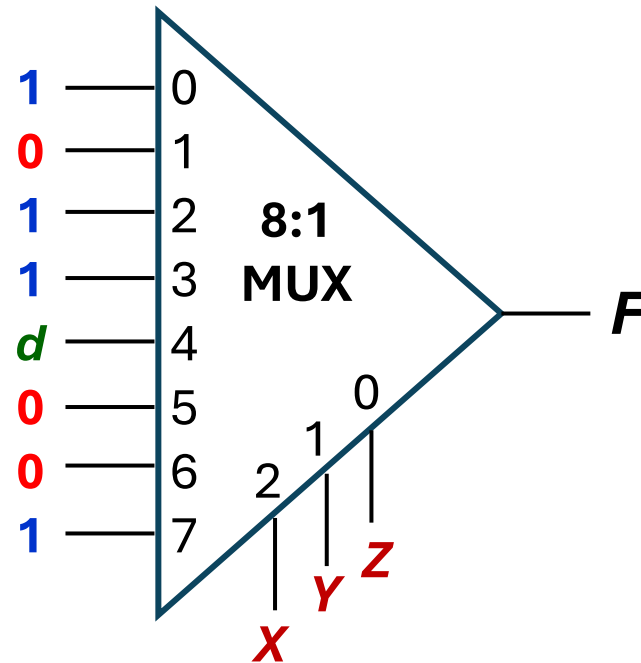
$$F(X,Y,Z) = \Pi M(1,5,6) \cdot D(4)$$

Note:

Using *d* instead of *X* for don't care to avoid confusion with input *X*.

Q1) Using multiplexers

<i>X</i>	<i>Y</i>	<i>Z</i>	<i>F</i>
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	<i>d</i>
1	0	1	0
1	1	0	0
1	1	1	1

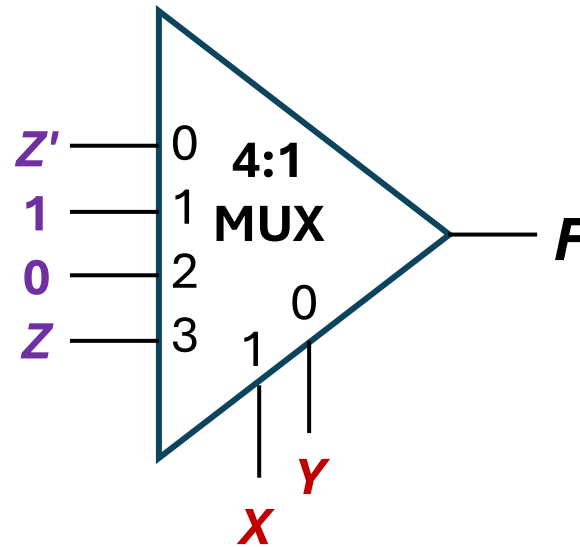


$$F(X,Y,Z) = \prod M(1,5,6) \cdot D(4)$$

Q1) Using multiplexers

<i>X</i>	<i>Y</i>	<i>Z</i>	<i>F</i>	<i>F</i>
0	0	0	1	<i>Z'</i>
0	0	1	0	
0	1	0	1	1
0	1	1	1	
1	0	0	<i>d</i>	0 or <i>Z'</i>
1	0	1	0	
1	1	0	0	<i>Z</i>
1	1	1	1	

$$F(X,Y,Z) = \prod M(1,5,6) \cdot D(4)$$

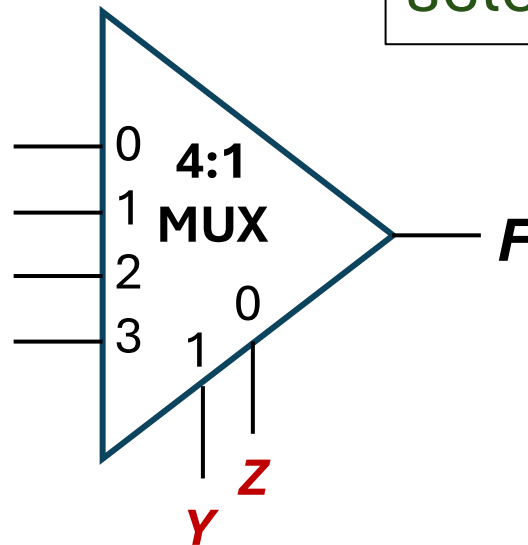


Q1) Using multiplexers

$$F(X,Y,Z) = \prod M(1,5,6) \cdot D(4)$$

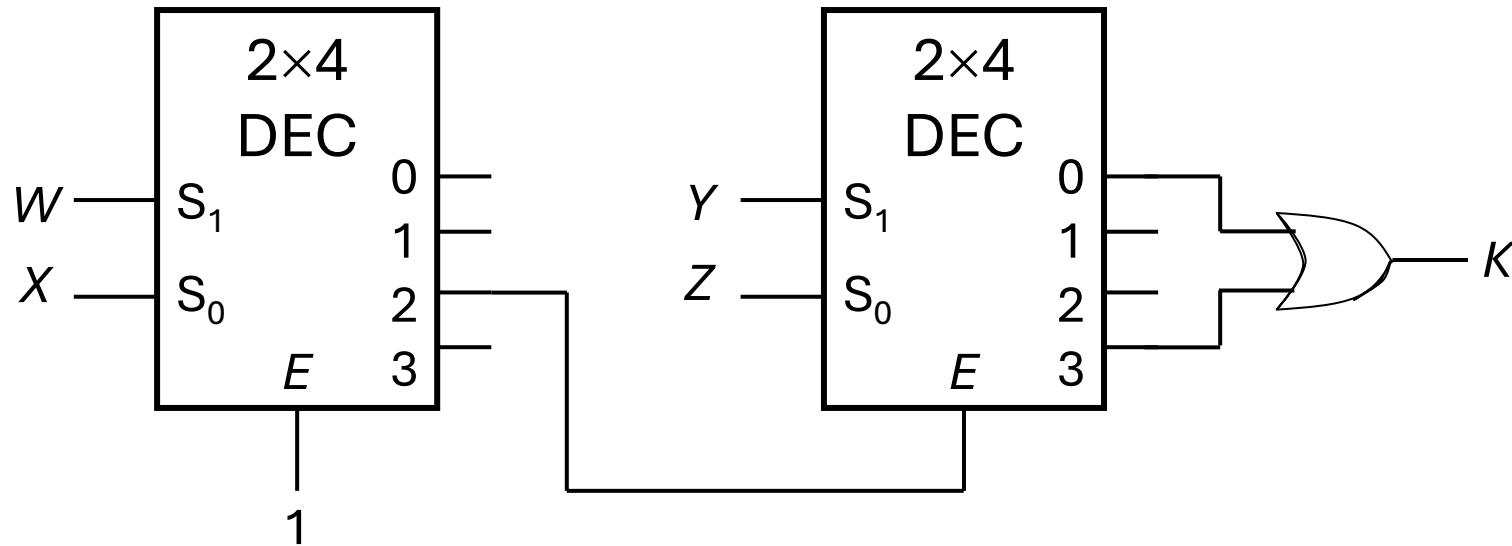
<i>X</i>	<i>Y</i>	<i>Z</i>	<i>F</i>	<i>F</i>
0	0	0	1	<i>Z'</i>
0	0	1	0	
0	1	0	1	1
0	1	1	1	
1	0	0	<i>d</i>	0 or <i>Z'</i>
1	0	1	0	
1	1	0	0	<i>Z</i>
1	1	1	1	

Extra question:
What if we change the
selector lines to *YZ*?



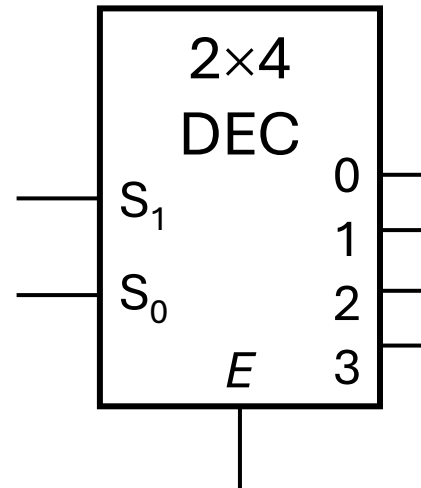
Q2) Is there a simpler circuit?

$$K(W,X,Y,Z) = \Sigma m(8,11)$$



Q2) Is there a simpler circuit?

$$K(W,X,Y,Z) = \Sigma m(8,11)$$



Q3. Designing converter

<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>	<i>F</i>	<i>G</i>	<i>H</i>
0	0	0	0	0	0	0
1	0	0	0	0	0	1
1	1	0	0	0	1	0
1	1	1	0	0	1	1
1	1	1	1	1	0	0
0	1	1	1	1	0	1
0	0	1	1	1	1	0
0	0	0	1	1	1	1

What is your observation?

Ideas:

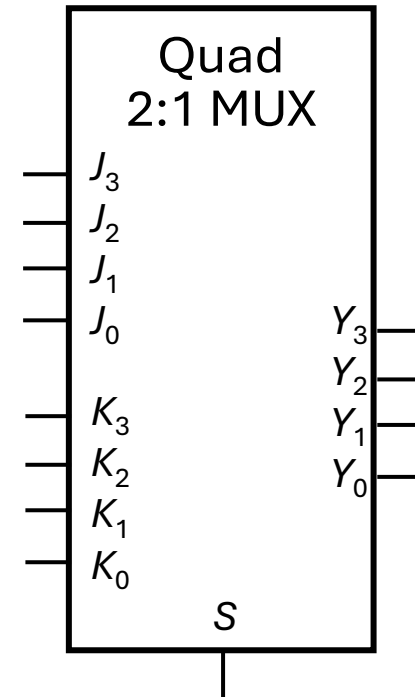
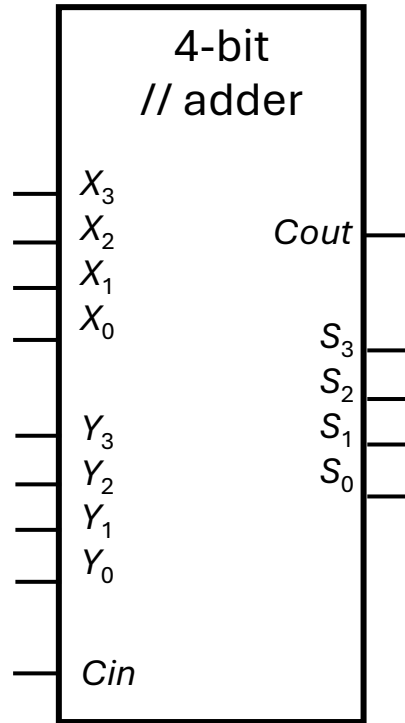
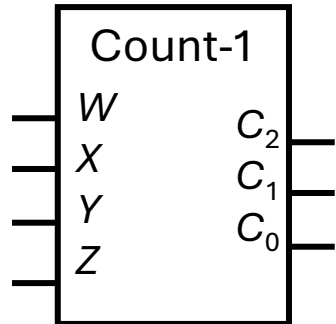
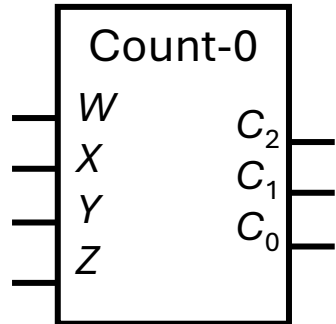
1. If $A=1$ (or $D=0$), count #1s in $ABCD$.
2. If $A=0$...?

A	B	C	D	F	G	H
0	0	0	0	0	0	0
1	0	0	0	0	0	1
1	1	0	0	0	1	0
1	1	1	0	0	1	1
1	1	1	1	1	0	0
0	1	1	1	1	0	1
0	0	1	1	1	1	0
0	0	0	1	1	1	1

Solution #1

Ideas:

1. If $A=1$ (or $D=0$), count #1s in $ABCD$.
2. If $A=0$ (or $D=1$), $4 + \#0$ s.

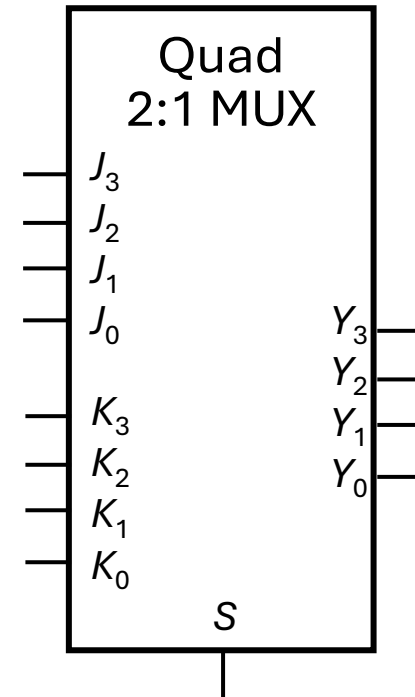
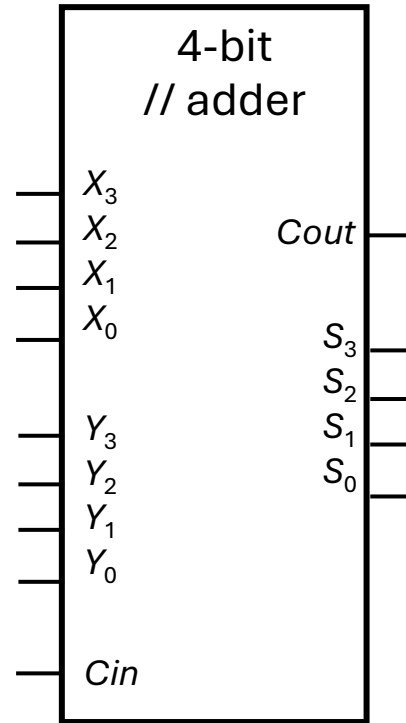
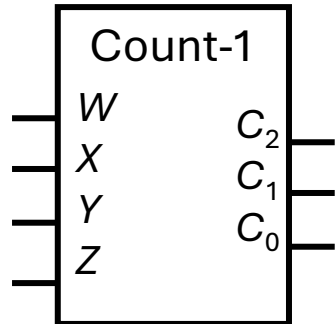
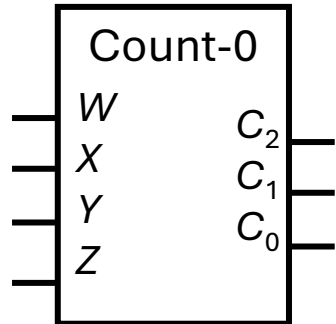


A	B	C	D	F	G	H
0	0	0	0	0	0	0
1	0	0	0	0	0	1
1	1	0	0	0	1	0
1	1	1	0	0	1	1
1	1	1	1	1	0	0
0	1	1	1	1	0	1
0	0	1	1	1	1	0
0	0	0	1	1	1	1

Solution #2

Ideas:

1. If $A=1$ (or $D=0$), count #1s in $ABCD$.
2. If $A=0$ (or $D=1$), $\#1s + 2 \times \#0s$.

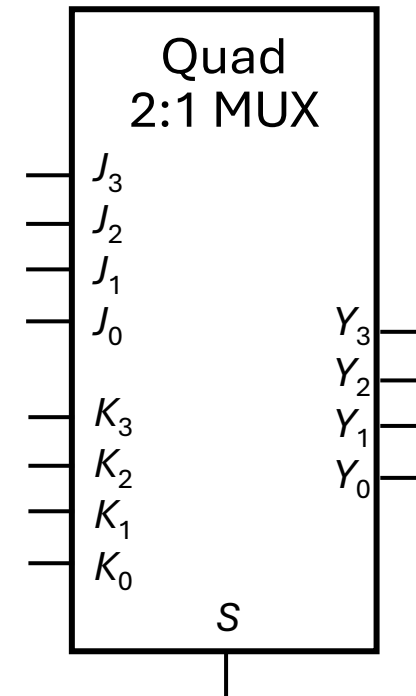
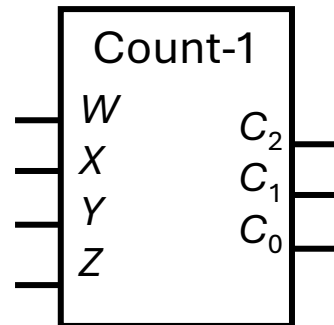
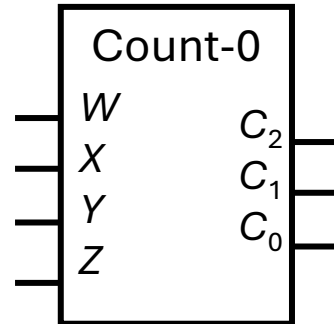


A	B	C	D	F	G	H
0	0	0	0	0	0	0
1	0	0	0	0	0	1
1	1	0	0	0	1	0
1	1	1	0	0	1	1
1	1	1	1	1	0	0
0	1	1	1	1	0	1
0	0	1	1	1	1	0
0	0	0	1	1	1	1

Solution #3

Ideas:

1. $D = F$
2. If $D = 0$, $GH = \#1\text{s}$ in ABCD
3. If $D = 1$, $GH = \#0\text{s}$ in ABCD

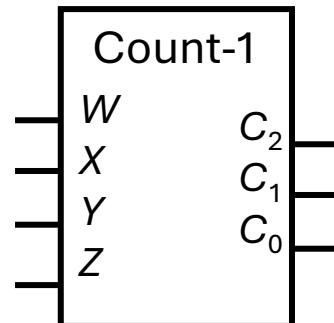
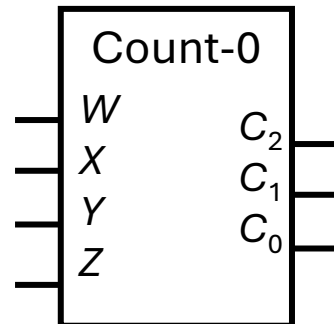


A	B	C	D	F	G	H
0	0	0	0	0	0	0
1	0	0	0	0	0	1
1	1	0	0	0	1	0
1	1	1	0	0	1	1
1	1	1	1	1	0	0
0	1	1	1	1	0	1
0	0	1	1	1	1	0
0	0	0	1	1	1	1

Solution #4

Ideas:

1. $F = D$
2. $G = \text{LSB of \#1s in BD}$
3. $H = \text{LSB of \#0s in ABCD}$

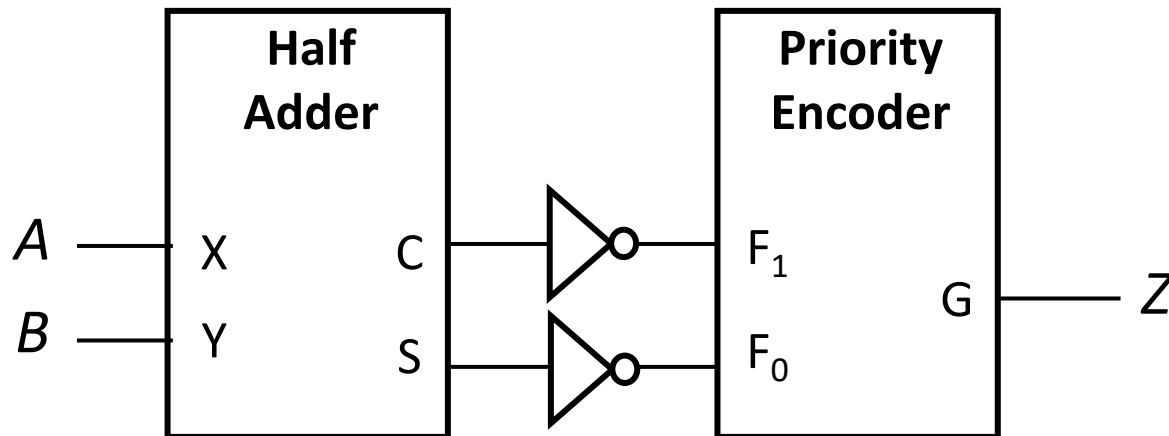


Q4. Equivalent logic gate

NAND gate

A Boolean function $Z(A,B)$ is implemented as shown below.

The circuit may be replaced by a single 2-input logic gate. What is the logic gate?



Half-adder

X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Priority encoder

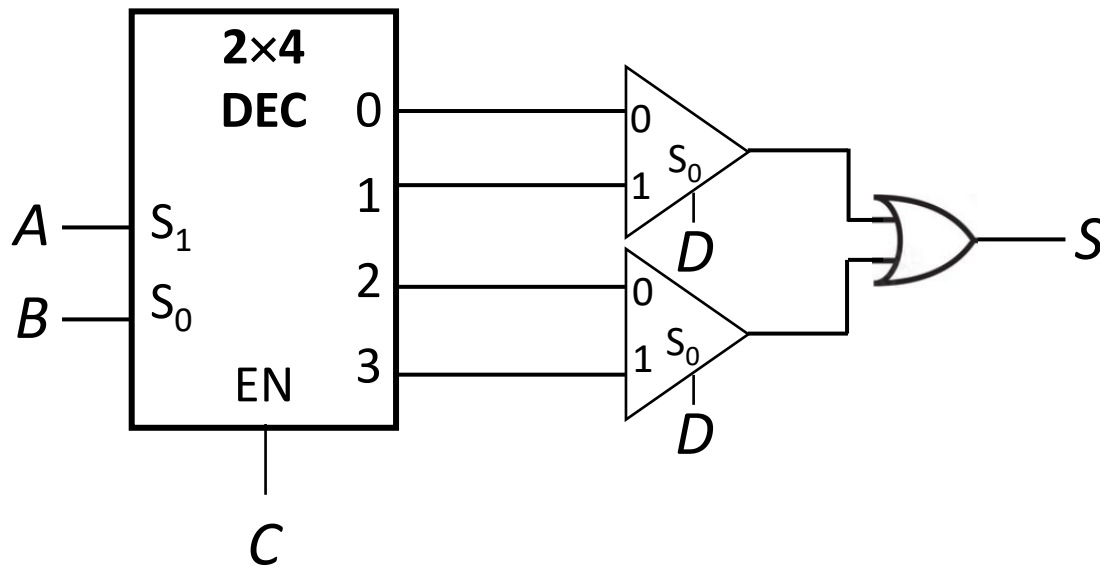
F ₁	F ₀	G
0	0	X
0	1	0
1	X	1

X	Y	C	S	F ₁	F ₀	G
0	0	0	0	1	1	1
0	1	0	1	1	0	1
1	0	0	1	1	0	1
1	1	1	0	0	1	0

Q5. Finding boolean fn from diagram

A Boolean function $S(A,B,C,D)$ is implemented with a 2×4 decoder with one-enable, two $2:1$ multiplexers and an OR gate as shown below.

What is $S(A,B,C,D)$ in Σm notation?



$$S(A,B,C,D) = \Sigma m(2,7,10,15).$$

End of Tutorial 8

- Slides uploaded on github.com/theodoreleebrant/TA-2425S1
- Email: theo@comp.nus.edu.sg
- Anonymous feedback:
bit.ly/feedback-theodore
(or scan on the right)



(Also reminder for me to take attendance)