8.5 Programming

8.5.1 I²C Communication

The I²C interface allows control and monitoring of the DRV8214 by a microcontroller. The I²C bus consists of a data line (SDA) and a clock line (SCL) with off-chip pull-up resistors. When the bus is idle, both SDA and SCL lines are pulled high.

A leader device, usually a microcontroller or a digital signal processor, controls the bus. The leader is responsible for generating the SCL signal and device addresses. The leader also generates specific conditions that indicate the START and STOP of data transfer. A follower device receives and/or transmits data on the bus under control of the leader device. DRV8214 is a follower device.

The lower four bits of the device address are derived from the inputs from the pins A1 and A0, which can be tied to VCC (logic high), GND (logic low), or left open. These four address bits are latched into the device at power up, so cannot be changed dynamically. The upper address bits of the device address are fixed at 0x60h, so the device address is as follows -

Table 8-28. Device Addresses

A1 Pin	A0 Pin	A3A2A1A0 bits	ADDRESS (WRITE)	ADDRESS (READ)
0	0	0000b	0x60h	0x61h
0	High-Z	0001b	0x62h	0x63h
0	1	0010b	0x64h	0x65h
High-Z	0	0011b	0x66h	0x67h
High-Z	High-Z	0100b	0x68h	0x69h
High-Z	1	0101b	0x6Ah	0x6Bh
1	0	0110b	0x6Ch	0x6Dh
1	High-Z	0111b	0x6Eh	0x6Fh
1	1	1000b	0x70h	0x71h

Using the A0 and A1 pins, up to 9 DRV8214 follower devices can be controlled by one I²C bus. The DRV8214 does not respond to the general call address. It is recommended to use a 2.2kΩ pull-up resistor for these pins.

8.5.1.1 I²C Write

To write on the I²C bus, the leader device sends a START condition on the bus with the address of the 7-bit follower device. Also, the last bit (the R/W bit) is set to 0b, which signifies a write. After the follower sends the acknowledge bit, the leader device then sends the register address of the register to be written. The follower device sends an acknowledge (ACK) signal again which notifies the leader device that the follower device is ready. After this process, the leader device sends 8-bit write data and terminates the transmission with a STOP condition.

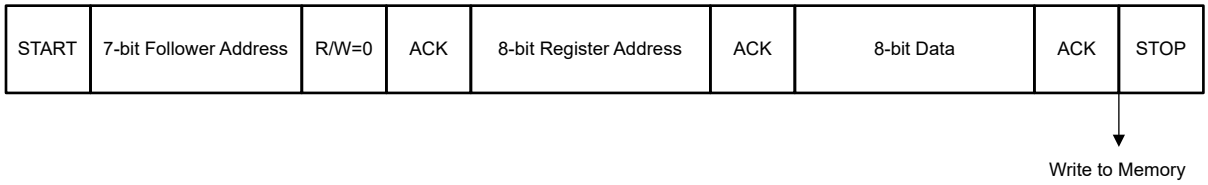

Figure 8-20. I²C Write Sequence

8.5.1.2 I²C Read

To read from a follower device, the leader device must first communicate to the follower device which register will be read from. This communication is done by the leader starting the transmission similarly to the write process which is by setting the address with the R/W bit equal to 0b (signifying a write). The leader device then sends the

register address of the register to be read from. When the follower device acknowledges this register address, the leader device sends a START condition again, followed by the follower address with the R/W bit set to 1b (signifying a read). After this process, the follower device acknowledges the read request and the leader device releases the SDA bus, but continues supplying the clock to the follower device.

During this part of the transaction, the leader device becomes the leader-receiver, and the follower device becomes the follower-transmitter. The leader device continues sending out the clock pulses, but releases the SDA line so that the follower device can transmit data. At the end of the byte, the leader device sends a negative-acknowledge (NACK) signal, signaling to the follower device to stop communications and release the bus. The leader device then sends a STOP condition.

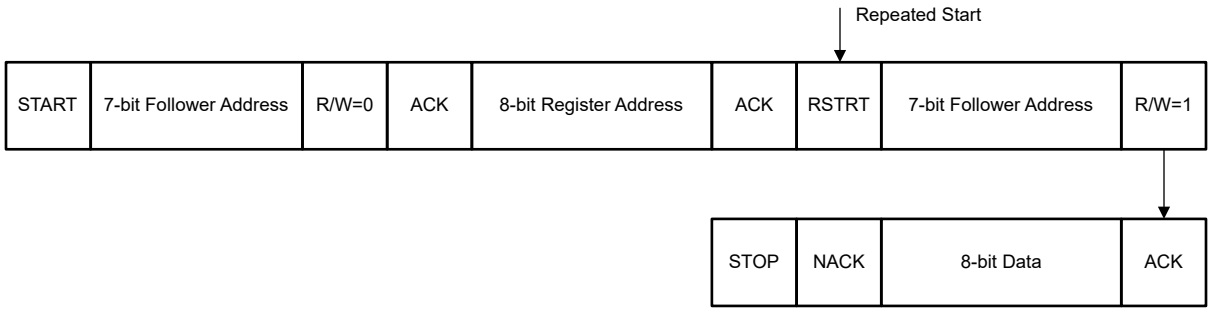

Figure 8-21. I²C Read Sequence

8.6 Register Map

The following table lists the memory-mapped I²C registers for the DRV8214. The I²C registers are used to configure the DRV8214 and for device diagnostics.

Note

Do not modify reserved registers or addresses not listed in the register map (Table 8-29). Writing to these registers can have unintended effects. For all reserved bits, the default value is 0b.

Table 8-29. I²C Registers

Address	Name	7	6	5	4	3	2	1	0	Access
0x00	FAULT	FAULT	RSVD	STALL	OCP	OVP	TSD	NPOR	CNT_DONE	R
0x01	RC_STATUS1	SPEED[7:0]								R
0x02	RC_STATUS2	RC_CNT[7:0]								R
0x03	RC_STATUS3	RC_CNT[15:8]								R
0x04	REG_STATUS1	VMTR[7:0]								R
0x05	REG_STATUS2	IMTR[7:0]								R
0x06	REG_STATUS3	RSVD		IN_DUTY[5:0]						R
0x09	CONFIG0	EN_OUT	EN_OVP	EN_STALL	VSNS_SEL*	VM_GAIN_SEL*	CLR_CNT	CLR_FLT	DUTY_CTRL*	RW
0x0A	CONFIG1	TINRUSH[7:0]								RW
0x0B	CONFIG2	TINRUSH[15:8]								RW
0x0C	CONFIG3	IMODE[1:0]*		SMODE*	INT_VREF*	TBLANK*	TDEG*	OCP_MODE*	TSD_MODE*	RW
0x0D	CONFIG4	RC_REP[1:0]		STALL_REP	CBC_REP	PMODE*	I2C_BC*	I2C_EN_IN1	I2C_PH_IN2	RW

Table 8-29. I²C Registers (continued)

Address	Name	7	6	5	4	3	2	1	0	Access
0x0E	REG_CTRL0	RSVD		EN_SS	REG_CTRL[1:0]*		PWM_FREQ*	W_SCALE[1:0]		RW
0x0F	REG_CTRL1	WSET_VSET[7:0]								RW
0x10	REG_CTRL2	OUT_FLT[1:0]		EXT_DUTY[5:0]						RW
0x11	RC_CTRL0	EN_RC	DIS_EC	RC_HIZ	FLT_GAIN_SEL[1:0]		CS_GAIN_SEL[2:0]			RW
0x12	RC_CTRL1	RC_THR[7:0]								RW
0x13	RC_CTRL2	INV_R_SCALE[1:0]		KMC_SCALE[1:0]		RC_THR_SCALE[1:0]		RC_THR[9:8]		RW
0x14	RC_CTRL3	INV_R[7:0]								RW
0x15	RC_CTRL4	KMC[7:0]								RW
0x16	RC_CTRL5	FLT_K[3:0]				RSVD				RW
0x17	RC_CTRL6	EC_PULSE_DIS	T_MECH_FLT			EC_FALSE_PER		EC_MISS_PER		RW
0x18	RC_CTRL7	KP_DIV[2:0]			KP[4:0]					RW
0x19	RC_CTRL8	KI_DIV[2:0]			KI[4:0]					RW

Note

*Writable only when EN_OUT=0.

Table 8-30. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1 DRV8214_STATUS Registers

Table 8-31 lists the memory-mapped registers for the DRV8214_STATUS registers. All register offset addresses not listed in Table 8-31 should be considered as reserved locations and the register contents should not be modified.

Table 8-31. DRV8214_STATUS Registers

Offset	Acronym	Register Name	Section
0h	FAULT	Various fault registers' status.	Section 8.6.1.1
1h	RC_STATUS1	Ripple Counting Status Registers - 1.	Section 8.6.1.2
2h	RC_STATUS2	Ripple Counting Status Registers - 2.	Section 8.6.1.3
3h	RC_STATUS3	Ripple Counting Status Registers - 3.	Section 8.6.1.4
4h	REG_STATUS1	Regulation Status Registers - (1/3).	Section 8.6.1.5
5h	REG_STATUS2	Regulation Status Registers - (2/3).	Section 8.6.1.6
6h	REG_STATUS3	Regulation Status Registers - (3/3).	Section 8.6.1.7

Complex bit access types are encoded to fit into small table cells. Table 8-32 shows the codes that are used for access types in this section.

Table 8-32. DRV8214_STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.1 FAULT Register (Offset = 0h) [Reset = 00h]

FAULT is shown in Table 8-33.

Return to the Summary Table.

Status of various fault and protection bits.

Table 8-33. FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FAULT	R	0h	0b during normal operation, 1b during a fault condition. nFAULT pin is pulled down when FAULT bit is 1b. nFAULT pin is released during normal operation.
6	RSVD	R	0h	Reserved.
5	STALL	R	0h	When this bit is 1b, it indicates motor stall.
4	OCP	R	0h	0b during normal operation, 1b if OCP event occurs.
3	OVP	R	0h	0b during normal operation, 1b if OVP event occurs.
2	TSD	R	0h	0b during normal operation, 1b if TSD event occurs.
1	NPOR	R	0h	Reset and latched low if VCC>VUVLO. Remains reset until the CLR_FLT bit is set to issue a clear fault command. After power up, automatically latched high once CLR_FLT command is issued. Refer to Section 8.3.8.3 for further explanation.
0	CNT_DONE	R	0h	Status flag. Latched high when RC_CNT exceeds the ripple counting threshold. Can be cleared by CLR_CNT command.

8.6.1.2 RC_STATUS1 Register (Offset = 1h) [Reset = 00h]

RC_STATUS1 is shown in Table 8-34.

Return to the Summary Table.

Speed estimated by the ripple counting algorithm.

Table 8-34. RC_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SPEED	R	0h	Outputs the motor speed estimated by the ripple counting algorithm.

8.6.1.3 RC_STATUS2 Register (Offset = 2h) [Reset = 00h]

RC_STATUS2 is shown in Table 8-35.

Return to the Summary Table.

Output corresponding to number of current ripples (1/2).

Table 8-35. RC_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RC_CNT_7:0	R	0h	Lower half 8-bit output out of the 16-bit output of the ripple counter corresponding to the number of current ripples.

8.6.1.4 RC_STATUS3 Register (Offset = 3h) [Reset = 00h]

RC_STATUS3 is shown in Table 8-36.

Return to the Summary Table.

Output corresponding to number of current ripples (2/2).

Table 8-36. RC_STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RC_CNT_15:8	R	0h	Upper half 8-bit output out of the 16-bit output of the ripple counter corresponding to the number of current ripples.

8.6.1.5 REG_STATUS1 Register (Offset = 4h) [Reset = 00h]

REG_STATUS1 is shown in Table 8-37.

Return to the Summary Table.

Value corresponding to the output voltage across the motor terminals.

Table 8-37. REG_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VMTR	R	0h	Outputs the voltage across the motor terminals, maximum value FFh. 00h corresponds to 0 V and B0h corresponds to 11 V.

8.6.1.6 REG_STATUS2 Register (Offset = 5h) [Reset = 00h]

REG_STATUS2 is shown in Table 8-38.

Return to the Summary Table.

Output corresponding to current flowing through the motor.

Table 8-38. REG_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IMTR	R	0h	Outputs the current flowing through the motor. 00h corresponds to 0 A and C0h corresponds to the maximum value set by the CS_GAIN_SEL bits.

8.6.1.7 REG_STATUS3 Register (Offset = 6h) [Reset = 00h]

REG_STATUS3 is shown in Table 8-39.

Return to the Summary Table.

Internal pwm duty cycle and device id.

Table 8-39. REG_STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	0h	Reserved.
5-0	IN_DUTY	R	0h	Represents the bridge control duty cycle generated by an internal regulation logic. This register is applicable when speed or voltage regulation is activated. When speed or voltage regulation is inactive, set DUTY_CTRL to 1b and program the duty cycle in EXT_DUTY explained later. The range of duty cycle is 0% (000000b) to 100% (111111b). Refer to Section 8.3.7 for further explanation on the internal PWM generation scheme.

8.6.2 DRV8214_CONFIG Registers

Table 8-40 lists the memory-mapped registers for the DRV8214_CONFIG registers. All register offset addresses not listed in Table 8-40 should be considered as reserved locations and the register contents should not be modified.

Table 8-40. DRV8214_CONFIG Registers

Offset	Acronym	Register Name	Section
9h	CONFIG0	Configuration Registers - Faults (1/5).	Section 8.6.2.1
Ah	CONFIG1	Configuration Registers - (2/5).	Section 8.6.2.2
Bh	CONFIG2	Configuration Registers - (3/5).	Section 8.6.2.3
Ch	CONFIG3	Configuration Registers - (4/5).	Section 8.6.2.4
Dh	CONFIG4	Configuration Registers - (5/5).	Section 8.6.2.5

Complex bit access types are encoded to fit into small table cells. Table 8-41 shows the codes that are used for access types in this section.

Table 8-41. DRV8214_CONFIG Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.1 CONFIG0 Register (Offset = 9h) [Reset = 60h]

CONFIG0 is shown in Table 8-42.

Return to the Summary Table.

Enable/Disable various faults like OCP, OVP, STALL, etc.

Table 8-42. CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_OUT	R/W	0h	0b: All driver FETs are Hi-Z. 1b: Enables the driver outputs.
6	EN_OVP	R/W	1h	Enables the OVP feature. 1b by default, can be made 0b after power-up to disable the OVP feature. Refer to Section 8.3.8.1 for further explanation.
5	EN_STALL	R/W	1h	Enables the Stall Detection feature. Stall detection feature can be disabled by setting this bit to 0b. Refer to EN_STALL configuration under Section 8.3.5 for further explanation.
4	VSNS_SEL	R/W	0h	0b: Use the analog low-pass filter to average out the output voltage for voltage regulation. Refer to OUT_FLT for further description of the analog low-pass filter. 0b is the recommended value. 1b: Use the digital low-pass filter for voltage regulation. This option perfroms multiplication of the duty cycle with VM to obtain the output voltage.
3	VM_GAIN_SEL	R/W	0h	Selects the voltage range for better resolution during voltage regulation for smaller voltages. 0b: Voltage range is 0V - 15.7V. 1b: Voltage range is 0V - 3.92V. Refer to Section 8.3.7.2.1 for further explanation.
2	CLR_CNT	R/W	0h	Resets the ripple counter to 0, and resets CNT_DONE. Also releases nFAULT when RC_REP = 10b. CLR_CNT is automatically reset.
1	CLR_FLT	R/W	0h	Clears all latched faults when set to 1b. CLR_FLT is automatically reset.
0	DUTY_CTRL	R/W	0h	When speed regulation is disabled and the DUTY_CTRL bit is 1b, user can write desired PWM duty to EXT_DUTY bits. The range of duty is 0% (000000b) to 100% (111111b).

8.6.2.2 CONFIG1 Register (Offset = Ah) [Reset = 00h]

CONFIG1 is shown in Table 8-43.

Return to the Summary Table.

Configure the inrush time (1/2).

Table 8-43. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TINRUSH_7:0	R/W	0h	Lower half 8-bit output out of the total 16-bit output for inrush time blanking for stall detection. Sets the amount of time for which the stall detection scheme ignores motor inrush current. Refer to Section 8.3.7.3.1 for further explanation.

8.6.2.3 CONFIG2 Register (Offset = Bh) [Reset = 00h]

CONFIG2 is shown in Table 8-44.

Return to the Summary Table.

Configure the inrush time (2/2).

Table 8-44. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TINRUSH_15:8	R/W	0h	Upper half 8-bit output out of the total 16-bit output for inrush time blanking for stall detection. Sets the amount of time for which the stall detection scheme ignores motor inrush current. Refer to Section 8.3.7.3.1 for further explanation.

8.6.2.4 CONFIG3 Register (Offset = Ch) [Reset = 63h]

CONFIG3 is shown in Table 8-45.

Return to the Summary Table.

Enable/Disable various device modes like IMODE, SMODE and parameters like blanking time.

Table 8-45. CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	IMODE	R/W	1h	Determines the behavior of current regulation. Refer to IMODE configuration under Section 8.3.4.2 for further explanation.
5	SMODE	R/W	1h	Programs device response to a stall condition. Refer to SMODE configuration under Section 8.3.5 for further explanation.
4	INT_VREF	R/W	0h	If set to 1b, sets VREF voltage to 500mV internally. Voltage is not fixed if INT_VREF is set to 0b. Refer to Section 8.3.5 for further explanation.
3	TBLANK	R/W	0h	Sets the current sense blanking time. If set to 0b, t_{BLANK}=1.8µs. If set to 1b, t_{BLANK}=1.0µs.
2	TDEG	R/W	0h	Sets the current regulation and stall detection deglitch time. If set to 0b, t_{DEG}=2µs. If set to 1b, t_{DEG}=1µs.
1	OCP_MODE	R/W	1h	Programs device response to an overcurrent event. If set to 0b, device is latched off in case of an OCP event. Can be cleared using CLR_FLT. If set to 1b, device performs auto-retry after time tretry in case of an OCP event. Refer to Section 8.3.8.1 for further explanation.
0	TSD_MODE	R/W	1h	Programs device response to an overtemperature event. If set to 0b, device is latched off in case of a TSD event. If set to 1b, device performs auto-retry when $T_J<T_{TSD}–T_{HYS}$.

8.6.2.5 CONFIG4 Register (Offset = Dh) [Reset = 38h]

CONFIG4 is shown in Table 8-46.

Return to the Summary Table.

Configure the report registers like RC_REP and STALL_REP.

Table 8-46. CONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RC_REP	R/W	0h	Determines whether nFAULT is pulled low when RC_CNT exceeds threshold, and the behavior of RC_CNT when it reaches maximum value of (2^{16}-1). Refer to RC_REP Settings under Section 8.3.6 for further explanation.
5	STALL_REP	R/W	1h	Determines whether stall is reported on the nFAULT pin. When set to 1b, nFAULT is low whenever stall is detected. When set to 0b, stall is not reported on nFAULT output. Refer to Section 8.3.5 for further explanation.
4	CBC_REP	R/W	1h	When REG_CTRL is set to 01b, the device enters cycle-by-cycle mode of current regulation. In this mode, the device can indicate whenever the H-bridge enters internal current regulation. CBC_REP bit is used to determine device outputs' behavior in the cycle-by-cycle mode. 1b: nFAULT is pulled low when H-Bridge enters internal current regulation. 0b: nFAULT is not pulled low when H-Bridge enters internal current regulation. Refer to Section 8.3.4.2.2 for further explanation.
3	PMODE	R/W	1h	Switch between phase/enable mode and PWM mode. 0b: PH/EN. 1b: PWM.
2	I2C_BC	R/W	0h	Decides the H-Bridge Control Interface. 0b: Bridge control configured by INx pins. 1b: Bridge control configured by I2C bits I2C_EN_IN1 and I2C_PH_IN2.
1	I2C_EN_IN1	R/W	0h	Enable/PWM Input Bit 1 for internal bridge control. Used when I2C_BC=1b. Ignored when I2C_BC=0b.
0	I2C_PH_IN2	R/W	0h	Phase/PWM Input Bit 2 for internal bridge control. Used when I2C_BC=1b.Ignored when I2C_BC=0b.

8.6.3 DRV8214_CTRL Registers

Table 8-47 lists the memory-mapped registers for the DRV8214_CTRL registers. All register offset addresses not listed in Table 8-47 should be considered as reserved locations and the register contents should not be modified.

Table 8-47. DRV8214_CTRL Registers

Offset	Acronym	Register Name	Section
Eh	REG_CTRL0	Regulation control registers (1/3).	Section 8.6.3.1
Fh	REG_CTRL1	Regulation control registers (2/3).	Section 8.6.3.2
10h	REG_CTRL2	Regulation control registers (3/3).	Section 8.6.3.3
11h	RC_CTRL0	Ripple Counting Control Registers - (1/9).	Section 8.6.3.4
12h	RC_CTRL1	Ripple Counting Control Registers - (2/9).	Section 8.6.3.5
13h	RC_CTRL2	Ripple Counting Control Registers - (3/9).	Section 8.6.3.6
14h	RC_CTRL3	Ripple Counting Control Registers - (4/9).	Section 8.6.3.7
15h	RC_CTRL4	Ripple Counting Control Registers - (5/9).	Section 8.6.3.8
16h	RC_CTRL5	Ripple Counting Control Registers - (6/9).	Section 8.6.3.9
17h	RC_CTRL6	Ripple Counting Control Registers - (7/9).	Section 8.6.3.10
18h	RC_CTRL7	Ripple Counting Control Registers - (8/9).	Section 8.6.3.11
19h	RC_CTRL8	Ripple Counting Control Registers - (9/9).	Section 8.6.3.12

Complex bit access types are encoded to fit into small table cells. Table 8-48 shows the codes that are used for access types in this section.

Table 8-48. DRV8214_CTRL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.3.1 REG_CTRL0 Register (Offset = Eh) [Reset = 27h]

REG_CTRL0 is shown in Table 8-49.

Return to the Summary Table.

Set features like Soft Start/Stop, speed scaling factor, etc.

Table 8-49. REG_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R/W	0h	Reserved.
5	EN_SS	R/W	1h	Used to enable/disable soft start/stop. 1b: Target motor voltage or speed is soft-started and soft-stopped over the duration of t_{INRUSH} time. 0b: Soft-start/stop feature is disabled. Refer to Section 8.3.7.3 for further explanation.
4-3	REG_CTRL	R/W	0h	Selects the current regulation scheme (fixed off-time or cycle-by-cycle) or motor speed and voltage regulation. 00b: Fixed Off-Time Current Regulation. 01b: Cycle-By-Cycle Current Regulation. 10b: Motor speed is regulated. Ripple counting must be enabled in this mode by setting EN_RC to 1b. 11b: Motor voltage is regulated. Refer to Section 8.3.4.2 for further explanation.
2	PWM_FREQ	R/W	1h	Sets the PWM frequency when bridge control is configured by INx bits (I2C_BC=1b). 0b: PWM frequency is set to 50kHz. 1b: PWM frequency is set to 25kHz.
1-0	W_SCALE	R/W	3h	Scaling factor that helps in setting the target ripple speed. 00b: 16 01b: 32 10b: 64 11b: 128 Refer to Section 8.3.7.2.2 for further explanation.

8.6.3.2 REG_CTRL1 Register (Offset = Fh) [Reset = FFh]

REG_CTRL1 is shown in Table 8-50.

Return to the Summary Table.

Set the target motor voltage and speed.

Table 8-50. REG_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WSET_VSET	R/W	FFh	Sets the target motor voltage or ripple speed. A detailed explanation is provided in Section 8.3.7.2.1.

8.6.3.3 REG_CTRL2 Register (Offset = 10h) [Reset = 00h]

REG_CTRL2 is shown in Table 8-51.

Return to the Summary Table.

Set the duty cycle and cut-off frequency for output voltage filtering.

Table 8-51. REG_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT_FLT	R/W	0h	Programs the cut-off frequency of the output voltage filtering. 00b: 250Hz 01b: 500Hz 10b: 750Hz 11b: 1000Hz For best results, choose a cut-off frequency equal to a value at least 20 times lower than the PWM frequency. Eg, if you PWM at 20kHz, OUT_FLT=11b (1000Hz) is sufficient.
5-0	EXT_DUTY	R/W	0h	Available when using external bridge control (I2C_BC=0b). DUTY_CTRL must be set to 1b. Speed and voltage regulation modes are inactive in this case. User can program the desired duty cycle in the EXT_DUTY bits. The range of duty cycle is 0% (000000b) to 100% (111111b).

8.6.3.4 RC_CTRL0 Register (Offset = 11h) [Reset = 88h]

RC_CTRL0 is shown in Table 8-52.

Return to the Summary Table.

Set various functions for RC including enable/disable.

Table 8-52. RC_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_RC	R/W	1h	Enable/Disable Ripple Counting. 0b: Disable 1b: Enable
6	DIS_EC	R/W	0h	Enable/Disable the Error Correction module. 0b: Error Correction is enabled. 1b: Error Correction is disabled. Please note that this is different from the EC_PULSE_DIS described earlier.
5	RC_HIZ	R/W	0h	0b: H-bridge stays enabled when RC_CNT exceeds threshold. 1b: H-bridge is disabled (High-Z) when RC_CNT exceeds threshold.
4-3	FLT_GAIN_SEL	R/W	1h	Filter input scaling factor. This factor scales the magnitude of current ripples for ease of detection and algorithmic calculation by the Ripple Counter. The options are: 00b: 2 01b: 4 10b: 8 11b: 16 Refer to Section 8.3.6.1.6 for further explanation.
2-0	CS_GAIN_SEL	R/W	0h	Used to select the current mirror gain, A_{IPROPI}. Settings are as follows: 000b: 4 A 001b: 2 A 010b: 1 A 011b: 0.5 A 1X0b: 0.25 A 1X1b: 0.125 A Refer to Section 8.3.4.1 for further explanation.

8.6.3.5 RC_CTRL1 Register (Offset = 12h) [Reset = FFh]

RC_CTRL1 is shown in Table 8-53.

Return to the Summary Table.

Threshold for ripple counting.

Table 8-53. RC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RC_THR	R/W	FFh	Lower 8 bits of the 10-bit RC_THR Register. Threshold level to compare against the RC_CNT based on the expected time of motor actuation. Ripple counting threshold = RC_THR x RC_THR_SCALE

8.6.3.6 RC_CTRL2 Register (Offset = 13h) [Reset = 7Fh]

RC_CTRL2 is shown in Table 8-54.

Return to the Summary Table.

Set values of various scaling parameters.

Table 8-54. RC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	INV_R_SCALE	R/W	1h	Scaling factor for the INV_R parameter. 00b: INV_R_SCALE = 2 01b: INV_R_SCALE = 64 10b: INV_R_SCALE = 1024 11b: INV_R_SCALE = 8192 Refer to Section 8.3.6.1.2 for further explanation.
5-4	KMC_SCALE	R/W	3h	Scaling factor for KMC parameter. 00b: KMC_SCALE = 24 x 2^8 01b: KMC_SCALE = 24 x 2^9 10b: KMC_SCALE = 24 x 2^{12} 11b: KMC_SCALE = 24 x 2^{13} Refer to Section 8.3.6.1.3 for further explanation.
3-2	RC_THR_SCALE	R/W	3h	Scaling factor for RC_THR. 00b: RC_THR_SCALE = 2 01b: RC_THR_SCALE = 8 10b: RC_THR_SCALE = 16 11b: RC_THR_SCALE = 64
1-0	RC_THR_9:8	R/W	3h	Upper two bits of the 10-bit RC_THR Register. Threshold level to compare against RC_CNT based on the expected time of motor actuation. Ripple counting threshold = RC_THR x RC_THR_SCALE

8.6.3.7 RC_CTRL3 Register (Offset = 14h) [Reset = 00h]

RC_CTRL3 is shown in Table 8-55.

Return to the Summary Table.

Set the INV_R parameter.

Table 8-55. RC_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	INV_R	R/W	32d	User input based on motor coil resistance. INV_R = INV_R_SCALE / Motor Resistance. Must not be set to 0. Refer to Section 8.3.6.1.1 for further explanation.

8.6.3.8 RC_CTRL4 Register (Offset = 15h) [Reset = 00h]

RC_CTRL4 is shown in Table 8-56.

Return to the Summary Table.

Set the KMC parameter.

Table 8-56. RC_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	KMC	R/W	163d	Represents a proportional value of the motor back emf constant. KMC = (K_V) / N_R)*KMC_SCALE. Refer to Section 8.3.6.1.4 for further explanation.

8.6.3.9 RC_CTRL5 Register (Offset = 16h) [Reset = 00h]

RC_CTRL5 is shown in Table 8-57.

Return to the Summary Table.

Set the filter damping constant.

Table 8-57. RC_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FLT_K	R/W	6d	Bandpass filter 1/Q factor. Sets the bandwidth of the bandpass filter. Recommended value is the default value: 6d. Refer to Section 8.3.6.1.5 for further explanation.
3-0	RSVD	R/W	0h	Reserved

8.6.3.10 RC_CTRL6 Register (Offset = 17h) [Reset = 45h]

RC_CTRL6 is shown in Table 8-58.

Return to the Summary Table.

Disable the Error Correction pulses for Ripple Counting.

Table 8-58. RC_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EC_PULSE_DIS	R/W	0h	Disable the Error Correction Pulses. Differs from the EN_EC bit described previously. 0b: Error correction is always enabled. 1b: Error correction will stop giving pulses under certain conditions described in Section 8.3.6.1.11.
6-4	T_MECH_FLT	R/W	4h	This parameter determines the cut-off frequency of a low pass filter at the output of the ripple counter to control the response time of the ripple counter to match the intertia of the mechanical system. Increase this value to for a slower response and decrease it for a faster response.
3-2	EC_FALSE_PER	R/W	1h	Sets the window during which the error corrector classifies a current ripple as an extra ripple. 00b: 20% 01b: 30% 10b: 40% 11b: 50%
1-0	EC_MISS_PER	R/W	1h	Sets the window during which the error corrector adds a missed ripple. 00b: 20% 01b: 30% 10b: 40% 11b: 50%

8.6.3.11 RC_CTRL7 Register (Offset = 18h) [Reset = 21h]

RC_CTRL7 is shown in Table 8-59.

Return to the Summary Table.

Set the proportional constant in PI control loop.

Table 8-59. RC_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	KP_DIV	R/W	1h	Used to select a division value for calculating the actual proportional constant for the PI control loop. Actual proportional constant = KP/KP_DIV. Settings are as follows: 000b: 32 001b: 64 010b: 128 011b: 256 100b: 512 101b: 16 110b: 1
4-0	KP	R/W	1h	Represents the PI loop KP constant. This is not the actual proportional constant that is fed into the gain block of the PI control loop. Rather, the actual proportional constant can be calculated using this value of the KP register. Actual Proportional Constant = KP/KP_DIV. For example, if actual proportional constant is 0.0625, then KP can be set to 1 (00001b), and KP_DIV can be set to 16 (corresponds to 101b), hence, Actual proportional constant = 1/16 = 0.0625.

8.6.3.12 RC_CTRL8 Register (Offset = 19h) [Reset = 21h]

RC_CTRL8 is shown in Table 8-60.

Return to the Summary Table.

Set the integral constant in PI control loop.

Table 8-60. RC_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	KI_DIV	R/W	1h	Used to select a division value for calculating the actual integral constant for the PI control loop. Actual integral constant = KI/KI_DIV. Settings are as follows: 000b: 32 001b: 64 010b: 128 011b: 256 100b: 512 101b: 16 110b: 1
4-0	KI	R/W	1h	Represents the PI loop KI constant. This is not the actual integral constant that is fed into the gain block of the PI control loop. Rather, the actual integral constant can be calculated using this value of the KI register. Actual Integral Constant = KI/KI_DIV. For example, if actual integral constant is 0.90625, then KI can be set to 29 (11101b), and KI_DIV can be set to 32 (corresponds to 000b), hence, Actual integral constant = 29/32 = 0.90625.