77 STM32WB30xx/35xx/50xx/55xx devices

77.1 Bootloader configuration

The STM32WB30xx/35xx/50xx/55xx bootloader is activated by applying Pattern 16 (described in *Table 2*). *Table 171* shows the hardware resources used by this bootloader.

Table 171. STM32WB30xx/35xx/50xx/55xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all	RCC	MSI enabled	The system clock frequency is 64 MHz (using PLL clocked by MSI).
		-	CRS is enabled for the DFU to allow USB to be clocked by HSI 48 MHz.
	RAM	-	20 Kbytes, starting from address 0x20000000, are used by the bootloader firmware
	System memory	-	28 Kbytes, starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The IWDG prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (if the hardware IWDG option was previously enabled by the user).
USART1	USART1	Enabled	Once initialized, the configuration is 8-bit, even parity, and one stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode. Used in alternate push-pull, pull-up mode.
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode. Used in alternate push-pull, pull-up mode.
I2C1	I2C1	Enabled	The I2C1 configuration is: – I2C speed: up to 1 MHz – 7-bit address – Target mode – Analog filter ON – Target 7-bit address: 0b1001111x (x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/output	PB6 pin: clock line is used in open-drain no pull mode.
	I2C1_SDA pin	Input/output	PB7 pin: data line is used in open-drain no pull mode.

Table 171. STM32WB30xx/35xx/50xx/55xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
I2C3	I2C3	Enabled	The I2C3 configuration is: – I2C speed: up to 1 MHz – 7-bit address – Target mode – Analog filter ON – Target 7-bit address: 0b1001111x (x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/output	PC0 pin: clock line is used in open-drain no pull mode.
	I2C3_SDA pin	Input/output	PC1 pin: data line is used in open-drain no pull mode.
SPI1	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL low, CPHA low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: slave data input line, used in push-pull, pull-down mode
	SPI1_MISO pin	Output	PA6 pin: slave data output line, used in push-pull, pull-down mode
	SPI1_SCK pin	Input	PA5 pin: slave clock line, used in push-pull, pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull, pull-down mode. Note: This IO can be tied to GND if the SPI master does not use it.

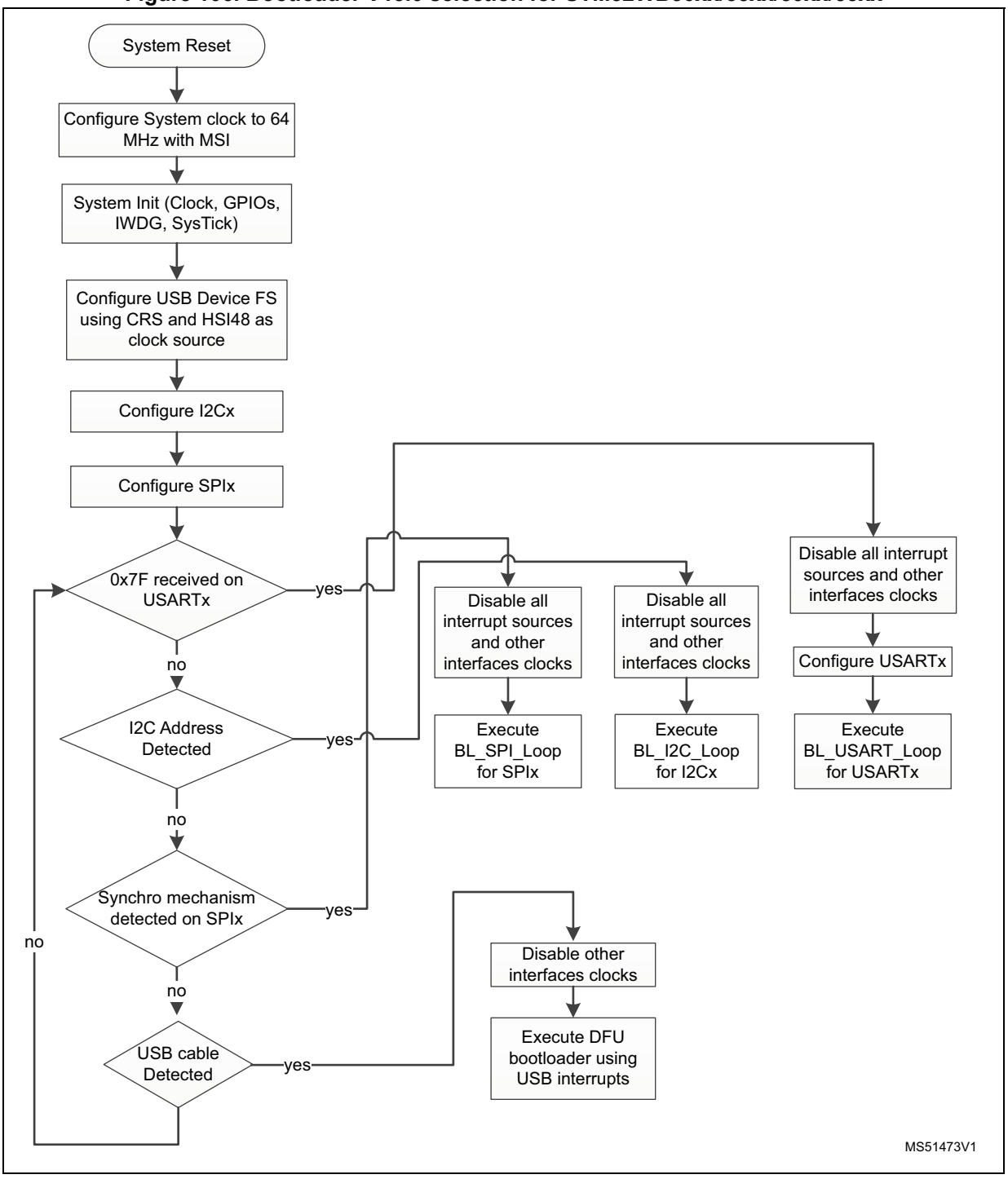
Table 171. STM32WB30xx/35xx/50xx/55xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
SPI2	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL low, CPHA low, NSS hardware.
	SPI2_MOSI pin	Input	PB15 pin: slave data input line, used in push-pull, pull-down mode
	SPI2_MISO pin	Output	PB14 pin: slave data output line, used in push-pull, pull-down mode
	SPI2_SCK pin	Input	PB13 pin: slave clock line, used in push-pull, pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull, pull-down mode. **Note:** This IO can be tied to GND if the SPI master does not use it.
DFU	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications. **Note**: VDDUSB IO must be connected to 3.3 V as USB peripheral is used by the bootloader.
	USB_DM pin	Input/output	PA11: USB DM line. Used in input no pull mode.
	USB_DP pin		PA12: USB DP line. Used in input no pull mode. No external pull-up resistor is required

77.2 Bootloader selection

Figure 106 shows the bootloader selection mechanism.

Figure 106. Bootloader V13.0 selection for STM32WB30xx/35xx/50xx/55xx



77.3 Bootloader version

Table 172. STM32WB30xx/35xx/50xx/55xx bootloader versions

Version number	Description	Known limitations
V13.5	Initial bootloader version	– Readout Unprotect Command is not working properly as at the end of the command an NVIC_SystemReset is done instead of a flash option bytes reload. This makes the change of the RDP level not effective until a power off/on. – I2C Write Protect command (0x73) performs a Read Unprotect instead of disabling write protection. Workaround: Uses No-Stretch Write Unprotect command (0x74) that is performing correctly the write unprotect operation

Note: Instability when performing multiple resets during operations ongoing causing Overrun or FrameError errors on USART Bootloader and not recoverable unless Hardware Reset is performed. Fixed by workaround in FUS V1.0.1 and V1.0.2.