B2. Summary of Instructions

Mnemonic, Operand		Description	Cycles	Status Affected	16-bit instruction word			
Byte-Oriented File Register Operands								
ADDWF	f, d, a	Add WREG and f	1	C, DC, Z, OV, N	0010	01da	ffff	ffff
ADDWFC	f, d, a	Add WREG and carry bit to f	1	C, DC, Z, OV, N	0010	00da	ffff	ffff
ANDWF	f, d, a	AND WREG with f	1	Z, N	0001	01da	ffff	ffff
CLRF	f, a	Clear f	1	Z	0110	101a	ffff	ffff
COMF	f, d, a	Complement f	1	Z, N	0001	11da	ffff	ffff
CPFSEQ	f, a	Compare f with WREG, skip =	1 (2 or 3)	None	0110	001a	ffff	ffff
CPFSGT	f, a	Compare f with WREG, skip >	1 (2 or 3)	None	0110	010a	ffff	ffff
CPFSLT	f, a	Compare f with WREG, skip <	1 (2 or 3)	None	0110	000a	ffff	ffff
DECF	f, d, a	Decrement f	1	C, DC, Z, OV, N	0000	01da	ffff	ffff
DECFSZ	f, d, a	Decrement f, skip if 0	1 (2 or 3)	None	0010	11da	ffff	ffff
DCFSNZ	f, d, a	Decrement f, skip if not 0	1 (2 or 3)	None	0100	11da	ffff	ffff
INCF	f, d, a	Increment f	1	C, DC, Z, OV, N	0010	10da	ffff	ffff
INCFSZ	f, d, a	Increment f, skip if 0	1 (2 or 3)	None	0011	11da	ffff	ffff
INFSNZ	f, d, a	Increment f, skip if not 0	1 (2 or 3)	None	0100	10da	ffff	ffff
IORWF	f, d, a	Inclusive OR WREG with f	1	Z, N	0001	00da	ffff	ffff
MOVF	f, d, a	Move f	1	Z, N	0101	00da	ffff	ffff
MOVFF	fs, fd	Move fs to fd	2	None	1100	ffff	ffff	ffff
					1111	ffff	ffff	ffff
MOVWF	f, a	Move WREG to f	1	None	0110	111a	ffff	ffff
MULWF	f, a	Multiply WREG with f	1	None	0000	001a	ffff	ffff
NEGF	f, a	Negate f	1	C, DC, Z, OV, N	0110	110a	ffff	ffff
RLCF	f, d, a	Rotate left f through carry	1	C, Z, N	0011	01da	ffff	ffff
RLNCF	f, d, a	Rotate left f (no carry)	1	Z, N	0100	01da	ffff	ffff
RRCF	f, d, a	Rotate right f through carry	1	C, Z, N	0011	00da	ffff	ffff
RRNCF	f, d, a	Rotate right f (no carry)	1	Z, N	0100	00da	ffff	ffff
SETF	f, a	Set f	1	None	0110	100a	ffff	ffff
SUBFWB	f, d, a	Subtract from WREG with borrow	1	C, DC, Z, OV, N	0101	01da	ffff	ffff
SUBWF	f, d, a	Subtract WREG from f	1	C, DC, Z, OV, N	0101	11da	ffff	ffff
SUBWFB	f, d, a	Subtract WREG from f with borrow	1	C, DC, Z, OV, N	0101	10da	ffff	ffff
SWAPF	f, d, a	Swap nibbles in f	1	None	0011	10da	ffff	ffff
TSTFSZ	f, a	Test f, skip if 0	1 (2 or 3)	None	0110	011a	ffff	ffff
XORWF	f, d, a	Exclusive OR WREG with f	1	Z, N	0001	10da	ffff	ffff
Bit-Oriented File Register Operands								
BCF	f, b, a	Bit clear f	1	None	1001	bbba	ffff	ffff
BSF	f, b, a	Bit set f	1	None	1000	bbba	ffff	ffff
BTFSC	f, b, a	Bit test f, skip if clear	1 (2 or 3)	None	1011	bbba	ffff	ffff
BTFSS	f, b, a	Bit test f, skip if set	1 (2 or 3)	None	1010	bbba	ffff	ffff
BTG	f, b, a	Bit toggle	1	None	0111	bbba	ffff	ffff

Table B1 ■ PIC18 Instruction set summary (redraw with permission of Microchip)

Mnemonic, Operand		Description	Cycles	Status Affected	16-bit instruction word			
Control Operations								
BC	n	Branch if carry	1 (2)	None	1110	0010	nnnn	nnnn
BN	n	Branch if negative	1 (2)	None	1110	0110	nnnn	nnnn
BNC	n	Branch if not carry	1 (2)	None	1110	0011	nnnn	nnnn
BNN	n	Branch if not negative	1 (2)	None	1110	0111	nnnn	nnnn
BNOV	n	Branch if not overflow	1 (2)	None	1110	0101	nnnn	nnnn
BNZ	n	Branch if not zero	2	None	1110	0001	nnnn	nnnn
BOV	n	Branch if overflow	1 (2)	None	1110	0100	nnnn	nnnn
BRA	n	Branch unconditionally	1 (2)	None	1101	0nnn	nnnn	nnnn
BZ	n	Branch if zero	1 (2)	None	1110	0000	nnnn	nnnn
CALL	n, s	Call subroutine	2	NOne	1110	110s	kkkk	kkkk
					1111	kkkk	kkkk	kkkk
CLRWDT		Clear watchdog timer	1	$\overline{TO}$, $\overline{PD}$	0000	0000	0000	0100
DAW		Decimal adjust WREG	1	C	0000	0000	0000	0111
GOTO	n	Goto	2	None	1110	1111	kkkk	kkkk
					1111	kkkk	kkkk	kkkk
NOP		No operation	1	None	0000	0000	0000	0000
NOP		No operation	1	None	1111	xxxx	xxxx	xxxx
POP		Pop top of return address	1	None	0000	0000	0000	0110
PUSH		Push top of return address	1	None	0000	0000	0000	0101
RCALL	n	Relative call	2	None	1101	1nnn	nnnn	nnnn
RESET		Software device RESET	1	All	0000	0000	1111	1111
RETFIE	s	Return from interrupt enable	2	GIE/GIEH,PEIE	0000	0000	0001	000s
RETLW	k	Return with literal in WREG	2	None	0000	1100	kkkk	kkkk
RETURN	s	Return from subroutine	2	None	0000	0000	0001	001s
SLEEP		Go into standby mode	1	$\overline{TO}$, $\overline{PD}$	0000	0000	0000	0011
Literal Operations								
ADDLW	k	Add literal and WREG	1	C, DC, Z, OV, N	0000	1111	kkkk	kkkk
ANDLW	k	AND literal with WREG	1	Z, N	0000	1011	kkkk	kkkk
IORLW	k	Inclusive OR literal with WREG	1	Z, N	0000	1001	kkkk	kkkk
LFSR	f, k	Move literal (12-bit) 2nd word to FSRx 1st word	2	None	1110	1110	00ff	kkkk
					1111	0000	kkkk	kkkk
MOVLB	k	Move literal to BSR<3:0>	1	None	0000	0001	0000	kkkk
MOVLW	k	Move literal to WREG	1	None	0000	1110	kkkk	kkkk
MULLW	k	Multiply literal with WREG	1	None	0000	1101	kkkk	kkkk
RETLW	k	Return with literal in WREG	2	None	0000	1100	kkkk	kkkk
SUBLW	k	Subtract WREG from literal	1	C, DC, Z, OV, N	0000	1000	kkkk	kkkk
XORLW	k	Exclusive OR literal with WREG	1	Z, N	0000	1010	kkkk	kkkk
Data memory to and from Program memory Operations								
TBLRD*		Table read	2	None	0000	0000	0000	1000
TBLRD*+		Table read with post-increment		None	0000	0000	0000	1001
TBLRD*–		Table read with post-decrement		None	0000	0000	0000	1010
TBLRD+*		Table read with pre-increment		None	0000	0000	0000	1011
TBLWT*		Table write	2 (5)	None	0000	0000	0000	1100
TBLWT*+		Table write with post-increment		None	0000	0000	0000	1101
TBLWT*–		Table write with post-decrement		None	0000	0000	0000	1110
TBLWT+*		Table write with pre-increment		None	0000	0000	0000	1111

Table B1 ■ *(continued)*