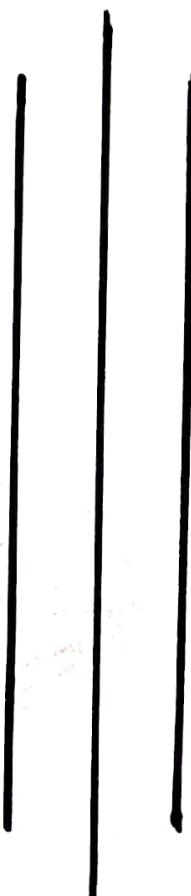


\* Electrical Engineering, Materials.

Chapter: 7

\* Semiconductor device processing.



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## Chapter 7

### (\*) Semiconductor device fabrication (processing)

Semiconductor device fabrication is the process used to create the integrated circuits that are present in everyday electrical and electronic devices. It is a multiple-step sequence of photolithographic and chemical processing steps during which electronic circuits are gradually created on a special shaped (wafer) made of pure semiconducting material. Silicon is almost always used, but various compound semiconductors are used for specialized applications.

The entire manufacturing process, from start to packaged chips ready for shipment, takes six to eight weeks & is performed in highly specialized facilities referred to as fabrication.

### (\*) Silicon purification process

The fabrication of discrete and integrated circuit (IC) solid-state devices requires semiconductor crystals with impurity concentrations as low as possible and crystals that contain very few imperfections. A number of laboratory techniques are available for growing high-purity semiconductor crystals.

Generally they involve either solidification from the melt or condensation of atoms from the vapour state. The initial process in IC fabrication technique requires large-single-crystal wafers that are typically 15cm in dimension diameter and 0.6 mm thick.

Large, single Si crystals for IC fabrication are often grown by the Czochralski method.

#### (a) Czochralski method:

This method involves growing a single-crystal ingot from the melt, using solidification on a seed crystal, as schematically illustrated in fig. below.

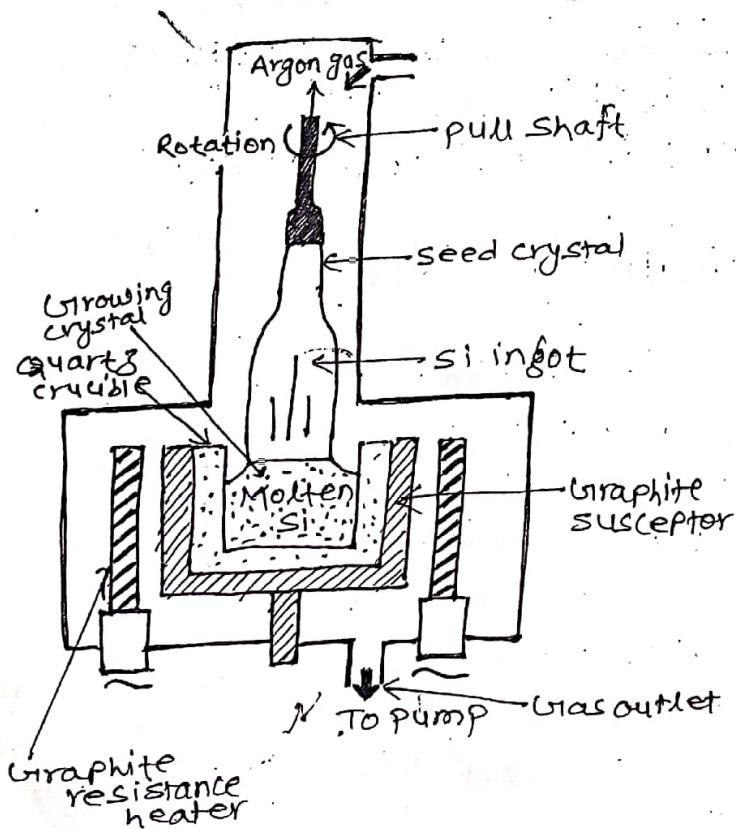


fig.(a)  
Schematic illustration of the growth of a single-crystal Si ingot by the Czochralski technique

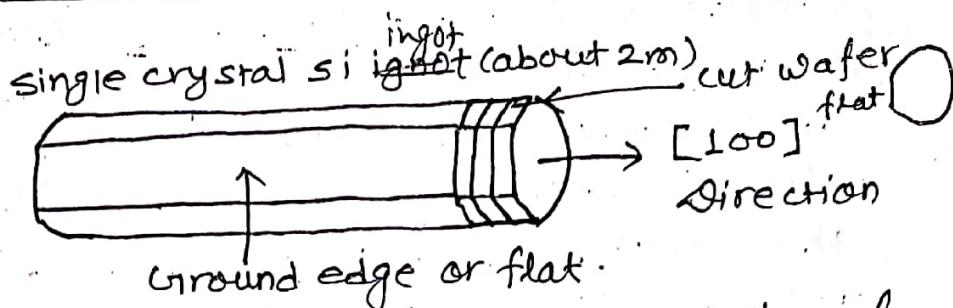


fig.(b) The crystallographic orientation of the silicon ingot is marked by grounding a flat.

→ operation

Molten Si is held in a quartz (crystalline  $\text{SiO}_2$ ) crucible in a graphite susceptor, which is either heated by a graphite resistance heater or by radio frequency induction coil (a process called RF heating). A small dislocation-free crystal, called a seed is lowered to touch the melt & then slowly pulled out of the melt; a crystal grows by solidifying on the seed crystal. The seed is rotated during the pulling stage, to obtain a cylindrical ingot. To suppress evaporation from the melt & prevent oxidation, argon gas is passed through the system.

The sizes and diameters of the crystals grown by the Czochralski method are obviously limited by the equipment, though crystals 20-30cm in diameter and 1-2 m in length are routinely grown for the IC fabrication industry. Also the crystal orientation of the seed and its flatness with melt

Surface are important engineering requirements. For example, for very large scale integration, the seed is placed with its (100) plane flats to the melt, so that the axis of the cylindrical ingot is along the [100] direction.

### Epitaxial growth.

The term 'Epitaxial' is derived from the Latin terms 'Epi' meaning 'upon' and 'taxis' meaning 'arrangement'.

To construct an epitaxially grown diode, a very thin (single crystal) high impurity, layer of semiconductor material (silicon or germanium) is heavily doped substrate (base) of the same material.

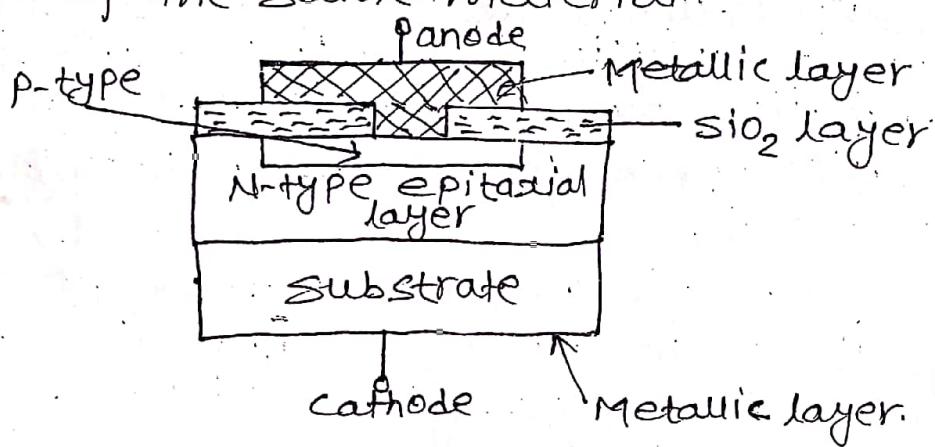


fig:- Epitaxially grown or planar diffused diode.

This complete structure then forms the N-region on which P-region is diffused.  $\text{SiO}_2$  layer is thermally grown on the top surface, photo-etched and the aluminium contact is made to the P-region. A metallic layer at the bottom of the substrate forms the cathode to attached with the epitaxial layer through substrate.

The process is usually employed in the fabrication of IC chips.

### (\*) Photolithography.

Photolithography (or optical lithography) or (UV lithography) is a process used in micro fabrication to selectively remove parts of a thin film or the bulk of a substrate. It uses light to transfer a geometric pattern from a photomask to a light sensitive chemical photoresist or simply 'resist' on substrate.

Photolithography shares same fundamental principles with photography.

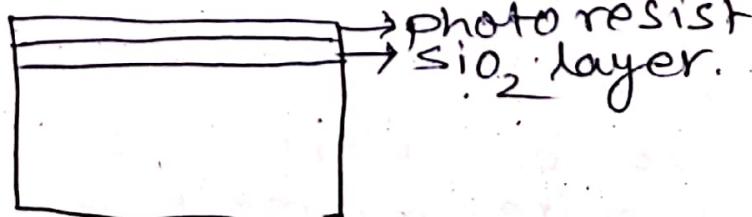


fig: A single crystal of Si.

(43)

## PN junction fabrication

In practice, the P-N Junction is formed from a single monocrystalline structure by adding carefully controlled amounts of donor and acceptor impurities.

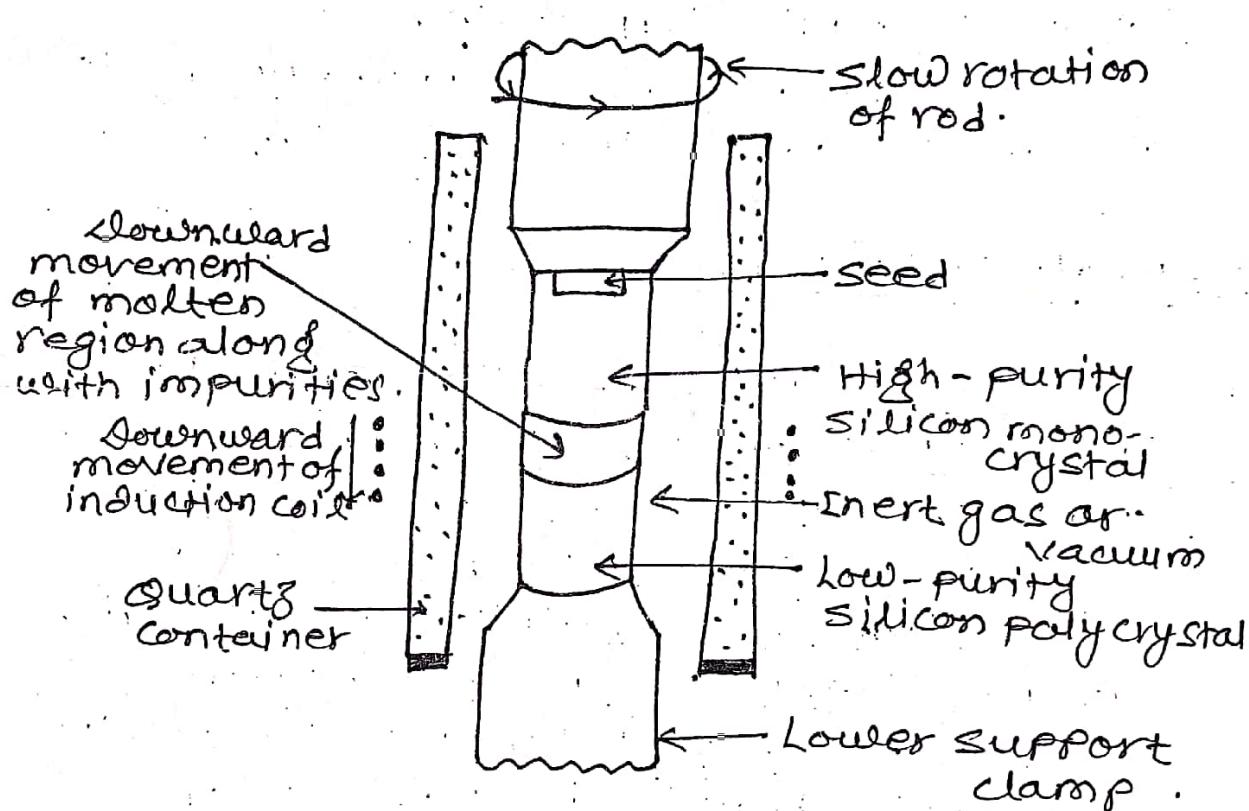


fig:- PN-junction fabrication..

The first and foremost requirement is to obtain an extremely pure germanium or silicon. Impurity of less than one part in 10 billion ( $10^{10}$ ) is required for most semiconductor device fabrication today. For obtaining pure semiconductor material, it is first purified chemically.

For reducing the impurities further, to ensure the formation of a monocrystalline structure, a technique known as flatting zone is quite often employed. The monocrystalline structure is formed through the use of a small seed of semiconductors (e.g. silicon or germanium). Support clamps are employed to hold the low-purity polycrystalline rod.

Once a pure monocrystalline semiconductor has been produced, carefully controlled some amount of donor and acceptor impurities are added to the semiconductor without disturbing the orderly monocrystalline structure. Thus P-N junction is formed.

### (\*) NPN transistor fabrication:

A conventional bipolar junction transistor (BJT) is made up from a triple sandwich of alternating P-type and N-type layers, which can be arranged in either P-N-P or N-P-N order & there are electrical connection to each layer.

It is a current controlled device, with the collector or emitter current as a output, normally controlled by the base current or sometimes the emitter current.

The way in which the N-type & P-type layers are fabricated to create a BJT has developed as permitted by available technology. The trend being towards creating devices with smaller physical dimensions, which generally permits faster operation; because

- (i) It takes less time for holes & electrons to cross regions of the transistor.
- (ii) The stray capacitances & inductances are smaller.



## Diffusion system:-

This is one of the primary method of introducing impurities such as boron, phosphorous, antimony into silicon to control the majority carrier type and sheet resistivity of layers formed in the wafer.

The mathematical expression of diffusion process in 1-dimension can be derived using Fick's law of diffusion. Fick's first law of diffusion states that the particle flow per unit area (particle fluid),  $J$  is directly proportional to the concentration gradient of the particle.

i.e.

$$J = -D \frac{\partial N}{\partial x} \quad (1)$$

where  $N$  is the particle concentration and  $D$  is the diffusion coefficient. The -ve sign indicates that the particles move from the region of high concentration to low concentration.

The Continuity equation for particle flux is,

$$\frac{\partial N}{\partial t} = - \frac{\partial J}{\partial x} \quad (2)$$

Now combining Eqn's ① & ② we get,

$$\frac{\partial N}{\partial t} = D \frac{\partial^2 N}{\partial x^2} \quad (3)$$

Fick's The above Equation (3) is called the 2<sup>nd</sup> law of diffusion.

Two specific boundary conditions, namely Constant Source diffusion and Limited-source diffusion are important in modelling the diffusion.

During the constant source diffusion, the impurity concentration is held constant at the surface of the wafer. As time progresses, the diffusion front proceeds further and further into the wafer with the surface concentration remaining constant.

In Limited source diffusion, the impurity atoms per unit area remains constant throughout the diffusion process. As the diffusion front moves into wafer, the surface concentration must decrease so that the area under the curve can remain constant with time.

### (\*) Ion Implantation process

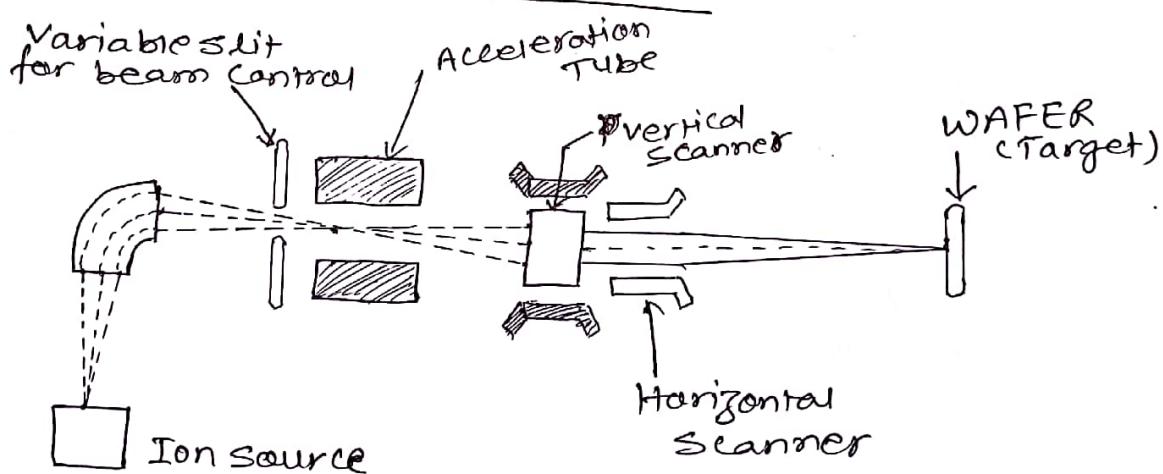


Fig:- Typical Ion Implanter.

Ion implantation process has many advantages over diffusion for the production of impurity atoms into the silicon wafer, so it is the most widely used technology in Modern IC fabrication.

An Ion implanter is a high-voltage particle accelerator producing a high-velocity beam of impurity ions, which can penetrate the surface of Si wafers.

The ion source, which operates at high voltage (25 KV), is meant for producing plasma containing desired impurity, but it produces undesired impurities as well. An analyzer magnet bends the ion beam through a right angle to select the desired impurity ion, which then passes through an aperture slit into the main accelerator column. The main function of accelerator column is to add energy of upto 175 KEV to the beam and accelerate the ions to their final velocity. Scanning system consists of x-and y-axis's deflection plates to scan the beam across the wafer to give a uniform implantation & to build upto the desired number of impurities atoms per unit area. The beam is bent slightly to prevent the neutral particles hitting the target. The target chamber has the silicon wafers, which will be targeted by the impurity ions.

In this way, the wafer is cleaned and is ready for the further processing.

Note: By Ion implantation process, wide range of impurities can be implanted compared to that of diffusion. The main drawback of ion implantation process is the high costing.

[Silicon purification process; Neat method].

(\*) Floating zone method of crystal growth.

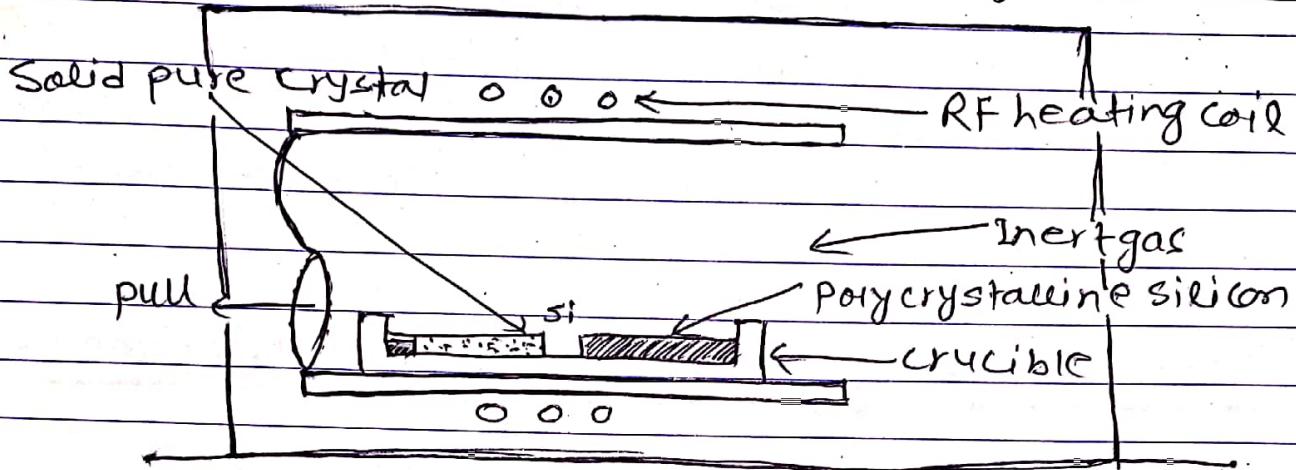


fig:- Floating zone method of crystal growing.

This method, in addition to, being capable of producing single crystals and also removing the extra impurities contained in the semiconductor material. The impurities can be removed very easily as they prefer to go to the liquid phase.

This type of crystal growing material is rarely used because of the high temperature requirement of silicon, there is always possibility of silicon crystals adhering to their crucible wall which causes deviation from the perfect lattice structure required for the silicon crystal.

The RF (Radio Frequency) heating coils heats the crucible in which the polycrystalline silicon is placed. As the ~~is~~ Si is heated, it melts at high temperature and by solidification

by slowly pulling it to the left where there is seed crystal; single pure crystal for IC fabrication is obtained. The inert gas is used to suppress the evaporation and prevent oxidation.

### Monolithic IC Fabrication: planar process:

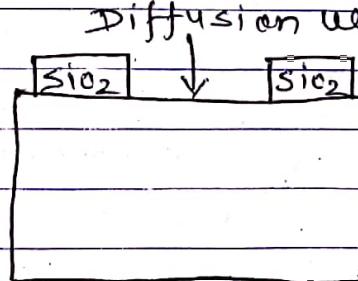
In the planar process, the fabrication of IC is done by plane at which one surface of the wafer so that the deepest region tends to be fabricated first. we will consider fabrication of a npn bipolar junction transistor. The fabrication follows the following steps.

- (1.) we start with a p-type single crystal of thickness about 200 μm, oriented [1,1,1] and with a resistivity of 10 Ωm.

p-type substrate (wafer).

fig(1)

- (2.) Make a diffusion window by photolithography.



fig(2).

3.) Dope the donors heavily which diffuses through window creating n-region by compensation doping.

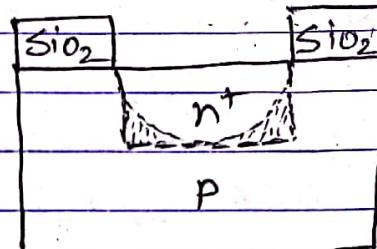


fig:3.

(4.) Remove the oxide layer by etching.

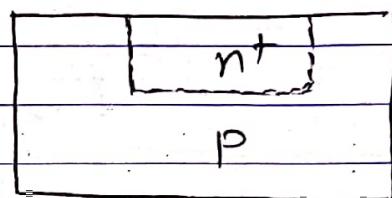


fig.(4).

(5.) Grow n-type epitaxial layer on the top of wafer by epitaxy (epitaxy - arranged upon). The epitaxial layer is very much thinner to the original layer of Bulk. This grown epitaxial layer is going to be collector of npn transistor.

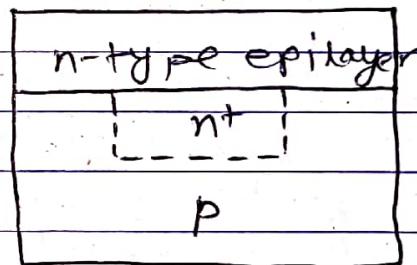


fig.(5)

- (6) Grow an oxide layer over the whole surface and then etch windows at the corners for isolation diffusion (after photolithography)

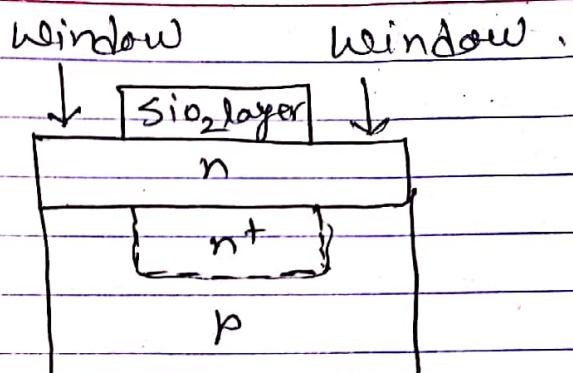


fig.(6)

- (7) Diffuse acceptor dopants heavily through the window in oxide.

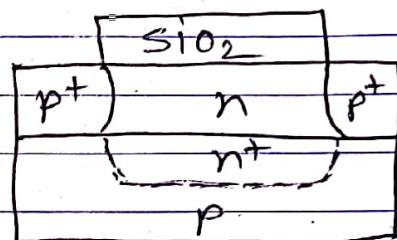


fig.(7)

- (8) For integrated circuits, the extended form of fig.(7) will be as shown in fig.(8). Here the two transistors are isolated called pn-junction isolation.

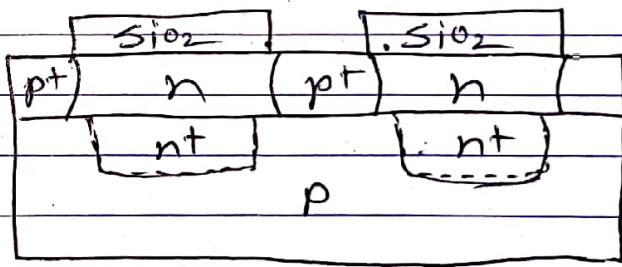


fig.(8)

- (9) Again focusing on the single n-p-n transistor fig. 9(a). Now doping acceptors over n-region to form p-region for base diffusion (after photolithography) (fig. 9(b)).

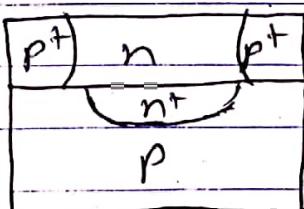


fig. 9(a)

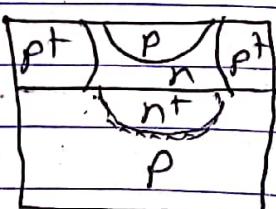


fig. 9(b)

o) Again dope donors to form emitter.  
(After photolithography)

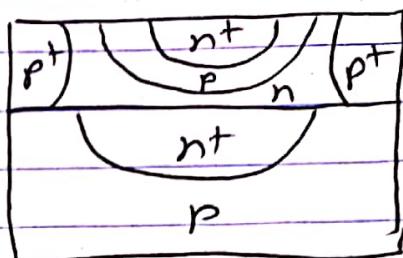


fig.(10)

(11.) Metallization involves deposition of metal (mostly aluminium) elements over base, collector and emitter, region (After photolithography) for a critical connection. Remove all oxide layer and unwanted metal deposition by etching. Thus fabricated 'npn' transistor can be used after electrically tested.

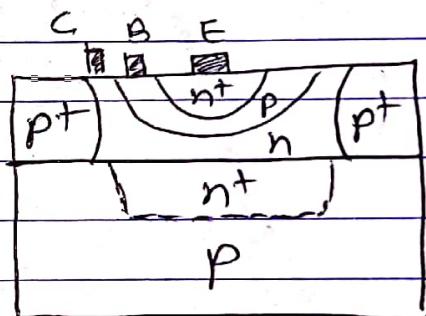


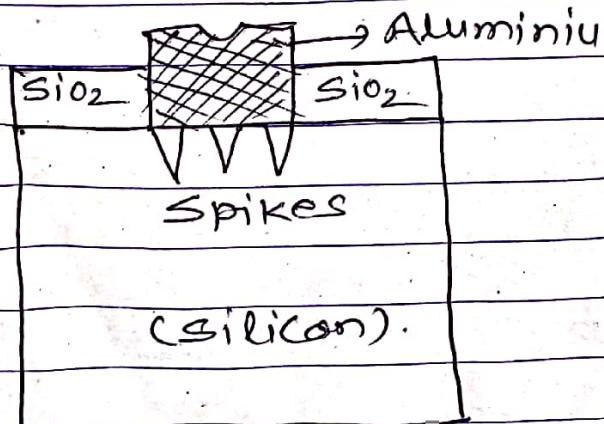
fig.(11)

Note:- Doping can be done either by diffusion or by Ion implantation method //.

## (\*) Metallization (Contacts in IC fabrication)

In IC fabrication, metallization is a last step. Metal contact is the connection of the integrated circuit to the outside world. This process

produces a thin film metal layer that will serve as the required conductor pattern for the interconnection of the various components on the chip. Most commonly used metals for metallization are aluminium and copper.



Aluminium is mostly used being cheaper having low resistance ( $3\text{m}\Omega\text{-cm}$ ) and adheres to  $\text{SiO}_2$ . Aluminium can easily form an Ohmic contact with p-type region and heavily doped n-region. But it is difficult to form Ohmic contact to moderately doped n-region. Rather it forms Schottky junction.