Theo **Olausson**

Master's Student · Researcher

Edinburgh, Scotland

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Summary

Master of Informatics student at the University of Edinburgh with an exceptional academic record (**A2 grade average**) and **3+ years experience in research**. Interested in applying formal reasoning and mathematical rigor to **computer architecture**, especially as it relates to **hardware security** and **machine learning**.

Education

University of Edinburgh — *Edinburgh, United Kingdom*

Master of Informatics (Hons), Expected **First Class** — *September 2016 - May 2021 (Estimated)*

- 5-year integrated Master's programme
- Grade average: A2
- Course highlights:
  - Parallel Architectures: Built a trace-driven cache coherence protocol simulator and learned about highly parallel architectures such as GPUs and superscalar processors.
  - Types & Semantics for Programming Languages: Formalized PL theory such as typed and untyped lambda calculus in the theorem prover Agda.
  - Machine Learning Practical: Deep learning with PyTorch. Carried out a substantial group project investigating image recognition techniques for memory-constrained devices, which later lead to a publication (see next page).

Professional Experience

Institute for Computing Systems Architecture, Univ. of Edinburgh — *Edinburgh, United Kingdom*

Funded Research Student — *March 2020 - May 2021*

- Member of the Consistency, Availability, Persistency via Synthesis (CAPS) group led by Dr. Vijay Nagarajan
- I conduct research into synthesis/design automation/debugging aids for cache coherence protocols
- Results of my research as of spring 2020 were presented in my 4th-year dissertation (see next page)

Arm — *Cambridge, United Kingdom*

Research Intern, Memory & Systems Architecture — *June 2019 - August 2019*

- Developed a novel method for verifying the Armv8 Memory Persistency Model on real hardware
- Implemented the method into the in-house memory model verification tool suite
- Gave an hour-long talk on my research, which was open to all staff in Arm's research division

Institute for Computing Systems Architecture, Univ. of Edinburgh — *Edinburgh, United Kingdom*

Research Intern — *May 2018 - August 2018*

- Began my collaboration with the CAPS research group (see above)

Teaching Experience

Fall 2018 **Informatics 1 – Introduction to Computation**, Tutor

Skills

Programming Languages Python C/C++ Kotlin Java OCaml Haskell

Tools/Frameworks Git VCS Linux PyTorch sk-learn Murphi (model checking) Agda (theorem proving)

Theory Deep Learning Neural Networks Computer Vision Memory Models Computer Architecture Algorithms/Data Structures

Languages English (fluent) Swedish (native)

Awards, Studentships & Grants

2020	**ICSA Studentship**, Institute for Computing Systems Architecture (University of Edinburgh)	*£25,620*
2019	**SDP 2018/19 Price for Entrepreneurship**, Informatics Business Development Team **SDP 2018/19 Price for Teamwork**, Sky	
2016/7	**Grants for Pursuing Further Education Abroad**, Hempel Foundation	*€3,500 + €2,000*

Publications

Peer Reviewed Papers

S. Müksch*, **T. Olausson***, J. Wilhelm*, P. Andreadis. Benchmarking the Accuracy of Algorithms for Memory-Constrained Image Classification. The First Workshop on Edge Computing and Communications (EdgeComm) at the Fifth ACM/IEEE Symposium on Edge Computing (SEC 2020), San Jose CA, November 11-13, 2020. *Note: * = **co-first author***.

Abstract: Convolutional Neural Networks, or CNNs, are the state of the art for image classification, but typically come at the cost of a large memory footprint. This limits their usefulness in edge computing applications, where memory is often a scarce resource. Recently, there has been significant progress in the field of image classification on such memory-constrained devices, with novel contributions like the ProtoNN, Bonsai and FastGRNN algorithms. These have been shown to reach up to 98.2% accuracy on optical character recognition using MNIST-10, with a memory footprint as little as 6KB. However, their potential on more complex multi-class and multi-channel image classification has yet to be determined. In this paper, we compare CNNs with ProtoNN, Bonsai and FastGRNN when applied to 3-channel image classification using CIFAR-10. For our analysis, we use the existing Direct Convolution algorithm to implement the CNNs memory-optimally and propose new methods of adjusting the FastGRNN model to work with multi-channel images. We extend the evaluation of each algorithm to a memory size budget of 8KB, 16KB, 32KB, 64KB and 128KB to show quantitatively that Direct Convolution CNNs perform best for all chosen budgets, with a top performance of 65.7% accuracy at a memory footprint of 58.23KB.

Preprints

S. Müksch*, **T. Olausson***, J. Wilhelm*, P. Andreadis. Quantitative Analysis of Image Classification Techniques for Memory-Constrained Devices. arXiv preprint 2005.04968, May 2020. Available online: `https://arxiv.org/pdf/2005.04968.pdf`. *Note: * = **co-first author.***

This is a longer version of the workshop paper presented at SEC'20.

Dissertations

T. Olausson. Towards the Automatic Synthesis of Cache Coherence Protocols. Undergraduate dissertation, School of Informatics, University of Edinburgh, May 2020. Available online: `https://theoxo.xyz/assets/dissertation1.pdf`. **Nominated for an award for best undergraduate dissertation.**

Abstract: This paper presents extensive contributions towards the automatic synthesis of cache coherence protocols. Motivated by the insight that even the most sophisticated current approaches still assume the existence of a correct Stable State Protocol (SSP), an abstract specification of the protocol under atomic conditions, it targets these abstractions in particular. It lays the groundwork for future research towards synthesis of SSPs by suggesting a concrete correctness criterion for SSPs, presenting the first publicly available dataset on which bug localization and synthesis efforts can be compared, and deriving a taxonomy of the bugs which appear in cache coherence protocols. Finally, two novel heuristic methods for the localisation of bugs in SSPs are presented and evaluated. The results of this evaluation indicate that the two methods can often identify bugs in protocols at a finer granularity than is currently possible with standard model checking engines. Thus, the methods may serve as useful debugging tools when developing cache coherence protocols, and open up for future work towards synthesising fixes to the bugs.