DCT Internship: Weekly Report

TODO: NEED TO UPDATE THIS WEEK

DCT Internship: Weekly Report

2.1 MON - JAN 26 2026

TODO: NEED TO UPDATE

- Hardware.

2.2 TUE - JAN 27 2026

TODO: NEED TO UPDATE

- Exam.
- Rough intro to STM32 nucleo board.

2.3 WED - JAN 28 2026

TODO: NEED TO UPDATE

- Familiarization of STM32 Board and IDE.
- LED blinking, interrupt, uart.

2.4 THU - JAN 29 2026

2.4.1 Architecture of Nucleo-H755ZI-Q

```
                  +--------------------------+
                  |  +--------+  +--------+  |
                  |  |  CM7   | +|  CM4   |  |
+---------+       |  +--------+  +--------+  |
| STLINK | <----> |                          |
+---------+       |                          |
                  |        +--------------+  |
                  |        | PERIPHERALS  |  |
                  |        +--------------+  |
                  |                          |
                  | NUCLEO-H755ZI-Q          |
                  +--------------------------+
```

Nucleo-H755ZI-Q has a asymmetric dual core architecture, having two cores Arm Cortex M7 and Arm Cortex M4.

Note Asymmetric Multi-processing: One Master and One or More Slaves. Master does all the configuration and task scheduling.

Note Symmetric Multi-processing: All have equal access to memory and resources.

Power Domains

The entire MCU is divided into 3 major power domains.

- D1: Where the M7 lies
- D2: Where the M4 lies
- D3: Where the RCC and PWR lies.
- BACKUP Domain: Where the EXTI lies.

Important From figure 2.1, we can see that the `EXTI`[a] is outside of the 3 domains. This enables to power down all 3 of these domains at the same time.

[a] External Interrupt Controller

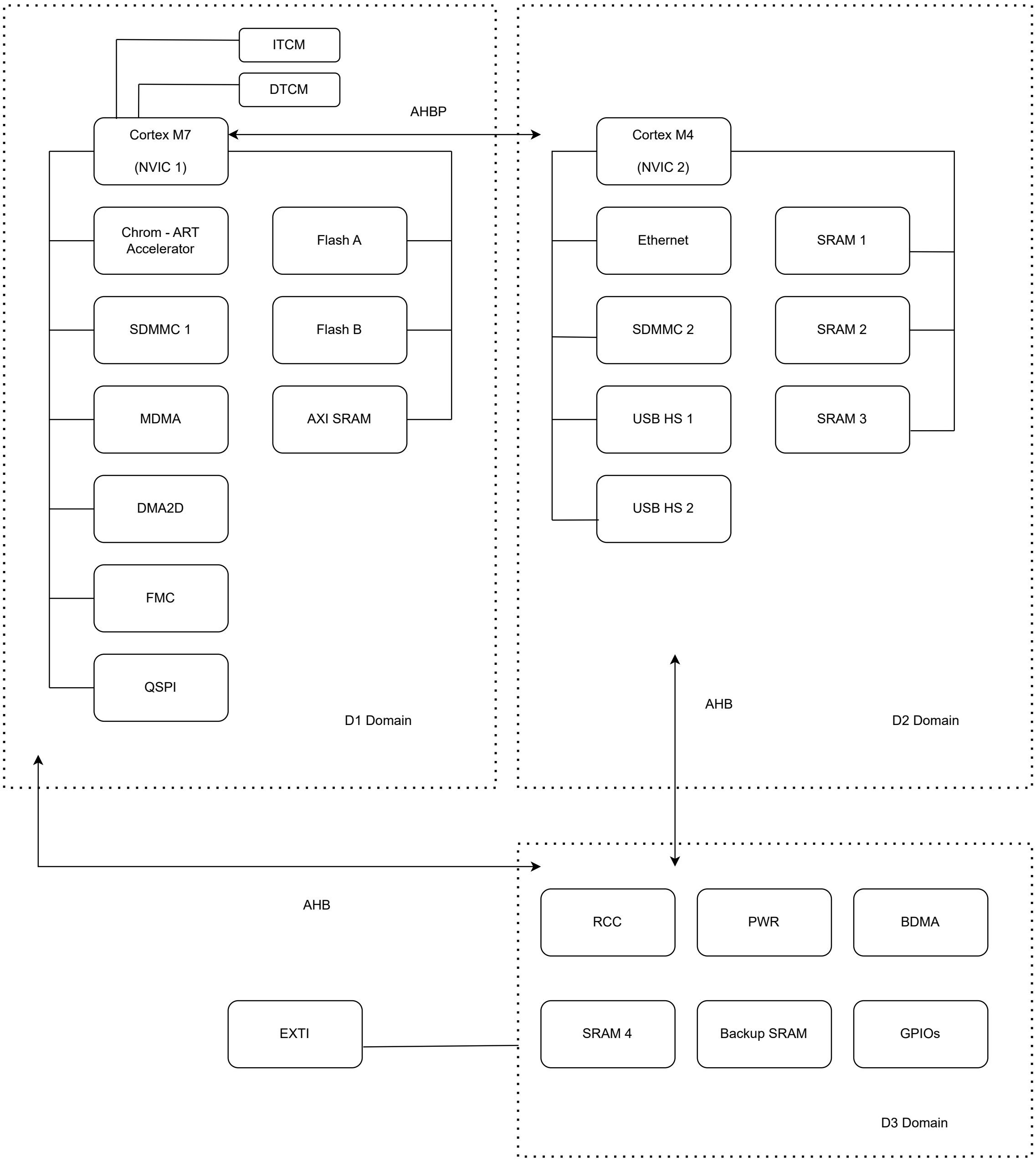

Figure 2.1: STM32 Architecture.

2.5 FRI - JAN 30 2026

2.5.1 Boot Process of STM32H755ZI

There are three power domains. CM7 and CM4 lies in the D1 and D2 domains respectively. Circuits that are responsible for power up and clock generation lies in the D3 domain.

`TODO: REST`

DCT Internship: Weekly Report

3.1 MON - FEB 02 2026

TODO: NEED TO UPDATE

- Interrupts.
- NVIC.
- EXIT.

3.2 TUE - FEB 03 2026

TODO: NEED TO UPDATE

- Ethernet.
- UART.

3.3 WED - FEB 04 2026