EC-441

Mixed Signal Design

Project Report

6-bit fully differential current steering DAC

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ABSTRACT

This project presents the design and implementation of a high-performance 6-bit fully differential current-steering Digital-to-Analog Converter (DAC) using a 180 nm CMOS process. The DAC is optimized for low-power and high-precision applications, operating with an analog supply voltage of 1.8 V and delivering a full-scale output voltage of 1.6 V peak-to-peak within an analog input range of 0 V to 1.6 V. The architecture ensures superior linearity, achieving a maximum Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) of ±0.5 LSB, meeting stringent precision requirements.

To enhance signal integrity, a fully differential design is employed, effectively mitigating common-mode noise and improving resilience to interference. The circuit integrates advanced techniques such as binary-weighted current sources and cascode current mirrors, ensuring high dynamic range and stability. Despite its robust performance, the DAC achieves remarkable energy efficiency, with a maximum static power consumption of less than 1 mW.

This design is compact and versatile, showcasing a low-power, high-precision solution suitable for modern mixed-signal systems, including high-speed data processing, wireless communication, and portable electronic devices. The project emphasizes achieving a balance between performance, efficiency, and scalability within stringent design constraints.

INTRODUCTION

Digital to analog converters required by digital signal processors, medical instruments, wireless communication and other various processing equipment has proved to be a continuous challenge for the analog designers to improve and develop new DAC architectures. Current steering DAC is most popular due to its high speed, high resolution and small size. The basic block diagram of Current Steering DAC (CS -DAC) is shown in Fig.1.

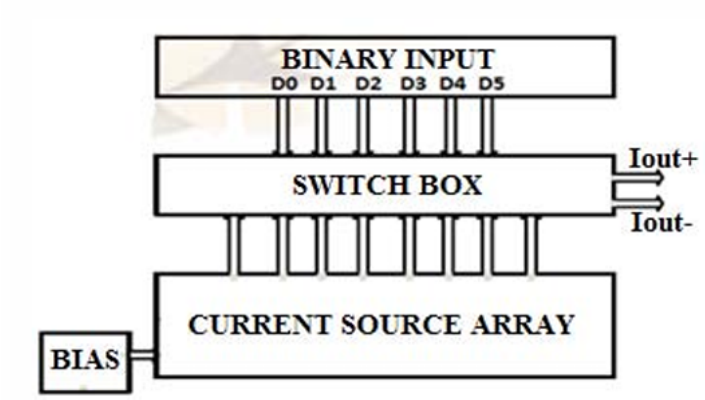


Fig. 1. Block Diagram of proposed Current Steering DAC [15]

This architecture consists of 6-bits binary weighted. The current sources are commuted on/off by means of complementary switches. In the binary implementation, the current sources, as shown in fig.2, are scaled according to the binary principle.

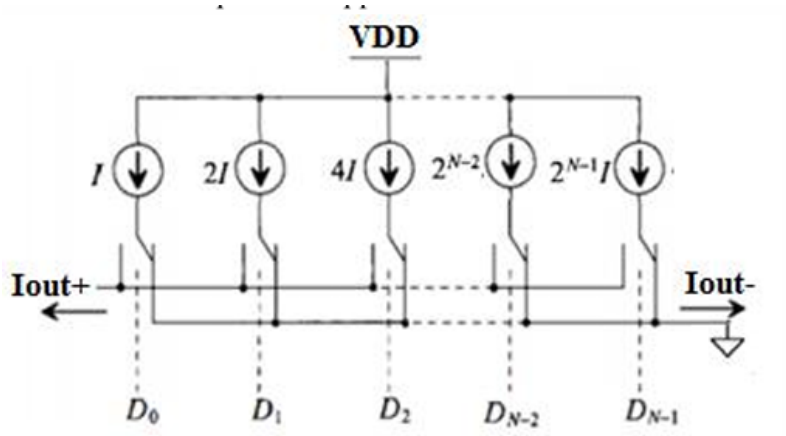


Fig. 2. Circuit diagram of a basic binary current steering DAC [14]

To design a fast DAC, the simplest solution is to associate CMOS switches with current sources weighted, as shown in fig 3 [6]. For N-bit converter, they should be used N current sources respectively

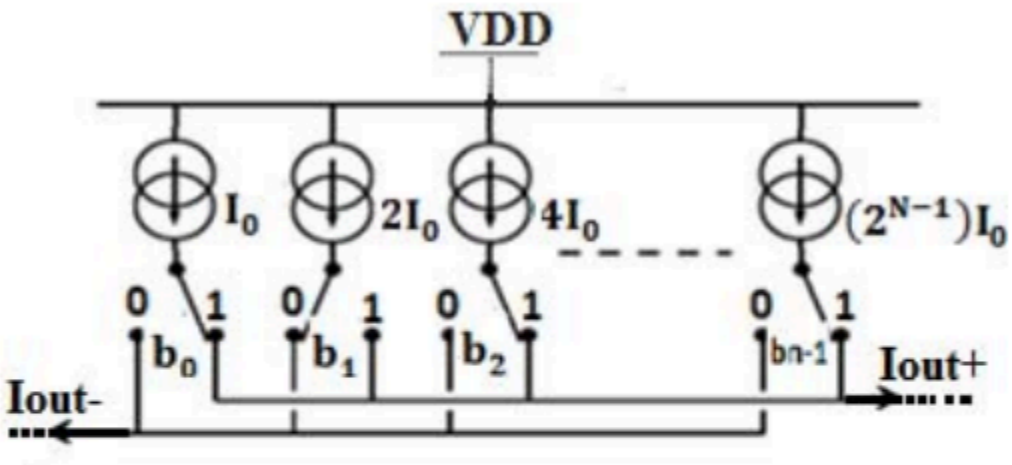


Fig. 3. DAC at switched current sources [14]

The resulting current output is:

$$I_{out+} = (b_0 + 2b_1 + 4b_2 + \cdots + 2^{N-1}b_{N-1})I_0 \quad (2)$$

$$I_{out+} = KI_0 \quad (3)$$

And its "complementary":

$$I_{out-} = (\overline{b_0} + 2\overline{b_1} + 4\overline{b_2} + \cdots + 2^{N-1}\overline{b_{N-1}})I_0$$

$$I_{out-} = (2^N - 1 - K)I_0$$

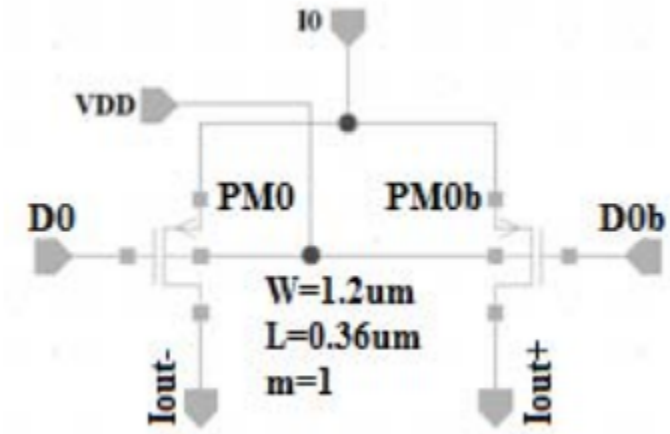
The total I_{tot} current drawn by the converter is:

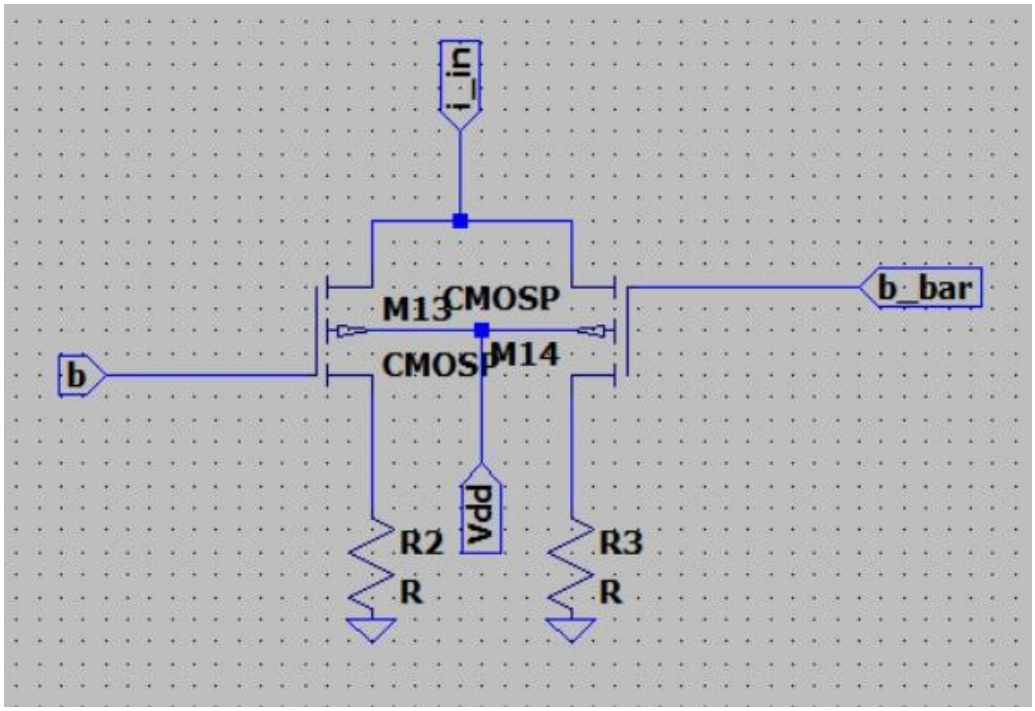
$$I_{tot} = I_{out-} + I_{out+} = (2^N - 1)I_0$$

CIRCUIT BREAKDOWN

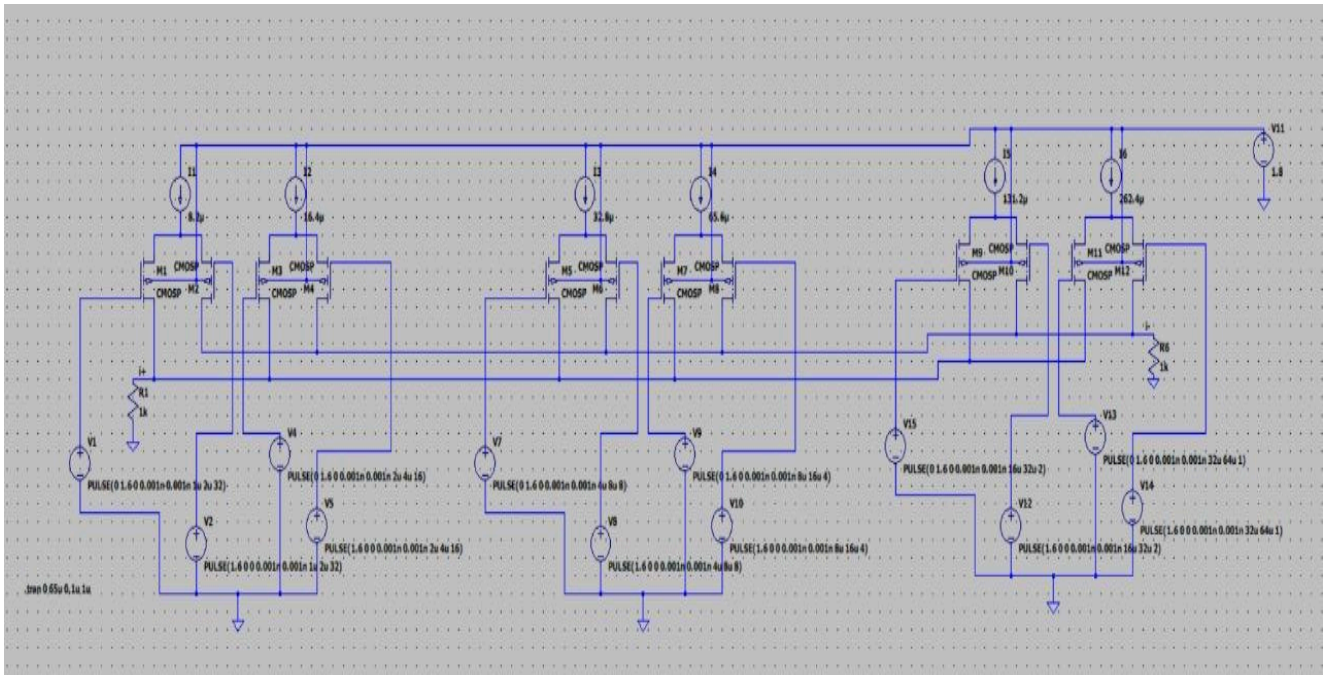
SWITCH

The purpose of this block is to orient the currents coming from the six array sources to the output Iout+ and Iout- . Controls signals coming from the block Binary Input (1) allow the switches to switch on the two branches of the DAC output is ON/OFF or OFF/ON. The current passing through these branches starts from 8.20uA to 516.60 uA depending on whether the switches correspond to the LSB or bits from the block Binary Input. The switching time should be equal regardless of the current passing through the branches in order to have good dynamic characteristics. This switching time is proportional to the amount of accumulated charges and inversely proportional to the size of the MOS which is traversed by the current. Thus, for a current 32 times it is necessary to increase the size of the transistor MOS 32times. Thus the MOS switch corresponding to the LSB are of minimum size (multiple m = 1, W = 4um, L = 0.36um) while the MOS switches corresponding to the MSB are 32 times greater (m = 32, W = 4um, L = 0.36um).

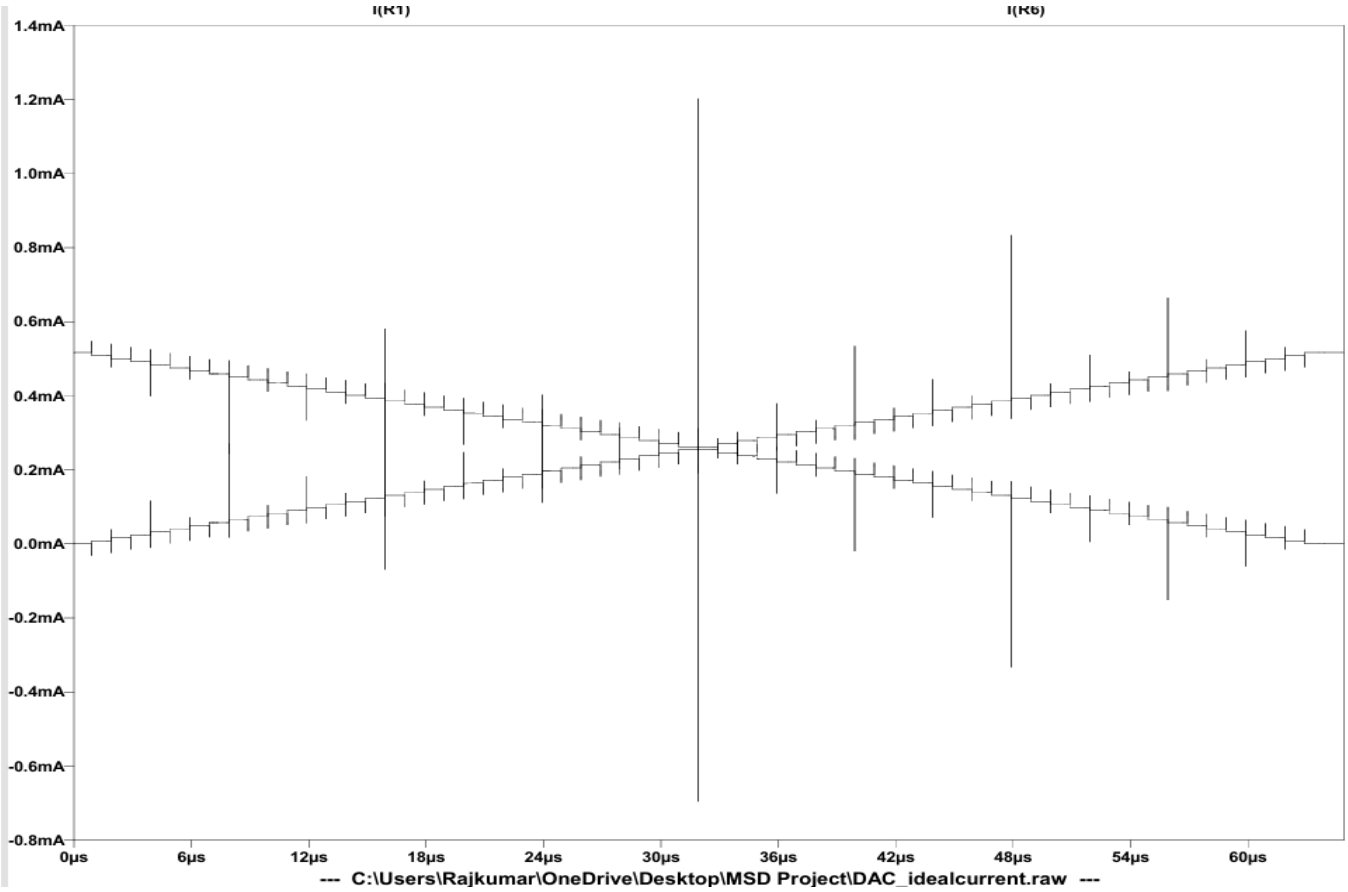




PART A USING IDEAL CURRENT SOURCE



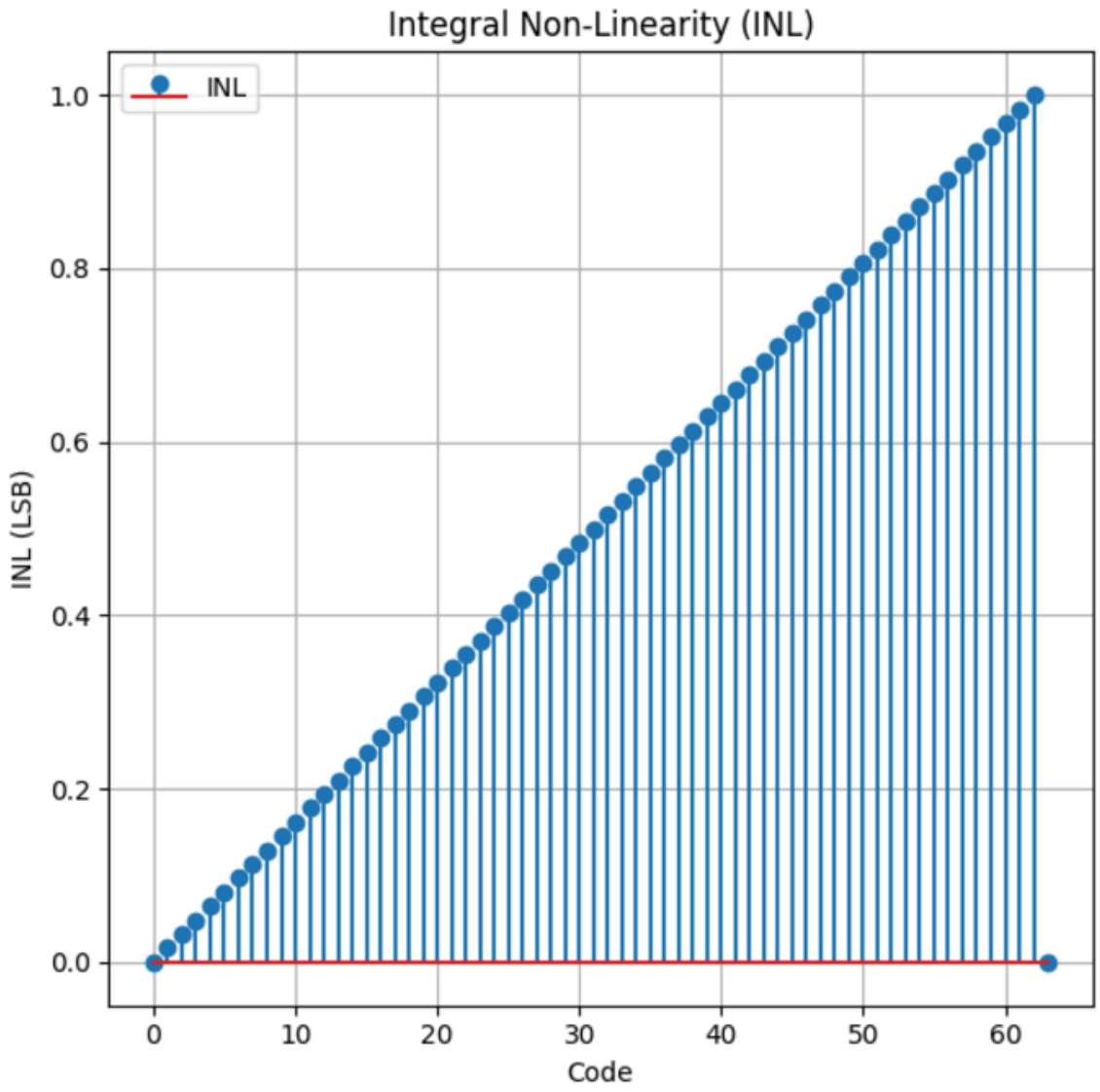
RESULTS



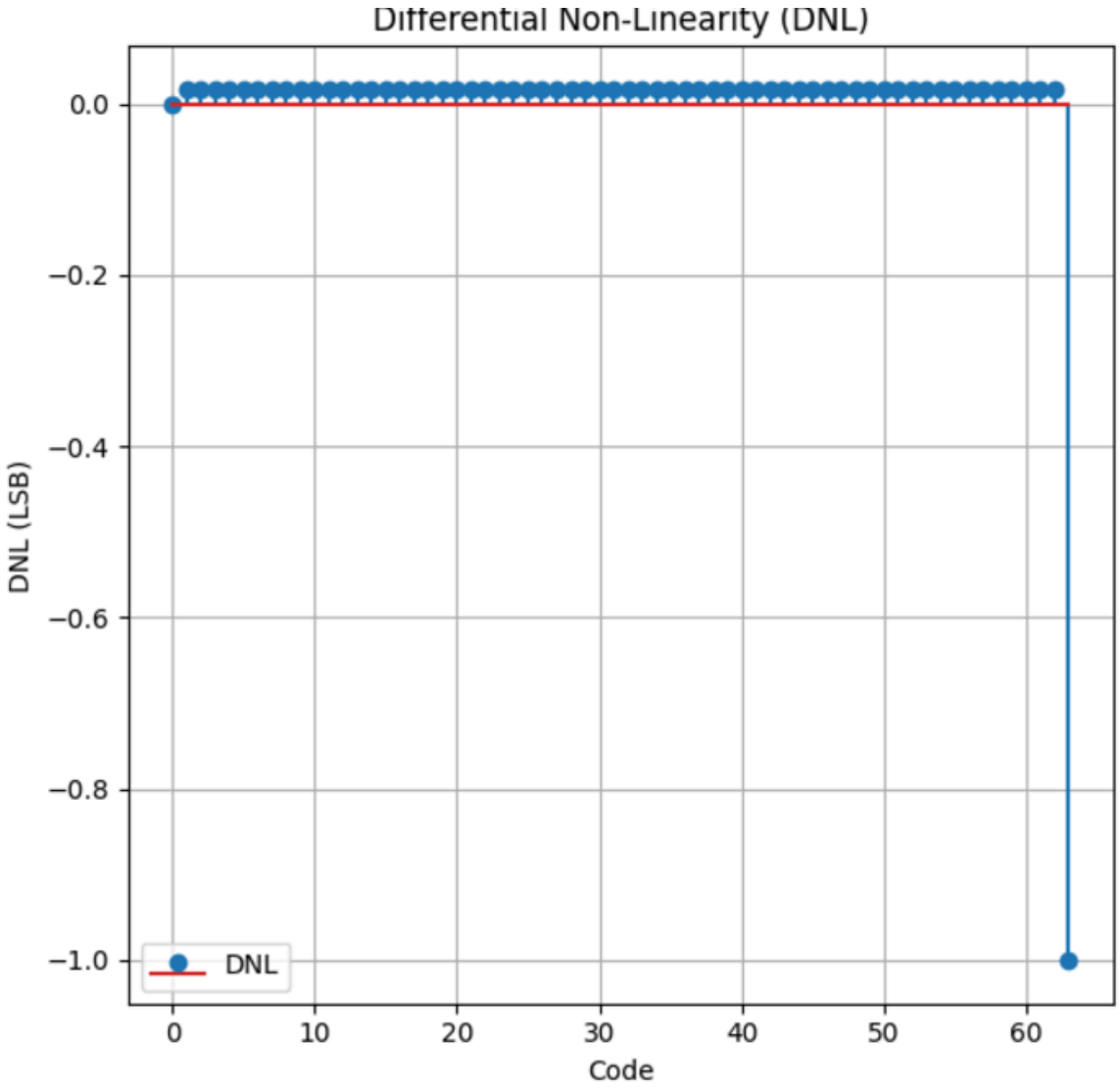
Power:

P=V*I=1.8*0.524=0.9432mW

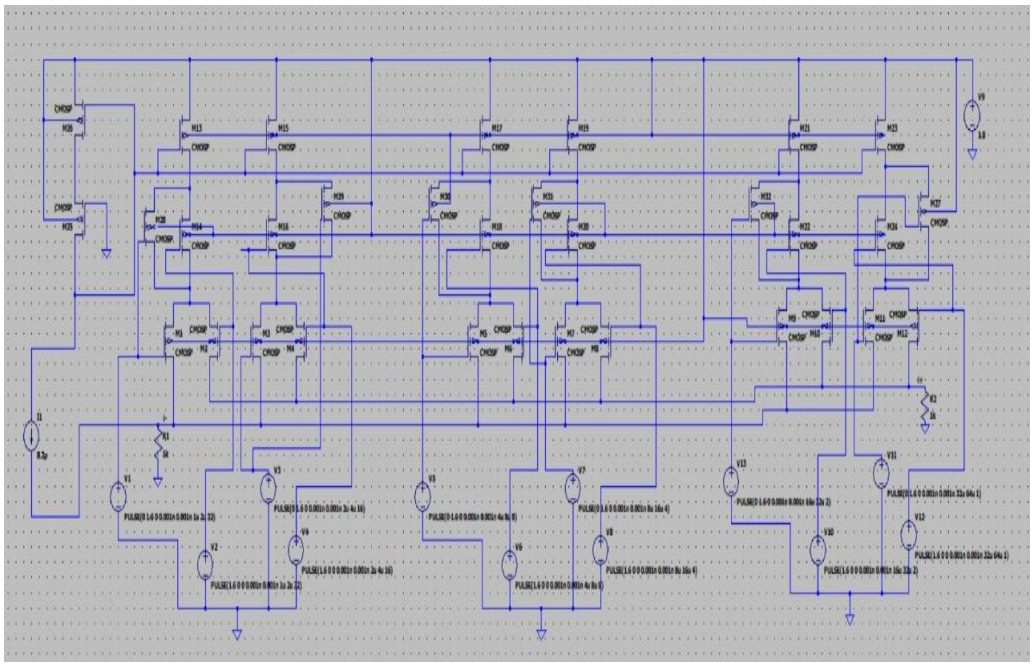
INL


Integral Non-Linearity (INL)
INL
INL (LSB)
1.0
0.8
0.6
0.4
0.2
0.0
0
10
20
30
40
50
60
Code

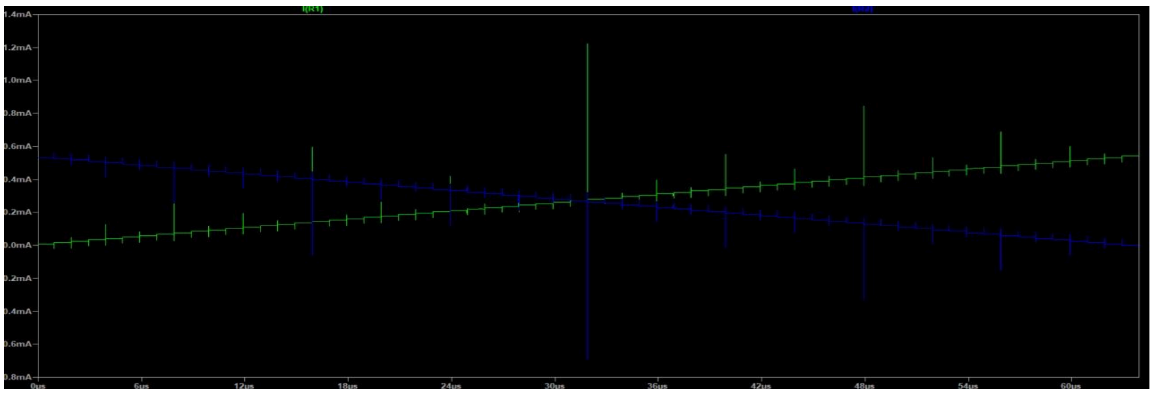
DNL


Differential Non-Linearity (DNL)
DNL (LSB)
0.0
−0.2
−0.4
−0.6
−0.8
−1.0
DNL
0
10
20
30
40
50
60
Code

DAC using PMOS current sources



RESULTS



DAC Using Row-Column decoder

BLOCK DIAGRAM:

let take b0 b1 b2 to decode Column and

b3 b4 b5 to decode Row.

1.Column decoder:

b2	b1	b0	c0	c1	c2	c3	c4	c5	c6	c7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0
0	1	0	1	1	1	0	0	0	0	0
0	1	1	1	1	1	1	0	0	0	0
1	0	0	1	1	1	1	1	0	0	0
1	0	1	1	1	1	1	1	1	0	0
1	1	0	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1

c0=1

c1=b0+b1+b2

c2=b1+b2

c3=b0b1+b2

c4=b2

c5=(b0+b1)b2

c6=b1b2

c7=b0b1b2

2.Row Decoder:

b5	b4	b3	r0	r1	r2	r3	r4	r5	r6	r7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0
0	1	0	1	1	1	0	0	0	0	0
0	1	1	1	1	1	1	0	0	0	0
1	0	0	1	1	1	1	1	0	0	0
1	0	1	1	1	1	1	1	1	0	0
1	1	0	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1

r0=1

r1=b3+b4+b5

r2=b4+b5

r3=b3b4+b5

r4=b5

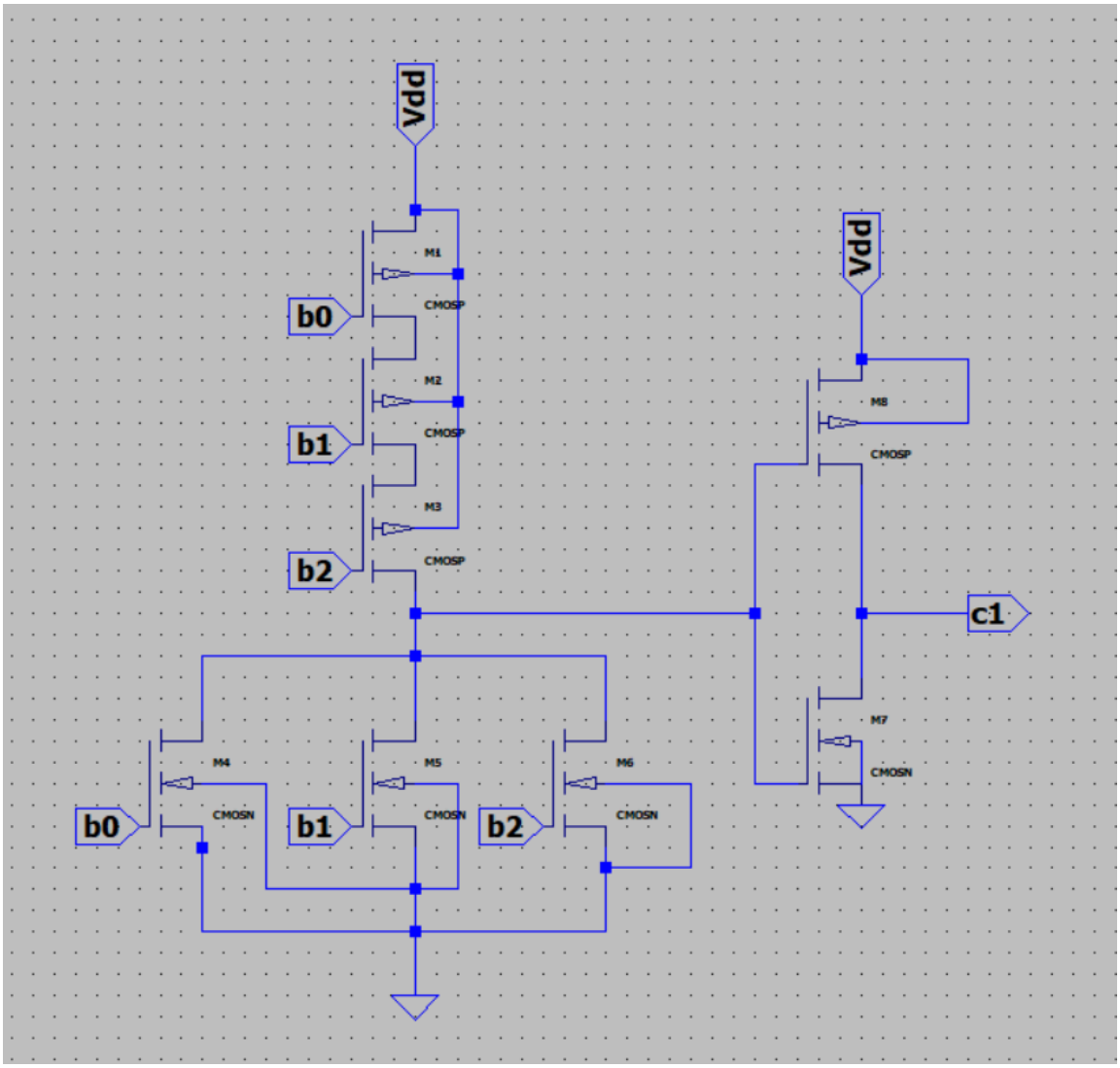
r5=(b3+b4)b5

r6=b4b5

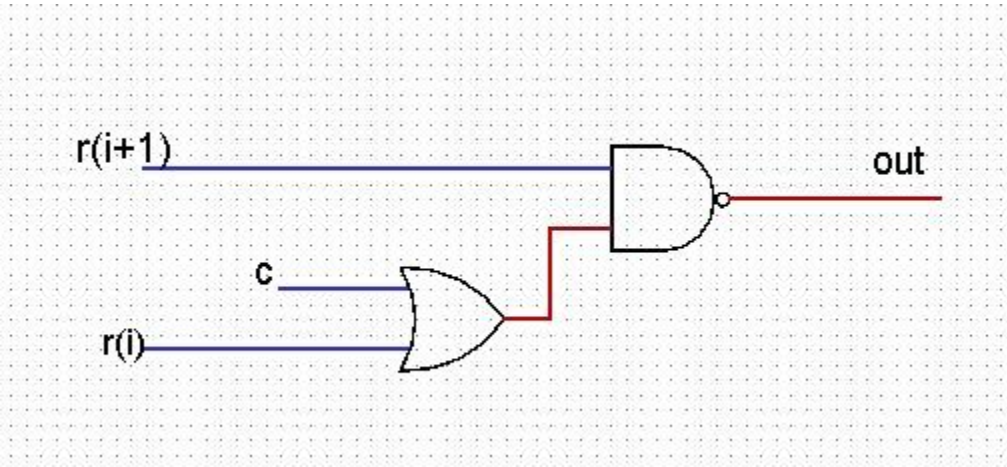
r7=b3b4b5

Example to decode c0:

using MOSFETs :

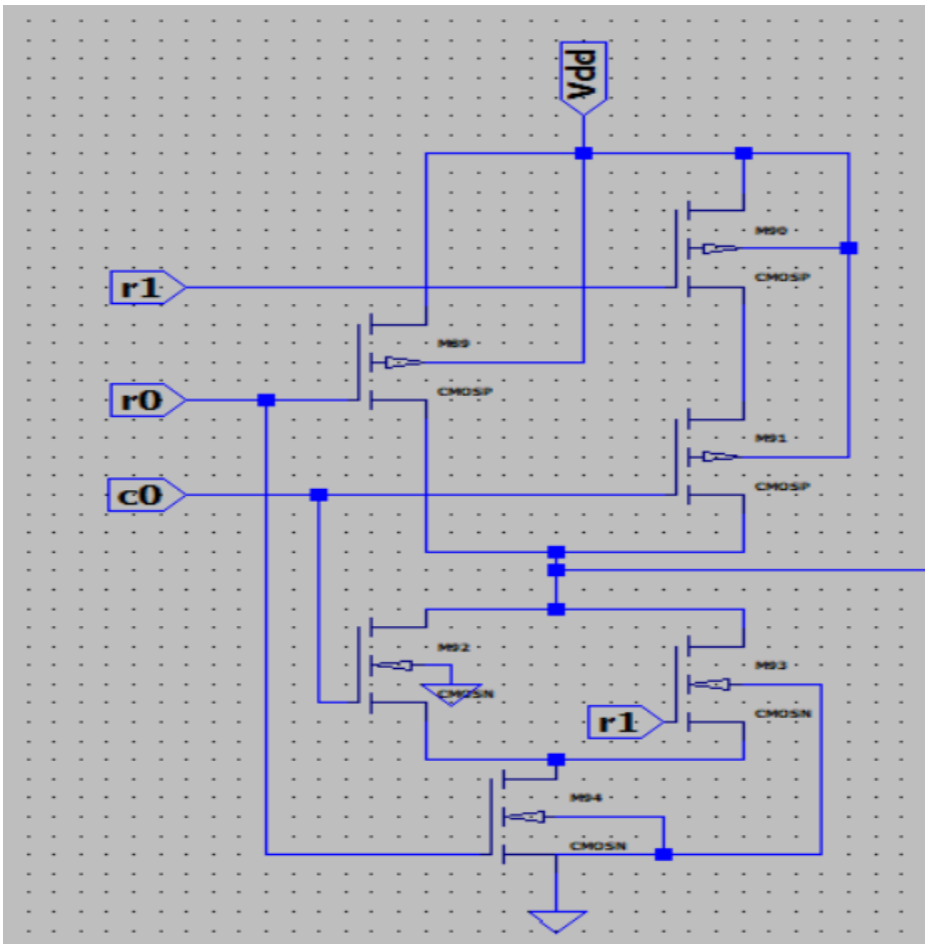


LOGIC to ON or OFF the current source:

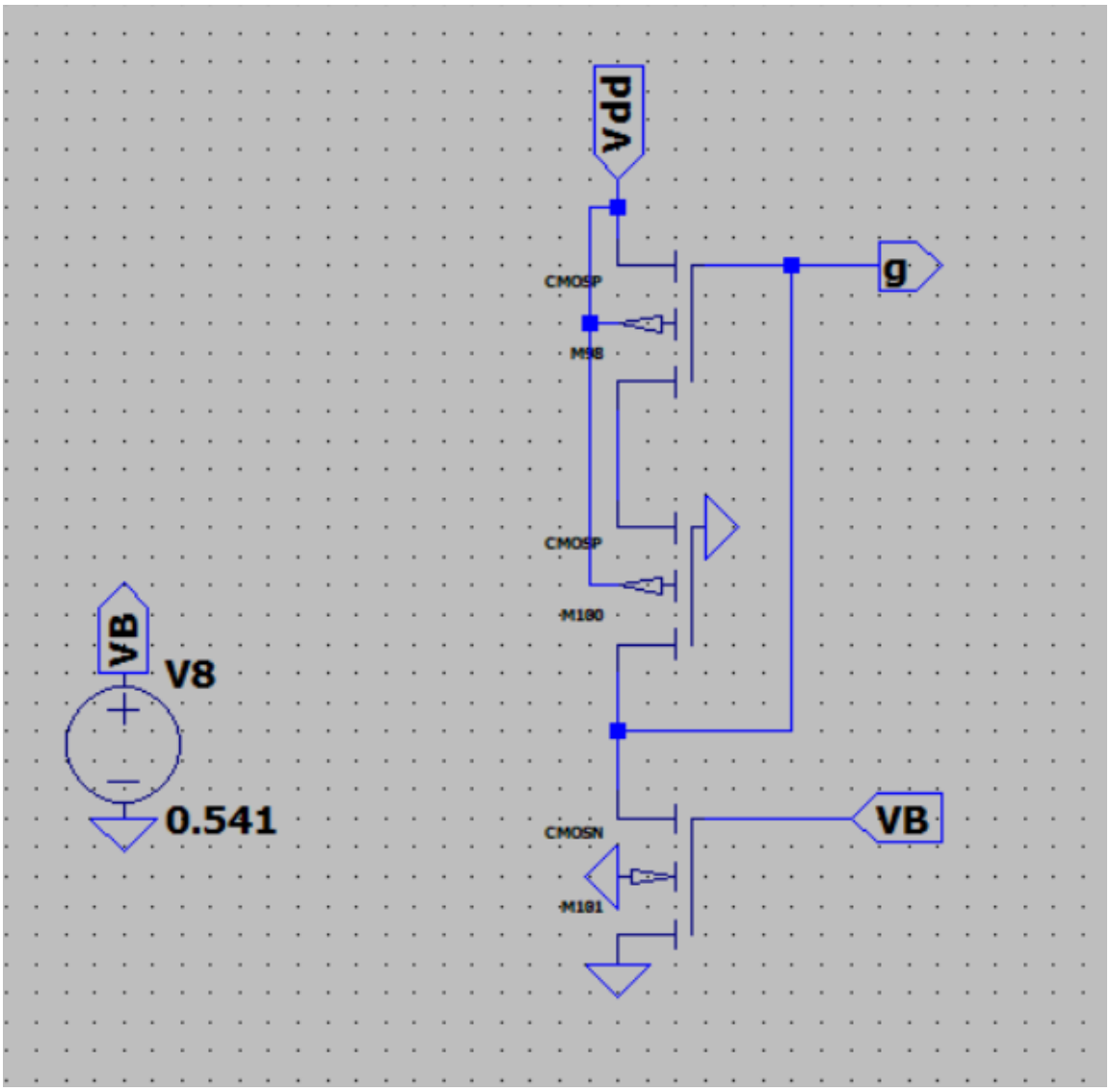


out=((c(i)+r(i))r(i+1))'

Logic for 0th current source:



Current Mirror Circuit:

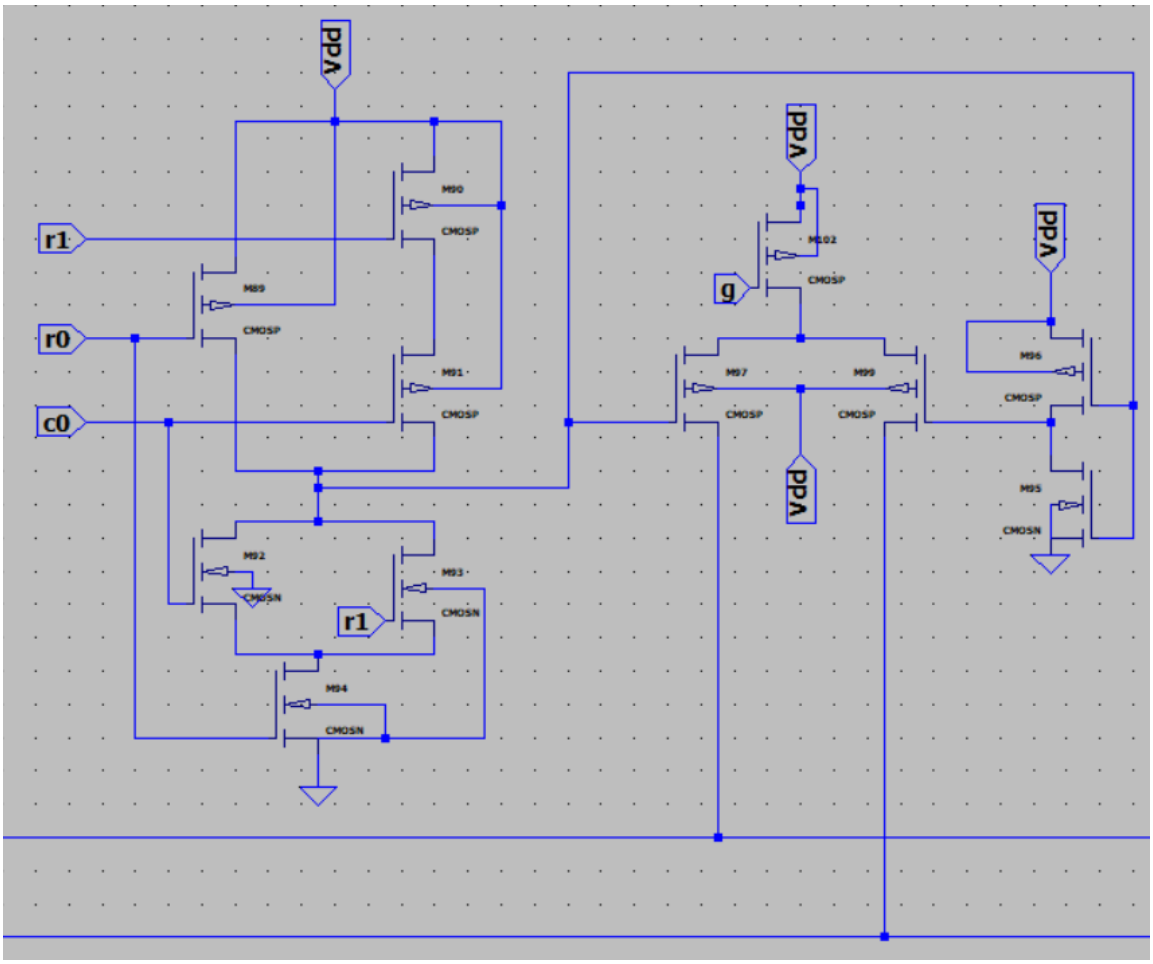


1.The two PMOS transistors form a **current mirror** in the top half of the circuit. The gate and drain of one PMOS transistor (M98) are connected to ensure it operates in saturation, while the other transistor (M180) mirrors the current.

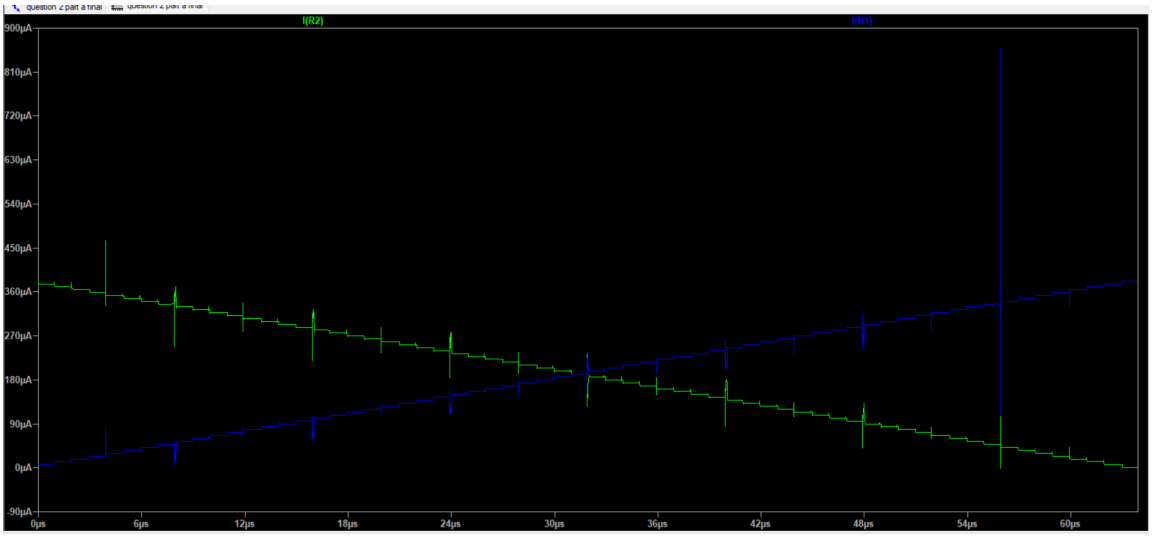
2.The NMOS transistors at the bottom also form a current mirror. They are likely used to sink the mirrored current or to stabilize the circuit.

3.The labeled node g is the output of the circuit, where the current is transferred.

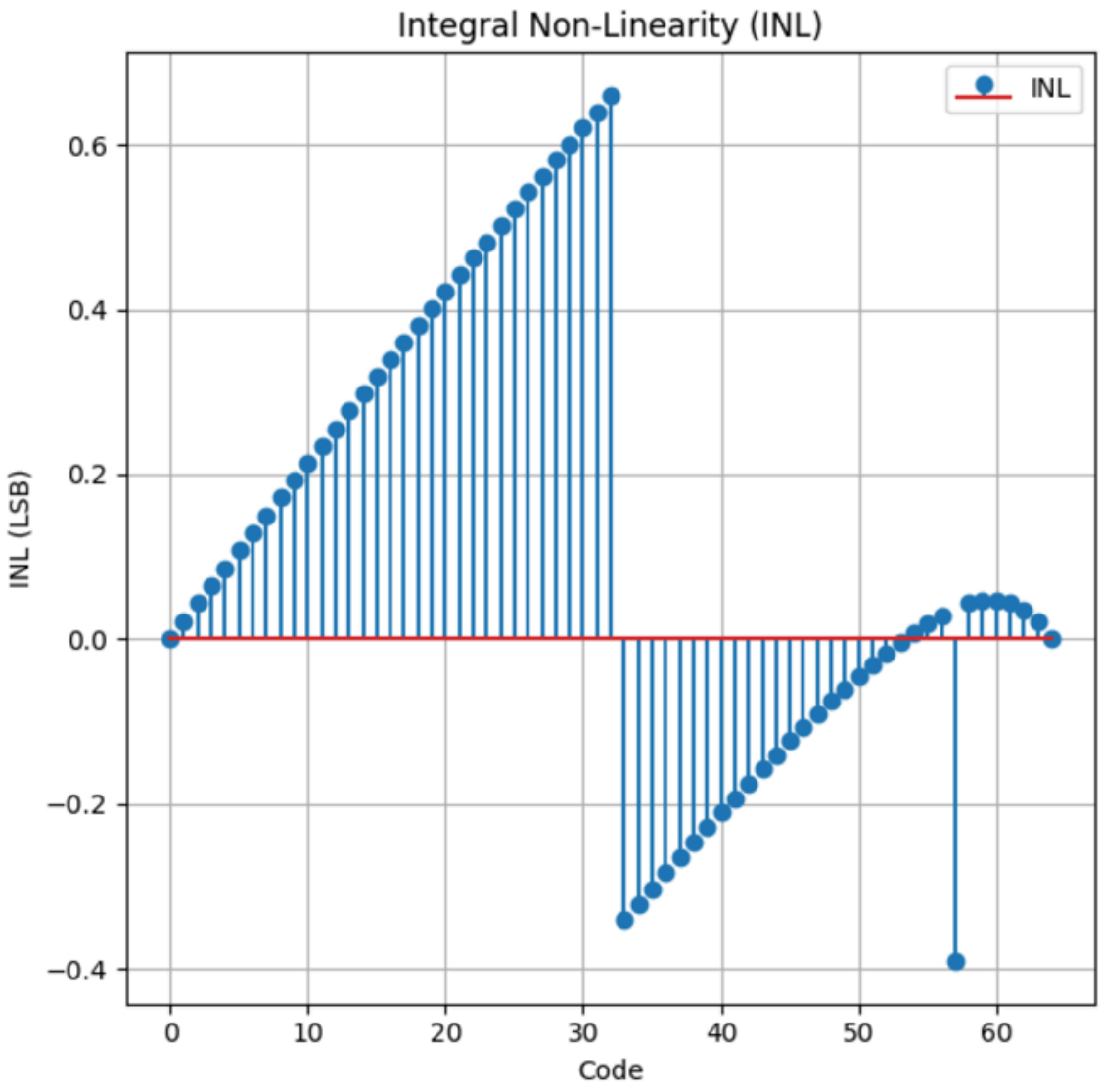
Zeroth block with unit current source and logic:



Result:


I(R2)
I(R1)
900µA
810µA
720µA
630µA
540µA
450µA
360µA
270µA
180µA
90µA
0µA
-90µA
0µs
6µs
12µs
18µs
24µs
30µs
36µs
42µs
48µs
54µs
60µs

INL:


Integral Non-Linearity (INL)
INL
INL (LSB)
0.6
0.4
0.2
0.0
−0.2
−0.4
0
10
20
30
40
50
60
Code

ds

DNL: