EC 445- Techniques in Low Power VLSI

Design of Multi-Bit Full Adder Using Low Power m-GDI Technique

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Abstract

The rapid advancement in portable and embedded electronic devices necessitates the development of low-power and high-performance arithmetic circuits. Among these, the full adder is a fundamental building block used in arithmetic and logic units (ALUs), multipliers, digital signal processors, and other data processing units. The efficiency of these complex circuits is heavily dependent on the design of the full adder unit. This project explores the design and implementation of a multi-bit full adder using the Modified Gate Diffusion Input (m-GDI) technique, which is known for its low-power and area-efficient characteristics. By utilizing m-GDI logic, the circuit achieves significant reductions in power consumption, delay, and transistor count compared to conventional CMOS-based designs. The design was implemented and simulated using the Cadence Virtuoso design suite with 180nm technology. Extensive simulations were carried out to validate the functionality and performance of the proposed design. The results highlight the superiority of m-GDI logic in achieving optimal power-delay product (PDP), making it a viable solution for modern low-power VLSI systems.

Introduction

With the emergence of handheld and battery-operated devices, power efficiency has become a critical parameter in the design of integrated circuits. One of the core operations in digital systems is arithmetic computation, where the full adder plays a pivotal role. A full adder circuit performs the addition of three binary inputs—two significant bits and one carry-in bit—and produces two outputs: a sum and a carry-out.

In traditional VLSI systems, the full adder is realized using CMOS technology, which provides robust noise margins and full voltage swing. However, these implementations often suffer from high power consumption, greater area requirements, and reduced speed due to higher transistor counts. Consequently, researchers have proposed several alternate logic families to overcome these drawbacks, among which the Gate Diffusion Input (GDI) technique stands out due to its low-power and compact design characteristics.

The m-GDI technique is a modification of the standard GDI method, tailored for compatibility with standard CMOS fabrication processes. It allows the implementation of logic functions using a smaller number of transistors without compromising logic swing and robustness. This project presents the design and evaluation of a multi-bit full adder using m-GDI logic and demonstrates its benefits over conventional designs in terms of power, delay, and overall efficiency.

Objectives

The primary aim of this project is to investigate and implement an energy-efficient design for multi-bit full adders using the Modified Gate Diffusion Input (m-GDI) technique. The specific objectives of the project are:

- To design a single-bit full adder circuit using the m-GDI approach, aiming to minimize the number of transistors while maintaining functional correctness.
- To extend the single-bit design into a multi-bit full adder structure (specifically a 4-bit ripple carry adder) to evaluate scalability and integration.
- To analyze and compare the performance of the m-GDI full adder against the conventional CMOS full adder design in terms of power consumption, propagation delay, and power-delay product (PDP).
- To simulate and verify the proposed designs using industry-grade tools such as Cadence Virtuoso under a 180nm CMOS technology node.
- To identify challenges and limitations in m-GDI design and propose recommendations for future research and optimization.

Literature Review

The full adder is a fundamental component in digital arithmetic circuits and has undergone various optimizations to meet the demands of modern low-power and high-speed applications.

The truth table for a **1-bit full adder** is shown below:

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure: Full Adder Truth table

The Boolean expressions for the outputs are:

- Sum = $A \oplus B \oplus Cin$
- Carry-out (Cout) = $A.B + B.Cin + A.Cin = = A.B + (A \oplus B).Cin$

Over the years, several architectures have been proposed to optimize the full adder in terms of power, speed, and area:

1. Static CMOS Full Adder (FA): The traditional full adder design uses static CMOS logic, employing complementary pull-up and pull-down networks to realize logic gates. While this approach offers good noise margins and full output voltage swing, it results in a high transistor count—typically 28 transistors for a complete adder. The larger area and increased parasitic capacitances associated with static CMOS design lead to higher power consumption and slower switching speeds, making it less suitable for energy-constrained applications.

2. Transmission Gate Full Adder (TG FA): To mitigate some of the drawbacks of static CMOS, Transmission Gate-based full adders have been developed. These designs reduce the transistor count by replacing certain logic blocks with transmission gates that pass logic levels more efficiently. TG FAs generally consume less power and occupy less area than CMOS FAs. However, they introduce challenges in signal integrity and may require additional buffers to restore logic levels, especially in deep submicron technologies.

3. Hybrid Full Adder: Hybrid FAs combine various logic styles such as CMOS, pass transistor logic (PTL), transmission gate logic, and others to optimize power and performance. For example, the carry logic might use pass transistor logic for speed, while the sum logic uses CMOS for robustness. These designs attempt to strike a balance between speed, power, and voltage swing. Although hybrid FAs offer improved efficiency compared to pure CMOS or TG implementations, the design process is more complex, and interfacing between different logic styles may introduce additional delay.

4. Proposed m-GDI Full Adder: The Modified Gate Diffusion Input (m-GDI) technique is a refinement of the original GDI method, adapted for compatibility with standard CMOS processes. In m-GDI, logic gates are realized with a minimal number of transistors, typically 8–10 for a full adder, without compromising functional correctness. The core advantage of m-GDI lies in its ability to implement various logic functions using a single cell structure, significantly reducing the area and dynamic power consumption.

Moreover, m-GDI designs overcome the fabrication limitations of classical GDI by ensuring proper source and bulk connections that comply with CMOS manufacturing rules. The proposed m-GDI-based full adder demonstrates superior performance in terms of reduced power consumption, lower delay, and improved power-delay product (PDP). These characteristics make it highly suitable for VLSI systems targeting portable and embedded applications.

Comparative studies in literature have shown that m-GDI full adders outperform CMOS, TG, and hybrid designs under identical simulation conditions, particularly in low-voltage operations. Their compactness, energy efficiency, and scalability make them a promising choice for next-generation arithmetic circuits.

Methodology

1. **Technology and Toolchain**
    - The design was implemented using Cadence Virtuoso, a professional EDA tool widely used in industry.
    - Simulations were carried out using Spectre simulator with a 180nm CMOS technology process.

2. **Design Process**
    - Boolean expressions for the sum and carry of the full adder were derived:
        - SUM = $A \oplus B \oplus Cin$
        - CARRY = $A.B + B.Cin + A.Cin = A.B + (A \oplus B).Cin$
    - These expressions were implemented using optimized m-GDI logic circuits to minimize transistor usage.
    - The m-GDI structure was tailored to provide full voltage swing and minimize short-circuit current.

3. **1-Bit Adder Construction and Validation**
    - Four architectures were constructed: CMOS, Transmission Gate (TG), Hybrid, and m-GDI based 1-bit full adders.
    - Each design was simulated individually to verify functional correctness and measure power, delay, and PDP metrics.

4. **Multi-Bit Extension and Comparison**
    - Each 1-bit architecture was expanded to form 4-bit and 8-bit ripple carry adders.
    - Cascading of full adder blocks was done by connecting the carry-out of each stage to the carry-in of the next.

- Comparative analysis was conducted for 4-bit and 8-bit versions of all architectures to evaluate how performance metrics scale.

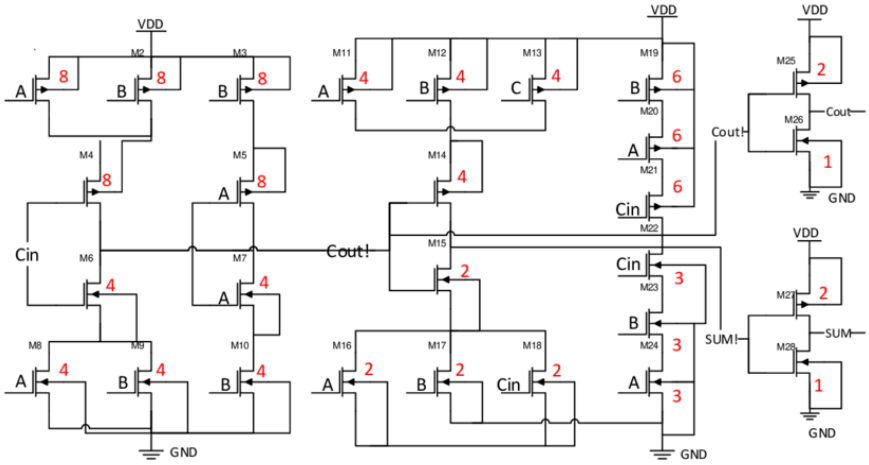


Figure: Circuit of Static CMOS based Full Adder

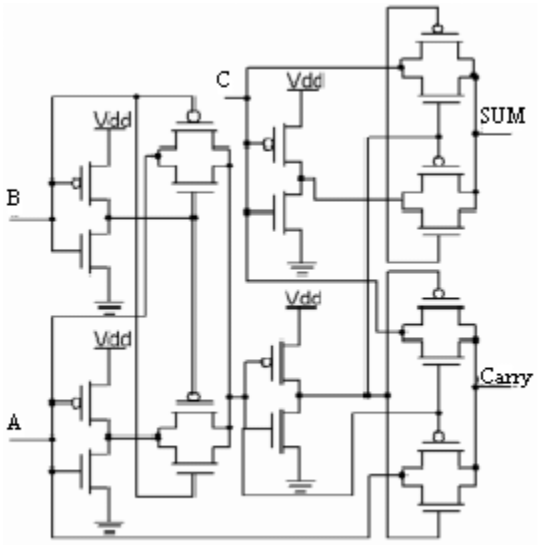


Figure: Transmission Gate based Full Adder

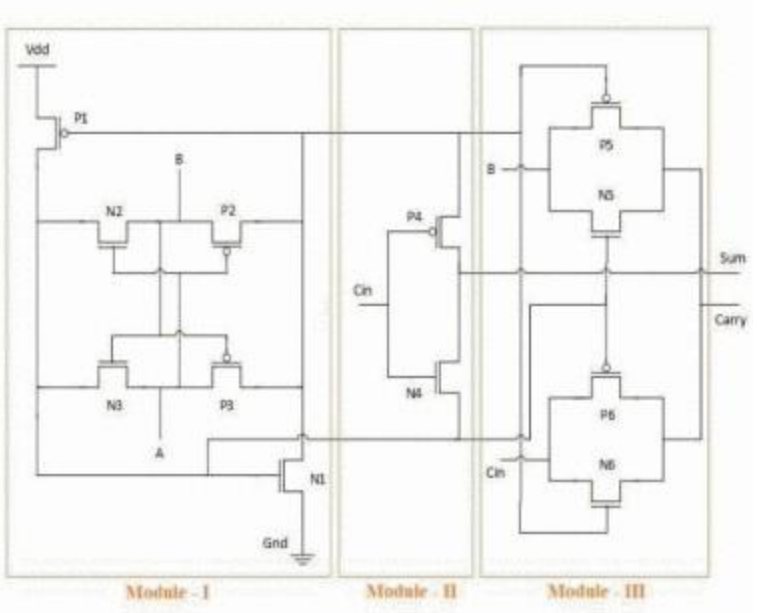


Figure: Hybrid Full adder adder using 12T

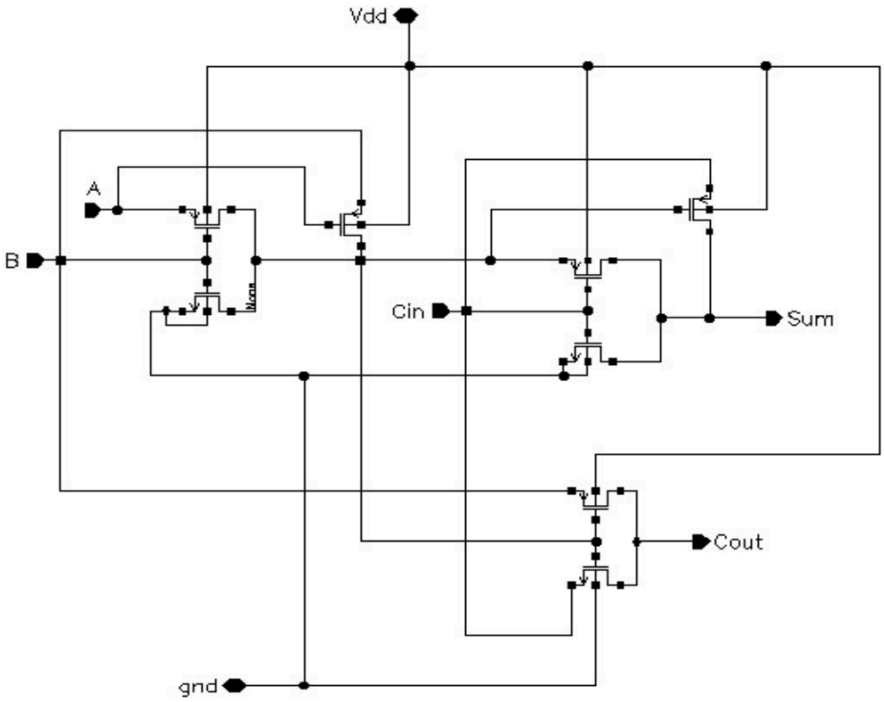


Figure: The structural design of full adder using the proposed GDI

Technique.

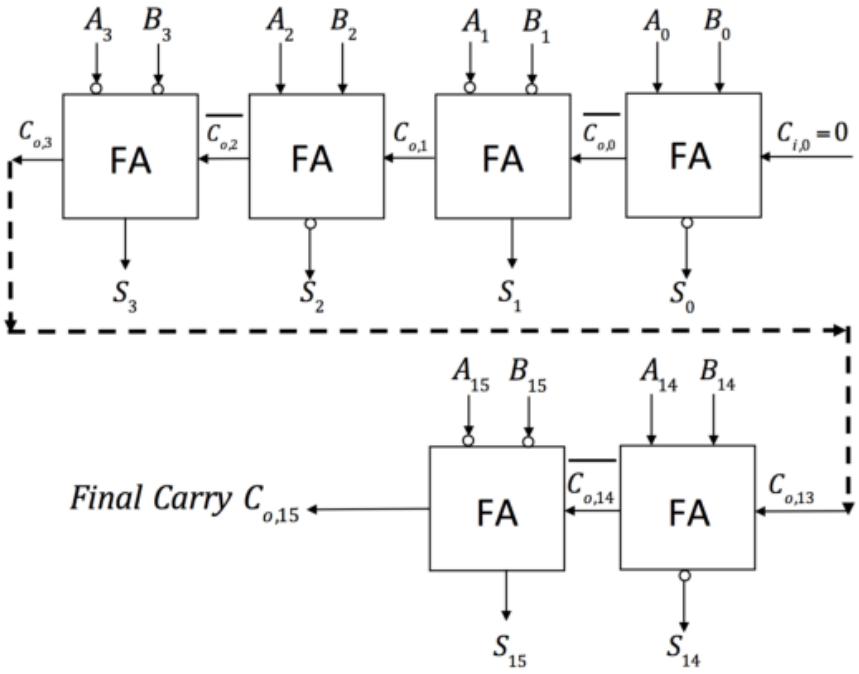


Figure: Structure of n-bit Full Adder

5. **Simulation and Verification**
    - DC and transient simulations were conducted to validate the functionality of the full adders at each bit-width.
    - Power consumption was measured by averaging the transient current over a set of input vectors.
    - Delay was calculated by measuring the time interval between input transition and output response.

6. **Comparison Setup**
    - A conventional CMOS-based full adder was also implemented using standard 28-transistor logic.
    - Both designs were tested under identical conditions for a fair comparison.

Cadence Virtuoso Schematics:

1. Static CMOS based adder:

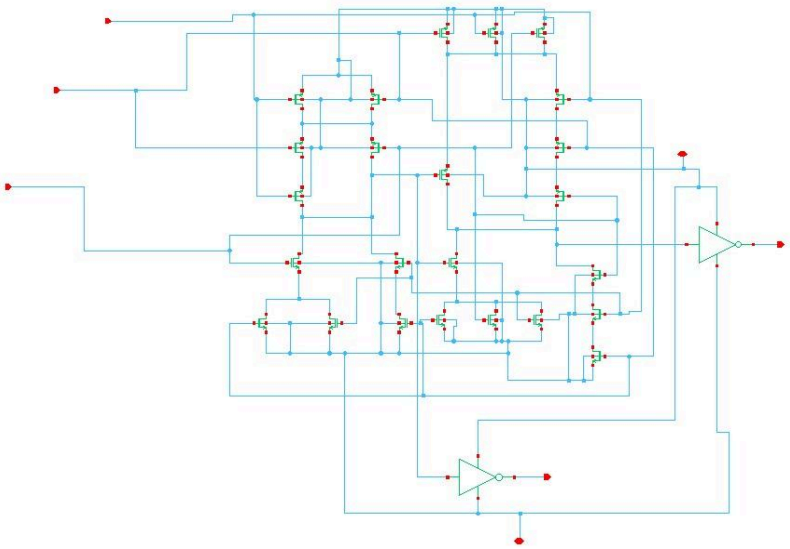


Figure: SCMOS based Full Adder

2. Transmission Gate based adder:

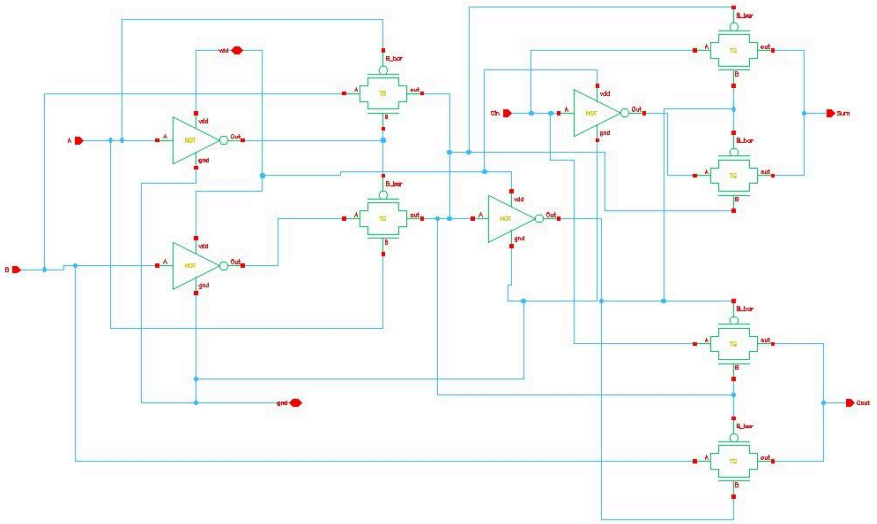


Figure: TG based FA

3. Hybrid Full Adder:

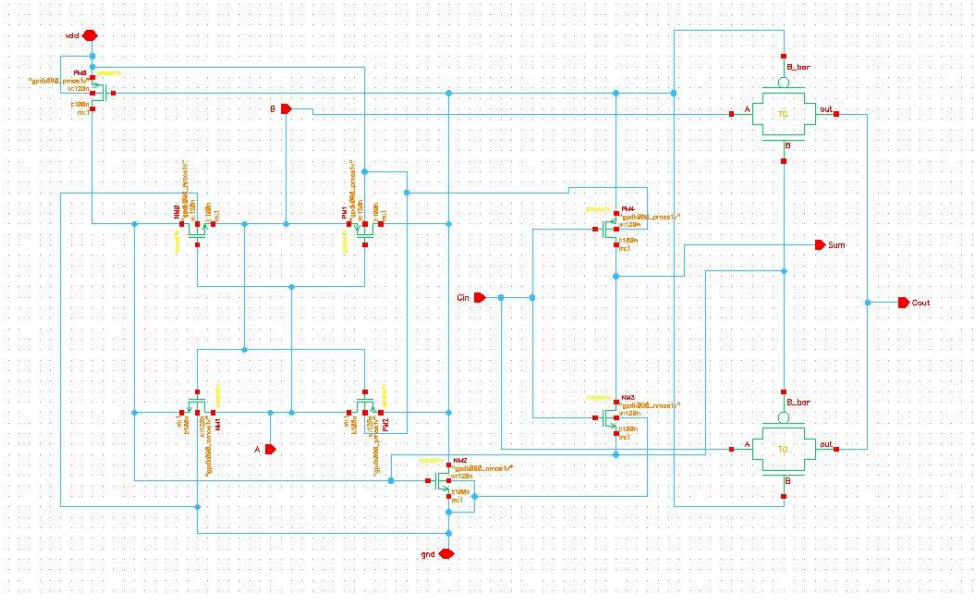


Figure: Hybrid Full Adder

4. Full Adder based on proposed GDI Technique:

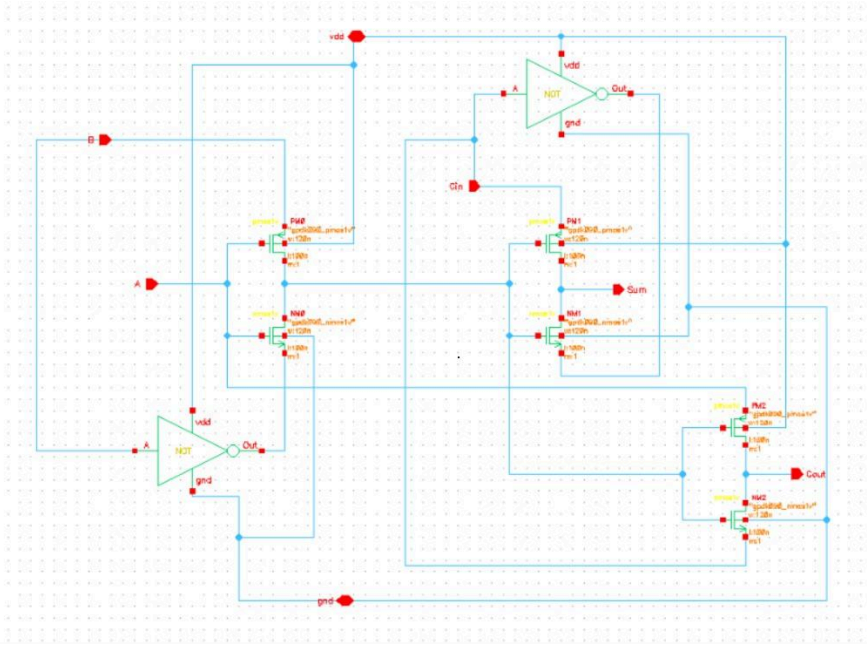


Figure: GDI based Full Adder

5. 4-bit SCMOS Full Adder:

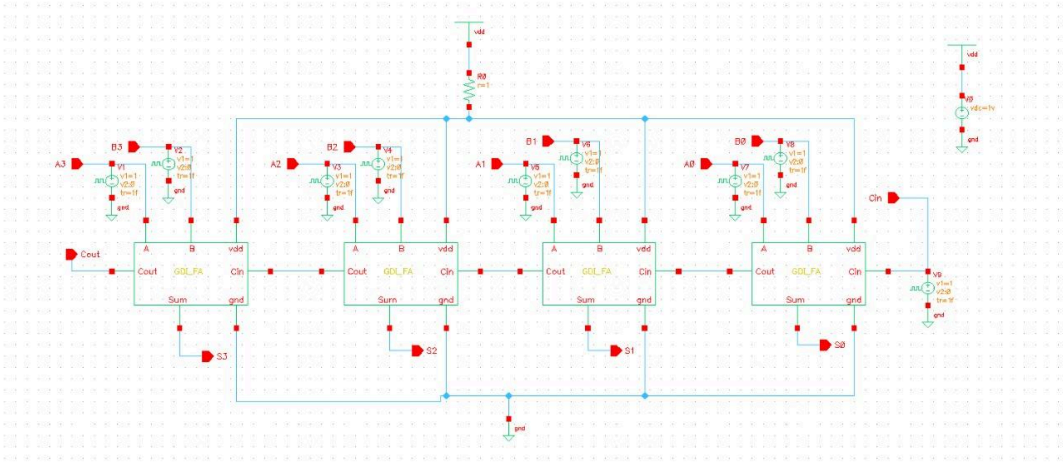


Figure: 4-bit Cascaded Full Adder

6. 8-bit SCMOS Full Adder:

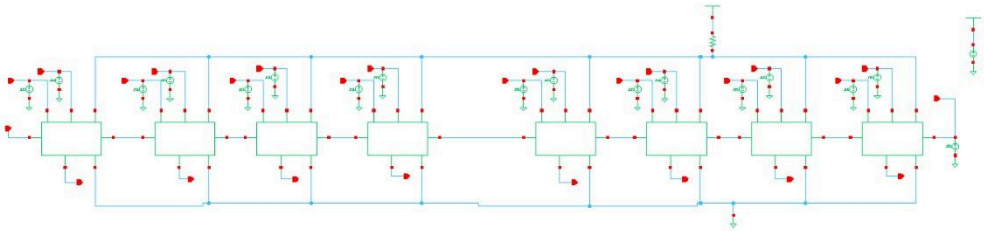
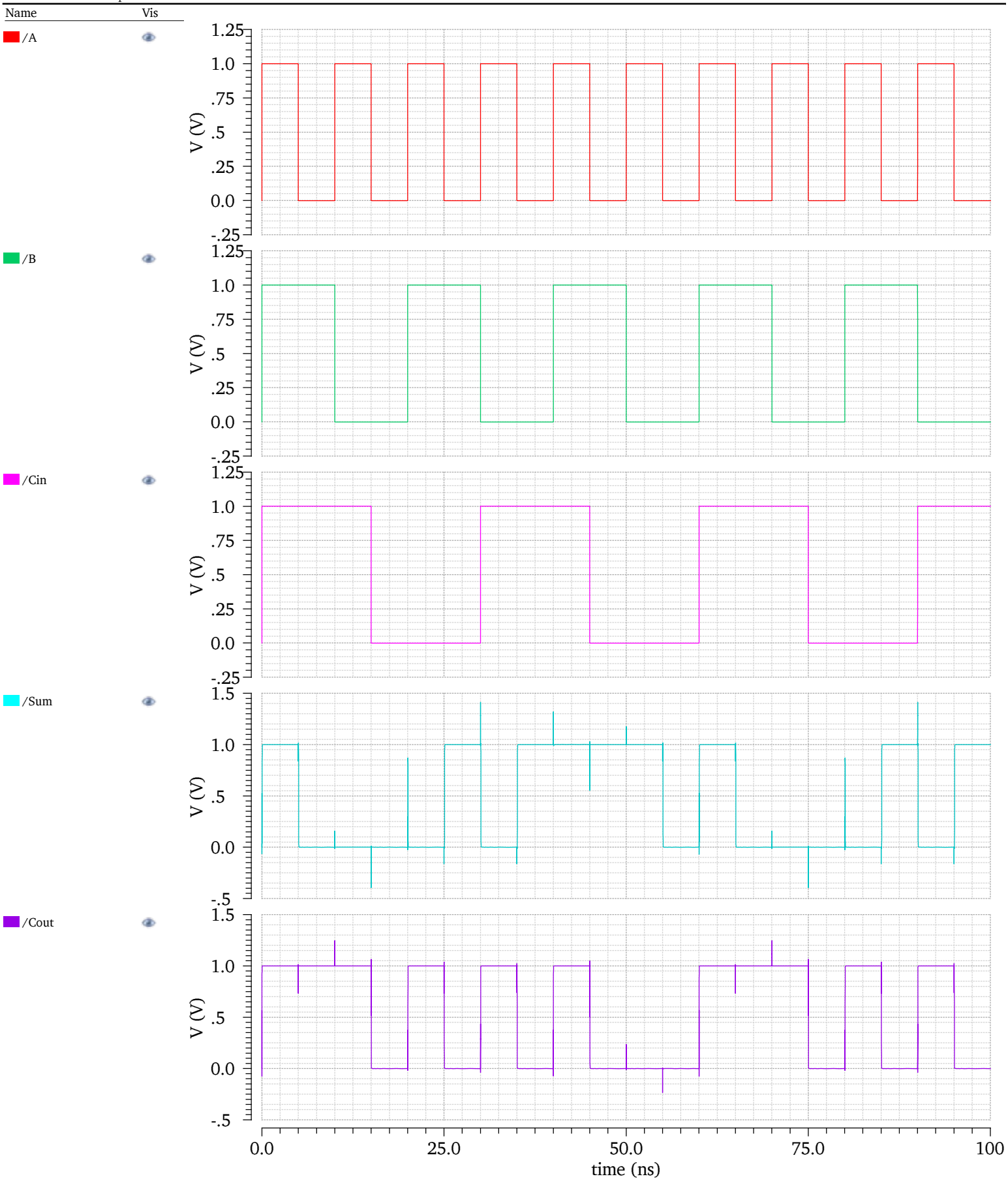


Figure: 8-bit Full Adder

Transient Response



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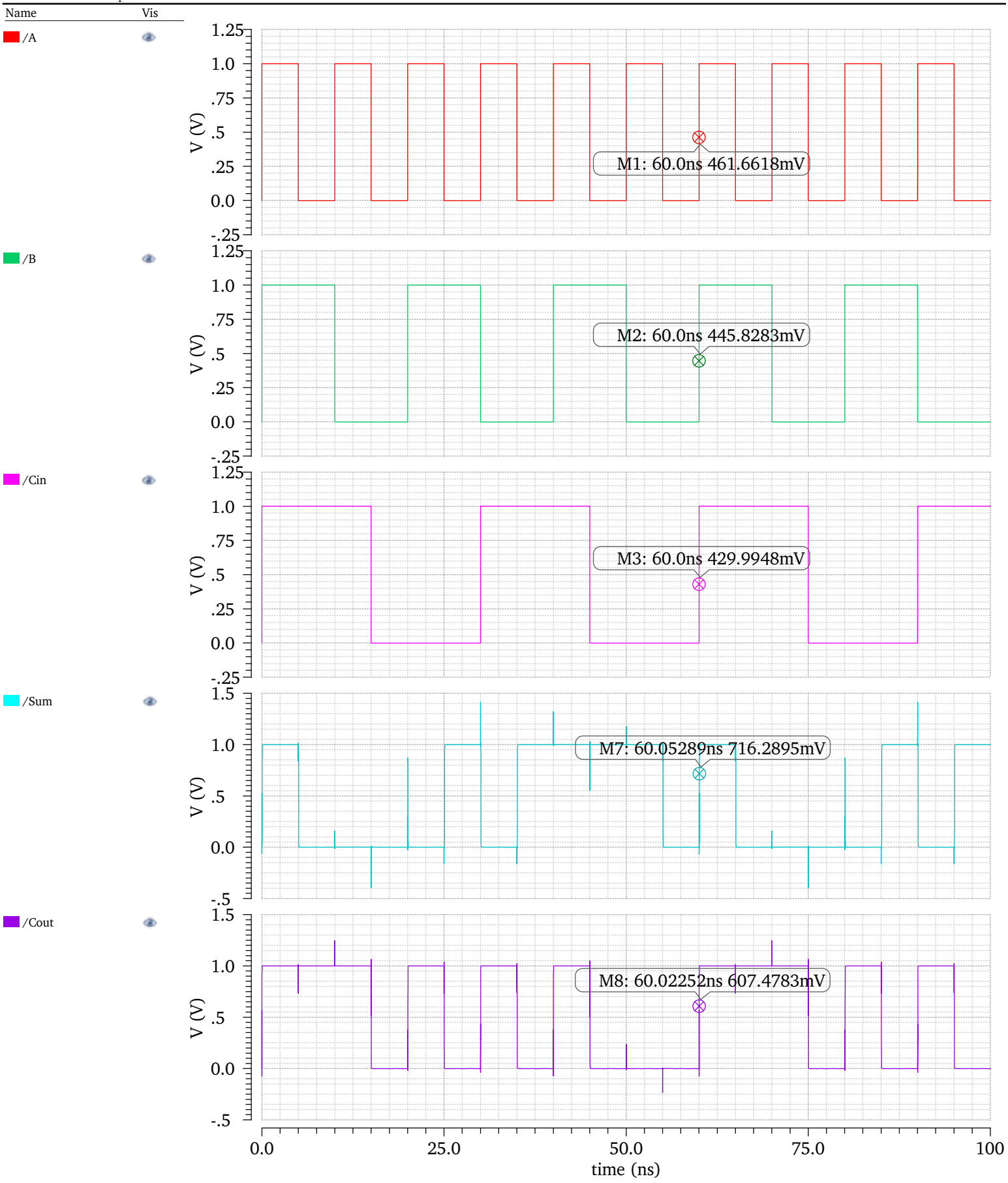

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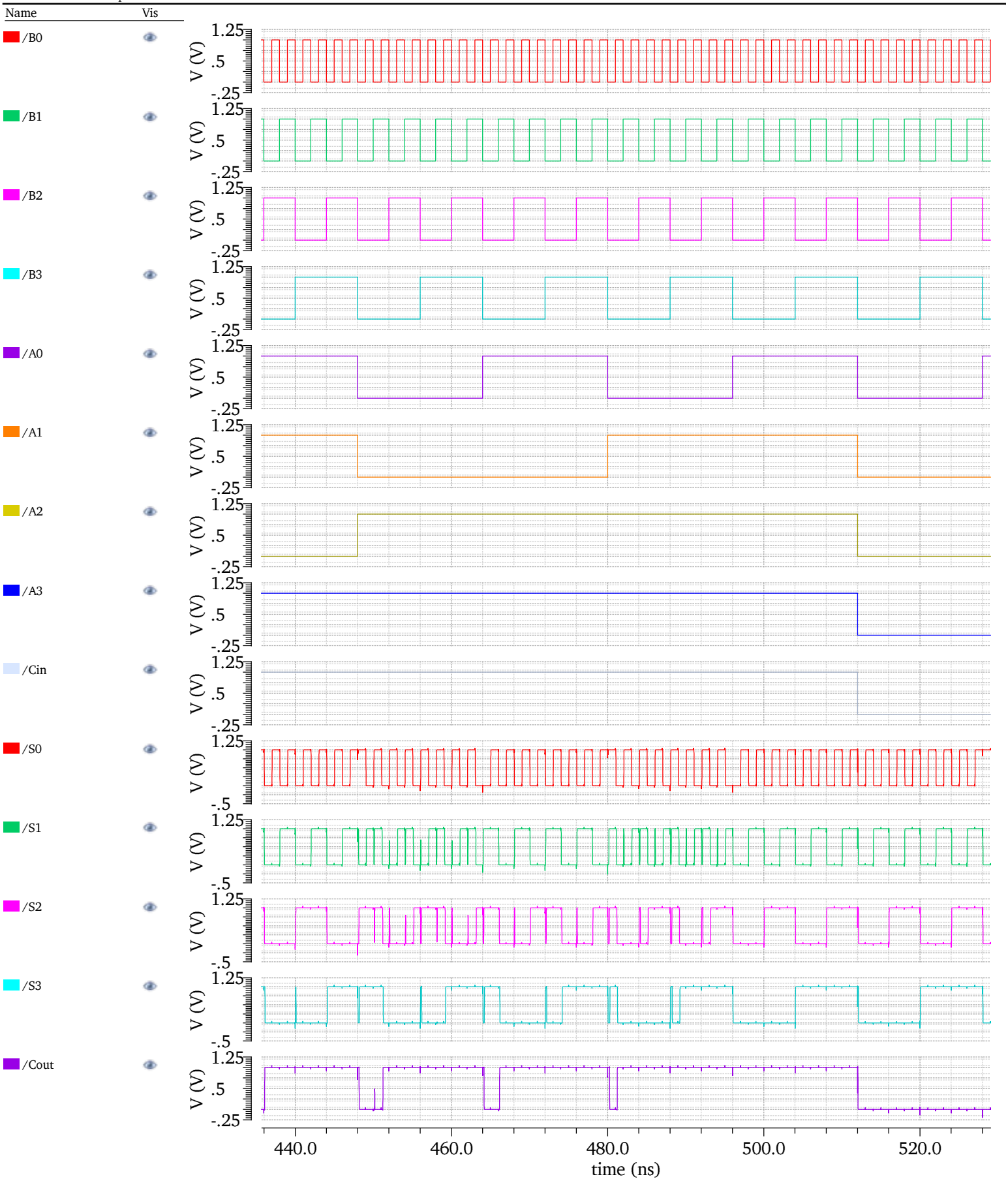

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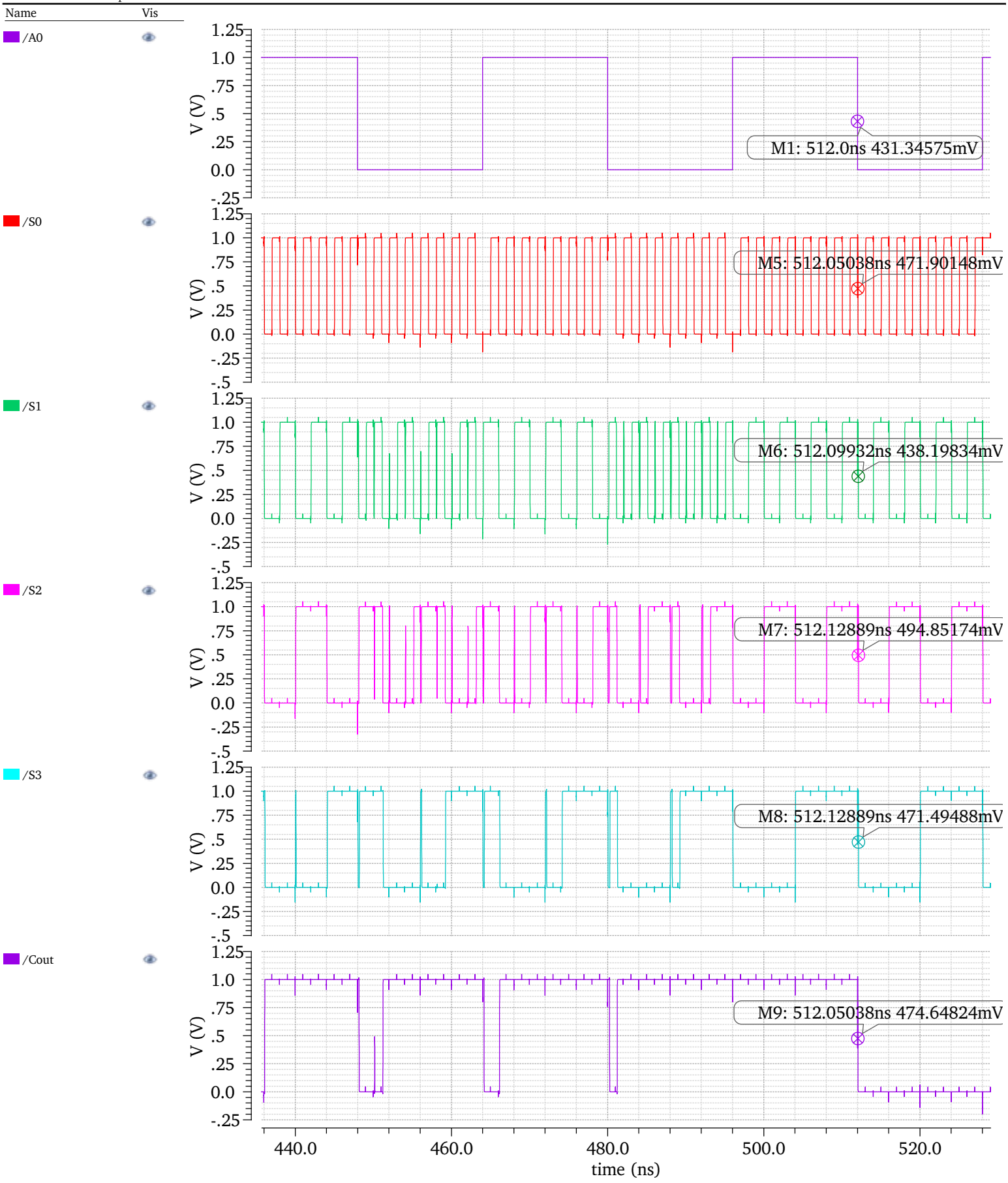

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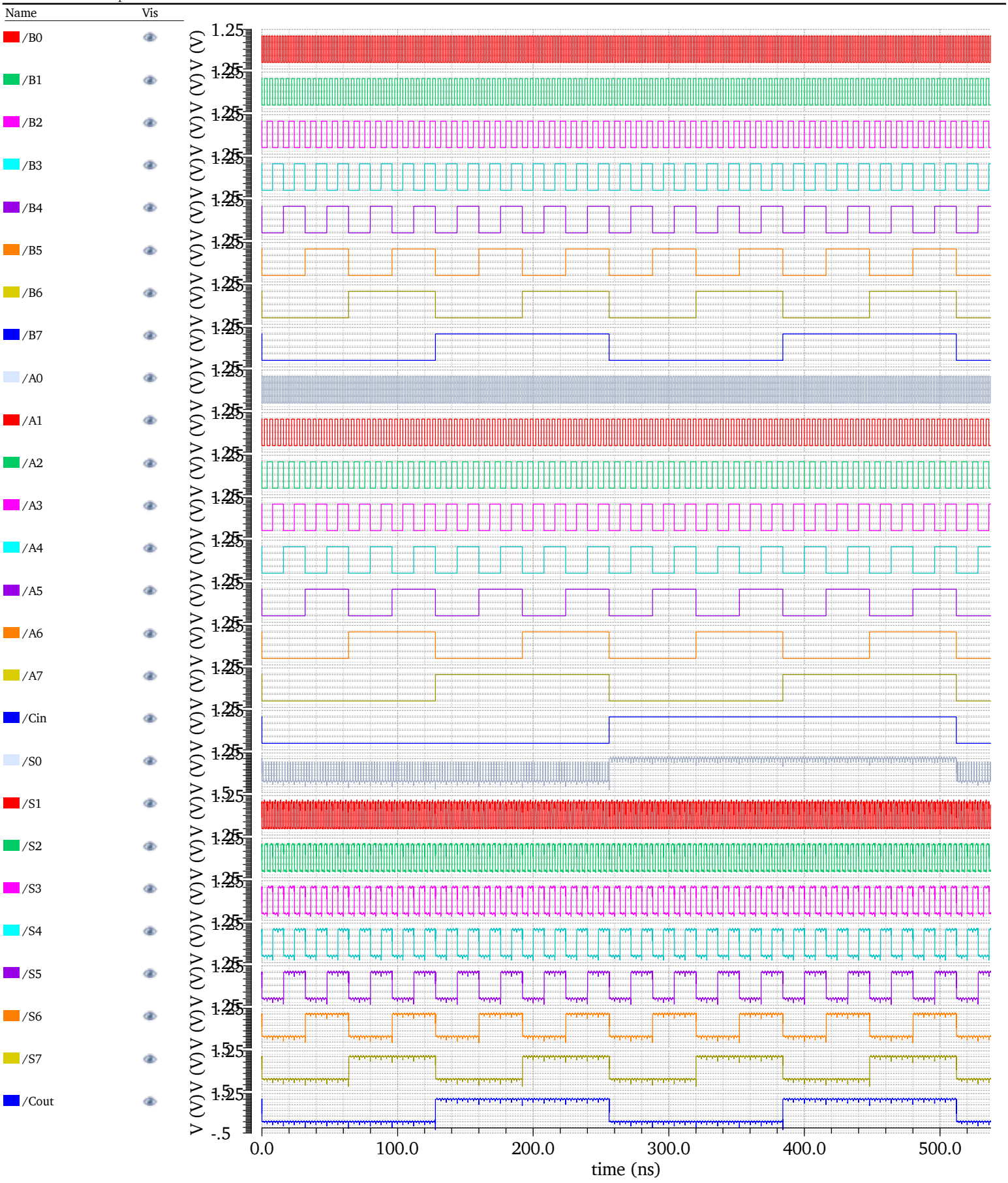

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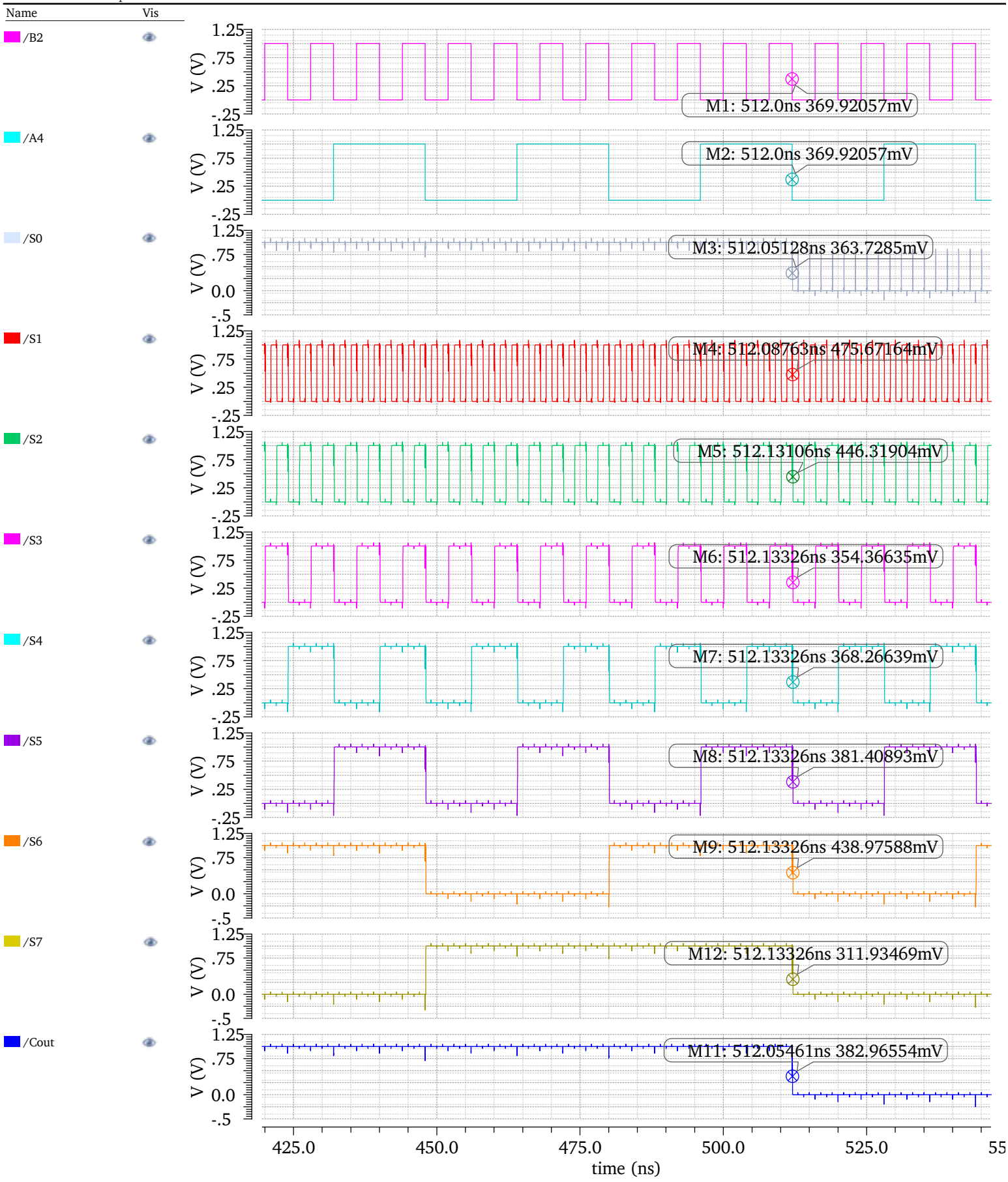

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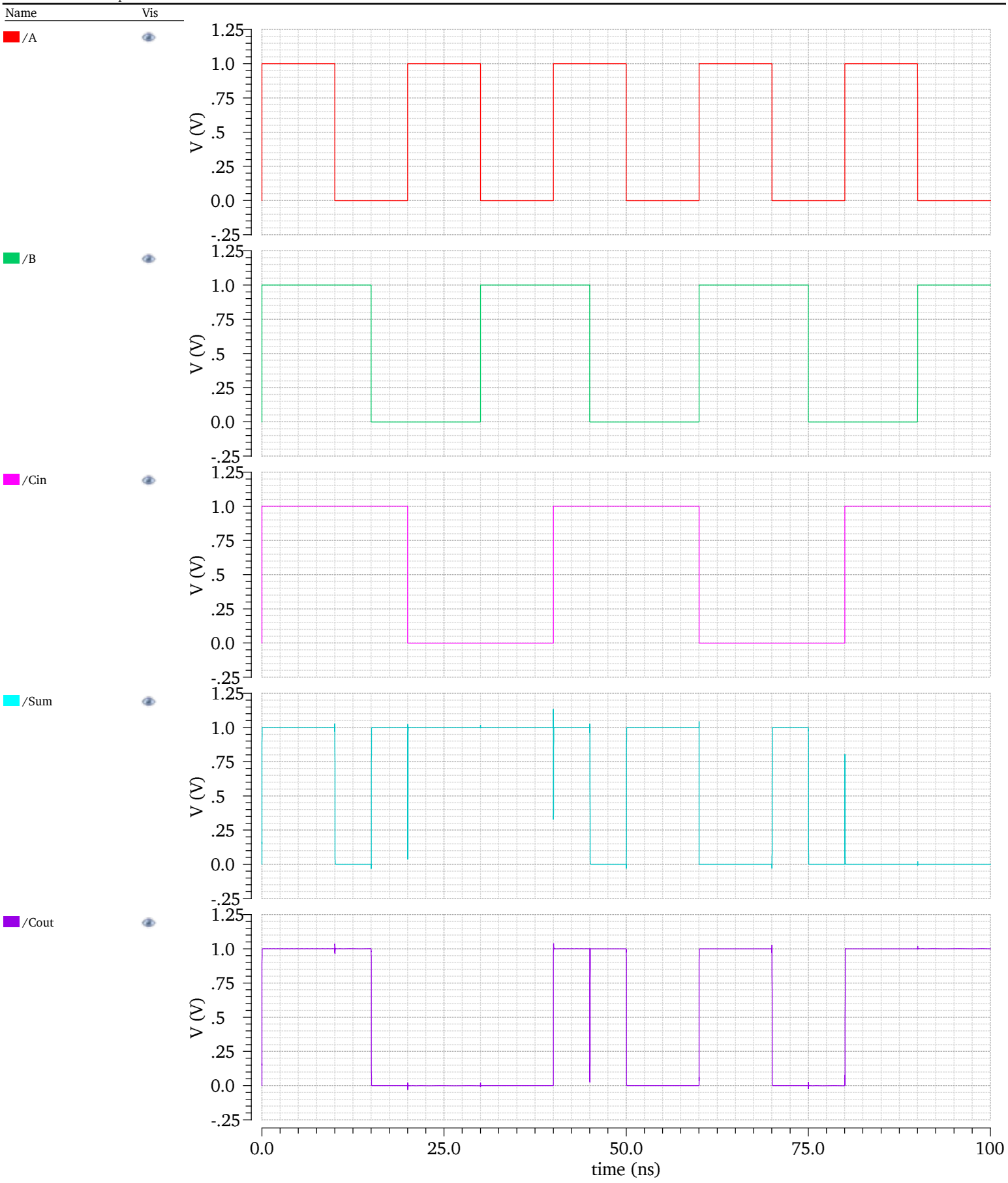

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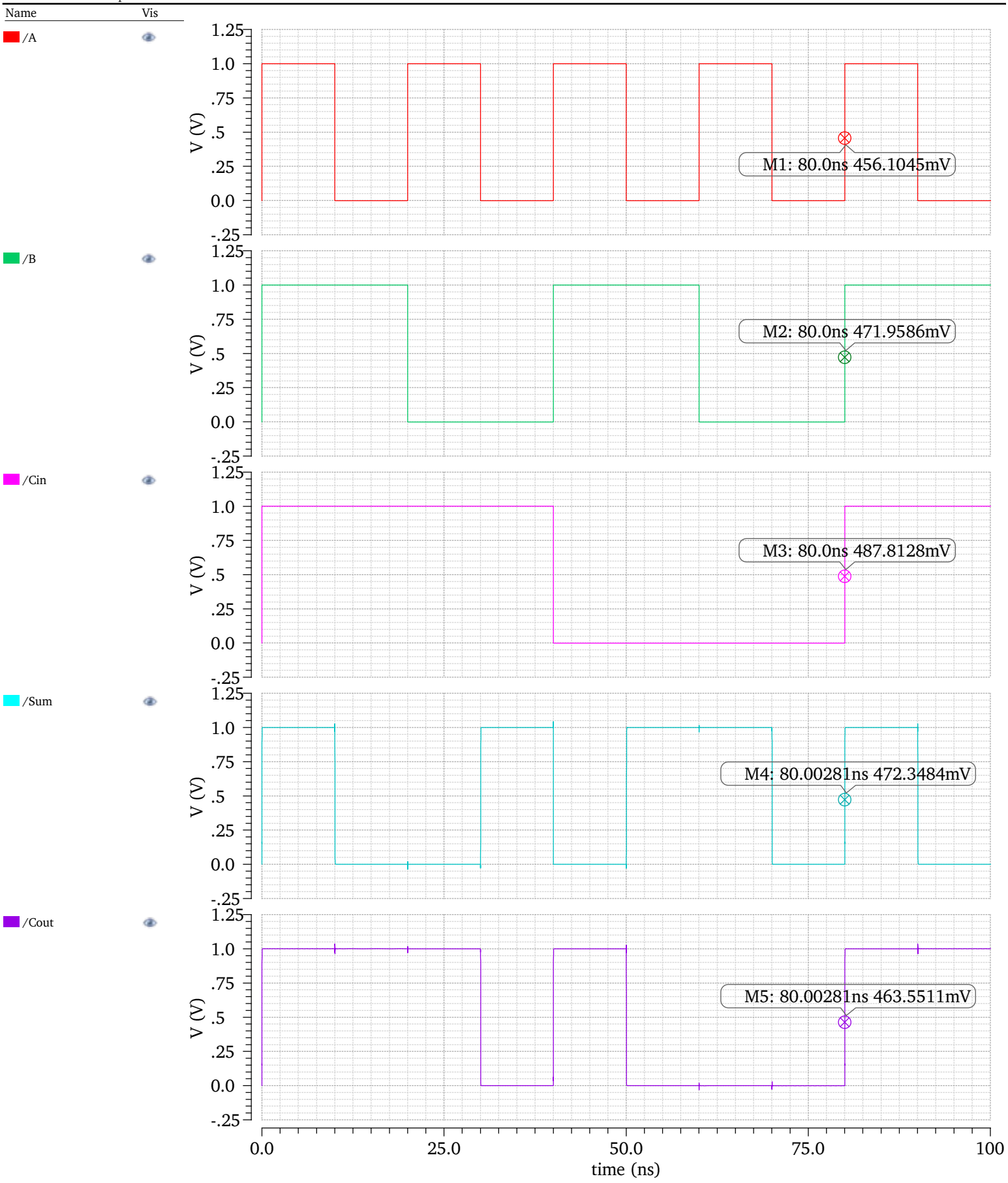

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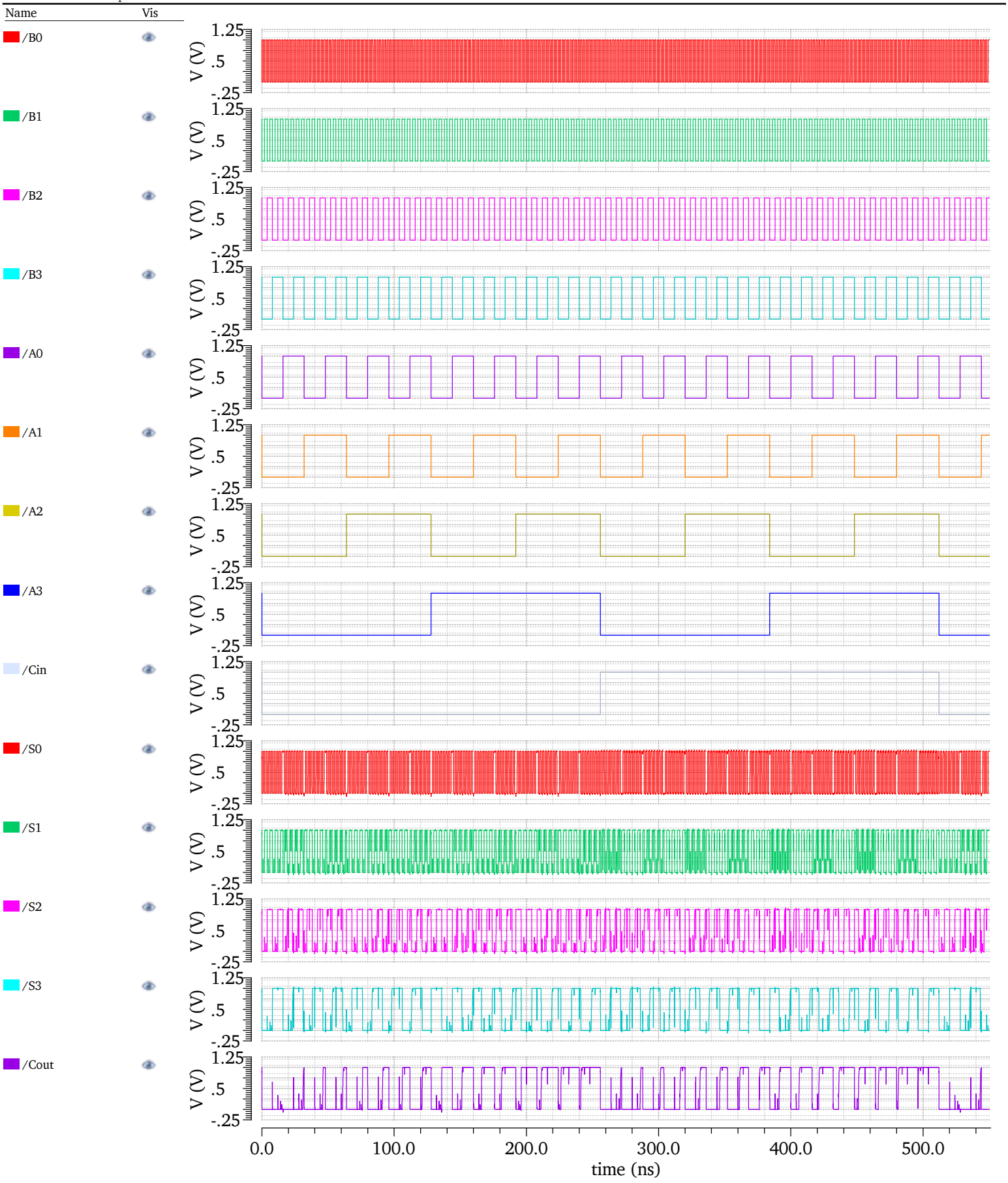

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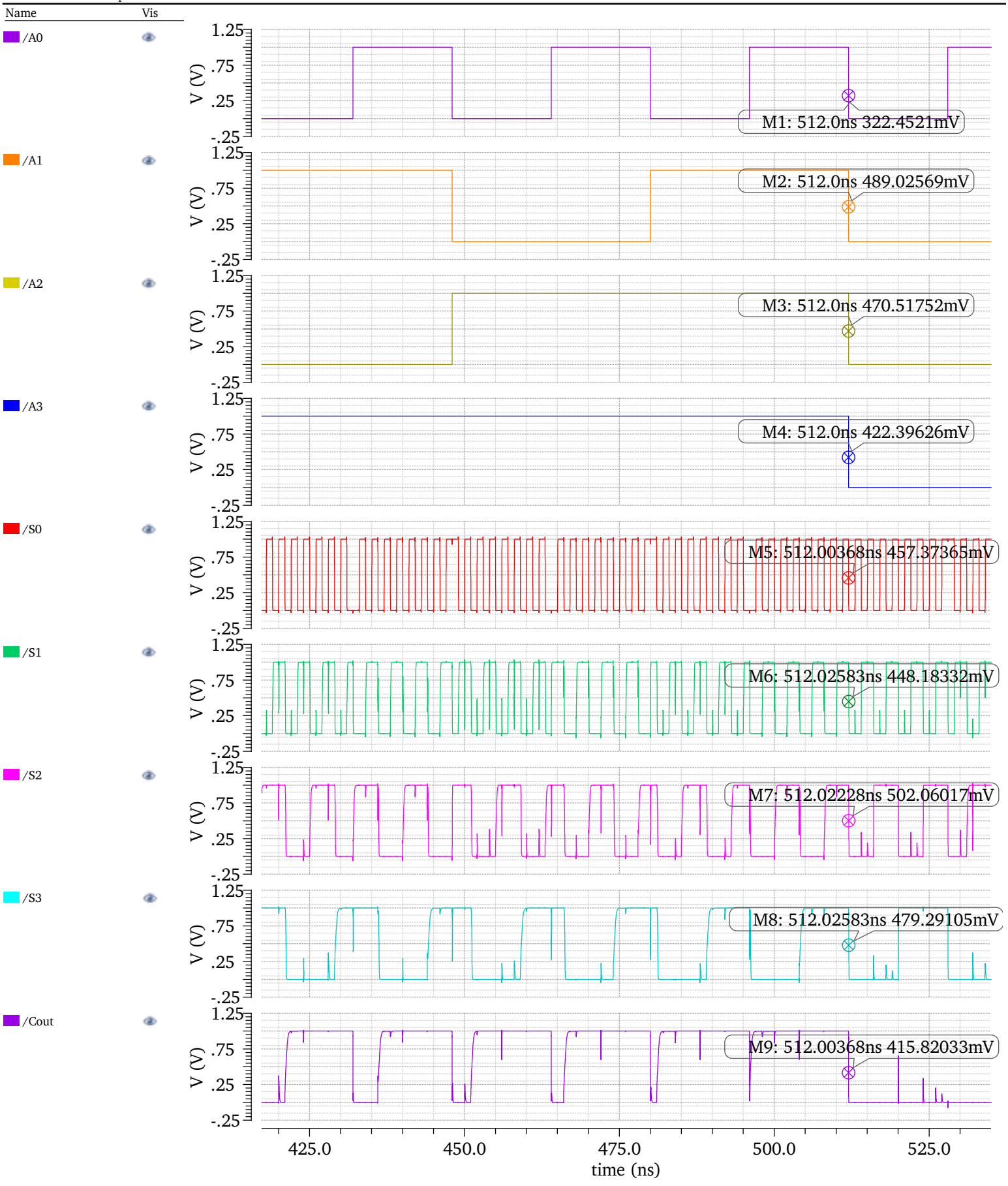

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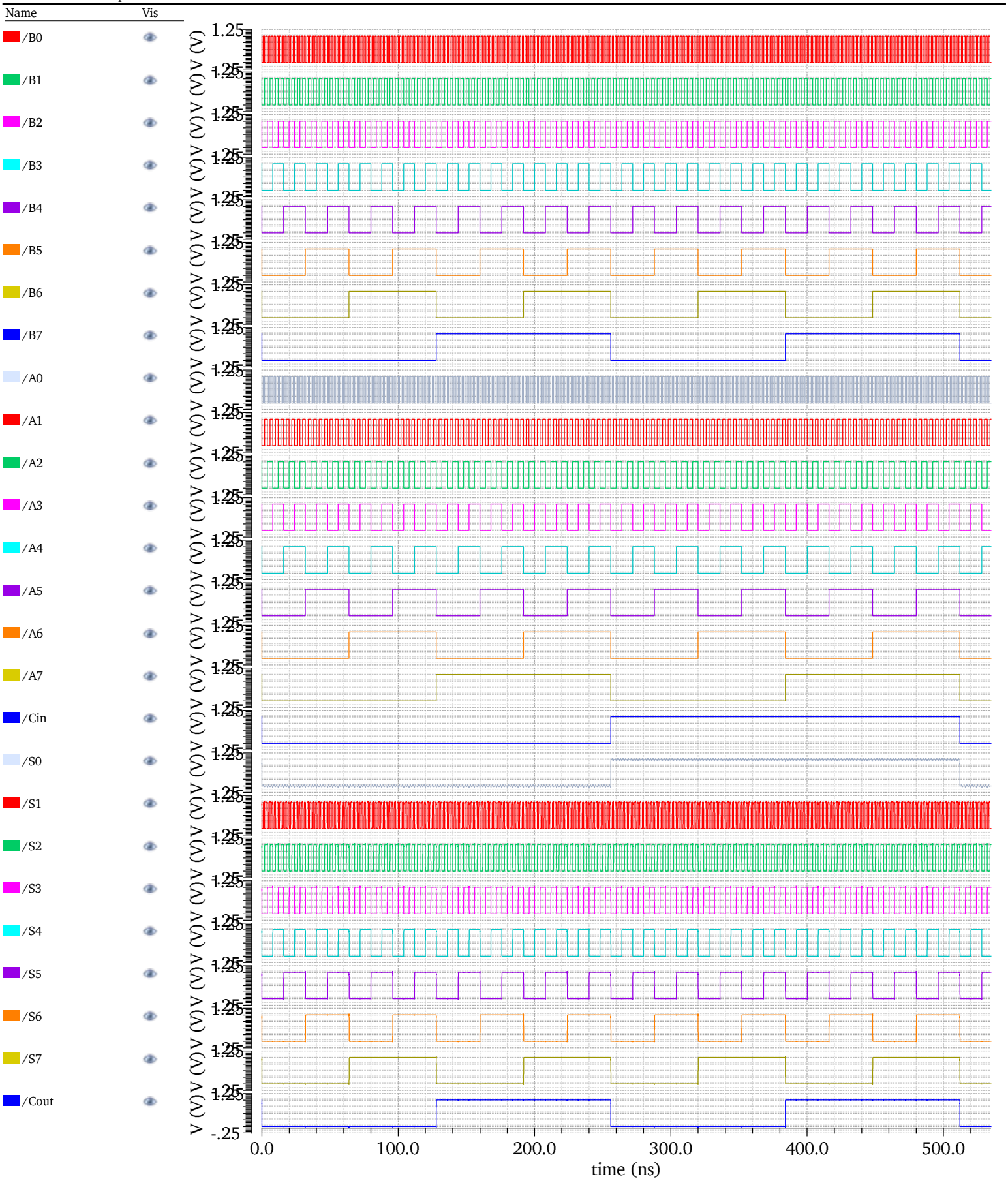

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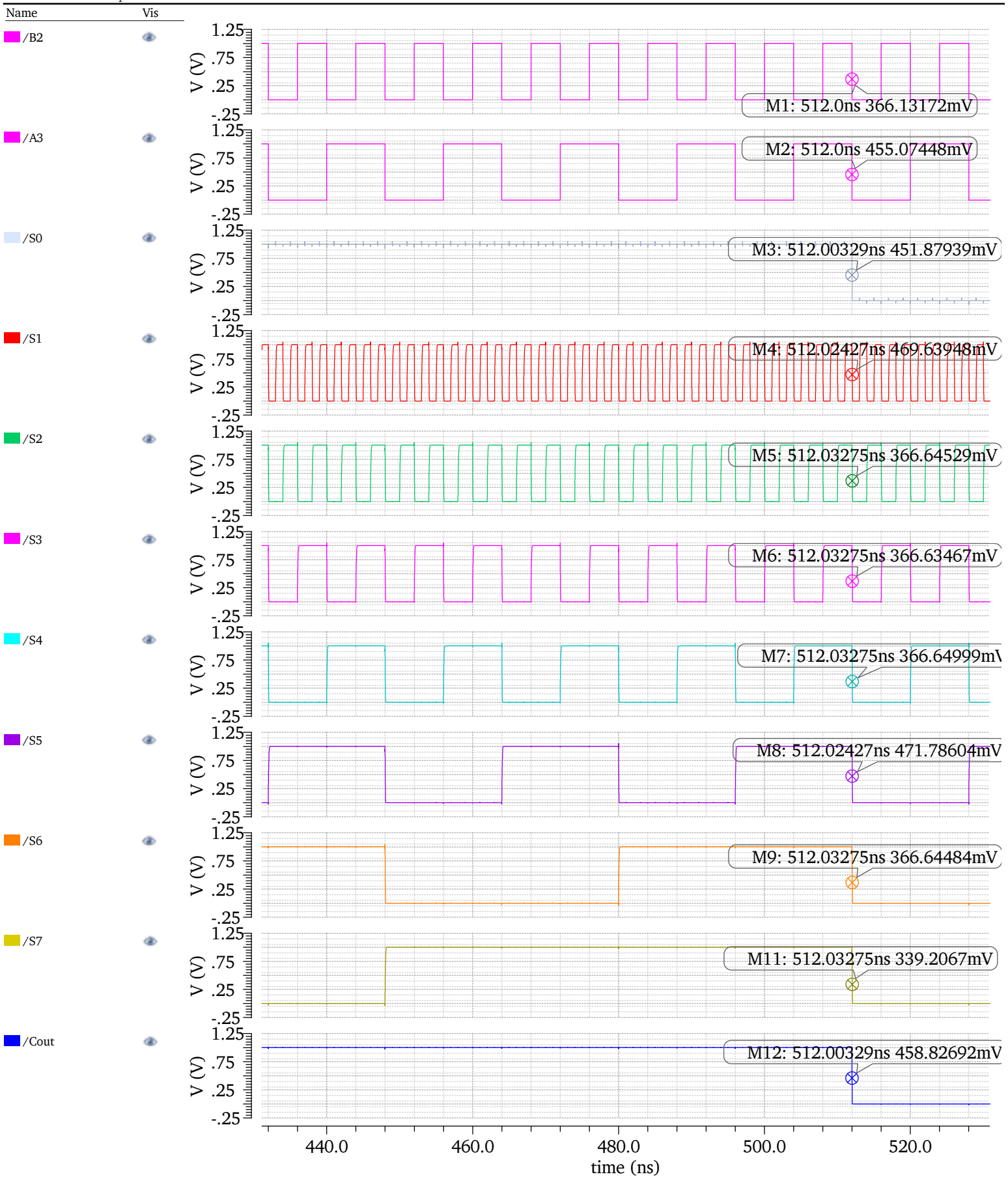

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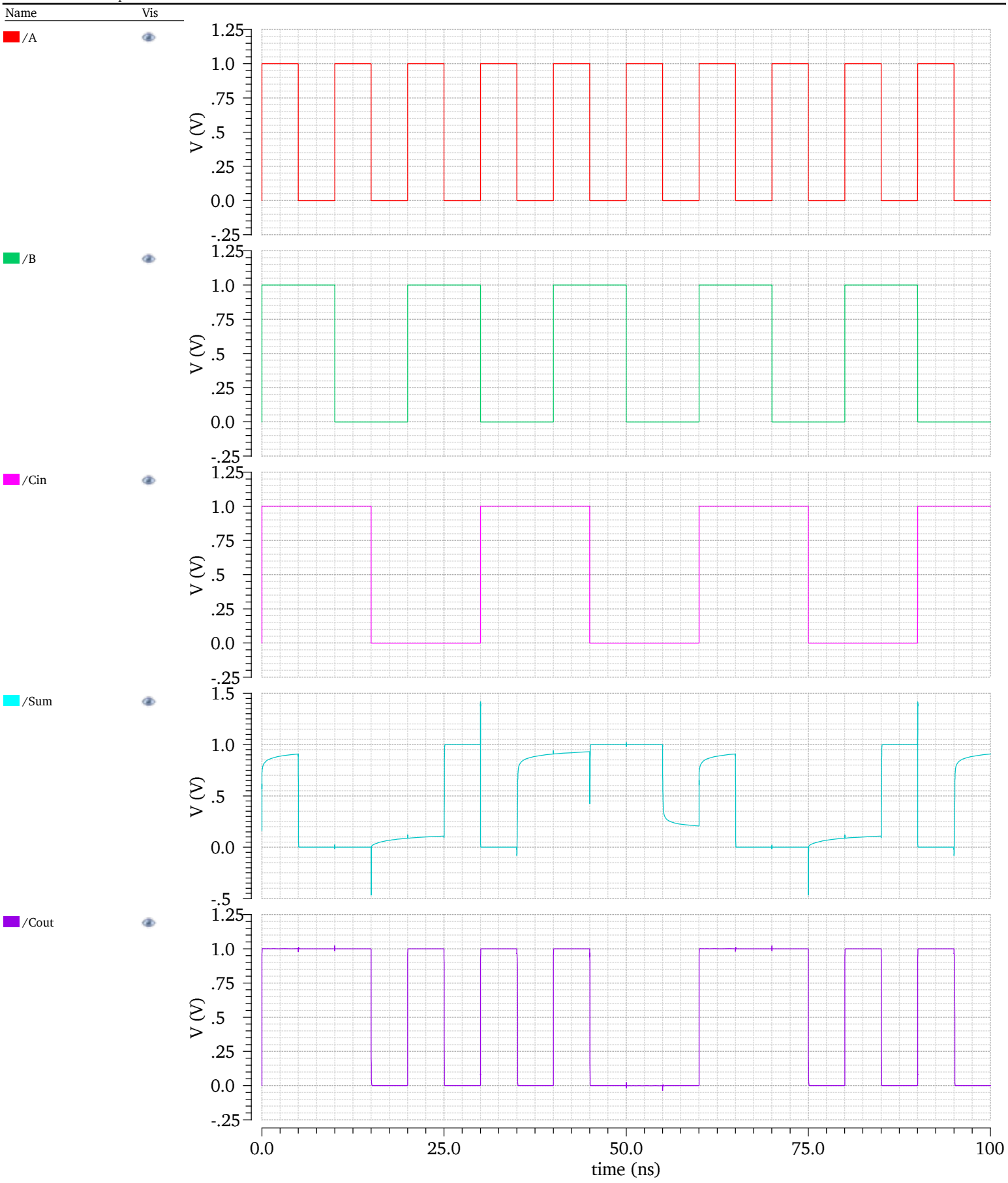

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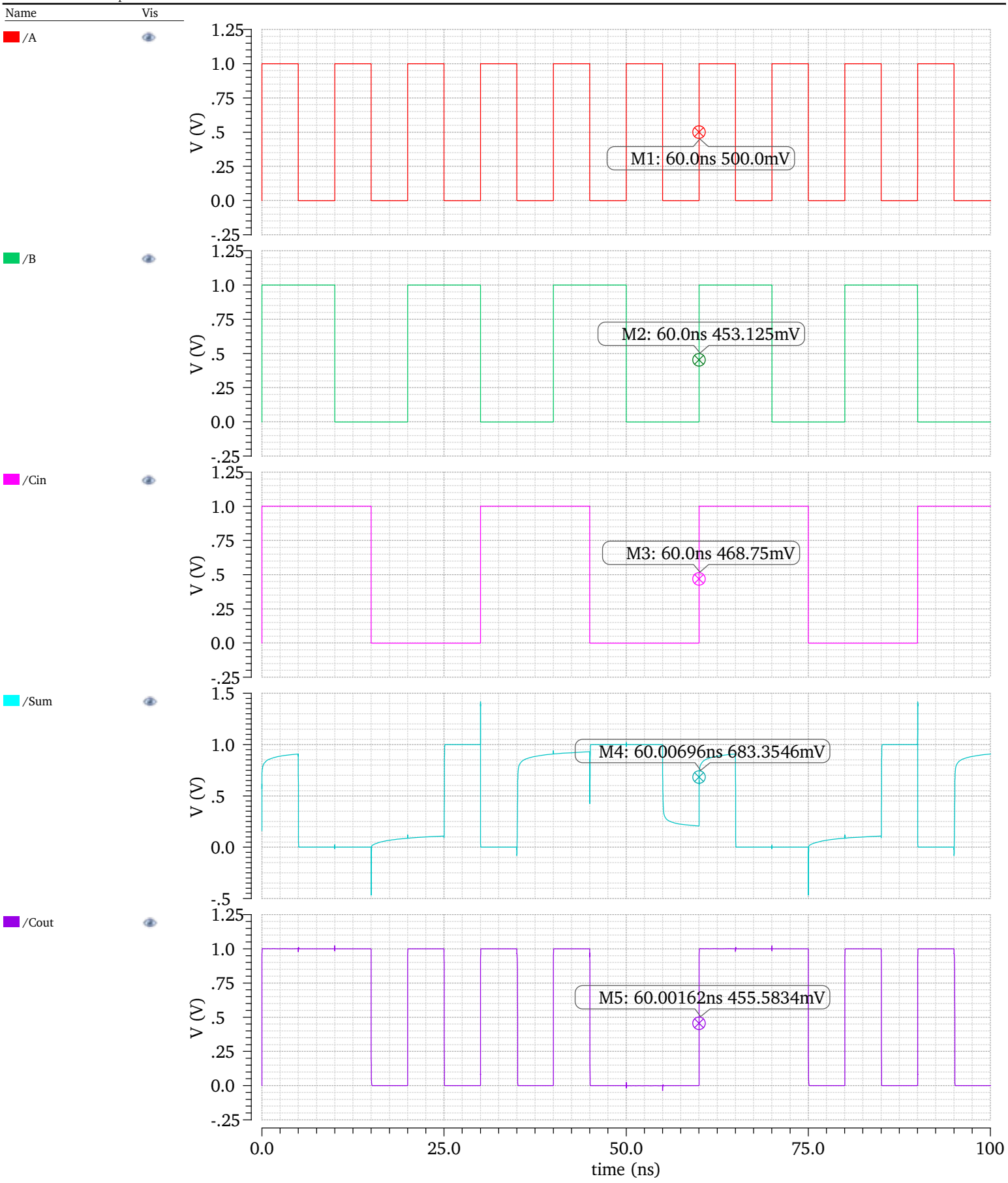

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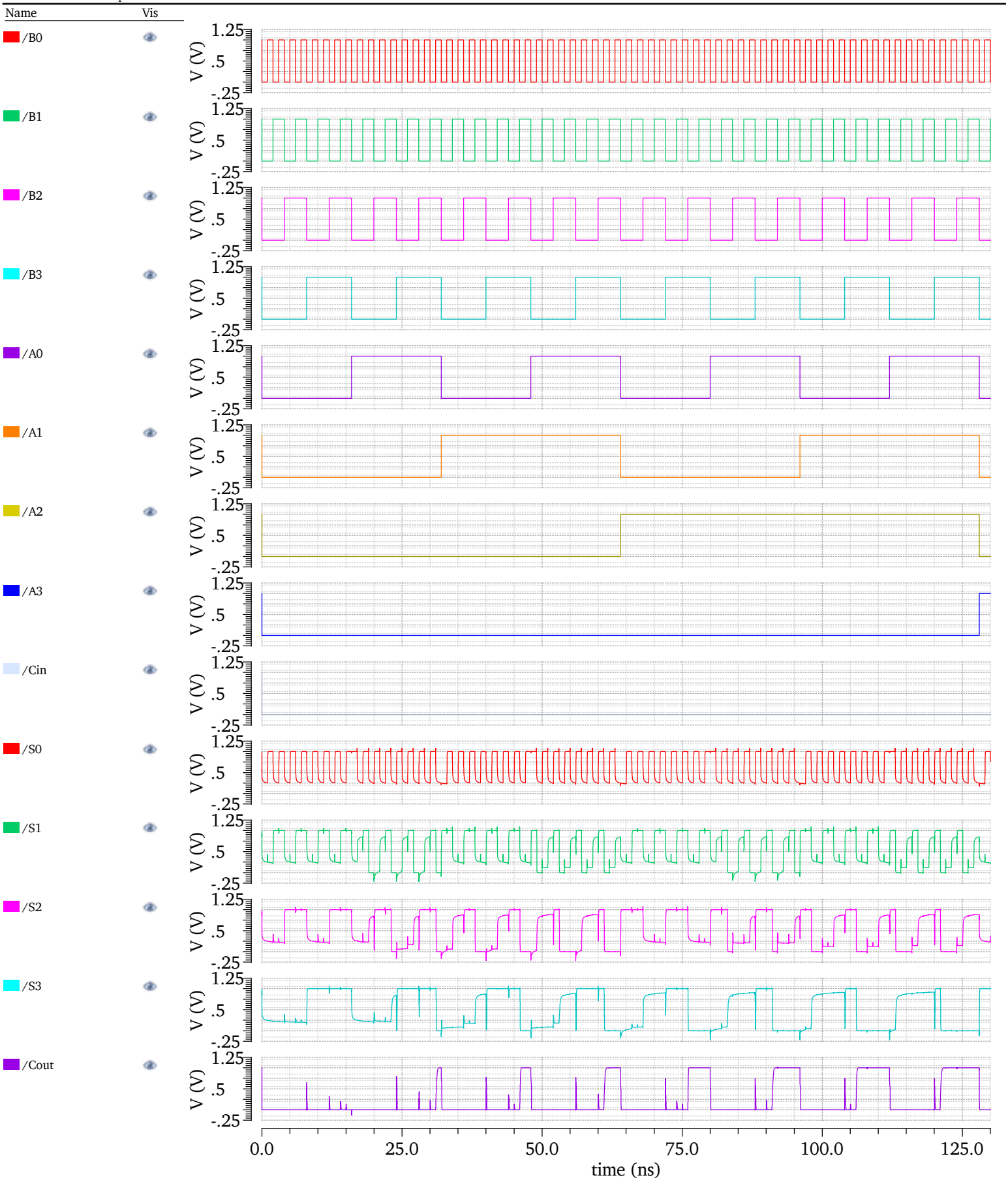

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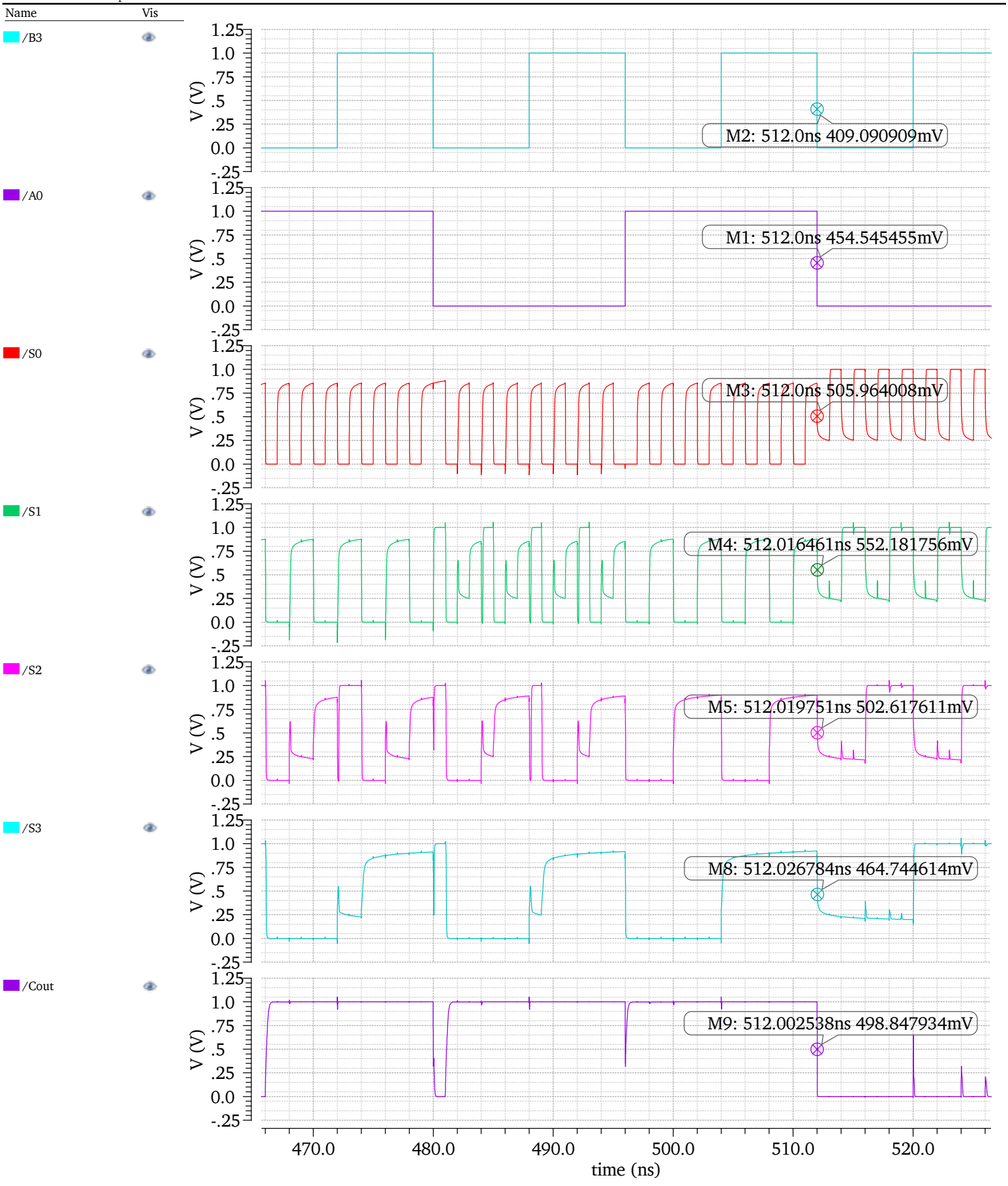

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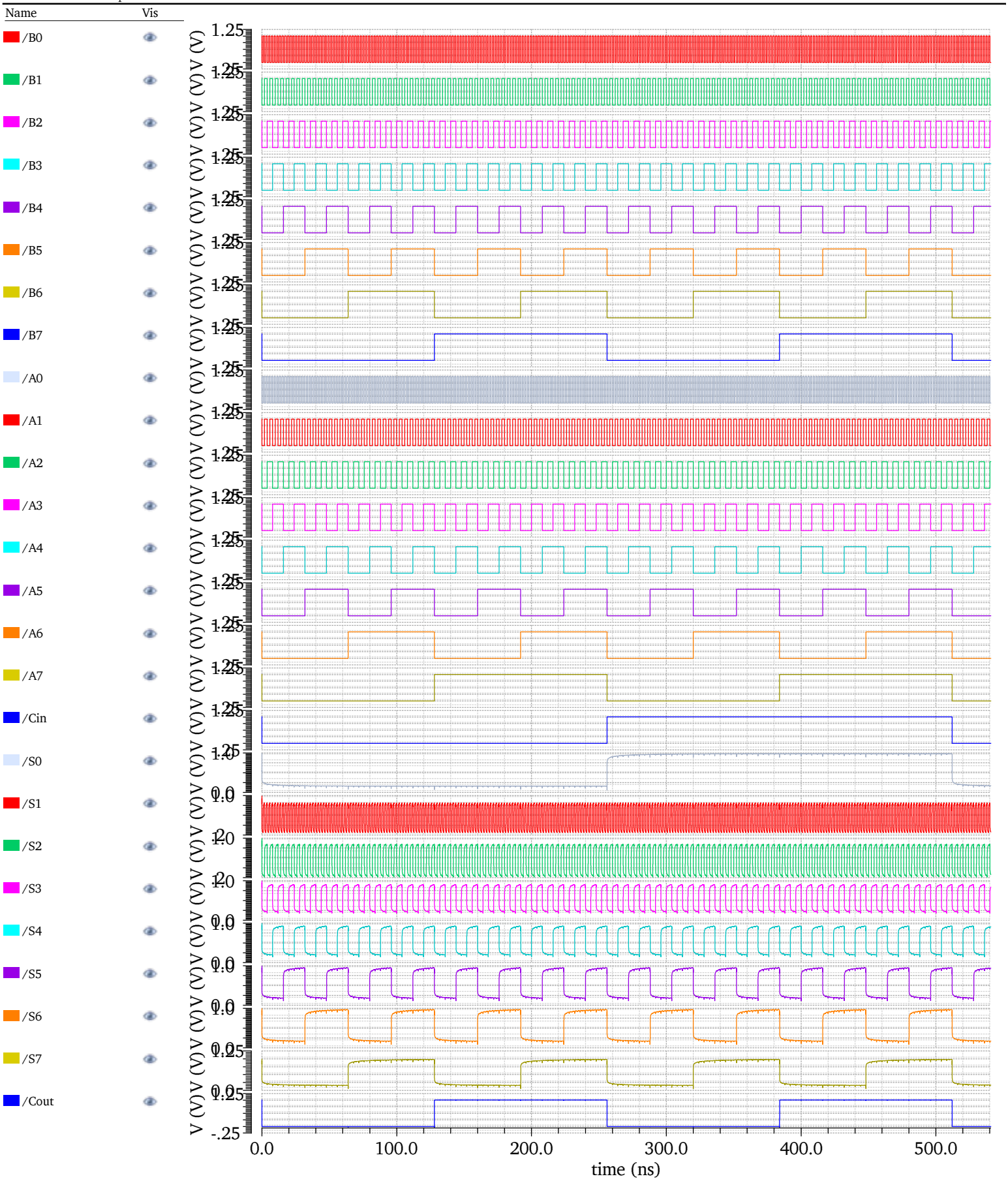

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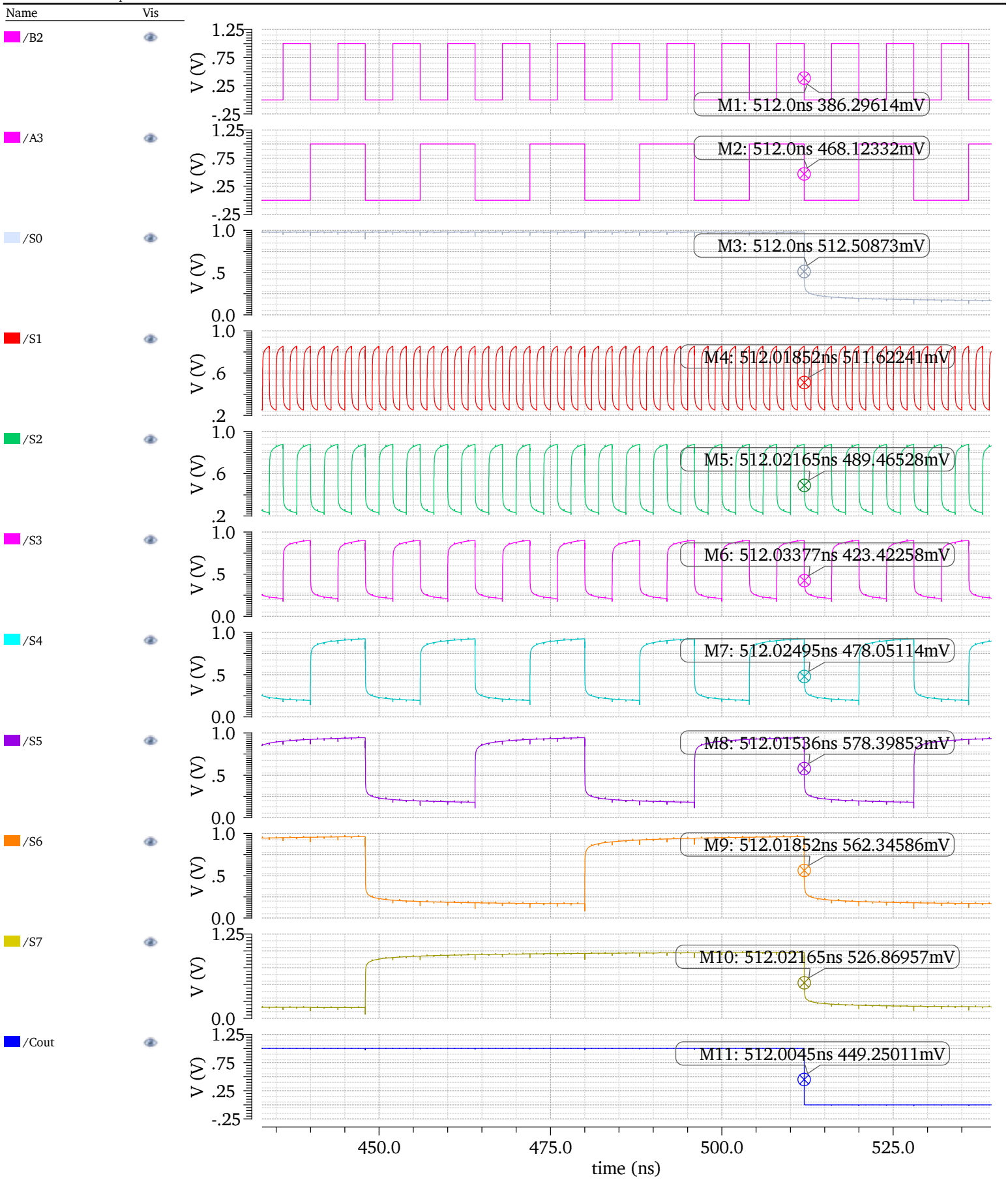

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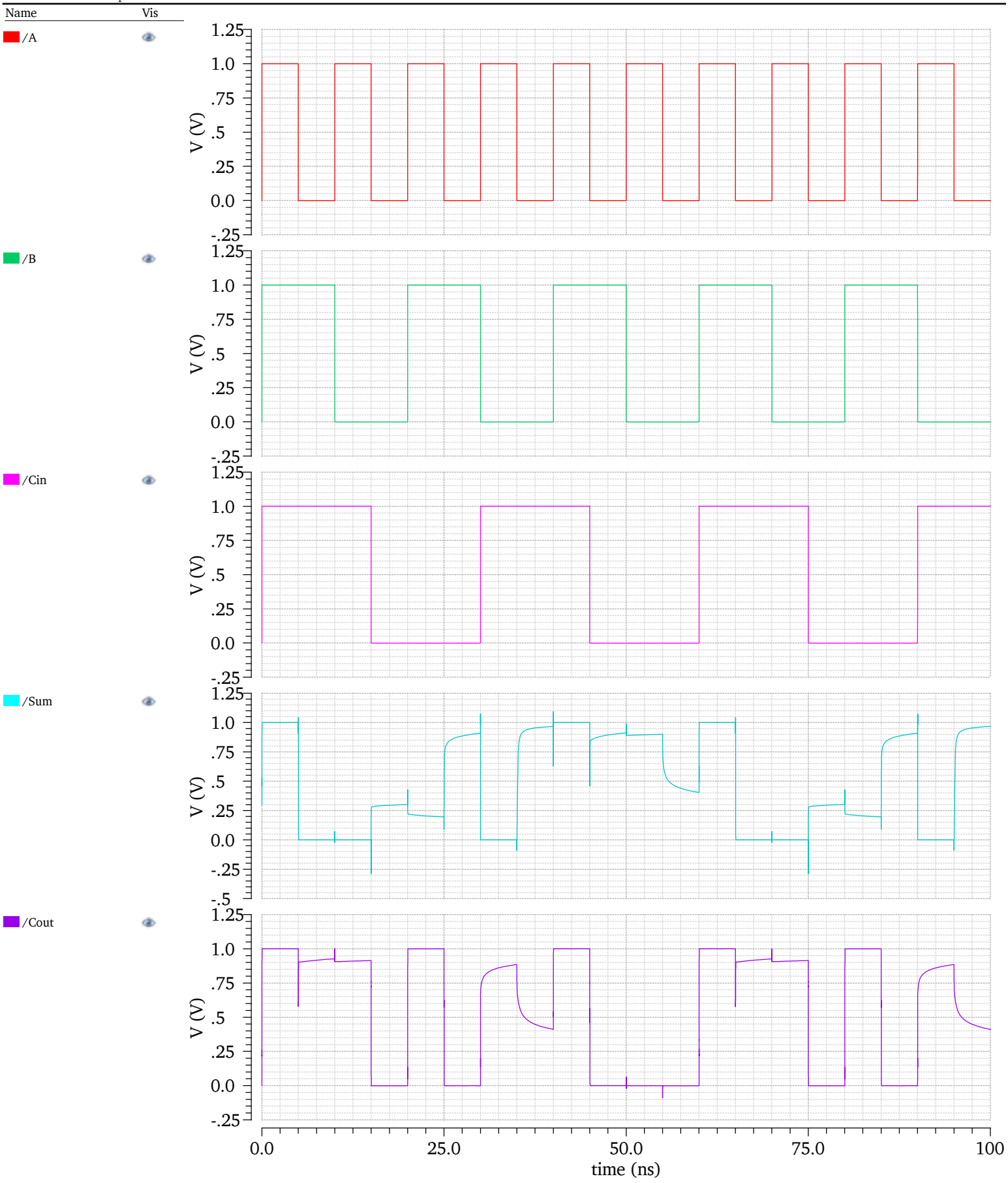

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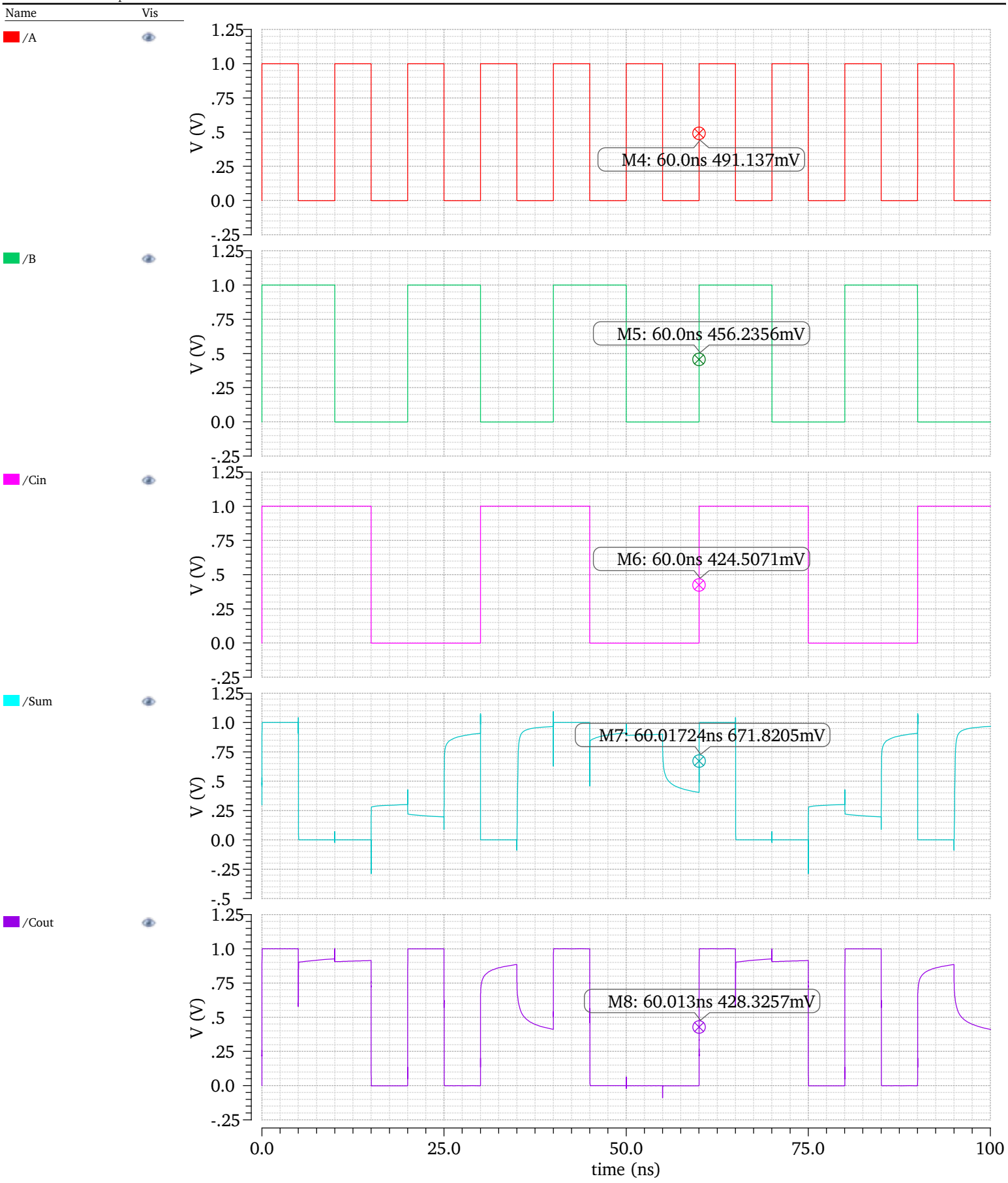

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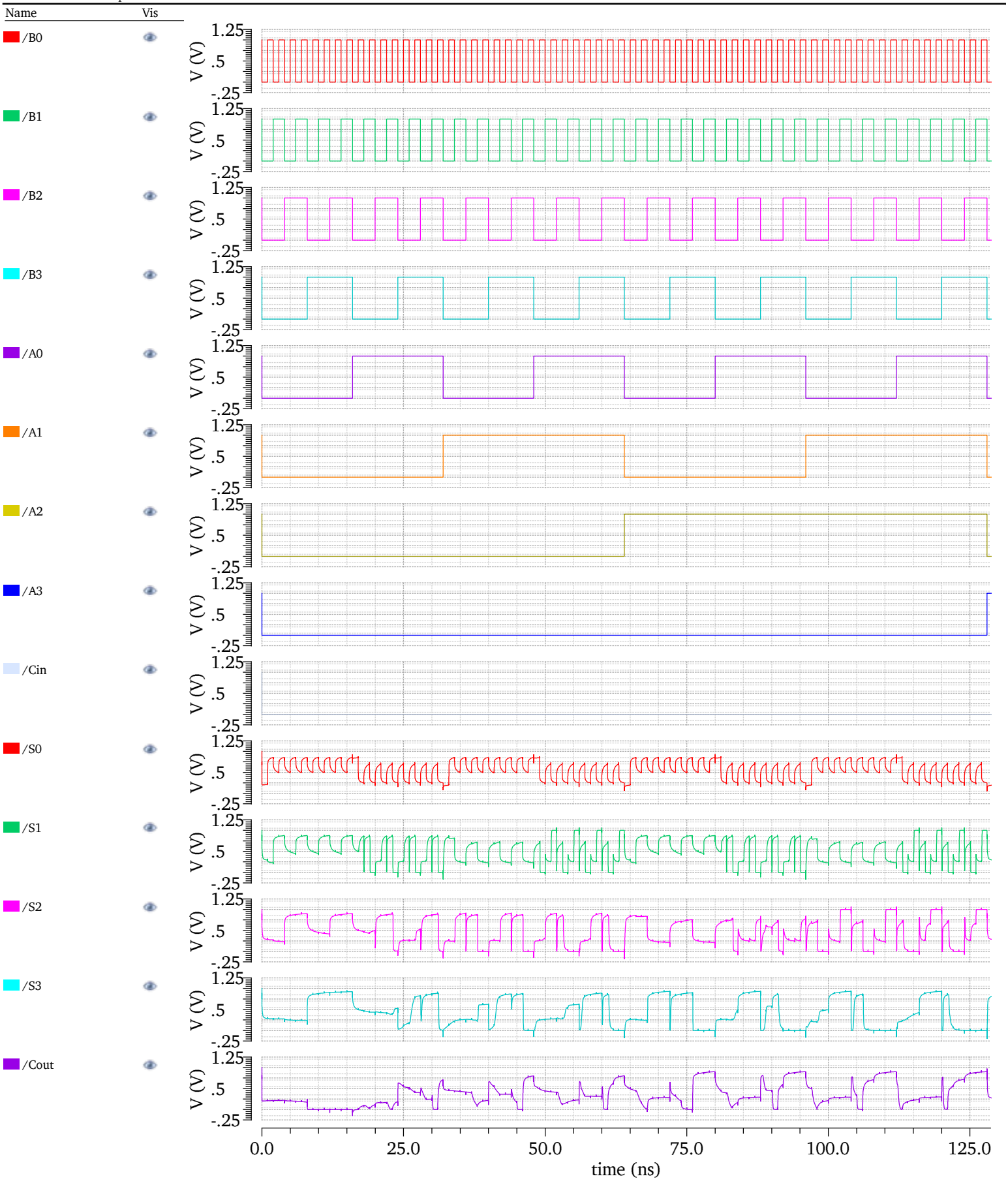

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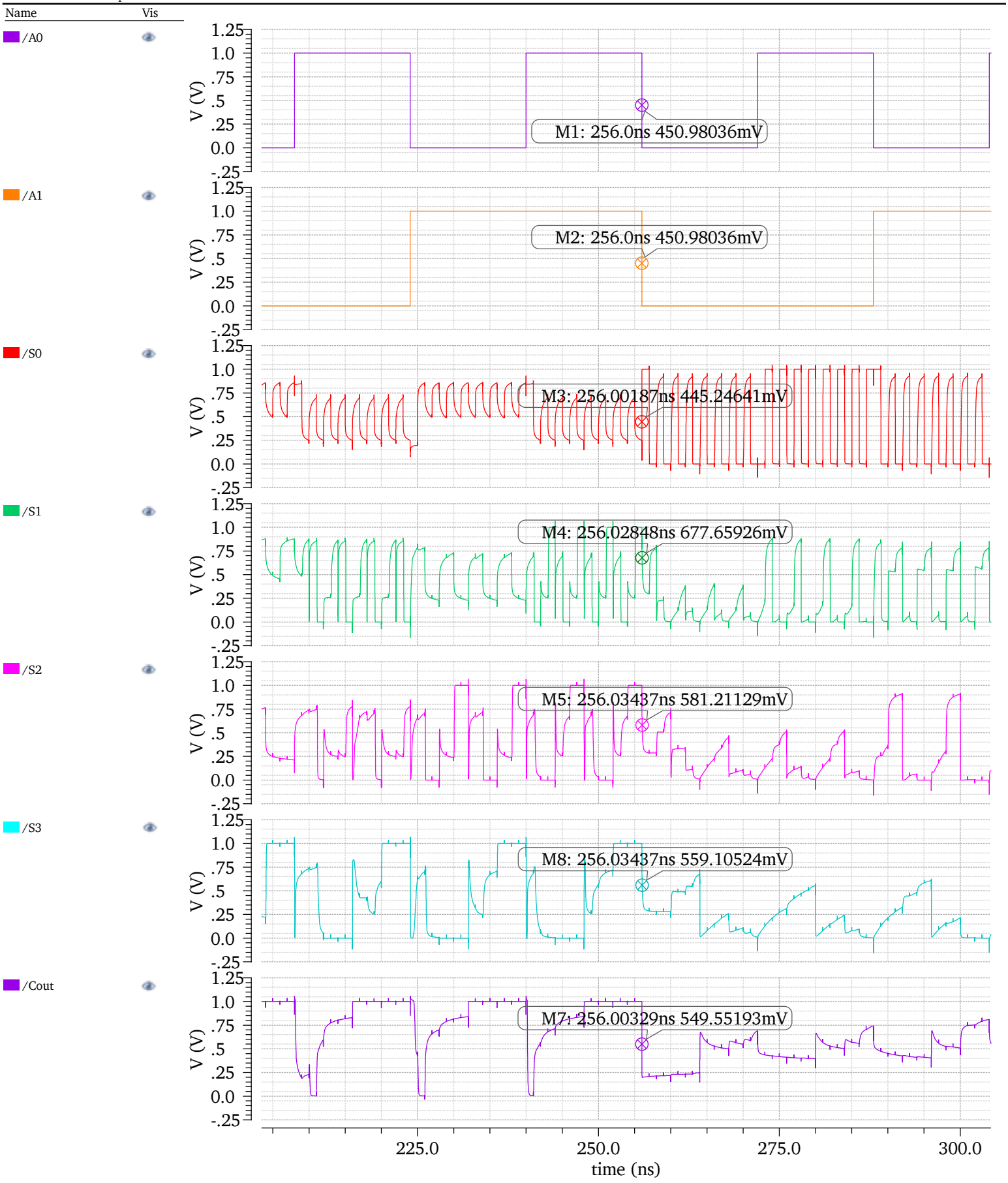

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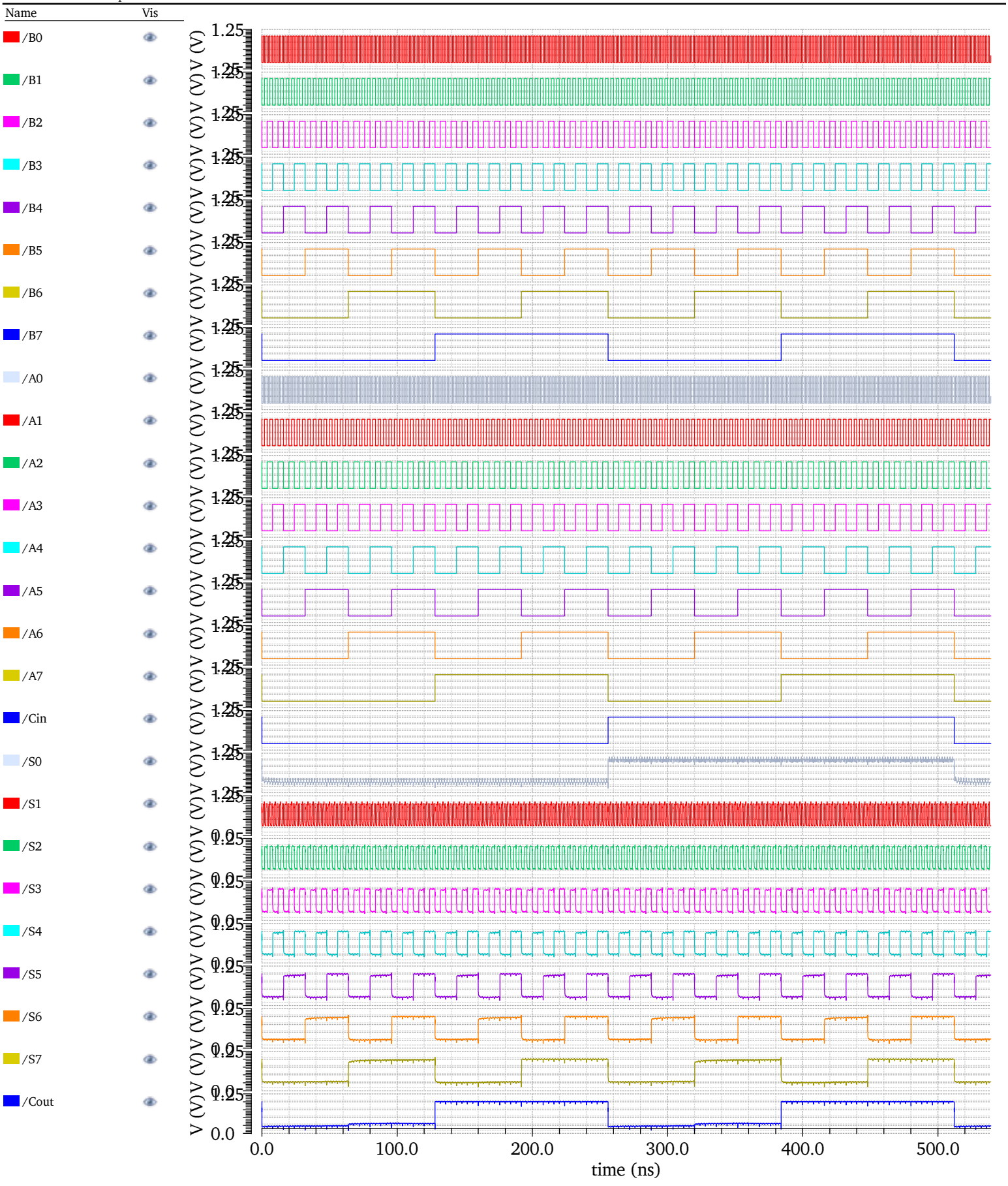

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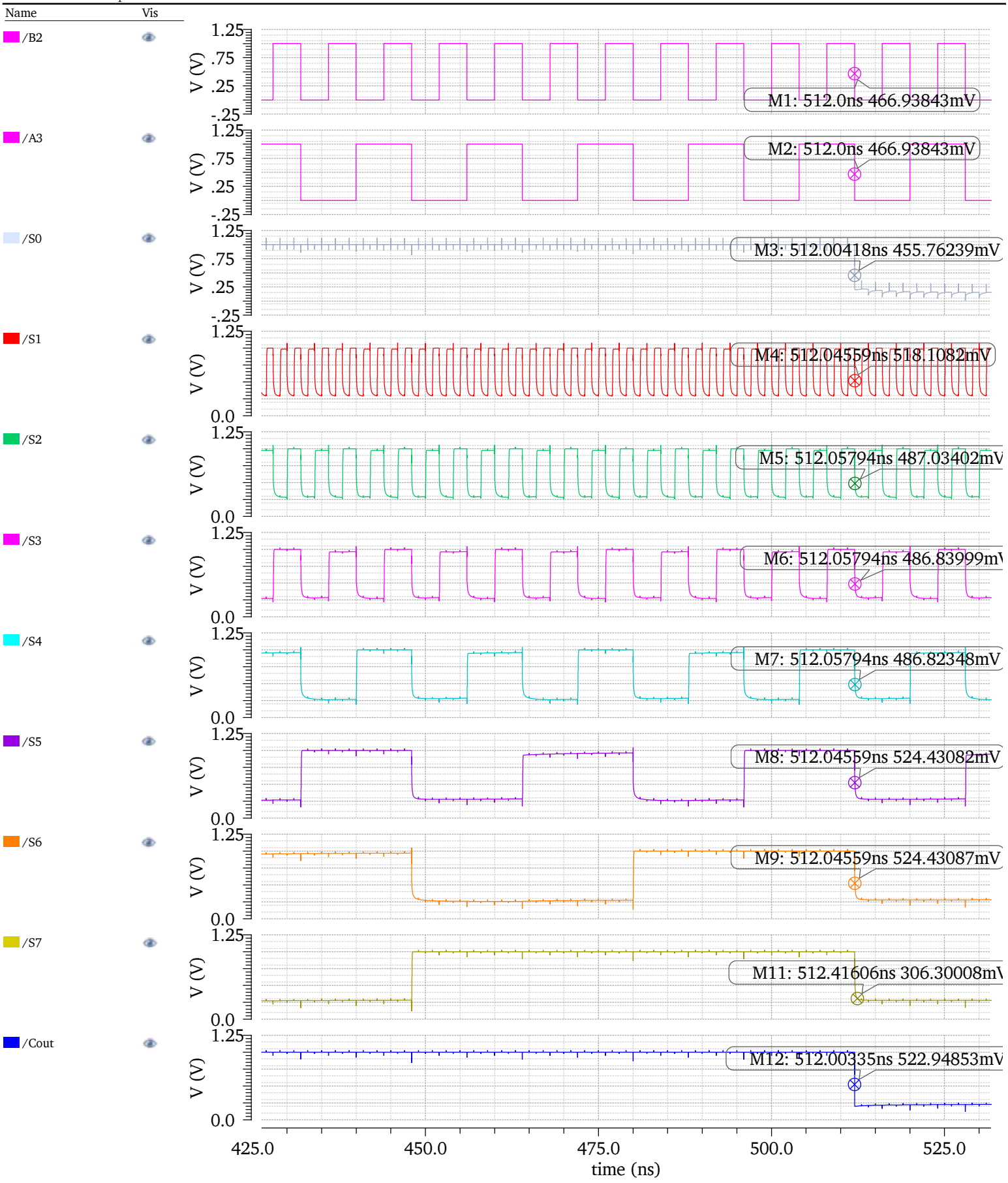

Results

1. 1 bit Full Adder Comparison

Metric	Static CMOS	TG	Hybrid FA	GDI
No. of Transistor	28	20	12	10
Average Power	11.4E−06	5.79E−06	4.43E−06	2.87E−06
Sum Delay	52.89E−12	2.81E−12	6.96E−12	17.24E−12
Carry Delay	22.52E−12	2.81E−12	1.62E−12	13E−12
PDP	6.02E-16	1.627E-17	3.08E-17	3.73E-17

2. 4- bit Full Adder Comparison

Metric	Static CMOS	TG	Hybrid FA	GDI
No. of Transistor	28×4	20×4	12×4	10×4
Average Power	28.8E−06	12.1E−06	2.94E−06	20E−05
Sum Delay	52.89E−12	2.81E−12	26.78E−12	34.37E−12
Carry Delay	22.52E−12	2.81E−12	2.53E−12	3.29E−12
PDP	1.5E-15	3.4E-17	7.873E-17	6.87E-16

3. 8- bit Full Adder Comparison

Metric	Static CMOS	TG	Hybrid FA	GDI
No. of Transistor	28×8	20×8	12×8	10×8
Average Power	40.14E−06	8.43E−06	1.09E−06	35.3E−06
Sum Delay	133.26E−12	32.7E−12	45.59E−12	45.59E−12
Carry Delay	54.61E−12	3.29E−12	3.35E−12	3.35E−12
PDP	5.35E-15	2.8E-16	5E-17	1.61E-15

Looking at the data from the 1-bit, 4-bit, and 8-bit adder designs, it's clear that the **GDI (Gate Diffusion Input)** and **Hybrid Full Adder (FA)** architectures stand out compared to the traditional **Static CMOS** and **Transmission Gate (TG)** adders — especially when it comes to power and speed.

Even though all architectures scale linearly in terms of transistor count as the number of bits increases, GDI and Hybrid FA consistently show much lower power consumption and delay on average. For the **1-bit adder**, **GDI is the most efficient**, with the lowest power and fastest response, making it a great choice for compact, low-power circuits. But as we move to **larger bit-widths like 4-bit and 8-bit**, GDI's delay starts to rise more noticeably. That's mainly due to signal degradation and weaker voltage levels when multiple GDI stages are cascaded.

That's where the **Hybrid FA** really shines. It handles carry and sum operations more efficiently in multi-bit setups, thanks to its well-balanced

logic design. It delivers **the fastest performance** overall in larger adders, making it ideal for high-speed applications.

Meanwhile, **Static CMOS**, while reliable and producing clean signals, lags behind in both power and speed — it's the least efficient across all bit-widths. **TG-based adders** offer some improvement over CMOS, but still can’t quite match the performance of the Hybrid FA, especially as designs scale up.

So, if you're designing for **modern, power-conscious, and high-speed digital systems**, the **Hybrid Full Adder** offers the best overall performance. That said, **GDI** remains a strong pick when ultra-low power is the top priority, particularly in small-scale designs.

GDI consumes less power than CMOS, but more than TG-based or Hybrid 12T adders.Why?

1.GDI circuits can suffer from threshold voltage drops and reduced noise margin, especially when cascading multiple GDI stages.

2.Not all logic levels are full swing — incomplete voltage swing causes short-circuit current in later stages.

3.TG Adders use transmission gates (which are full pass) — they avoid degraded logic levels and leakage is low.

4.Hybrid 12T designs carefully balance logic styles to minimize both power and delay — typically better optimized.

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Conclusion and Future Scope

The successful implementation and evaluation of the m-GDI-based full adder confirm its advantages over traditional CMOS-based designs. The proposed design achieves substantial reductions in power consumption, propagation delay, and silicon area. These improvements are particularly significant for portable and embedded systems, where power efficiency is a major constraint.

The m-GDI technique proves to be a promising alternative for low-power VLSI circuit design. The simplicity of the structure, combined with its compatibility with standard CMOS processes, makes it suitable for large-scale adoption in ASIC and SoC environments.

Future Scope:

- **Scalability:** The current 4-bit implementation can be extended to higher bit-widths such as 8-bit, 16-bit, or 32-bit for integration in more complex ALUs and DSP systems.
- **Post-Layout Analysis:** Perform layout design and post-layout simulations to study parasitic effects, routing complexity, and area estimation.
- **Technology Scaling:** Port the design to advanced nodes like 65nm or 45nm to evaluate its performance in modern fabrication technologies.
- **Real-World Deployment:** Implement the design on an FPGA or as part of an ASIC prototype to test real-world functionality and robustness.
- **Fault Tolerance and Reliability:** Analyze the behavior of m-GDI circuits under voltage scaling, process variation, and soft error conditions to enhance their reliability in critical applications.

This project lays a strong foundation for further research and development in low-power arithmetic circuit design using novel logic techniques like m-GDI.

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