1.

Student

rollNum	name	gender	marks
1	Naman	M	62
2	Aliya	F	70
3	Aliya	F	80
4	James	M	82
5	Swati	F	65

The SQL query below is executed on this database.

SELECT * FROM Student WHERE gender = 'F' AND marks > 65; The number of rows returned by the query is _____.

(2)

2. Emp (Empcode, Name, Gender, Salary, Deptt)

```
SELECT Deptt FROM Emp
WHERE Gender = 'M'
GROUP by Dept
Having avg (Salary) > {select avg (Salary) from Emp}
```

1. **The average salary of male employees is the average salary of the organization.**
2. **The average salary of male employees is less than the average salary of the organization.**
3. **The average salary of male employees is equal to the average salary of the organization.**
4. **The average salary of male employees is more than the average salary of the organization.**

(4)

4. Consider the relational database with the following four schemas and their respective instances.

Student(sNo, sName, dNo) Dept(dNo, dName)

Course(cNo, cName, dNo) Register(sNo, cNo)

Student		
sNo	sName	dNo
S01	James	D01
S02	Rocky	D01
S03	Jackson	D02
S04	Jane	D01
S05	Milli	D02

Dept	
dNo	dName
D01	CSE
D02	EEE

	Course	
cNo	cName	dNo
C11	DS	D01
C12	OS	D01
C21	DE	D02
C22	PT	D02
C23	CV	D03

Register	
sNo	cNo
S01	C11
S01	C12
S02	C11
S03	C21
S03	C22
S03	C23
S04	C11
S04	C12
S05	C11
S05	C21

SQL Query:

```
SELECT * FROM Student AS S WHERE NOT EXIST
        (SELECT cNo FROM Course WHERE dNo = "D01"
         EXCEPT
        SELECT cNo FROM Register WHERE sNo = S.sNo)
```

The number of rows returned by the above SQL query is_____

(2)

5. An 8-way set associative cache of size 64 KB (1 KB = 1024 bytes) is used in a system with a 32-bit address. The address is sub-divided into TAG, INDEX, and BLOCK OFFSET. The number of bits in the TAG is _____.

System is 32-bit address.
Cache Size : 64 KB = 2^6∗ 2^10=2^16
. So, cache bits = 16.
So Tag Bits = 32 – 16 = 16 bit.
As, Cache is an 8-way set associative. So, we have to transfer 3 bits to tag side.
So, final Tag bits = 16 + 3 = 19.
Number of bits in Tag Field = 19.

6. 11. Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively.

Solution

The correct option is **A** 10, 17

Size of cache = 32 KB

$= 32 \times 2^{10}$ byte $= 2^5 \times 2^{10}$ byte

$= 2^{15}$ byte = 15 bits

Size of tag = 32 − 15 = 17 bits

Cache index = LO − WO = 15 − 5 = 10 bits

7. Which one of the following facilitates transfer of bulk data from hard disk to main memory with the highest throughput?

1. **DMA based I/O transfer**
2. **Interrupt driven I/O transfer**
3. **Polling based I/O transfer**
4. **Programmed I/O transfer**

(1)

8. Let R1 and R2 be two 4-bit registers that store numbers in 2's complement form. For the operation R1+R2, which one of the following values of R1 and R2 gives an arithmetic overflow?

1. **R1 = 1011 and R2 = 1110**
2. **R1 = 1100 and R2 = 1010**
3. **R1 = 0011 and R2 = 0100**
4. **R1 = 1001 and R2 = 1111**

(2)

9. R=(A,B,C,D,E,F) FDs (C-> F,E-> A,EC->D,A->B) what are the candidate keys of this relation?

ANS> EC

10. Find the decimal equivalent for $(110110.101)_2$

11. Find Decimal $(123)_{10}$ to BCD code.

12. Draw a NAND logic diagram that implements the complement of the following function F(A,B,C,D)= (2,4,5,7,9,12,14)