



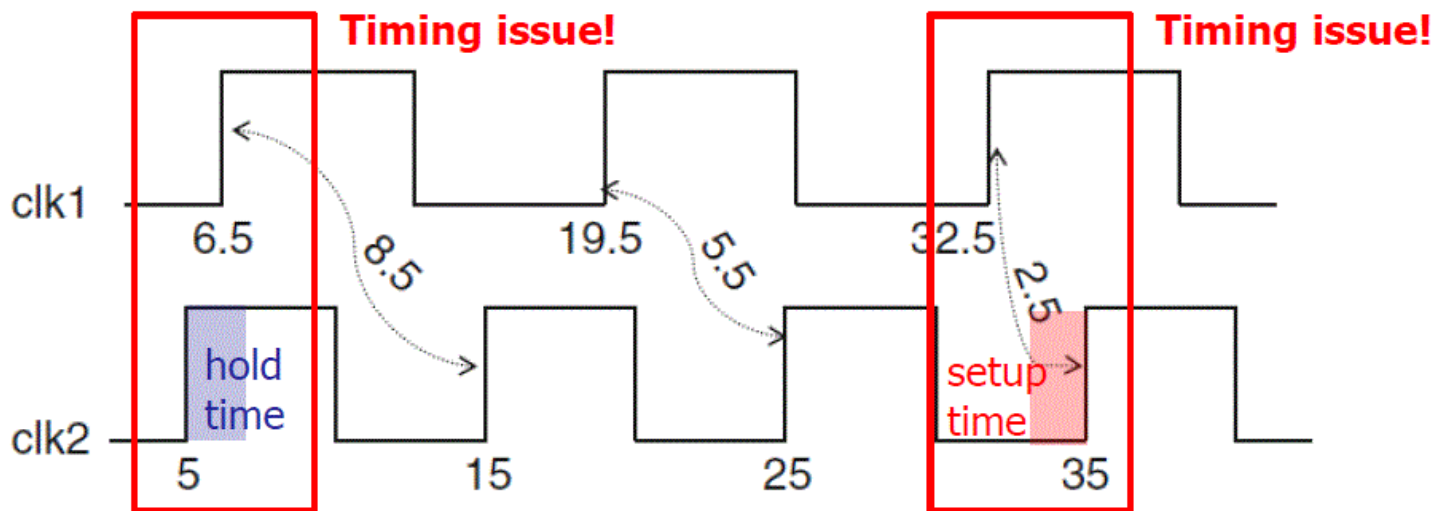
2022 DCS Lab 09

Clock Domain Crossing (CDC)

郭晏誠

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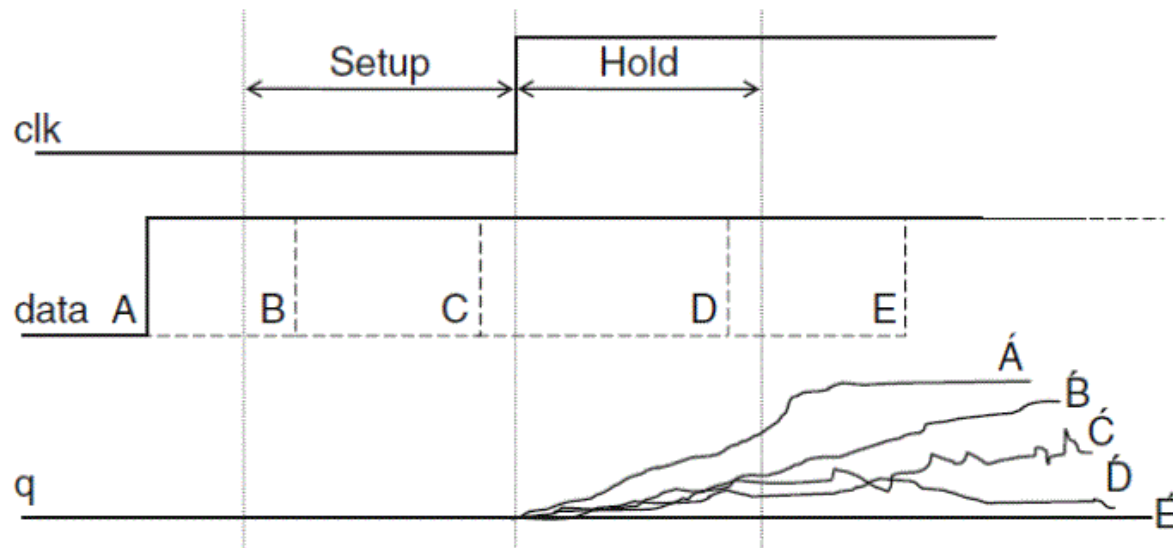
- CDC: When the data launched and captured by different (asynchronous) clock domain, this case is called Clock Domain Crossing.
- Consider two clocks, clk1 and clk2, with periods 13 and 10 respectively.



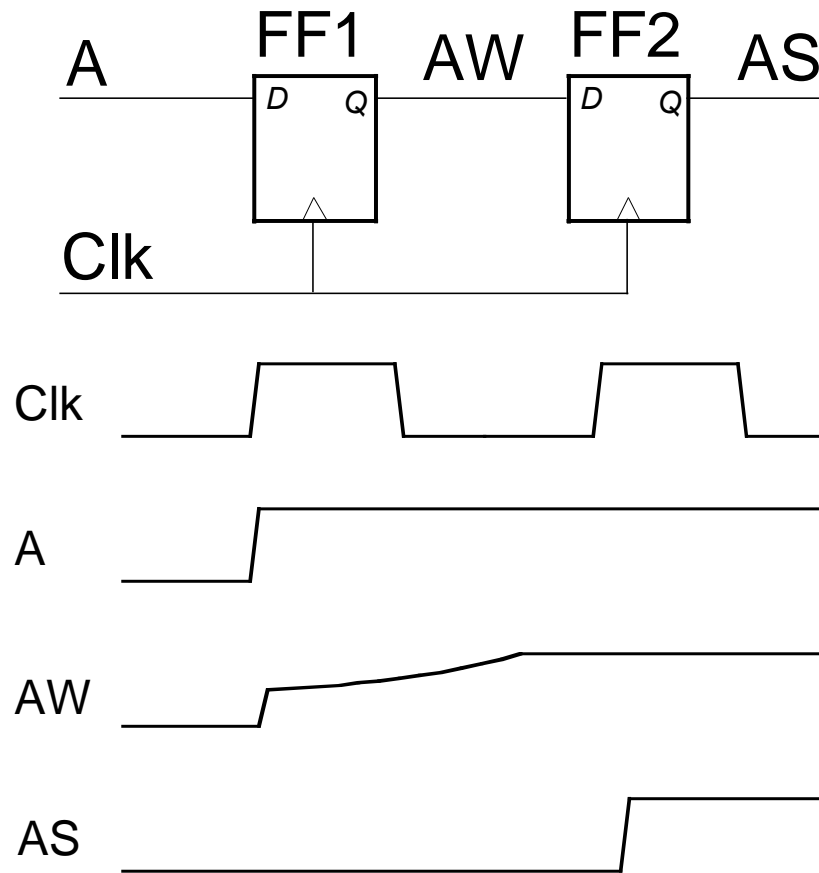
Asynchronous clocks

Metastability

- The unstable status due to non-ideal data transition is called metastability.
- To avoid this phenomenon, we have to ensure data transition during setup/hold timing check.
- However, CDC designs will inevitably face this problem.



Solution: A Brute-Force Synchronizer

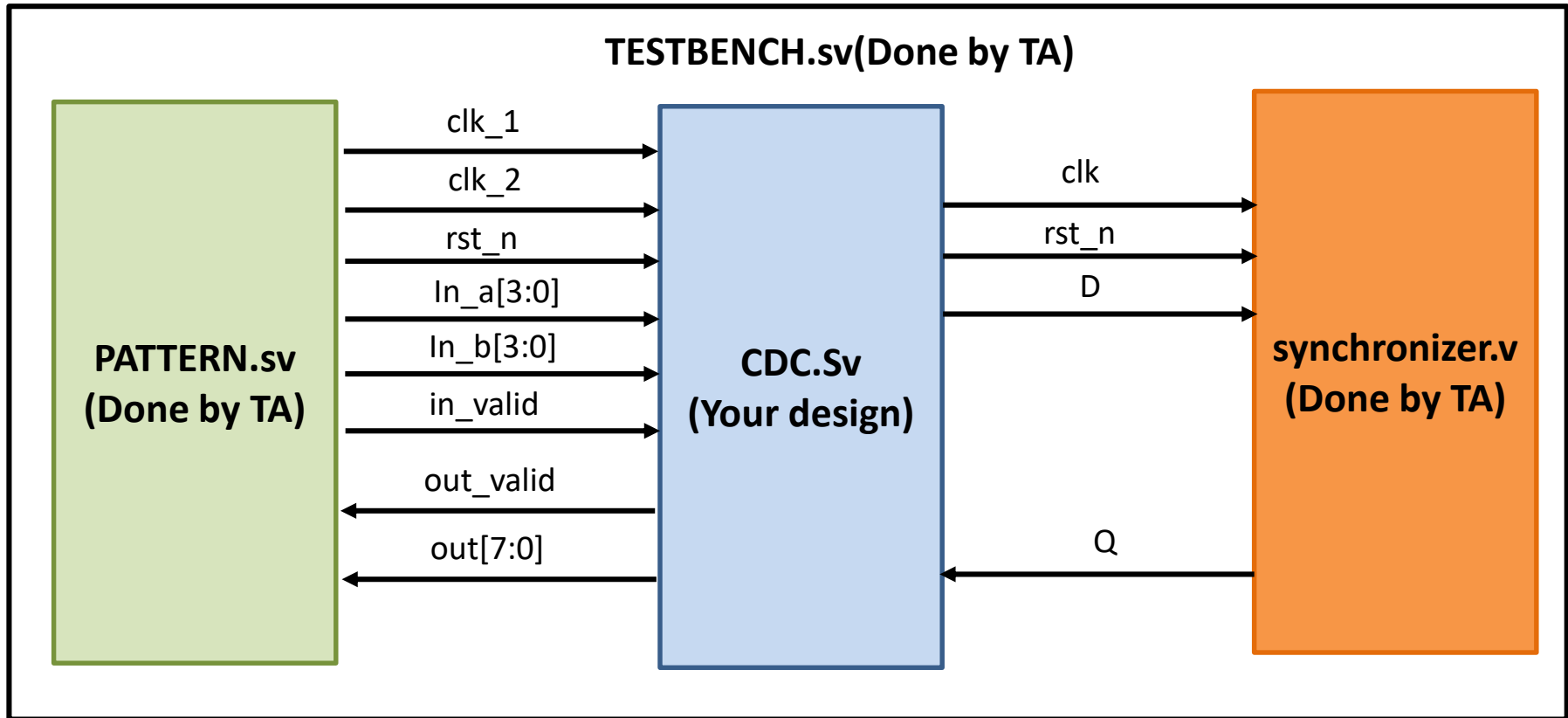


細節請參考: 上課講義 Lecture 12

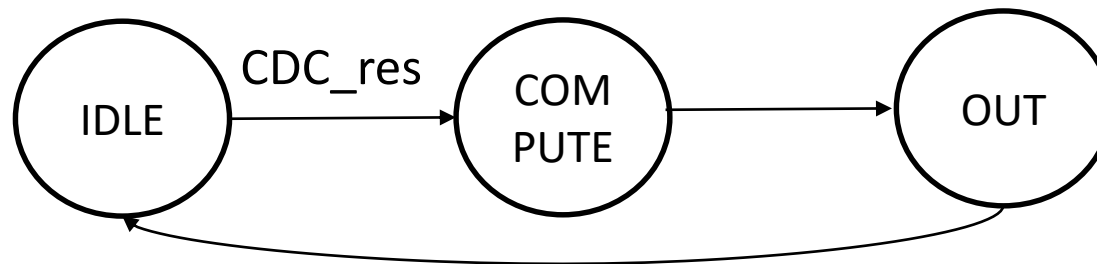
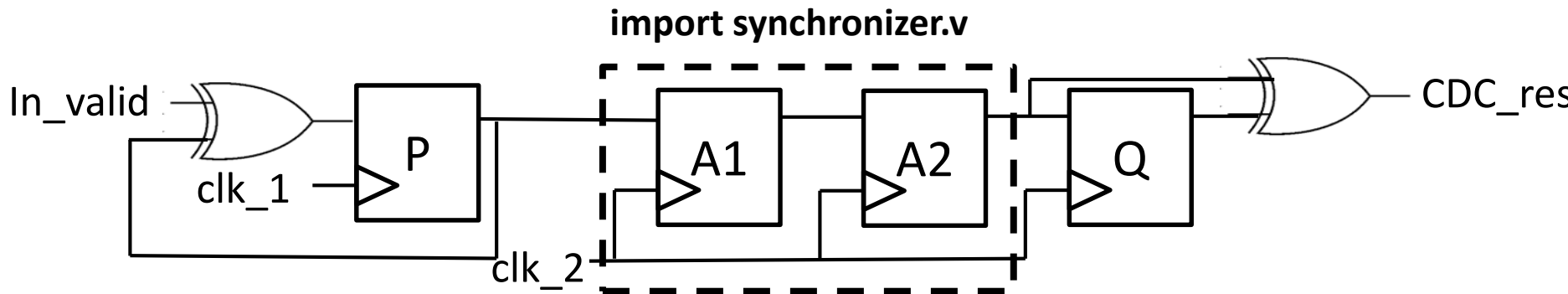
You need to design

- Clk1 = 14.1 ns , clk2 = 2.5 ns
- **Input** 在clk1 domain傳送兩筆4bit資料
- **Out** 在clk2 domain計算並接收一筆4bit資料

Block diagram



Block diagram



State	description	next_state
IDLE	IDLE	若CDC_res==1 則進入COMPUTE STATE
COMPUTE	mode = 0 , out = in_a + in_b mode = 1 , out = in_a * in_b	下個cycle無條件進入OUT STATE
OUT	將out_valid拉為high一個cycle	下個cycle無條件進入IDLE STATE

CDC.sv

Input Signal	Bit Width	Definition
clk1	1	clk2 domain 14.1ns
clk2	1	clk2 domain 2.5 ns
rst_n	1	Asynchronous active-low reset
in_a	4	在clk1 domain 且 in_valid = 1時，給予一筆資料
in_b	4	在clk1 domain 且 in_valid = 1時，給予一筆資料
in_valid	1	當此訊號拉起時給in_a和in_b
mode	1	0: out輸出in_a + in_b 1: out輸出in_a * in_b

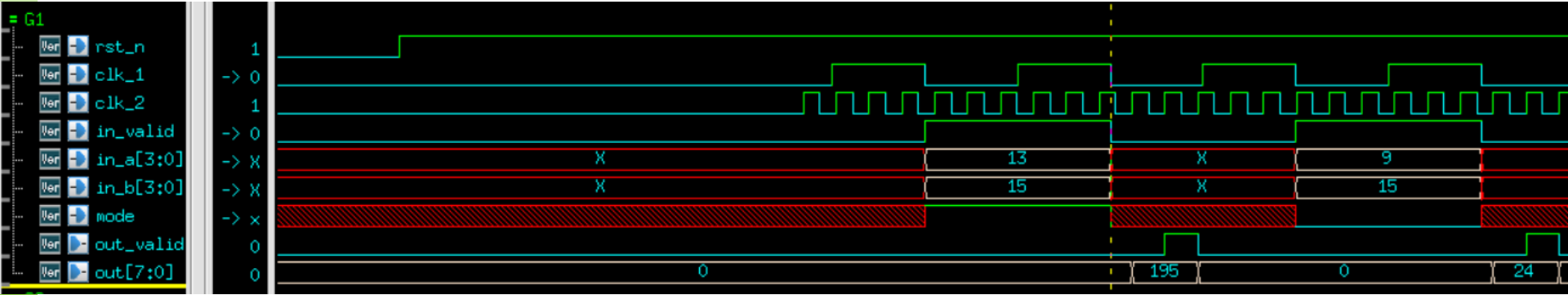
Output Signal	Bit Width	Definition
out_valid	1	在clk2 domain且out_valid = 1時，檢查out out_valid必須為1 個cycle，不能多也不能少 必須要在100個clk2 cycle內拉起out_valid
Out	4	根據mode輸出out

Spec

- 請使用synchronizer.v完成本次作業
- 所有output必須非同步負準位reset。
- 01_RTL 需要PASS。
- 02_SYN不能有error跟latches。
- 02_SYN時間timing slack必須為MET。
- 03_GATE 需要PASS
- 02_SYN， timing slack必須為MET。

Output & Waveform

negative trigger asynchronous reset



mode = 1
out = 13 * 15 = 195



mode = 0
out = 9 + 15 = 24

請在 `in_valid` 為 high 將 `in_a`, `in_b`, `mode` 存入 DFF

Command

- `tar -xvf ~dcsta01/Lab09.tar`
- Upload
 - `cd 09_upload`
 - `./01_upload`
 - `./02_download demoX`
- Separate combinational and sequential blocks

Demo1: 5/5(四), 16:25:00

Demo2: 5/5(四), 23:59:59