1-4.

(a). $1280 \times 1024 \times 3 = 3932160$ bytes #

(b). $\frac{3932160 \times 2^3}{100M} = 0.31457728$ sec #

1-5.

(a)

P1: $\frac{3GHz}{1.5} = 2 \times 10^9$

P2: $\frac{2.5GHz}{1.0} = 2.5 \times 10^9$

P3: $\frac{4GHz}{2.2} \fallingdotseq 1.82 \times 10^9$

Hence P_2 has the highest performance #

(b)

number of cycles

P1: $3GHz \cdot 10sec = 30 \times 10^9$ #

P2: $2.5GHz \cdot 10sec = 25 \times 10^9$ #

P3: $4GHz \cdot 10sec = 40 \times 10^9$ #

number of instructions

P1: $\frac{30 \times 10^9}{1.5} = 20 \times 10^9$ #

P2: $\frac{25 \times 10^9}{1.0} = 25 \times 10^9$ #

P3: $\frac{40 \times 10^9}{2.2} \fallingdotseq 18.18 \times 10^9$ #

(c)

execution time $= 10 \times 0.7 = 7$ sec

clock rate of $P_1 = \frac{20 \times 10^9 \times 1.5 \times 1.2}{7} \fallingdotseq 5.143GHz$ #

of $P_2 = \frac{25 \times 10^9 \times 1.0 \times 1.2}{7} \fallingdotseq 4.286GHz$ #

of $P_3 = \frac{18.18 \times 10^9 \times 2.2 \times 1.2}{7} \fallingdotseq 6.857GHz$ #

1-7.

(a)

CPI of $P_1 = 0.1 \times 1 + 0.2 \times 2 + 0.5 \times 3 + 0.2 \times 3 = 2.6$ #

$P_2 = 0.1 \times 2 + 0.2 \times 2 + 0.5 \times 2 + 0.2 \times 2 = 2.0$ #

(b)

clock cycles of $P_1 = 1M \times 2.6 = 2.6 \times 10^6$ #

$P_2 = 1M \times 2.0 = 2.0 \times 10^6$ #

which is faster?

CPU time of $P_1 = \frac{2.6\times10^6}{2.5\,GHz} = 1.04\,ms$

$P_2 = \frac{2.0\times10^6}{3\,GHz} \approx 0.667\,ms$

Hence P2 is faster #

1-9.

(1-9-1)

dynamic power = $\frac{1}{2}$ x capacitive load x Voltage^2 x Frequency

$\Rightarrow$ C of Pentium 4 = $\frac{2\times90W}{(1.25V)^2\times3.6GHz} = 32\,nF$ #

Core i5 Ivy Bridge = $\frac{2\times40W}{(0.9V)^2\times3.4GHz} \approx 29.049\,nF$ #

(1-9-2)

$\frac{\text{static power}}{\text{total dissipated power}}$ of Pentium 4 = $\frac{10W}{100W} = 10\%$ #

Core i5 Ivy Bridge = $\frac{30W}{70W} \approx 42.9\%$ #

$\frac{\text{static power}}{\text{dynamic power}}$ of Pentium 4 = $\frac{10W}{90W} = \frac{1}{9}$ #

Core i5 Ivy = $\frac{30W}{40W} = \frac{3}{4}$ #

(1-9-3)

Pentium 4:

new total dissipated power = $100W\times0.9 = 90W$

assume voltage should be reduced $X\cdot100\%$

$\Rightarrow 90 = 10\cdot(1-X) + 90(1-X)^2$

$\Rightarrow X \approx 5.40\%$ #

core is Ivy Bridge:

new total dissipated power = $70W\times0.9 = 63W$

assume voltage should be reduced $X\cdot100\%$

$\Rightarrow 63 = 30\cdot(1-X) + 40(1-X)^2$

$\Rightarrow X \approx 6.52\%$ #

1-11

(1-11-1)

15 cm :

$$\text{die area} = \frac{\pi \times 7.5^2}{84} \fallingdotseq 2.104\ cm^2$$

$$\text{yield} = \frac{1}{(1+(0.02 \times \frac{2.104}{2}))^2} \fallingdotseq 0.959\ \#$$

20 cm :

$$\text{die area} = \frac{\pi \times 10^2}{100} \fallingdotseq 3.142\ cm^2$$

$$\text{yield} = \frac{1}{(1+(0.031 \times \frac{3.142}{2}))^2} \fallingdotseq 0.909\ \#$$

(1-11-2)

15 cm :

$$\frac{12}{84 \times 0.959} \fallingdotseq 0.149\ \#$$

20 cm :

$$\frac{15}{100 \times 0.909} \fallingdotseq 0.165\ \#$$

(1-11-3)

15 cm :

$$\text{new die area} = \frac{\pi \times 7.5^2}{84 \times 1.1} \fallingdotseq 1.912\ cm^2\ \#$$

$$\text{new yield} = \frac{1}{(1+(0.02 \times 1.15 \times \frac{1.912}{2}))^2} \fallingdotseq 0.957\ \#$$

20 cm :

$$\text{new die area} = \frac{\pi \times 10^2}{100 \times 1.1} \fallingdotseq 2.856\ cm^2\ \#$$

$$\text{new yield} = \frac{1}{(1+(0.031 \times 1.15 \times \frac{2.856}{2}))^2} \fallingdotseq 0.905\ \#$$

(1-11-4)

0.92 :

$$\frac{1}{(1+(\text{defect per area} \times \frac{2\ cm^2}{2}))^2} = 0.92$$

$$\Rightarrow \text{defect per area} \fallingdotseq 0.043\ \text{defects}/cm^2\ \#$$

0.95:

$$\frac{1}{\left(1+\left(\text{defect per area} \times \frac{2cm^2}{2}\right)\right)^2} = 0.95$$

$\Rightarrow$ defect per area $\fallingdotseq$ 0.026 defects/cm^2 #

1-14.

(1-14-1)

$$\frac{70 \times 0.2}{250} = 5.6\%$$

Hence the total time reduce 5.6% #

(1-14-2)

$$\frac{250 \times 0.2}{55} \fallingdotseq 90.9\%$$

Hence the time for INT operations reduce 90.9% #

(1-14-3)

$250 \times 0.2 = 50$

$50 > 40$

(branch instruction)

Hence No #

1-15

(1-15-1)

total cycles $= 50 \times 10^6 \times 1 + 110 \times 10^6 \times 1 + 80 \times 10^6 \times 4 + 16 \times 10^6 \times 2$

$= 512 \times 10^6$

cycles of FP instructions $= 50 \times 10^6 \times 1 < \frac{1}{2} \times 512 \times 10^6 = 256 \times 10^6$

Hence it is impossible #

(1-15-2)

total cycles $= 512 \times 10^6$

$\frac{1}{2} \times 512 \times 10^6 = 256 \times 10^6$

$= 80 \times 10^6 \times 4 \times \underline{0.8}$

Hence we should improve the CPI of L/S by 80% #

(1-15-3)

new total cycles $= 50 \times 10^6 \times 1 \times 0.6 + 110 \times 10^6 \times 1 \times 0.6 + 80 \times 10^6 \times 4 \times 0.7$
$+ 16 \times 10^6 \times 2 \times 0.7$

$= 342.4 \times 10^6$

new CPU times = $\frac{342.4 \times 10^6}{2\,GHz} = 0.17125$

old CPU times = $\frac{512 \times 10^6}{2\,GHz} = 0.256$

$\Rightarrow \frac{0.1712}{0.256} = 0.66875$

Hence CPU time Improve by 33.125% #