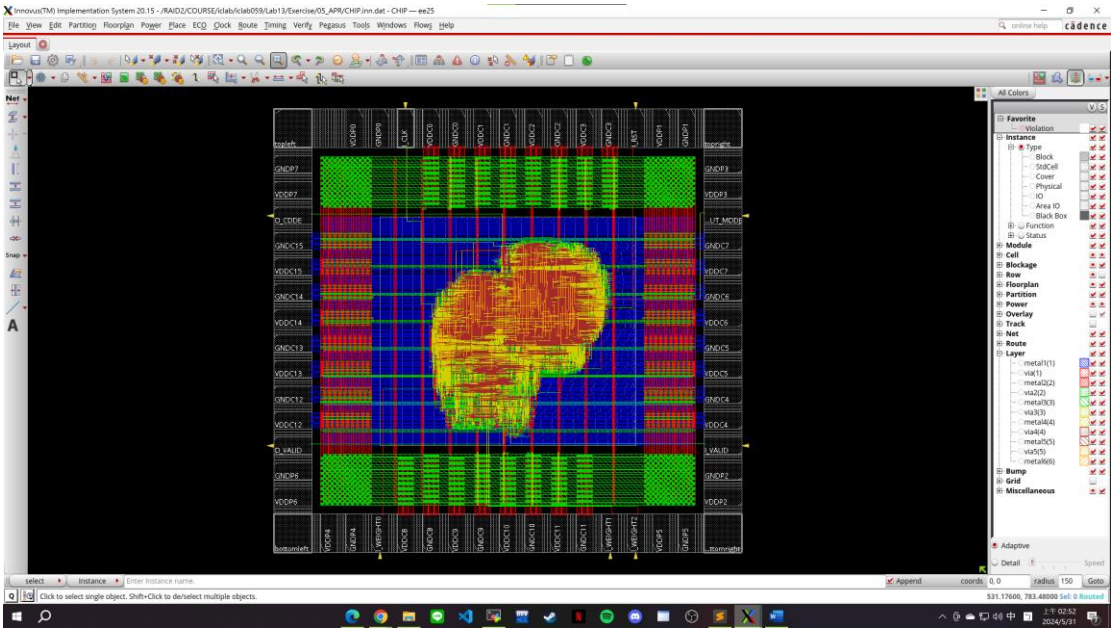
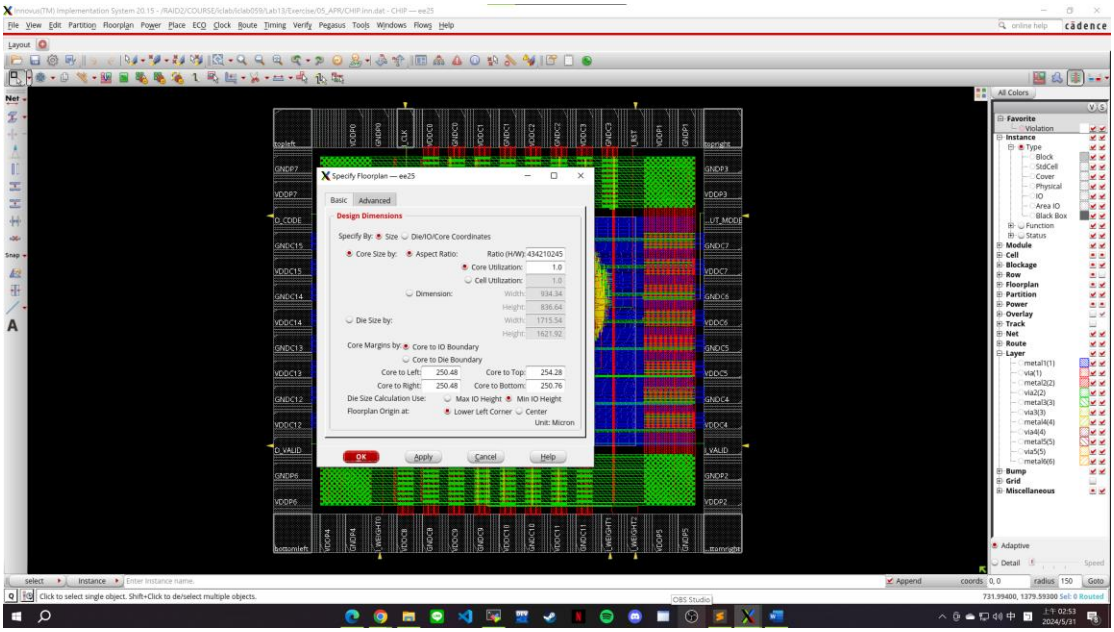
Report

1. Chip Layout View :

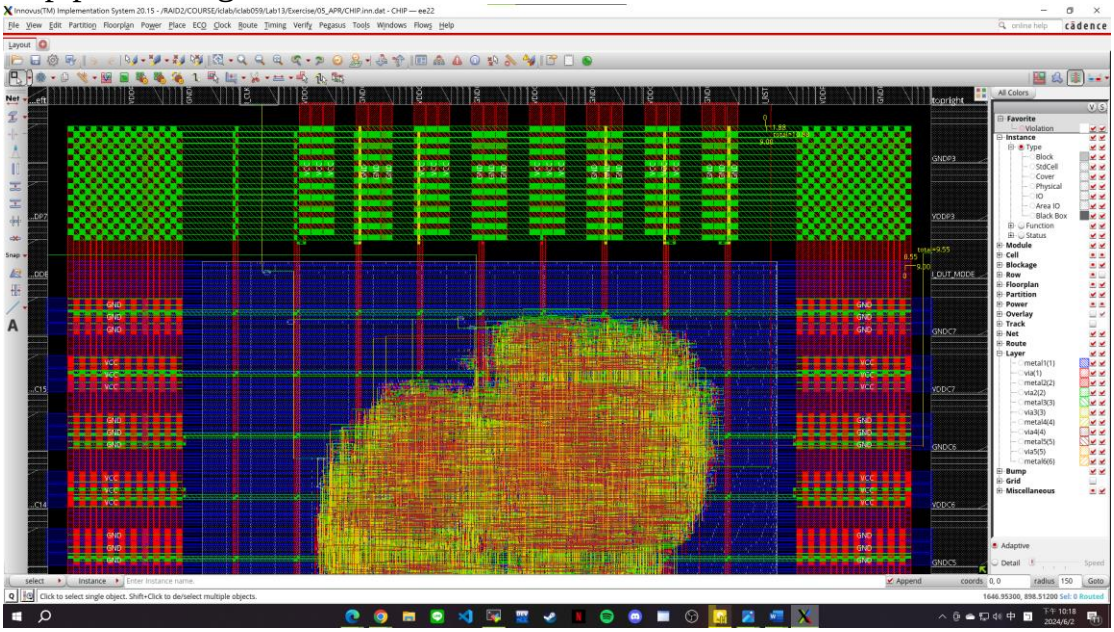


2. Core to IO boundary :

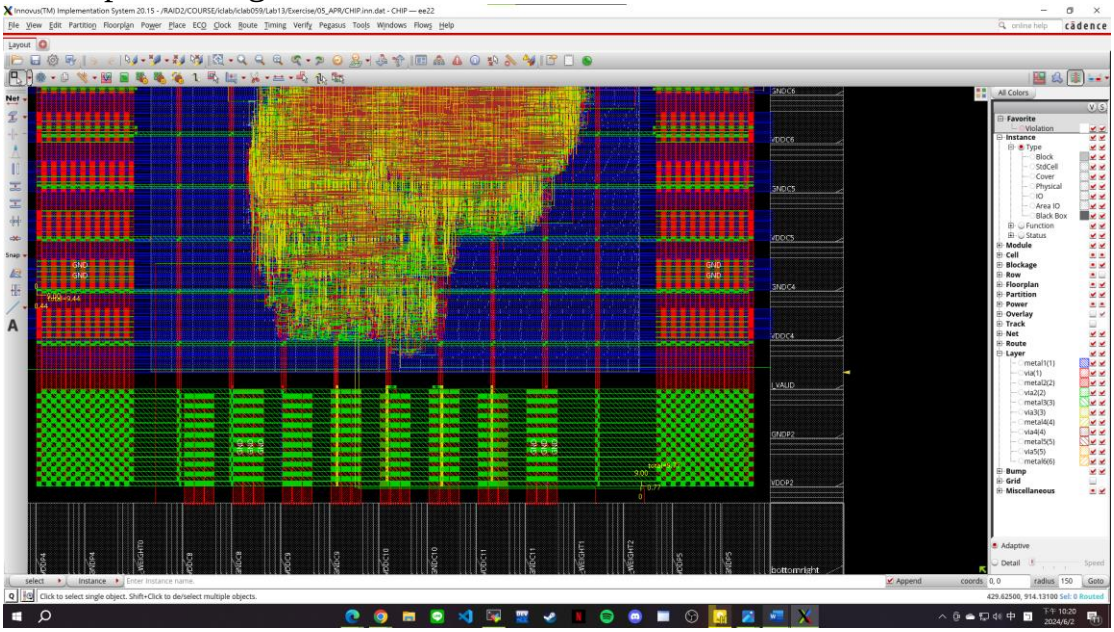


3. Core Ring :

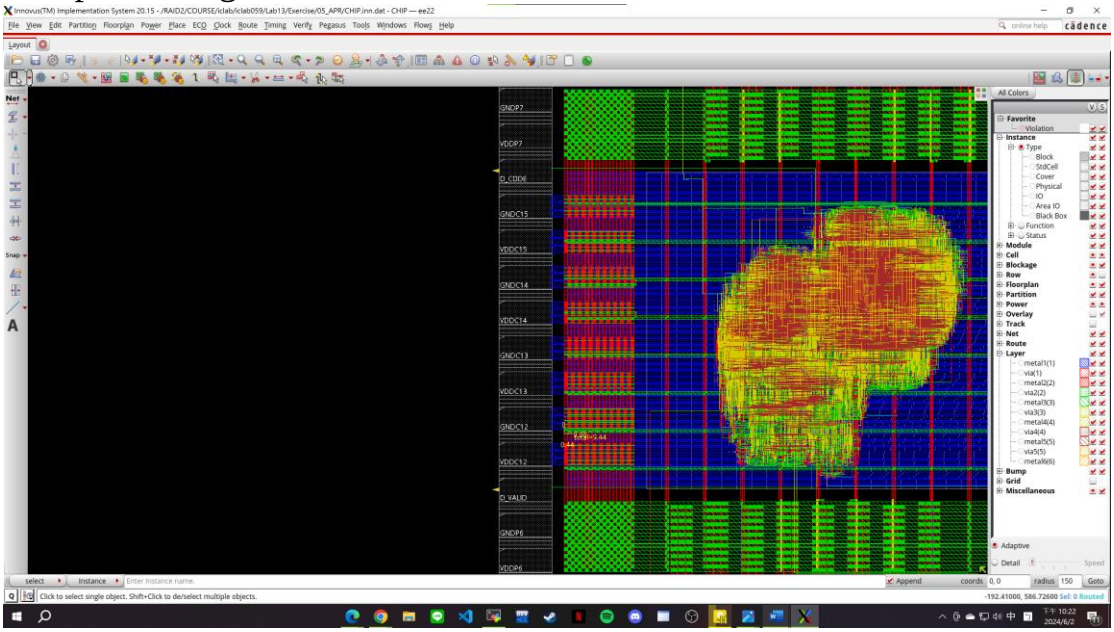
Top power ring

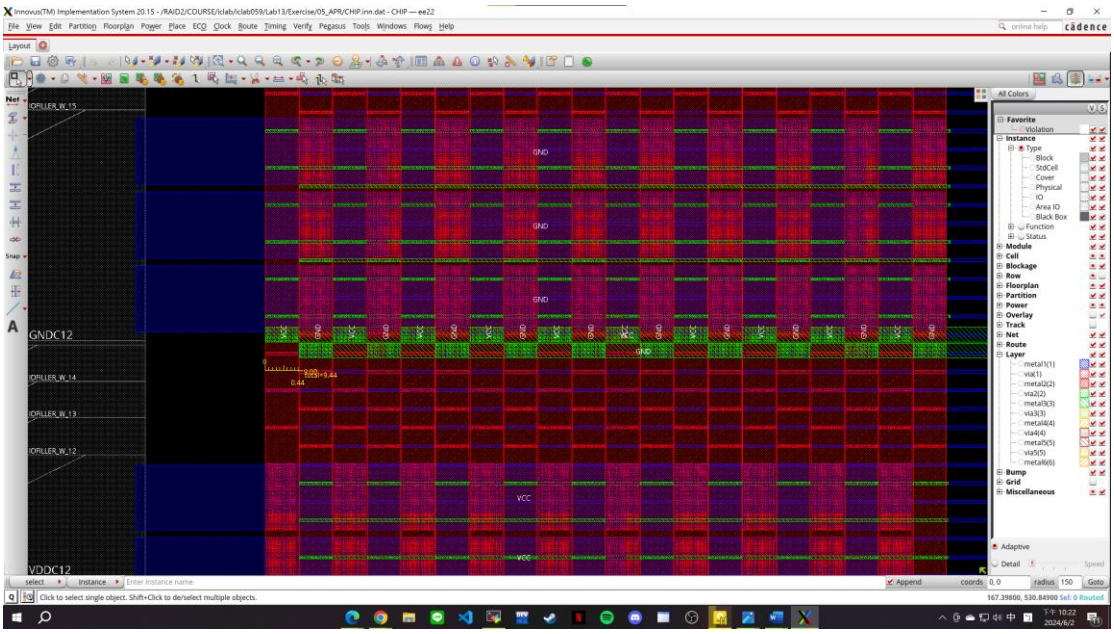


Down power ring

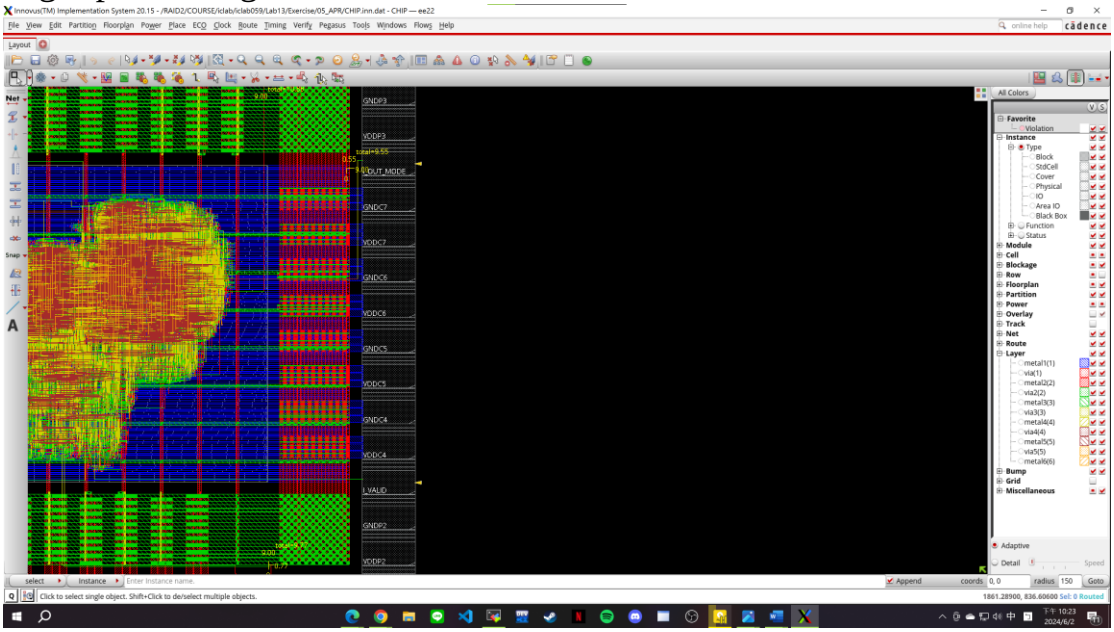


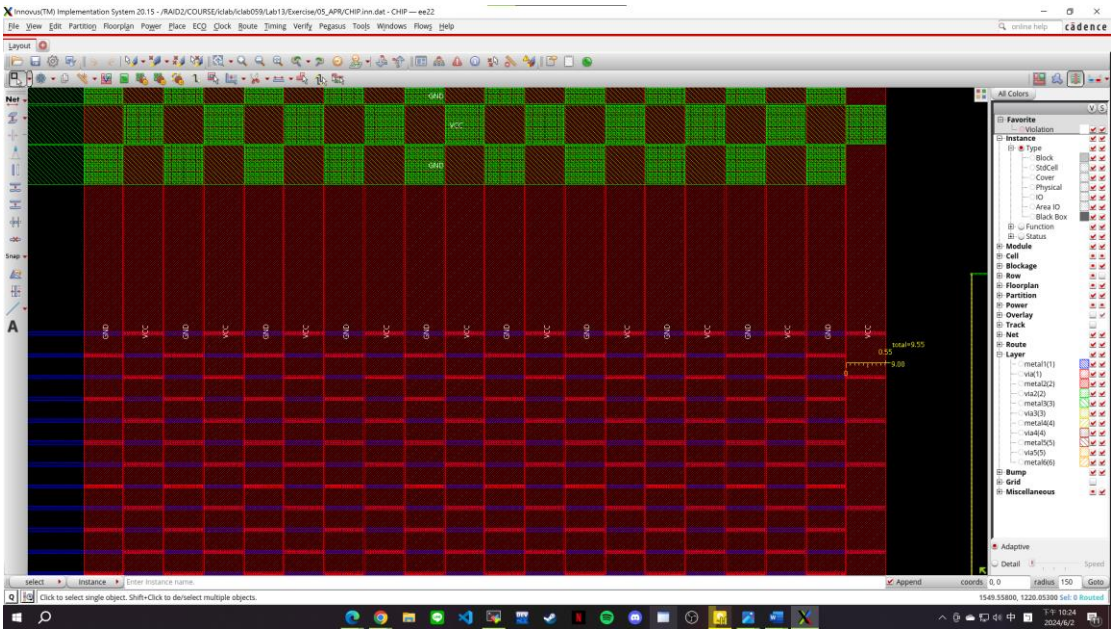
Left power ring



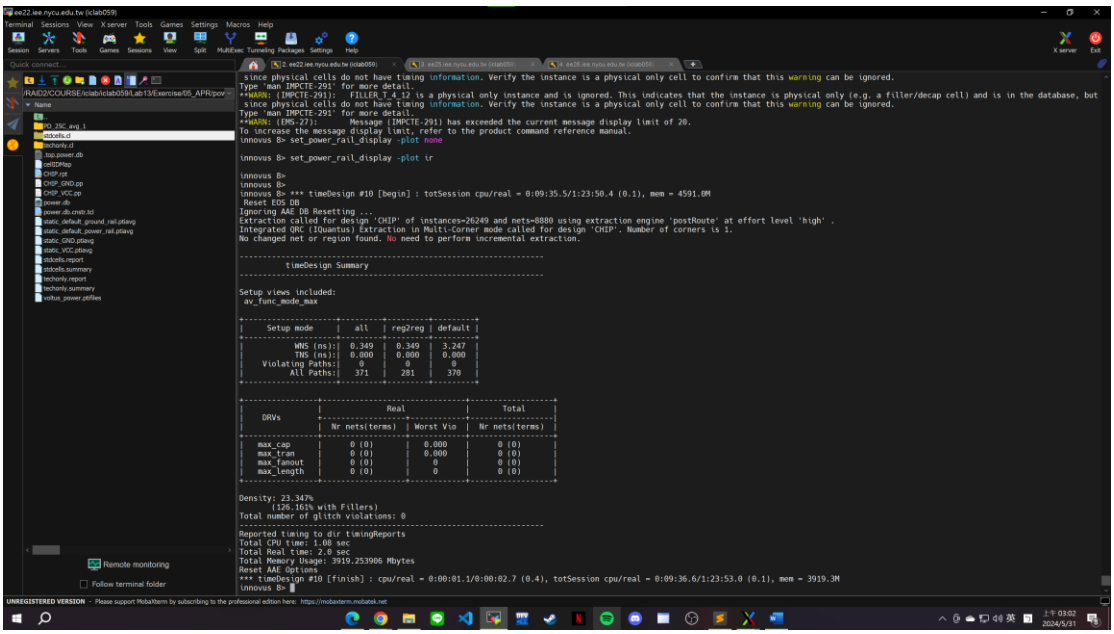


Right power ring

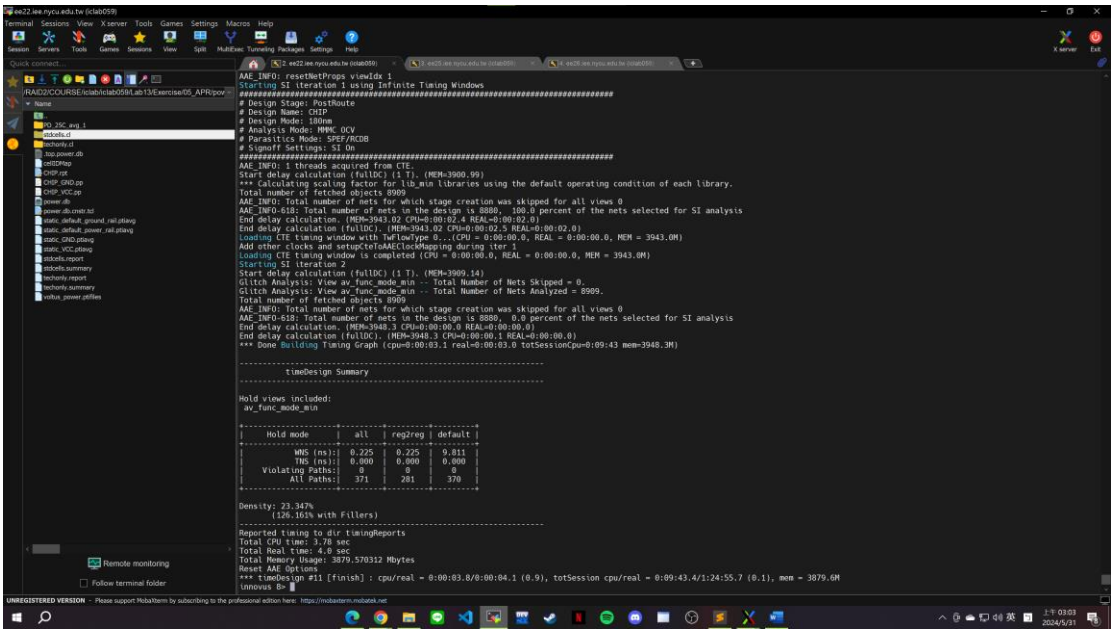




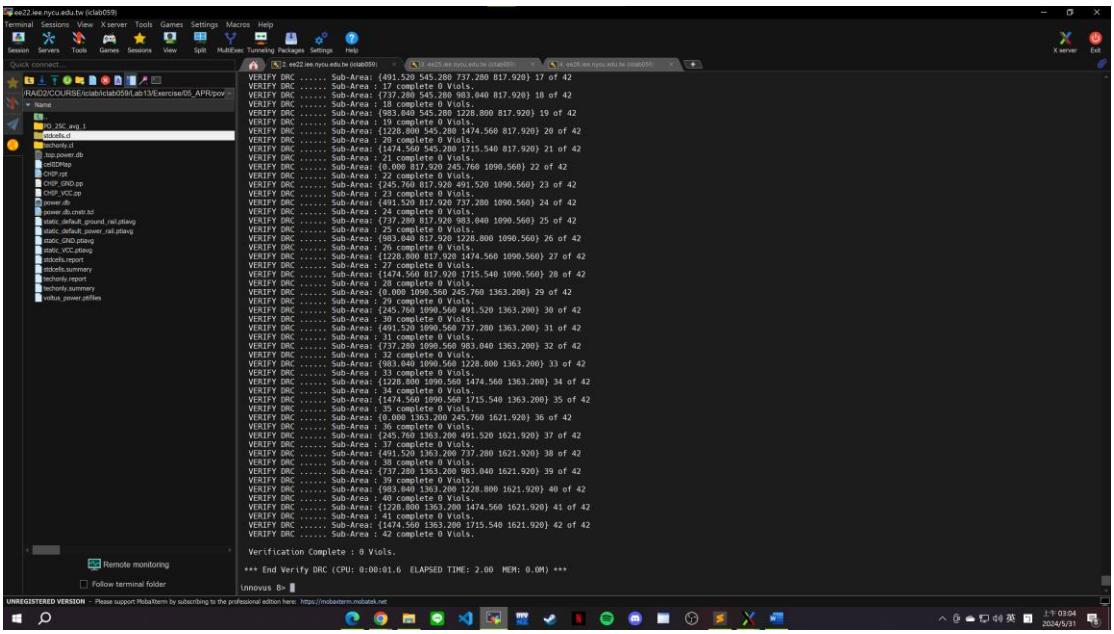
4. Post-Route setup time analysis :



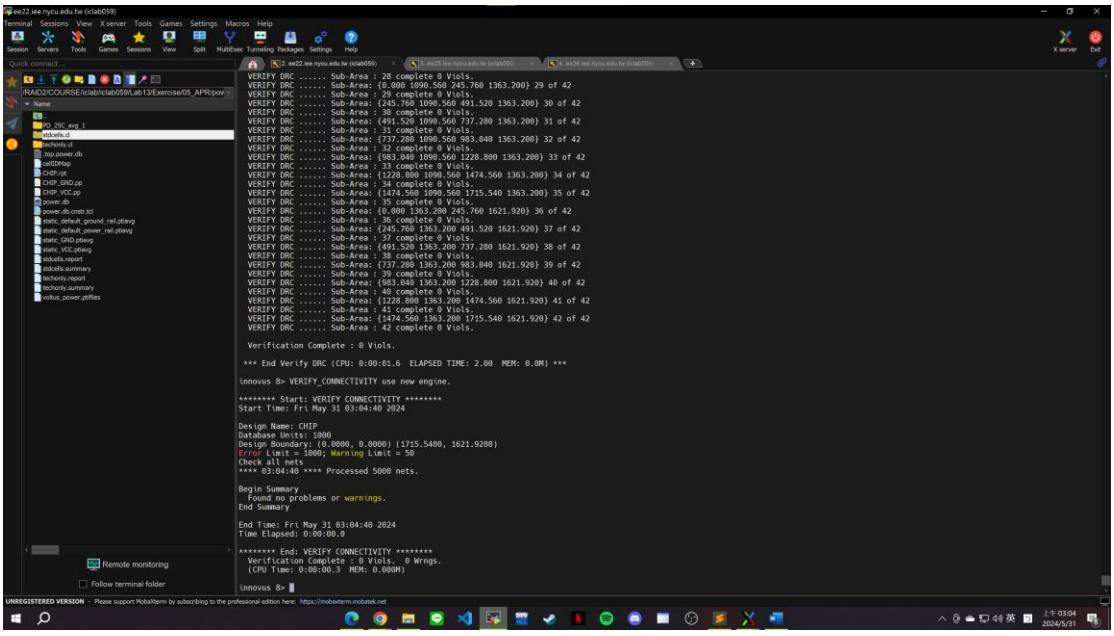
5. Post-Route hold time analysis :



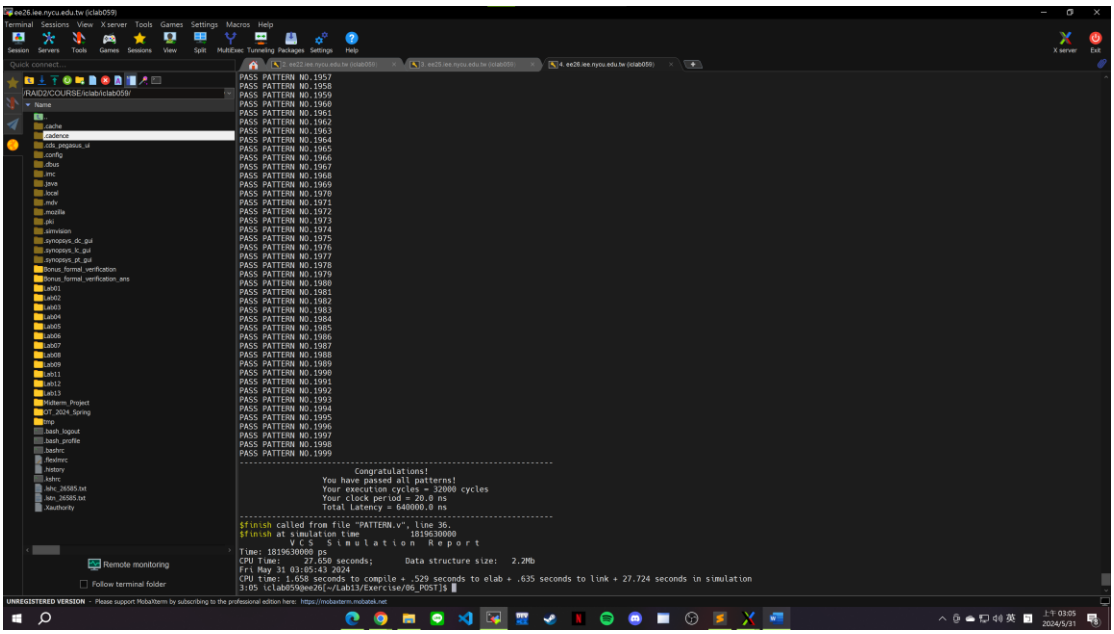
6. DRC result :



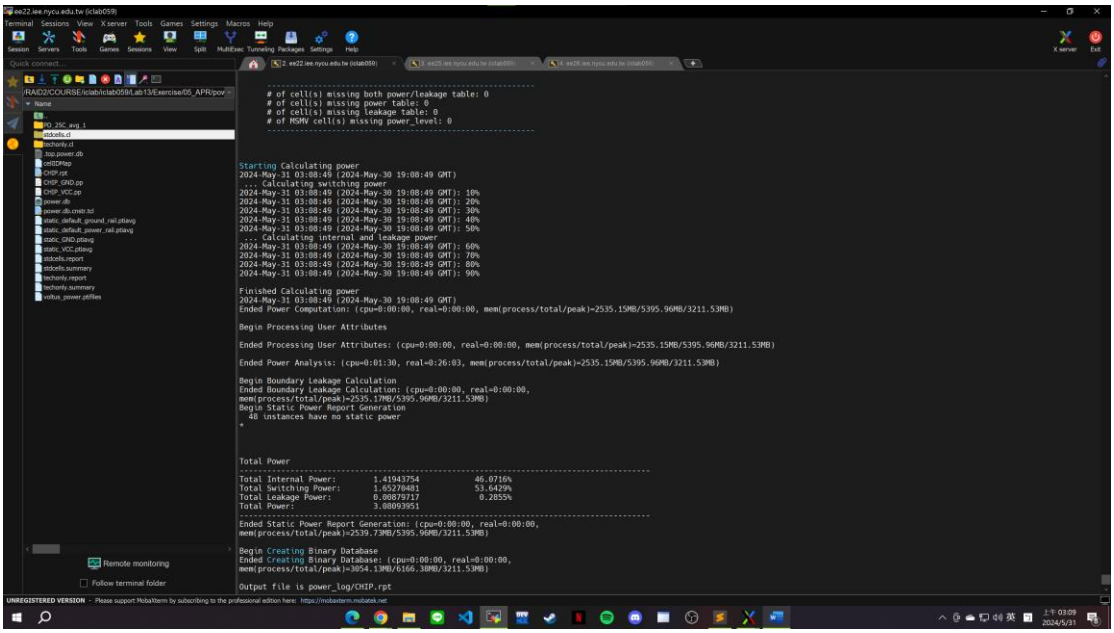
7. LVS result :



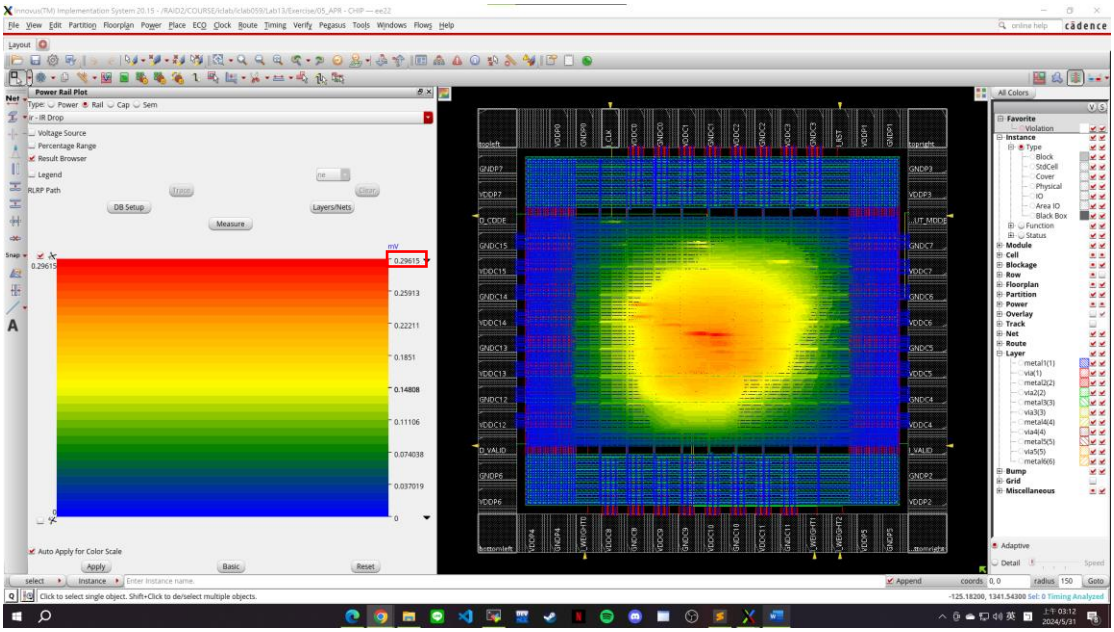
8. Post Layout simulation result :



9. Power result :



10. IR Drop Results :



Method to mitigate the IR drop issue:

1. Use several sets of core power pads; I placed four sets on each side, for a total of 16 sets of core power pads.
2. Increase the number of stripes and reduce the spacing between them.