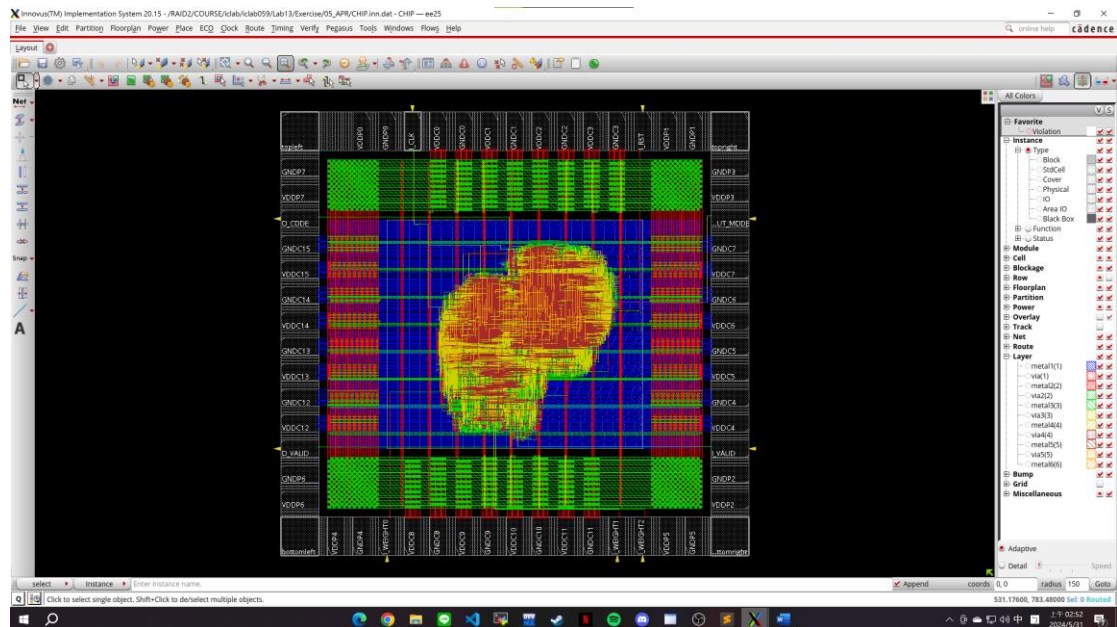
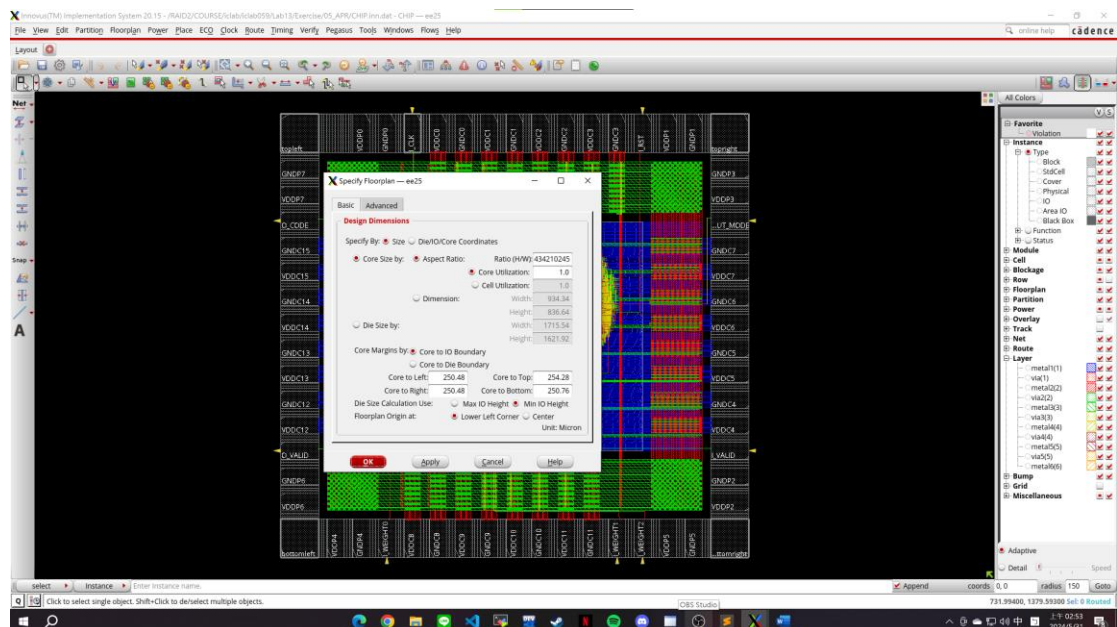


Report

1. Chip Layout View :

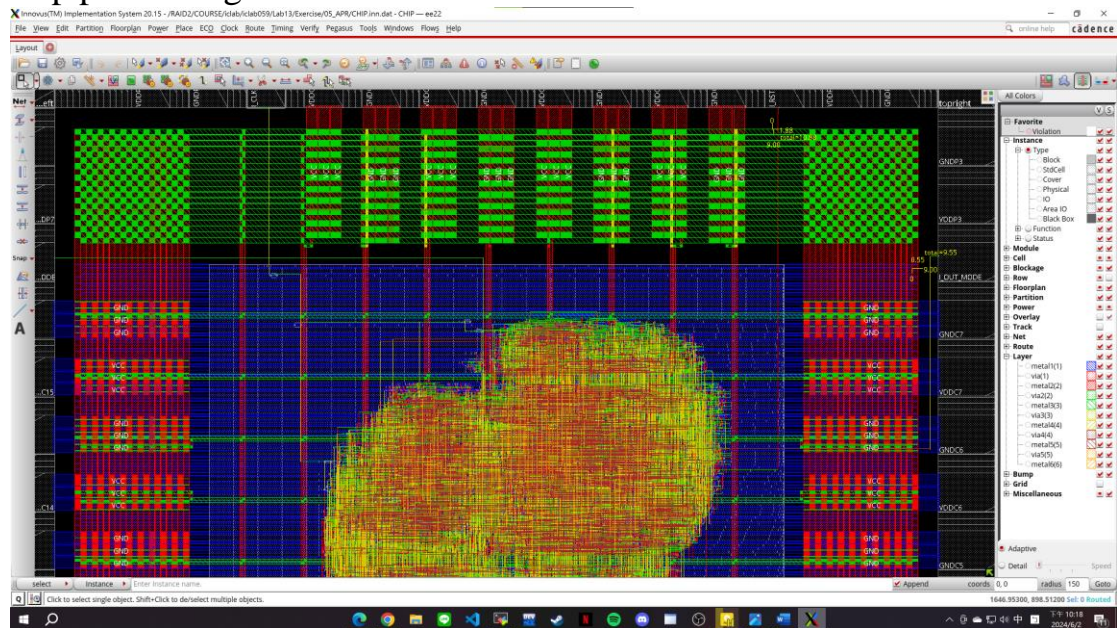


2. Core to IO boundary :

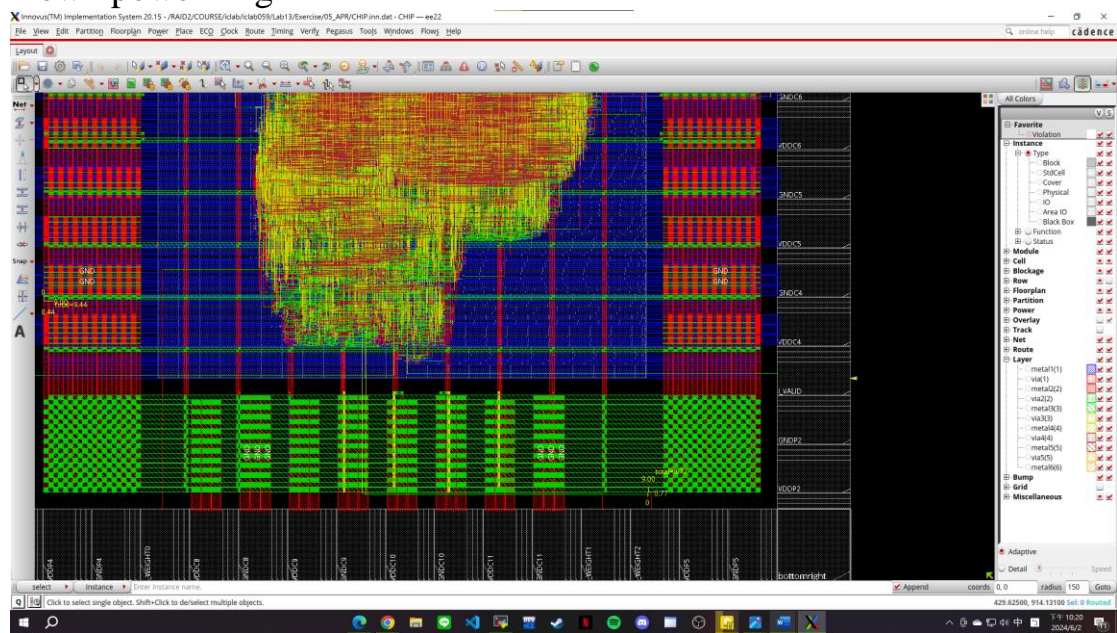


3. Core Ring :

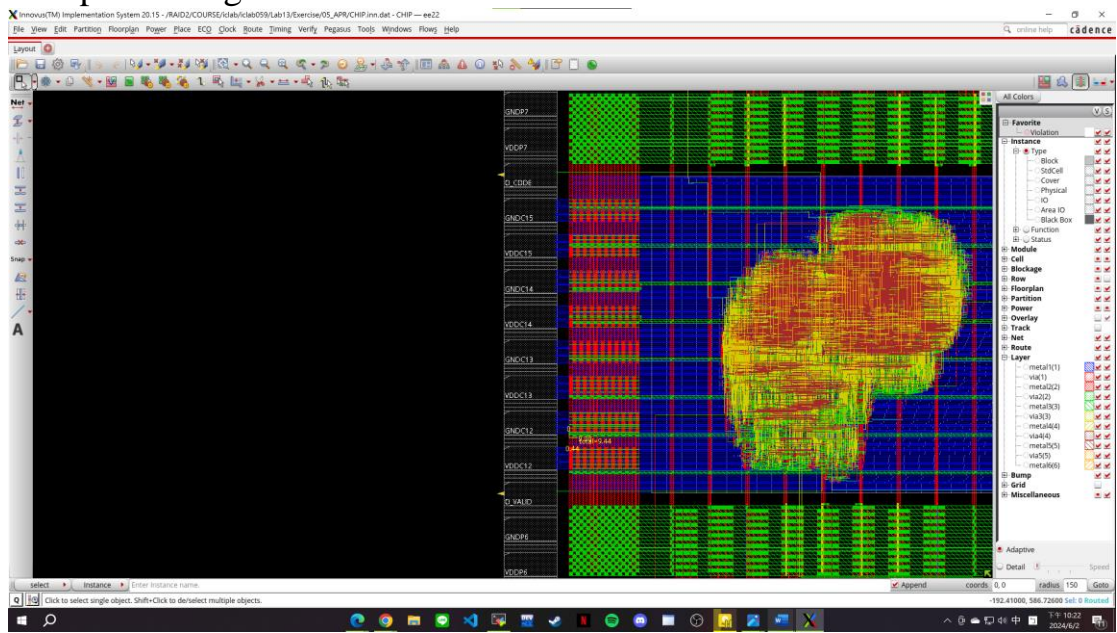
Top power ring



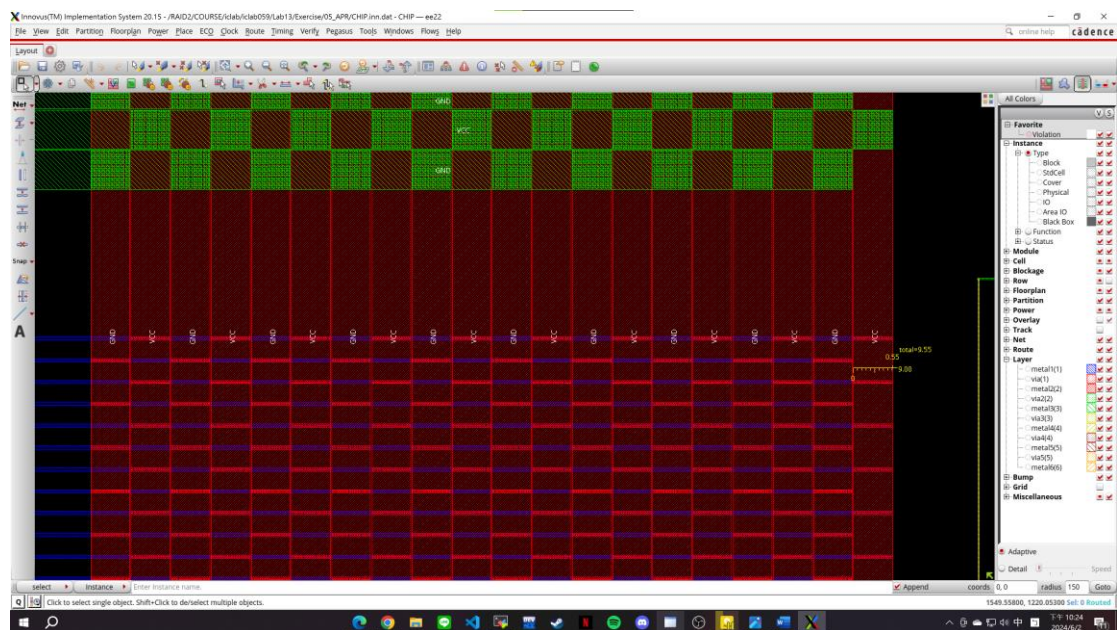
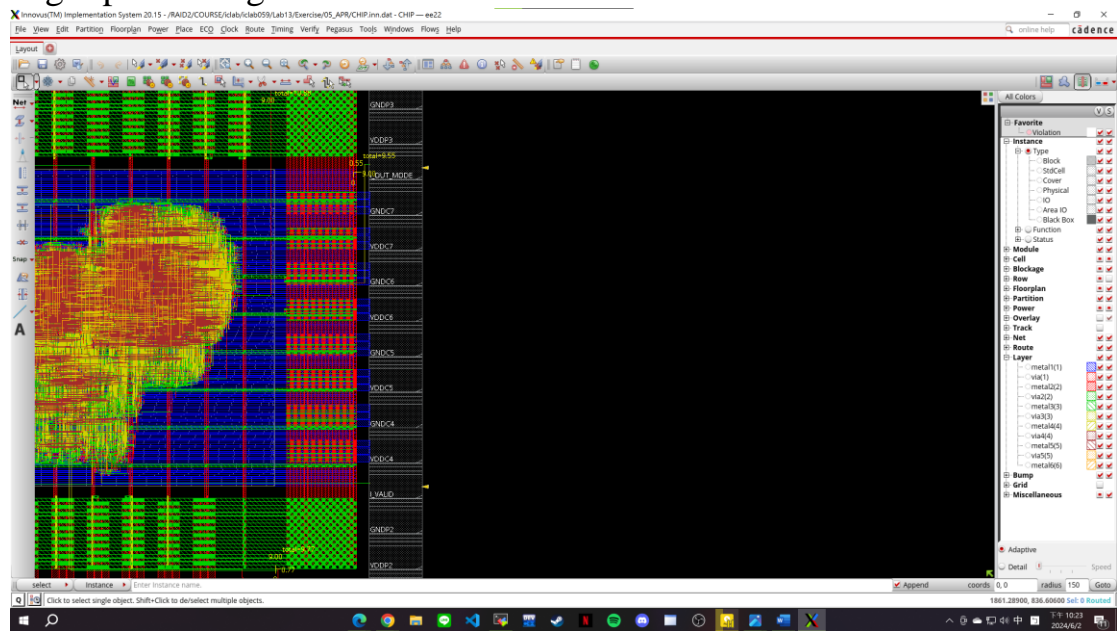
Down power ring



Left power ring



Right power ring



4. Post-Route setup time analysis :

The screenshot displays the Xilinx Vivado IDE interface. The left sidebar shows a project tree with files like 'chip.drc', 'chip.ncs', and 'chip.xdc'. The main window shows the 'Setup Time Summary' report for a design named 'CHIP'. The report includes a table for 'Setup views included' and a table for 'DRVs' (Design Rule Violations).

Setup views included:

Setup Mode	all	regreg	default
WNS (ns)	0.340	0.340	0.340
TNS (ns)	0.000	0.000	0.000
Violating Paths	0	0	0
All Paths	371	281	370

DRVs

DRVs	Real	Total
Nr nets/terms	Worst Vio	Nr nets/terms
max_cap	0 (0)	0 (0)
max_ttran	0 (0)	0 (0)
max_fanout	0 (0)	0 (0)
max_length	0 (0)	0 (0)

Density: 23.34%
(126.16% with Fillers)
Total number of glitch violations: 0
Reported timing to dir timingReports
Total CPU time: 1.08 sec
Total real time: 2.6 sec
Total Memory Usage: 3919.253906 Mbytes
Reset: All Options
*** timeDesign #10 [finish] : cpu/real = 0:00:01.1/0:00:02.7 (0.4), totSession cpu/real = 0:09:35.5/1:23:50.4 (0.1), mem = 4591.0M
Unnovus B+

5. Post-Route hold time analysis :

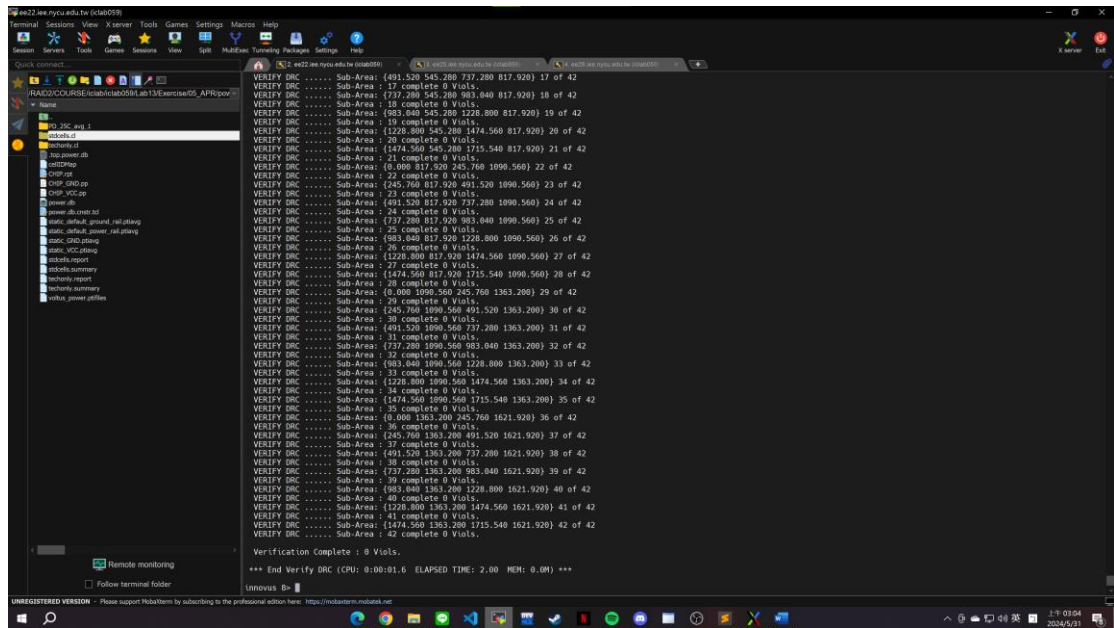
The screenshot displays the Xilinx Vivado IDE interface. The left sidebar shows a project tree with files like 'chip.drc', 'chip.ncs', and 'chip.xdc'. The main window shows the 'Hold Time Summary' report for a design named 'CHIP'. The report includes a table for 'Hold views included' and a table for 'DRVs' (Design Rule Violations).

Hold views included:

Hold mode	all	regreg	default
WNS (ns)	0.225	0.225	0.811
TNS (ns)	0.000	0.000	0.000
Violating Paths	0	0	0
All Paths	371	281	370

Density: 23.34%
(126.16% with Fillers)
Reported timing to dir timingReports
Total CPU time: 3.78 sec
Total real time: 4.6 sec
Total Memory Usage: 3879.570312 Mbytes
Reset: All Options
*** timeDesign #11 [finish] : cpu/real = 0:00:03.8/0:00:04.1 (0.9), totSession cpu/real = 0:09:43.4/1:24:55.7 (0.1), mem = 3879.0M
Unnovus B+

6. DRC result :



The screenshot shows the Cadence Virtuoso interface with the DRC (Design Rule Check) results displayed in the command window. The results show a total of 0 violations across 42 sub-areas. The interface includes a project tree on the left, a command window in the center, and a status bar at the bottom.

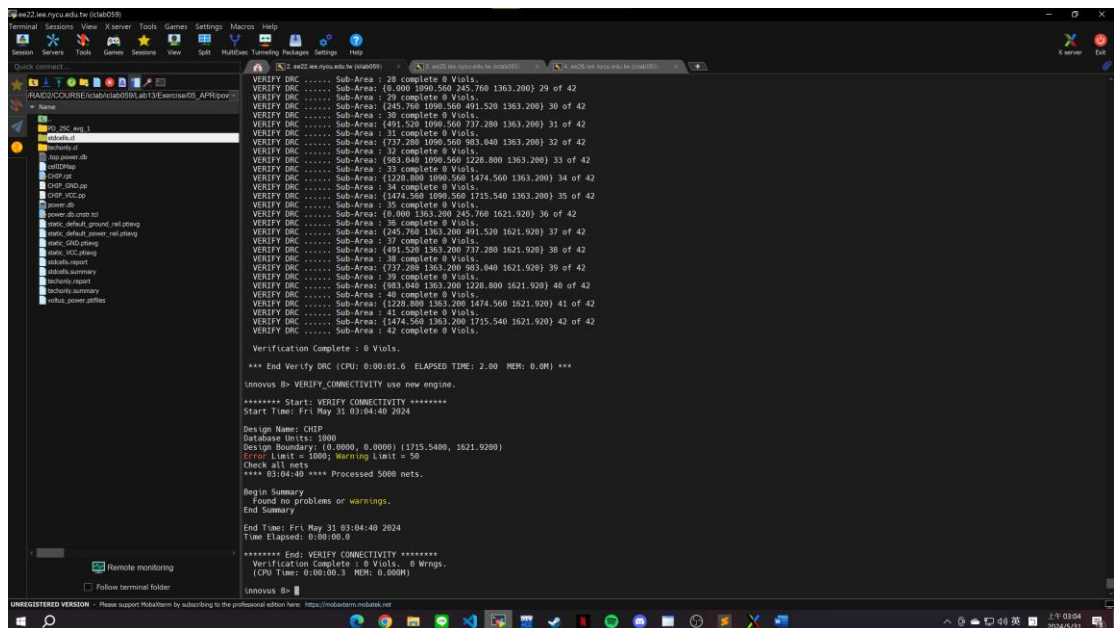
```
VERIFY DRC ..... Sub-Area : (491,520 545,280 737,280 817,920) 17 of 42
VERIFY DRC ..... Sub-Area : 17 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (737,280 545,280 983,040 817,920) 18 of 42
VERIFY DRC ..... Sub-Area : 18 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (983,040 545,280 1228,800 817,920) 19 of 42
VERIFY DRC ..... Sub-Area : 19 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1228,800 545,280 1474,560 817,920) 20 of 42
VERIFY DRC ..... Sub-Area : 20 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1474,560 545,280 1715,540 817,920) 21 of 42
VERIFY DRC ..... Sub-Area : 21 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (0,000 817,920 245,760 1090,560) 22 of 42
VERIFY DRC ..... Sub-Area : 22 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (245,760 817,920 491,520 1090,560) 23 of 42
VERIFY DRC ..... Sub-Area : 23 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (491,520 817,920 737,280 1090,560) 24 of 42
VERIFY DRC ..... Sub-Area : 24 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (737,280 817,920 983,040 1090,560) 25 of 42
VERIFY DRC ..... Sub-Area : 25 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (983,040 817,920 1228,800 1090,560) 26 of 42
VERIFY DRC ..... Sub-Area : 26 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1228,800 817,920 1474,560 1090,560) 27 of 42
VERIFY DRC ..... Sub-Area : 27 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1474,560 817,920 1715,540 1090,560) 28 of 42
VERIFY DRC ..... Sub-Area : 28 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (0,000 1090,560 245,760 1363,200) 29 of 42
VERIFY DRC ..... Sub-Area : 29 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (245,760 1090,560 491,520 1363,200) 30 of 42
VERIFY DRC ..... Sub-Area : 30 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (491,520 1090,560 737,280 1363,200) 31 of 42
VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (737,280 1090,560 983,040 1363,200) 32 of 42
VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (983,040 1090,560 1228,800 1363,200) 33 of 42
VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1228,800 1090,560 1474,560 1363,200) 34 of 42
VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1474,560 1090,560 1715,540 1363,200) 35 of 42
VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (0,000 1363,200 245,760 1621,920) 36 of 42
VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (245,760 1363,200 491,520 1621,920) 37 of 42
VERIFY DRC ..... Sub-Area : 37 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (491,520 1363,200 737,280 1621,920) 38 of 42
VERIFY DRC ..... Sub-Area : 38 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (737,280 1363,200 983,040 1621,920) 39 of 42
VERIFY DRC ..... Sub-Area : 39 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (983,040 1363,200 1228,800 1621,920) 40 of 42
VERIFY DRC ..... Sub-Area : 40 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1228,800 1363,200 1474,560 1621,920) 41 of 42
VERIFY DRC ..... Sub-Area : 41 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1474,560 1363,200 1715,540 1621,920) 42 of 42
VERIFY DRC ..... Sub-Area : 42 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.6 ELAPSED TIME: 2.00 MEM: 0.0M) ***

Uninovus B>
```

7. LVS result :



The screenshot shows the Cadence Virtuoso interface with the LVS (Layout Versus Schematic) results displayed in the command window. The results show a total of 0 violations across 42 sub-areas. The interface includes a project tree on the left, a command window in the center, and a status bar at the bottom.

```
VERIFY DRC ..... Sub-Area : (491,520 545,280 737,280 817,920) 17 of 42
VERIFY DRC ..... Sub-Area : 17 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (737,280 545,280 983,040 817,920) 18 of 42
VERIFY DRC ..... Sub-Area : 18 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (983,040 545,280 1228,800 817,920) 19 of 42
VERIFY DRC ..... Sub-Area : 19 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1228,800 545,280 1474,560 817,920) 20 of 42
VERIFY DRC ..... Sub-Area : 20 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1474,560 545,280 1715,540 817,920) 21 of 42
VERIFY DRC ..... Sub-Area : 21 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (0,000 817,920 245,760 1090,560) 22 of 42
VERIFY DRC ..... Sub-Area : 22 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (245,760 817,920 491,520 1090,560) 23 of 42
VERIFY DRC ..... Sub-Area : 23 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (491,520 817,920 737,280 1090,560) 24 of 42
VERIFY DRC ..... Sub-Area : 24 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (737,280 817,920 983,040 1090,560) 25 of 42
VERIFY DRC ..... Sub-Area : 25 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (983,040 817,920 1228,800 1090,560) 26 of 42
VERIFY DRC ..... Sub-Area : 26 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1228,800 817,920 1474,560 1090,560) 27 of 42
VERIFY DRC ..... Sub-Area : 27 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1474,560 817,920 1715,540 1090,560) 28 of 42
VERIFY DRC ..... Sub-Area : 28 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (0,000 1090,560 245,760 1363,200) 29 of 42
VERIFY DRC ..... Sub-Area : 29 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (245,760 1090,560 491,520 1363,200) 30 of 42
VERIFY DRC ..... Sub-Area : 30 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (491,520 1090,560 737,280 1363,200) 31 of 42
VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (737,280 1090,560 983,040 1363,200) 32 of 42
VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (983,040 1090,560 1228,800 1363,200) 33 of 42
VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1228,800 1090,560 1474,560 1363,200) 34 of 42
VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1474,560 1090,560 1715,540 1363,200) 35 of 42
VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (0,000 1363,200 245,760 1621,920) 36 of 42
VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (245,760 1363,200 491,520 1621,920) 37 of 42
VERIFY DRC ..... Sub-Area : 37 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (491,520 1363,200 737,280 1621,920) 38 of 42
VERIFY DRC ..... Sub-Area : 38 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (737,280 1363,200 983,040 1621,920) 39 of 42
VERIFY DRC ..... Sub-Area : 39 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (983,040 1363,200 1228,800 1621,920) 40 of 42
VERIFY DRC ..... Sub-Area : 40 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1228,800 1363,200 1474,560 1621,920) 41 of 42
VERIFY DRC ..... Sub-Area : 41 complete 0 Viols.
VERIFY DRC ..... Sub-Area : (1474,560 1363,200 1715,540 1621,920) 42 of 42
VERIFY DRC ..... Sub-Area : 42 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.6 ELAPSED TIME: 2.00 MEM: 0.0M) ***

Uninovus B> VERIFY_CONNECTIVITY use new engine.

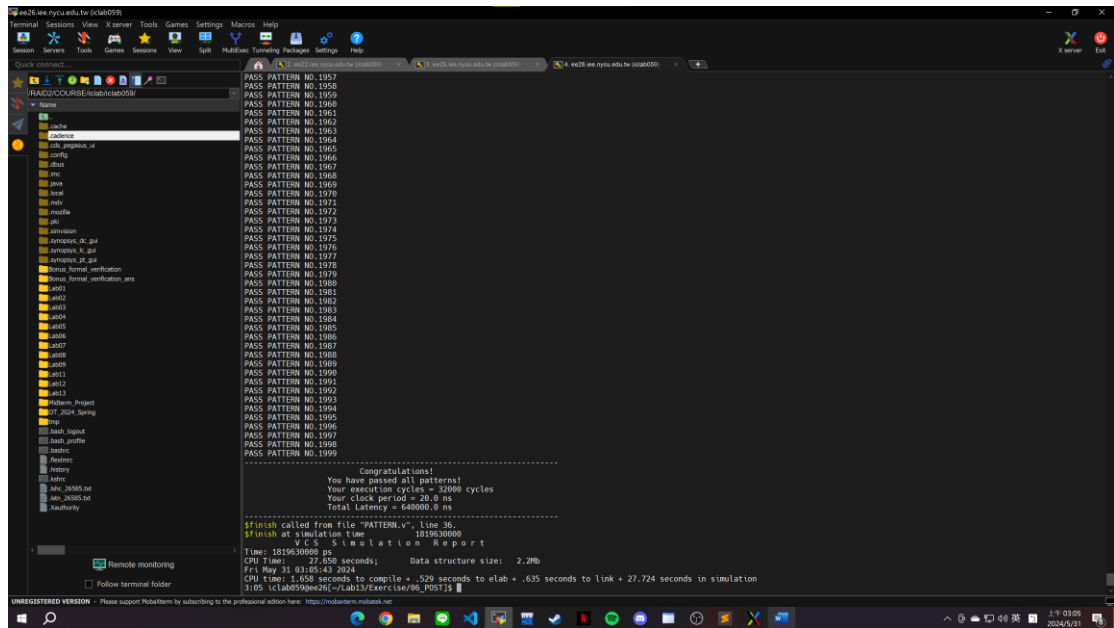
***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri May 31 03:04:40 2024
Design Name: CHIP
Design Boundary: (0,0000 0,0000) (1715,5400, 1621,9200)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 03:04:40 **** Processed 5000 nets.

Begin Summary
Found no problems or warnings.
End Summary

End Time: Fri May 31 03:04:40 2024
Time Elapsed: 0:00:00.0
***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.3 MEM: 0.000M)

Uninovus B>
```

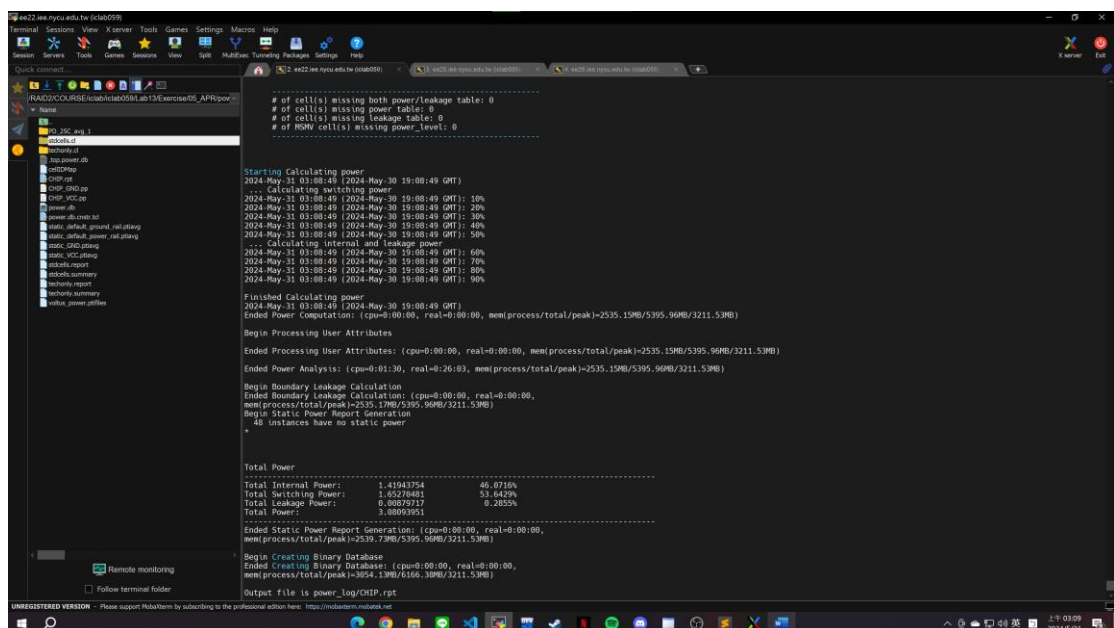
8. Post Layout simulation result :



```
PASS PATTERN NO.1957
PASS PATTERN NO.1958
PASS PATTERN NO.1959
PASS PATTERN NO.1960
PASS PATTERN NO.1961
PASS PATTERN NO.1962
PASS PATTERN NO.1963
PASS PATTERN NO.1964
PASS PATTERN NO.1965
PASS PATTERN NO.1966
PASS PATTERN NO.1967
PASS PATTERN NO.1968
PASS PATTERN NO.1969
PASS PATTERN NO.1970
PASS PATTERN NO.1971
PASS PATTERN NO.1972
PASS PATTERN NO.1973
PASS PATTERN NO.1974
PASS PATTERN NO.1975
PASS PATTERN NO.1976
PASS PATTERN NO.1977
PASS PATTERN NO.1978
PASS PATTERN NO.1979
PASS PATTERN NO.1980
PASS PATTERN NO.1981
PASS PATTERN NO.1982
PASS PATTERN NO.1983
PASS PATTERN NO.1984
PASS PATTERN NO.1985
PASS PATTERN NO.1986
PASS PATTERN NO.1987
PASS PATTERN NO.1988
PASS PATTERN NO.1989
PASS PATTERN NO.1990
PASS PATTERN NO.1991
PASS PATTERN NO.1992
PASS PATTERN NO.1993
PASS PATTERN NO.1994
PASS PATTERN NO.1995

-----
Congratulations!
You have passed all patterns!
Your execution cycles = 32000 cycles
Your clock period = 20.8 ns
Total Latency = 640000.0 ns
-----
Finish called from file "PATTERN.v", line 30,
at simulation time 199530000
VCS Simulation Report
-----
Time: 1019630000 ps
CPU Time: 27.650 seconds; Data structure size: 2.2Mb
Fri May 31 03:03:43 2024
CPU time: 1.658 seconds to compile + .529 seconds to elab + .635 seconds to link + 27.724 seconds in simulation
3:05 iclab5@iclab5:~/Lab13/Exercise/06_P051$
```

9. Power result :



```
# of cell(s) missing both power/leakage table: 0
# of cell(s) missing power table: 0
# of cell(s) missing leakage table: 0
# of RSNV cell(s) missing power_level: 0

Starting Calculating power
2024-May-31 03:08:49 (2024-May-30 19:08:49 GMT)
... Calculating switching power
2024-May-31 03:08:49 (2024-May-30 19:08:49 GMT): 10%
2024-May-31 03:08:49 (2024-May-30 19:08:49 GMT): 20%
2024-May-31 03:08:49 (2024-May-30 19:08:49 GMT): 30%
2024-May-31 03:08:49 (2024-May-30 19:08:49 GMT): 40%
2024-May-31 03:08:49 (2024-May-30 19:08:49 GMT): 50%
... Calculating internal and leakage power
2024-May-31 03:08:49 (2024-May-30 19:08:49 GMT): 60%
2024-May-31 03:08:49 (2024-May-30 19:08:49 GMT): 70%
2024-May-31 03:08:49 (2024-May-30 19:08:49 GMT): 80%
2024-May-31 03:08:49 (2024-May-30 19:08:49 GMT): 90%

Finished Calculating power
2024-May-31 03:08:49 (2024-May-30 19:08:49 GMT)
Ended Power Computation: (cpu=0:00:00, real=0:00:00, mem/process/total/peak)=2535.15MB/5395.96MB/3211.53MB)

Begin Processing User Attributes
Ended Processing User Attributes: (cpu=0:00:00, real=0:00:00, mem/process/total/peak)=2535.15MB/5395.96MB/3211.53MB)

Ended Power Analysis: (cpu=0:01:30, real=0:26:03, mem/process/total/peak)=2535.15MB/5395.96MB/3211.53MB)

Begin Boundary Leakage Calculation
Ended Boundary Leakage Calculation: (cpu=0:00:00, real=0:00:00, mem/process/total/peak)=2535.17MB/5395.96MB/3211.53MB)
Begin Static Power Report Generation
48 instances have no static power

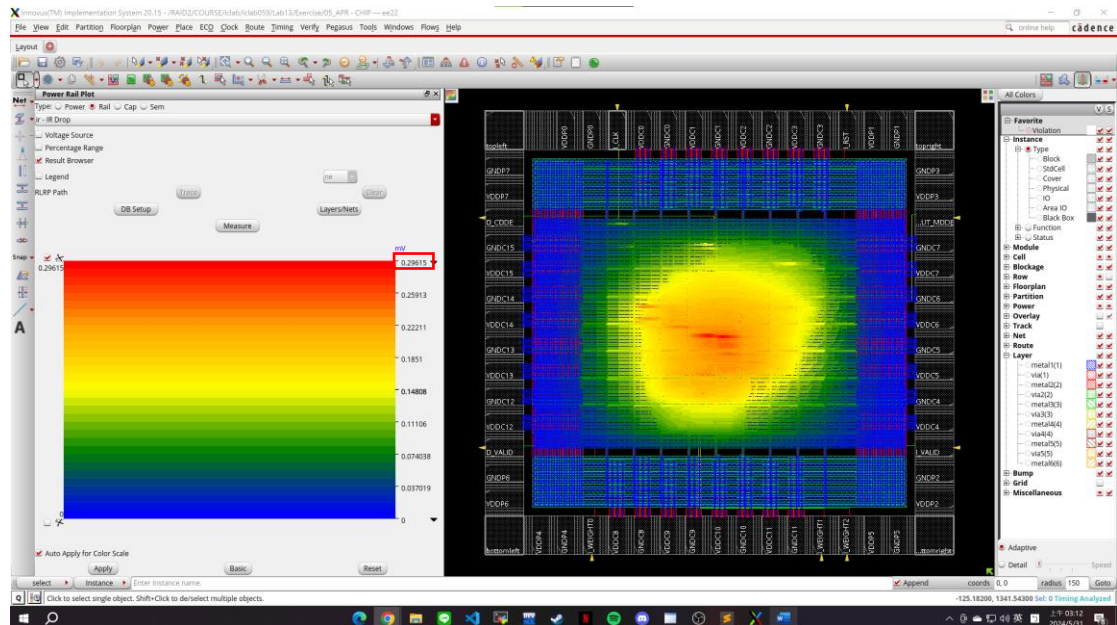
Total Power
-----
Total Internal Power: 1.41943754 46.0716%
Total Switching Power: 1.65257681 53.9429%
Total Leakage Power: 0.00875717 0.2655%
Total Power: 3.08077052

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00, mem/process/total/peak)=2535.17MB/5395.96MB/3211.53MB)

Begin Creating Binary Database
Ended Creating Binary Database: (cpu=0:00:00, real=0:00:00, mem/process/total/peak)=3054.12MB/6160.38MB/3211.53MB)

Output file is power_log/CHP.rpt
```


10. IR Drop Results :



Method to mitigate the IR drop issue:

1. Use several sets of core power pads; I placed four sets on each side, for a total of 16 sets of core power pads.
2. Increase the number of stripes and reduce the spacing between them.