COSC 250 MICROCOMPUTER ORGANIZATION
MIDTERM II

04/14/2021

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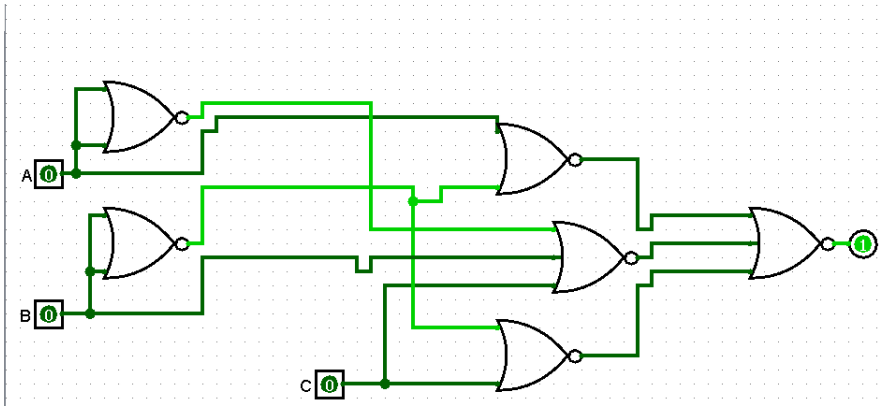
10 questions, 10 points each.
You can use Logisim to draw the circuits, remember you will need to upload one pdf file only!

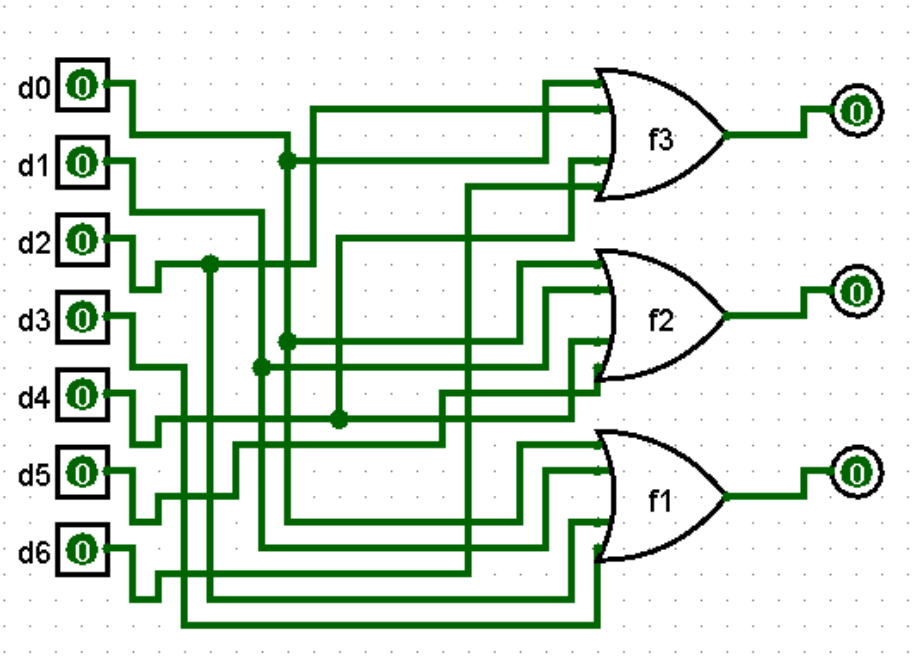
1. Implement the following function only using NOR gates:

$$F = (A'B)'(A'+B+C)(B'+C)$$



2. Describe the operation of an octal to binary Encoder (Include Truth Table and Logic diagram).

OCtal	d0	d1	d2	d3	d4	d5	d6	f1	f2	f3
0	Undefined									
1	0	0	0	0	0	0	1	0	0	1
2	0	0	0	0	0	1	0	0	1	0
3	0	0	0	0	1	0	0	0	1	1
4	0	0	0	1	0	0	0	1	0	0
5	0	0	1	0	0	0	0	1	0	1
6	0	1	0	0	0	0	0	1	1	0
7	1	0	0	0	0	0	0	1	1	1



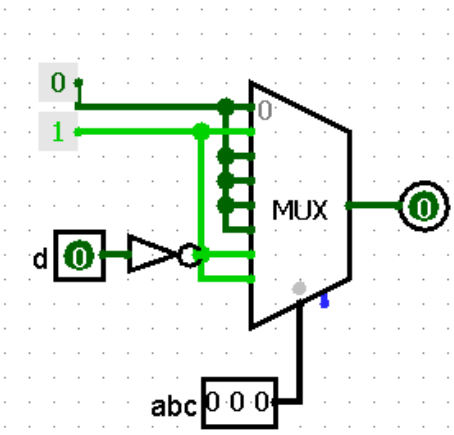
3. A combinational circuit is defined by the following Boolean Function:

$$F = A'B'CD+ABC'D'+ABC+ A'B'CD'+ABCD'$$

a	b	c	d	f	
0	0	0	0	0	0
0	0	0	1	0	
0	0	1	0	1	1
0	0	1	1	1	
0	1	0	0	0	0
0	1	0	1	0	
0	1	1	0	0	0
0	1	1	1	0	
1	0	0	0	0	0
1	0	0	1	0	
1	0	1	0	0	0
1	0	1	1	0	
1	1	0	0	1	d'
1	1	0	1	0	

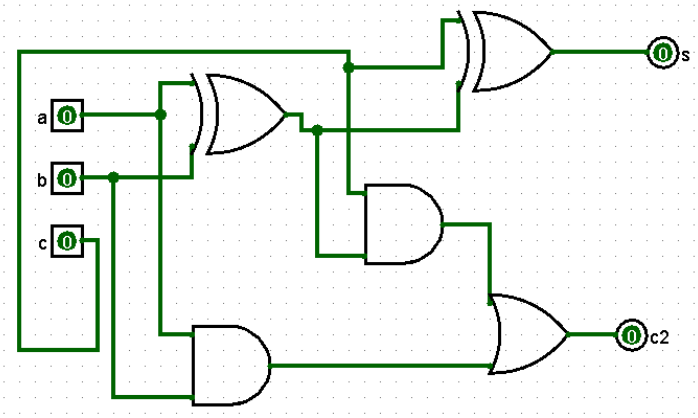
1	1	1	0	1	1
1	1	1	1	1	

Implement it only using a Multiplexer and NOT gates.

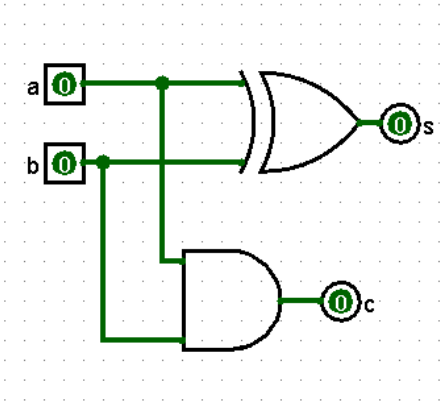


4. Design the Logic Diagram for a 3-bits Ripple Carry Adder using Full-Adders and Half-Adders. Explain the significance of the Carry out from the Most Significant Bit.

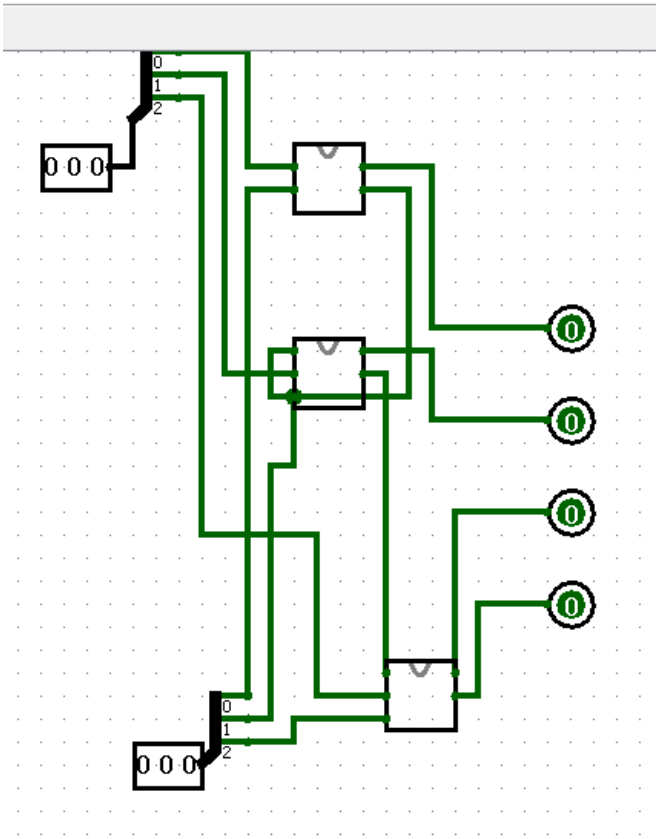
Full Adder



Half Adder

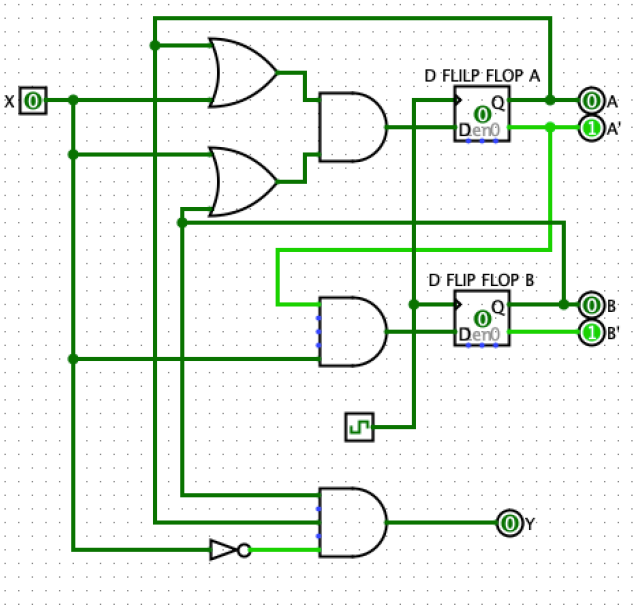


3 bits ripple carry adder

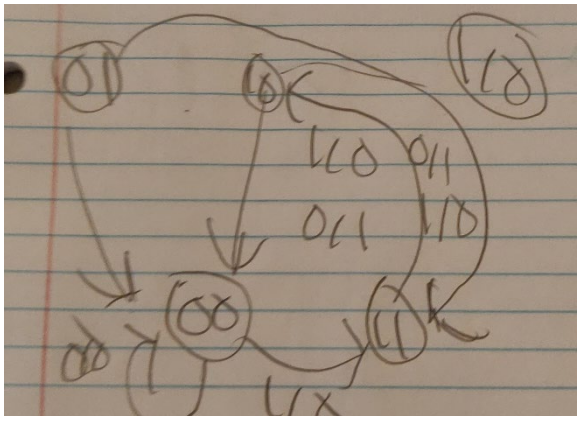


The last /largest bit shows the overflow of the operation

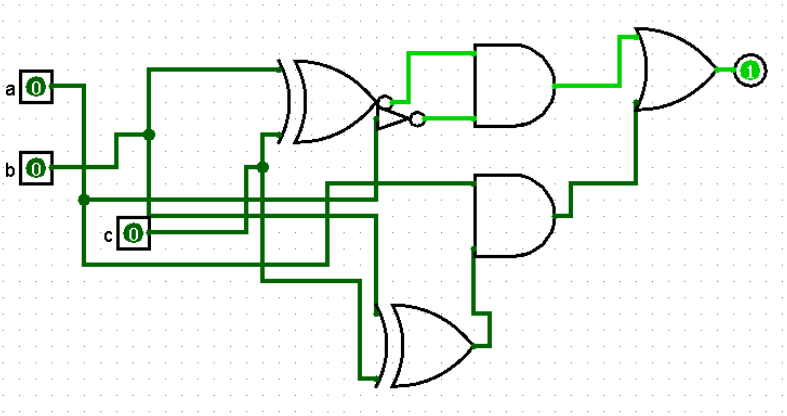
5. Analyze the following sequential circuit by deriving the State Table and the State Diagram



current		X	Next		Y
A	B		A	B	
0	0	0	0	0	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	1	0	0
1	1	1	1	0	0



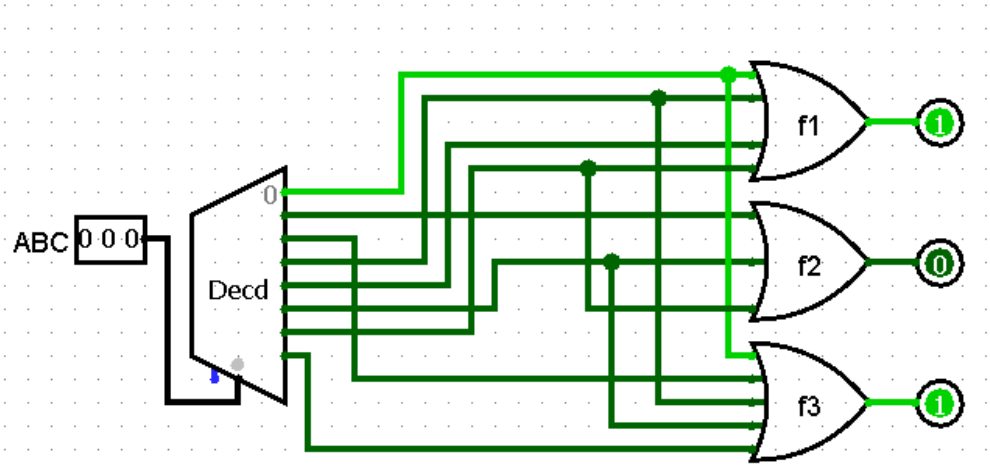
6. Show the implementation of a 3 variable EVEN Function (you can use any form: Basic Gates, NAND config, NOR Config, Decoder, MUX)



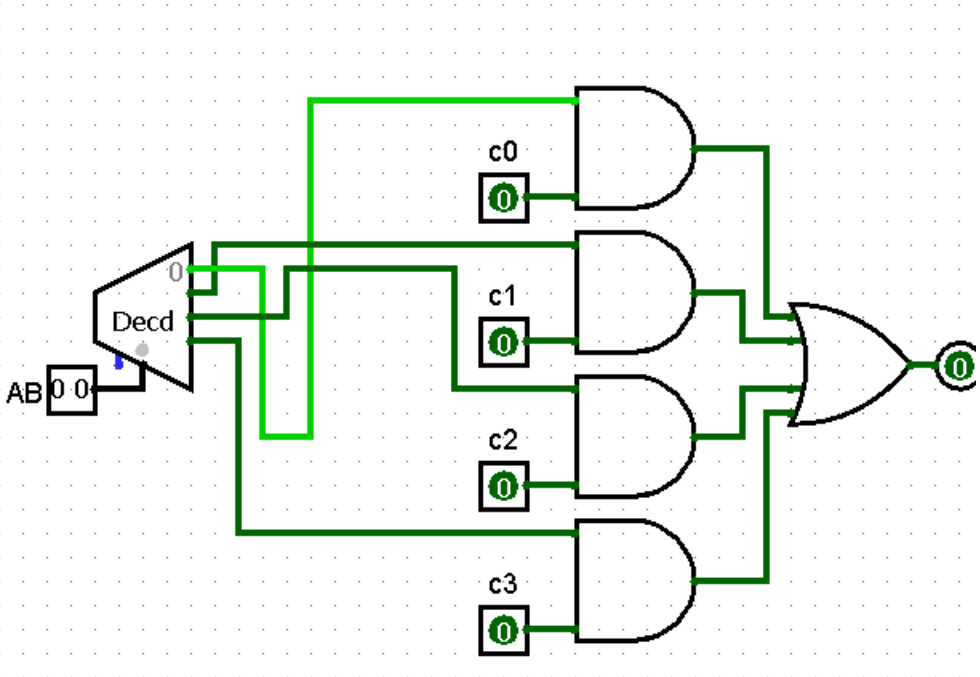
7. A combinational circuit is specified by the following three Boolean functions:

F1= (A,B,C) = m0+m3+m4+m6
F2= (A,B,C) = m1+m5+m6
F3= (A,B,C) = m0+m2+m3+m5+m7

Implement the circuit with a Decoder and external OR gates.



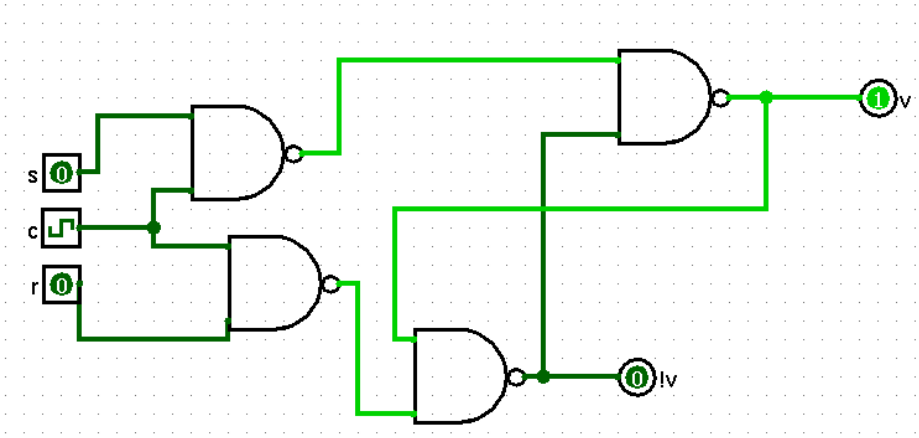
8. Design a 4 to 1 MUX using a 2-4 Decoder and basic gates.



9. Describe the operation of the SR Latch with control input VS the D Latch (show Logic Diagram and Characteristic Table). How the undefined state is eliminates?

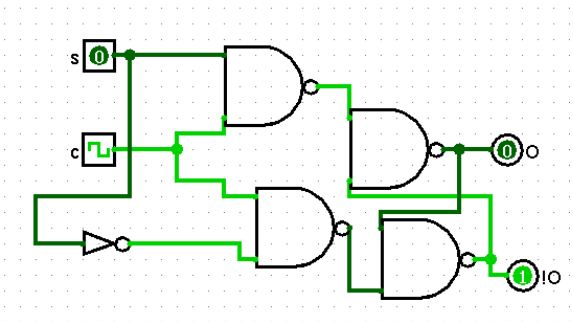
The function of SR latch is that when S and R are both 0 it has a choice to keep the previous state, however if they both become 1 it will be undefined. However, for d latch, unless the clock stops functioning properly it will never keep its previous state, it will only change SR latch so that r will take the reverse of S, this way they will never both be active, this way D latch will never be in the undefined state.

Sr latch w control input



clock	s	r	switch
1	0	0	No switch
1	0	1	v= 0
1	1	0	v = 1
1	1	1	undefined

D latch



clock	d	switch
1	0	Q = 0
1	1	Q = 1

When the clock is 0,neither sr latch w control or d latch change.

10. Briefly describe the Overflow. Which are the conditions when overflow can occur? How can we detect overflow? Show examples to demonstrate your theory.

Overflow is what happens when the computer goes past the significant digit it has. It happens when 2 numbers are being added together. If we are trying to detect overflow, the number after the most significant digit will be read and used to detect the overflow. IF there is a 2 bit adder and we do 10 +10 it is 100 which overflows because of the extra – making it more than 2 bits. AN example of overflow can actually be shown from the 4th e xercise in which the carry digit in the last full adder is being used to detect overflow.