COSC 250 – **STUDY GUIDE FOR MIDTERM II**

MAIN TOPICS:

- NAND/NOR only configuration
- ODD/EVEN Function
- Code converter
- 7 segment Display (DEC/HEX implementation)
- Decoders/Encoders
- MUX/DEMUX
- Adders
- Latches
- Flip Flops

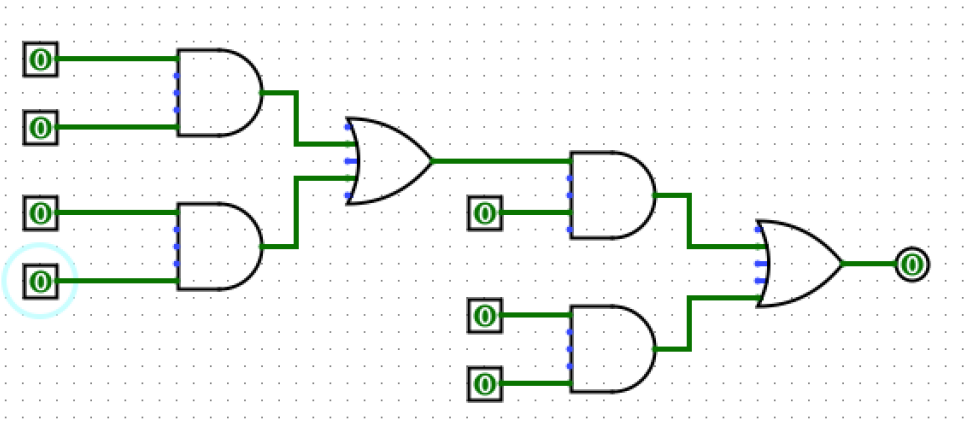
PRACTICE TEST:

1) Implement the following Functions only using NAND gates
   F = A'B'C+ AB'+B'C'+A'C

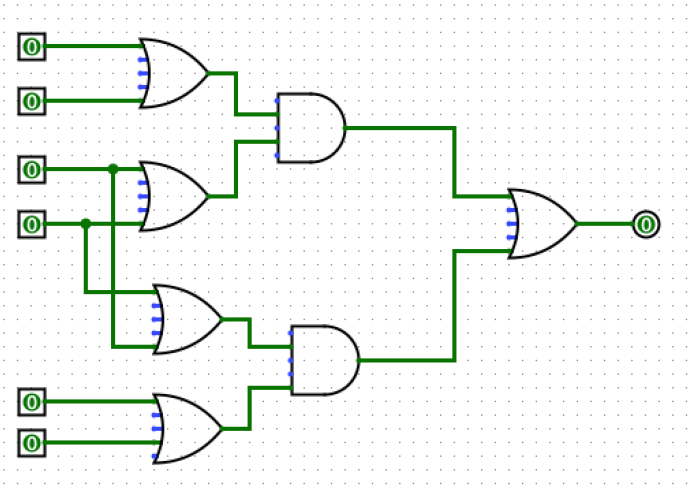
2) Realize Z = (A'+D) (A'+C) (A+B'+C'+D') using four NOR gates

3) Realize Z = ABC + AD +C'D' using only two-input NAND gates. Use as few gates as possible

4) Convert the following circuit to all NAND gates



5) Convert the following circuit to all NOR gates



6) Build a Logic Diagram which represent a 3 input EVEN function. Show all your work (Boolean Function, Truth Table…)

7) Implement a 4 variable ODD function

8) Briefly describe the following:
   - Hardware Description Languages
   - Computer-Aided Design
   - Top-Down Design
   - Hierarchical Design
   - Divide and Conquer approach

9) Design a code converter that converts BCD to code to 2421 code, refere to the following table:

BINARY	2-4-2-1
0000	**0**
0001	**1**
0010	**2**
0011	**3**
0100	**4**
0101	**NOT USED**
0110	**NOT USED**
0111	**NOT USED**
1000	**NOT USED**
1001	**NOT USED**
1010	**NOT USED**
1011	**5**
1100	**6**
1101	**7**
1110	**8**
1111	**9**

10) Derive the truth table for the BCD-to-Seven-Segment Decoder implementation

11) Draw the Logic Diagram and the truth table for a 3 x 8 Decoder

12) A combinational circuit is specified by the following three Boolean functions

$F_1(A,B,C) = \sum m(0,3,4)$

$F_2(A,B,C) = \sum m(1,2,7)$

$F_3(A,B,C) = \prod M(0,1,2,4)$

Implement the circuit with a decoder and external OR gates

13) Design a 4 to 2 line Encoder

14) Describe the operation of a Priority Encoder

15) Design an 8-to-1-line multiplexer using a 3-to-8 line decoder and eight 2 input AND gate and an 8 input OR gate

16) Design an 8-to-1-line multiplexer using two 4-to-1 line multiplexer and one 2-to-one line multiplexer

17) Implement the following Boolean functions with a multiplexer and an inverter with variable D as its input.

a) $F(A,B,C,D) = (\overline{A}+\overline{B}+D)(\overline{A}+\overline{D})(A+B+\overline{D})(A+\overline{B}+C+D)$

b) $F(A,B,C,D) = \sum m(2,4,6,9,10,11,15)$

18) Design a 4-1 Multiplexer using Decoder

19) A combinational circuit is specified by the following Boolean functions:

F1 = A'B'C' + A'B + AB'C' + AB
F2 = A'B'C' + A'B'C + A'BC' + A'BC + AB'C'
F3 = BC + B'C'

Implement the circuit with a decoder and external OR gates

20) A combinational circuit is defined with following Boolean function:

$F = A'B'C + A'C + A'BC' + A'BC + ABC$

Implement it only using a multiplexer and NOT gates.

21) Draw a logic circuit for a 4-to-1 multiplexer using gates

22) Design a 1 bit Full Adder only using NAND gates

23) Draw the general scheme for implementing a 2 bit Adder/Subtractor

24) Explain how to detect overflow using a simple logic circuit

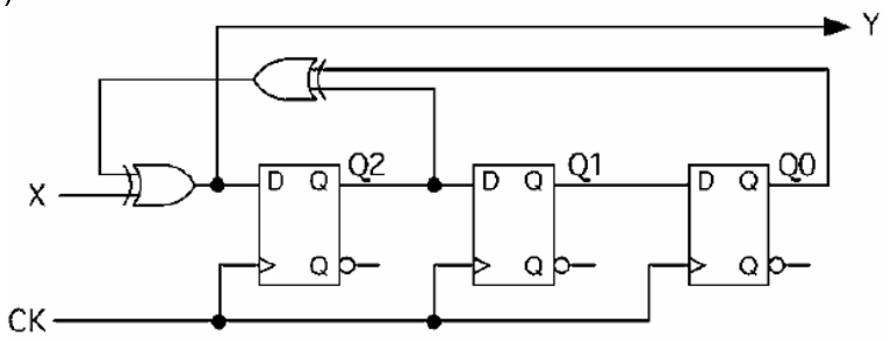
25) Briefly describe:

- Carry Lookahead Adder
- Ripple carry Adder

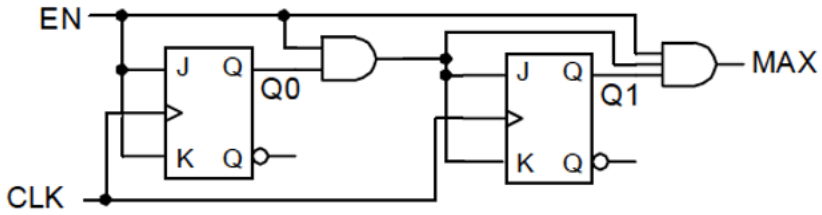
26) Implement the circuit and describe all the different latches we studied in class

27) Analyze the following sequential circuit by deriving the State Table and the State Diagram:

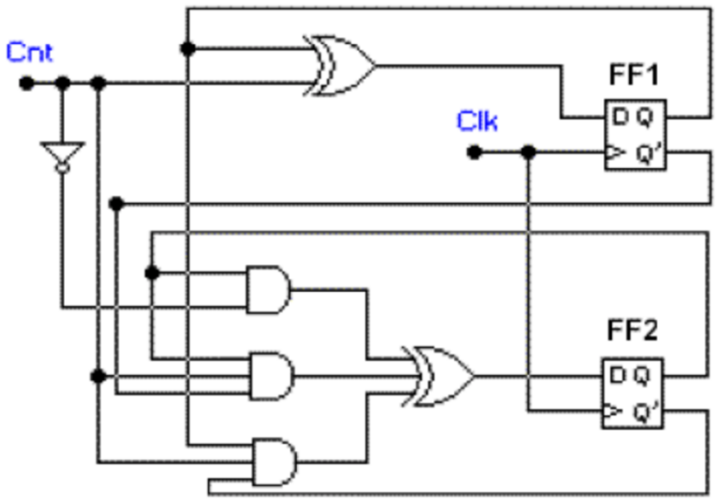
a)



b)



c)



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