FinFET – 14 nm Process Flow

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***Abstract*—The 14 nm process flow for a FinFET details the steps needed to fabricate a FinFET at the 14 nm node. Conventor SEMulator3D is used to illustrate the process flow.**

***Index Terms*—14nm, FinFET, process, flow, fabrication, Conventor, SEMulator3D**

I. Introduction

Various process flows are used by the electronics industry to fabricate transistors. One of the available nodes for manufacturing FinFET transistors is the 14 nm process node. This process will be outlined and explained. Renders from Conventor's SEMulator3D software will be used to illustrate various steps from the process flow.

The four main steps in 14 nm FinFET manufacturing are wafer setup, front-end-of-line (FEOL), middle-of-line (MOL), and extract devices according to Conventor's SEMulator3D. Wafer setup is where the manufacture gets the silicon ready, FEOL makes the FinFET, MOL connects to the FinFET, and extract devices is where the tool slices out the FinFET from the render.

II. Wafer Setup

III. Front-End-of-Line

a) LTH Mand: After low-temperature hydrogenation [1], the resist layer will be etched and expose the SiARC underneath. This results in the stack from Fig. 1. TODO: Explain what we use this for.

b) RIE Mand: Reactive ion etching (RIE) [2] is used to cut the SiARC layer, exposing the ODL underneath.

IV. Middle-of-Line

Explanation on MOL.

V. Extract Devices

Explanation on extracting devices.

VI. Conclusion

Lots of things happen in the 14 nm process flow.

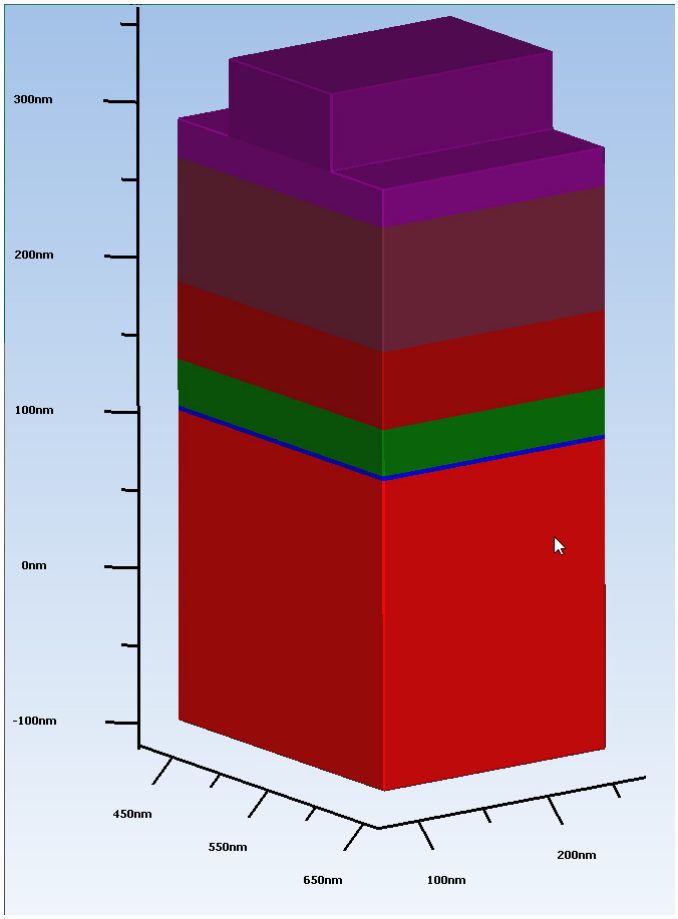

Fig. 1. The silicon stack after LTH Mand.

REFERENCES

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