



VIT[®]

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

EEE 1001 BASIC ELECTRICAL AND ELECTRONICS ENGINEERING LABORATORY MANUAL AY (FALL 20-21)

SCHOOL OF ELECTRICAL ENGINEERING
VELLORE INSTITUTE OF TECHNOLOGY
Chennai

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INDEX

S.No	Date	Experiment Title	Marks
1	27-10-2020	Thevenins & Maximum Power Transfer Theorem	
2	03-11-2020	PN Junction	
3	10-11-2020	Voltage Regulator using Zener Diode	
4	17-11-2020	Sinusoidal steady state response of RLC circuit	
5	01-12-2020	Verification of Truth Tables for Logic Gates	
6	15-12-2020	Design of Arithmetic logic Circuit using IC's - Half Adder	
7	15-12-2020	Design of Arithmetic logic Circuit using IC's - Full Adder	
8	22-12-2020	Full Wave Rectifier with or without Filter	
9	29-12-2020	Characteristics of MOSFET	
10	29-12-2020	Power Factor Improvement in Single Phase AC System	

Thevenins and Maximum power transfer theorem

(*Loud Speaker Application*)

EXP 1 -

Aim:

To design a simplified equivalent circuit in analyzing the power systems and other circuits where the load resistor is subject to change in order to determine the voltage across it and current through it using Thevenin's theorem. To design the circuit for maximizing, the power transferred from the amplifier to the loudspeaker using maximum power transfer theorem.

Software required:

LTspice software

A. Thevenin's Theorem

Theory & Circuit Diagram

Any two-terminal linear network composed of voltage sources, current sources, and resistors, can be replaced by an equivalent two-terminal network consisting of an independent voltage source in series with a resistor as shown in Fig. 1. The value of voltage source is equivalent to the open circuit voltage (V_{th}) across two terminals of the network and the resistance is equal to the equivalent resistance (R_{th}) measured between the terminals with all energy sources replaced by their internal resistances.

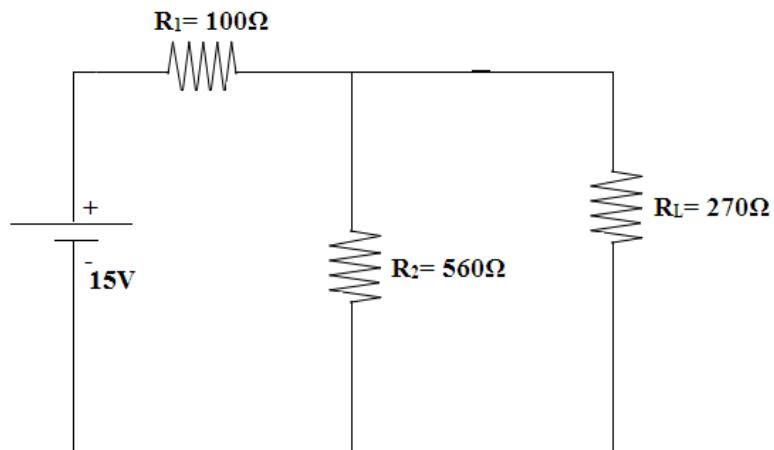
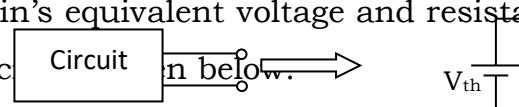
Formulae:

$$I_L = \frac{V_{Th}}{R_{Th} + R_L}$$

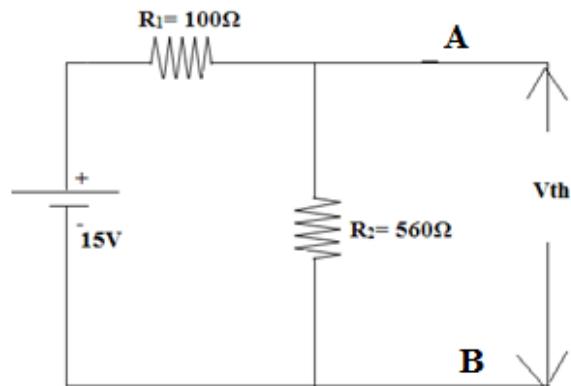
$$V_L = R_L I_L = \frac{R_L}{R_{Th} + R_L} V_{Th}$$

Theoretical Solution:

Find the thevenin's equivalent voltage and resistance considering R_L is the load terminal in the circuit below.

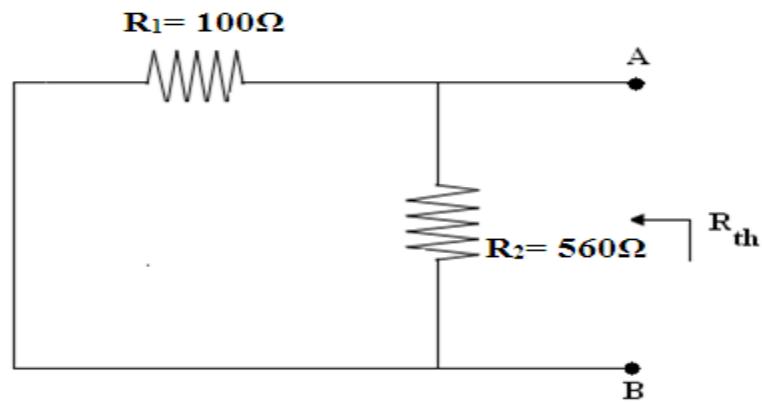


Circuit Diagram for the determination of Thevenin's Voltage, V_{th}



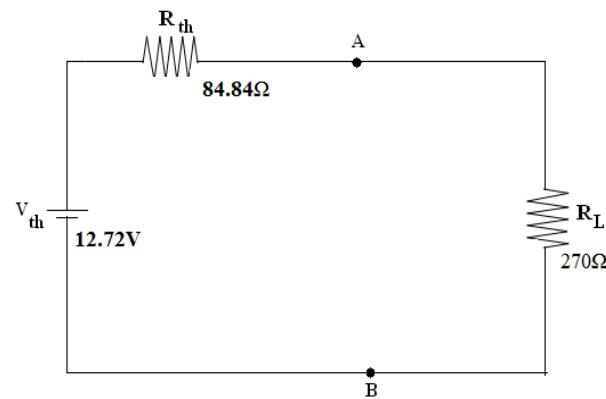
$$V_{th} = V_{AB} = \frac{15 \times 560}{100 + 560} = 12.72V \text{ (From Voltage division rule)}$$

Circuit Diagram for the determination of Thevenin's Resistance, R_{th}



$$R_{th} = \frac{100 \times 560}{100 + 560} = 84.84\Omega$$

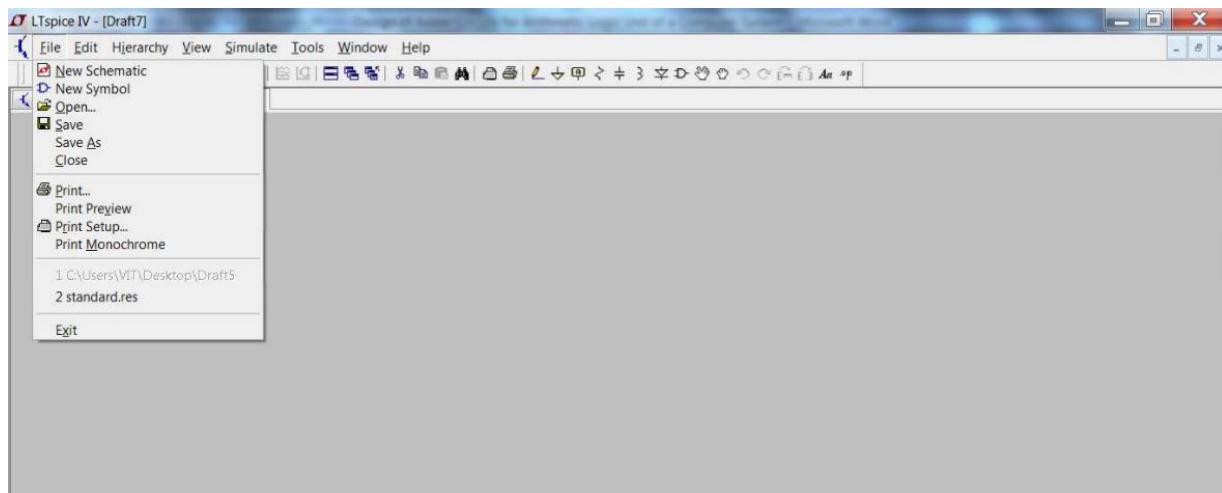
Circuit Diagram of Thevenin's equivalent Circuit



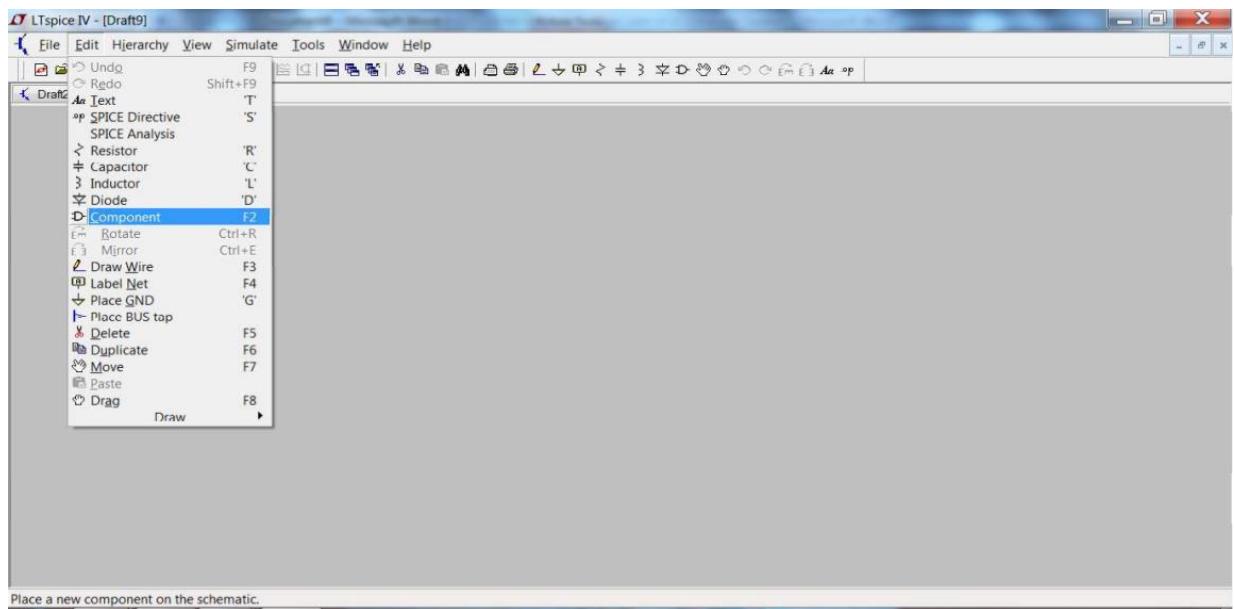
Verification by Simulation:

Procedure

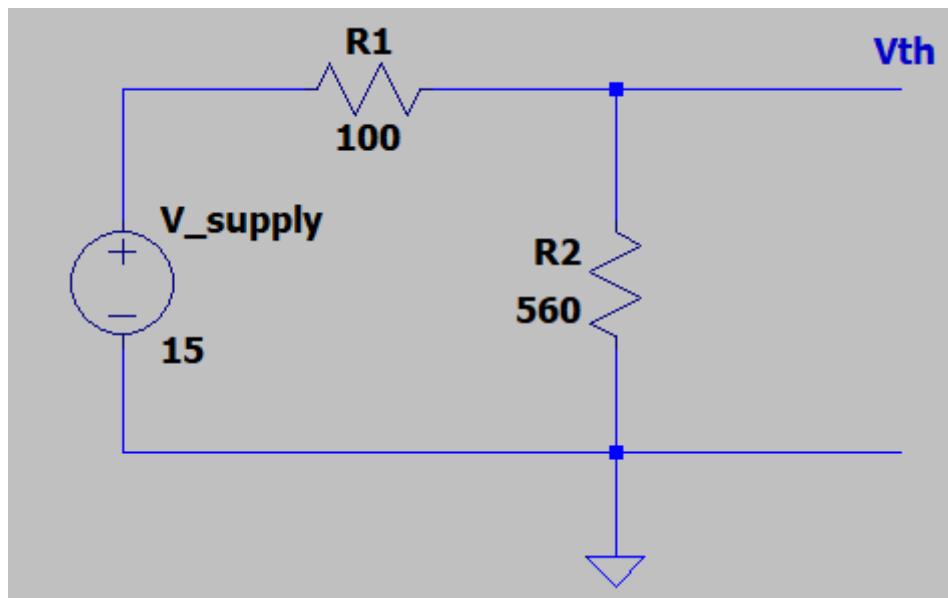
1. Open LTspice. Go to File New Schematic.

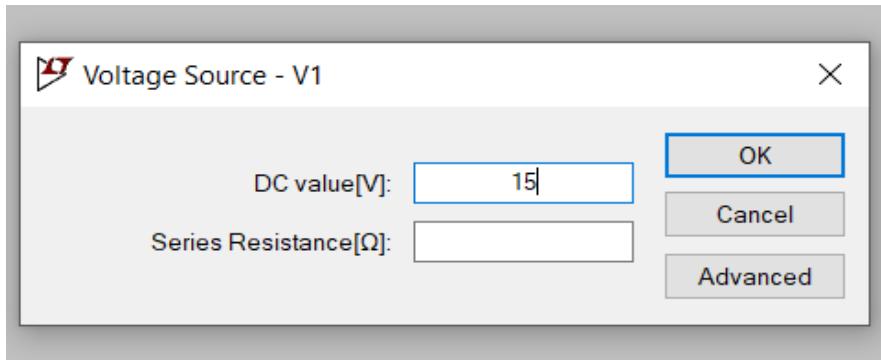


2. On the File Menu, click on Edit Component.

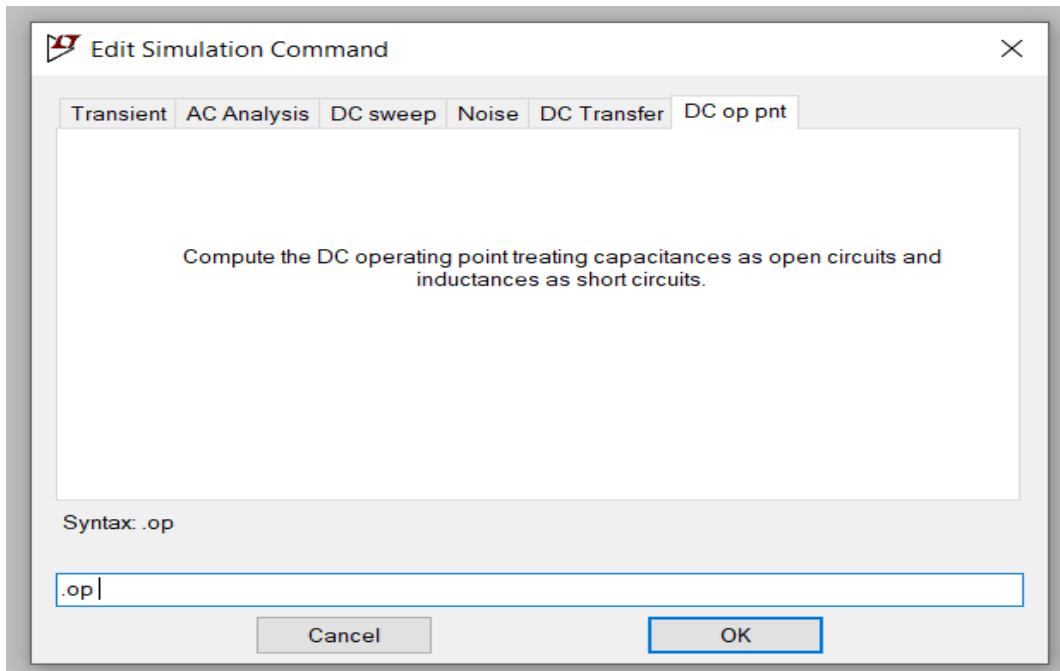


3. Determination of Thevenin's Voltage, V_{th} : Design a circuit using LTSPICE as per the circuit diagram shown in the fig. Note down the voltage using voltage probe. Enter the value of DC as shown in the fig Voltage source $_V1$.





Note down the value from the DC opt point, Go to Simulate →Edit simulation cmd, set the DC op pnt.

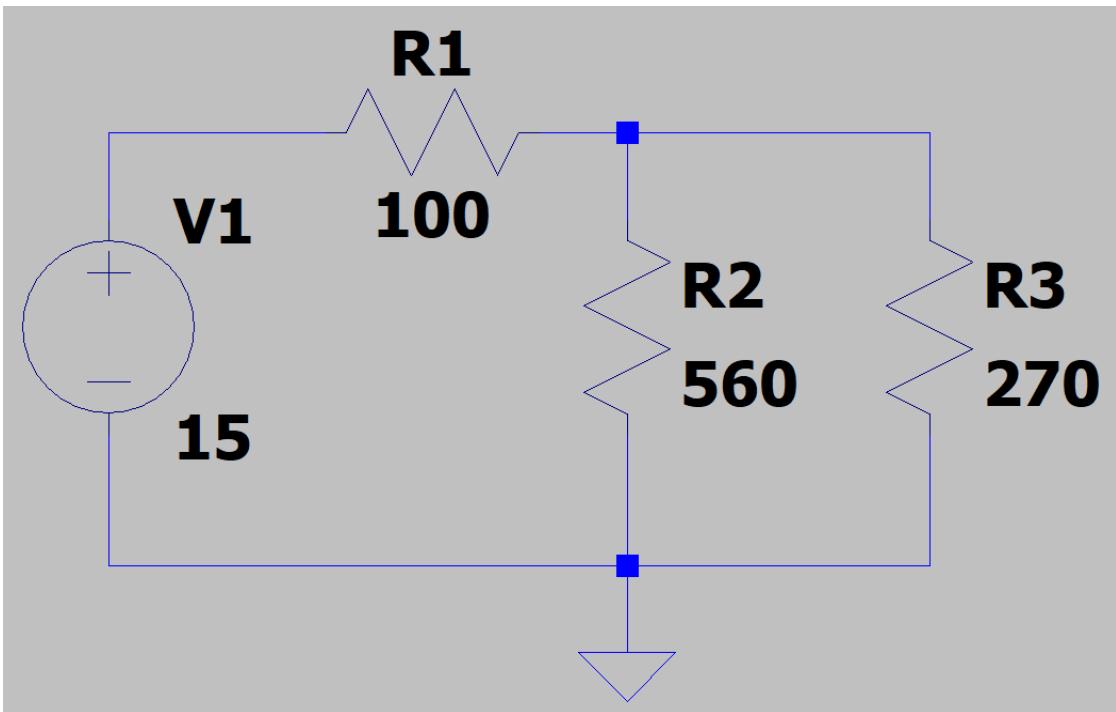


Observe the value of open circuit voltage ($V_{th} \rightarrow V_{n002}$) from the obtained output window below

```
* C:\Program Files\LTspiceXVII\Draft1.asc
--- Operating Point ---
V(n001) :      15      voltage
V(n002) :  12.7273  voltage
I(R2) :  0.0227273  device_current
I(R1) : -0.0227273  device_current
I(V1) : -0.0227273  device_current
```

4. Determination of Load Current I_L :

Make the connections as per the circuit diagram shown in below fig. Note down the current value from the output window.



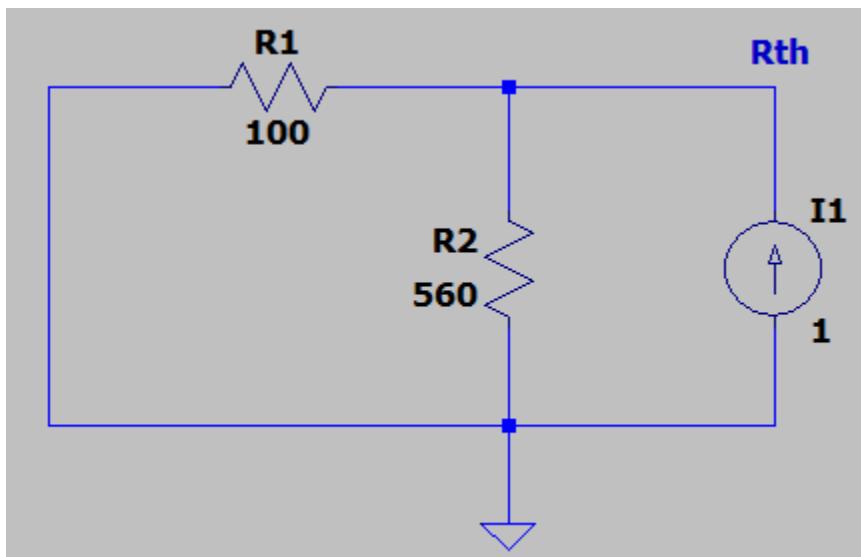
```
LT * C:\Program Files\LTC\LTspiceXVII\Draft1.asc
```

```
--- Operating Point ---
```

```
V(n001) : 15 voltage
V(n002) : 9.68403 voltage
I(R3) : 0.0358668 device_current
I(R2) : 0.0172929 device_current
I(R1) : -0.0531597 device_current
I(V1) : -0.0531597 device_current
```

5. Determination of Thevenin's Resistance, R_{th} :

Make the connections as per the circuit diagram shown in below fig. Determine the Resistance value seen from the open terminals. Add 1A current source in the circuit and obtain the R_{th} value from $V_{th}V(n001) \times I_L I(I1)$ from the output window.

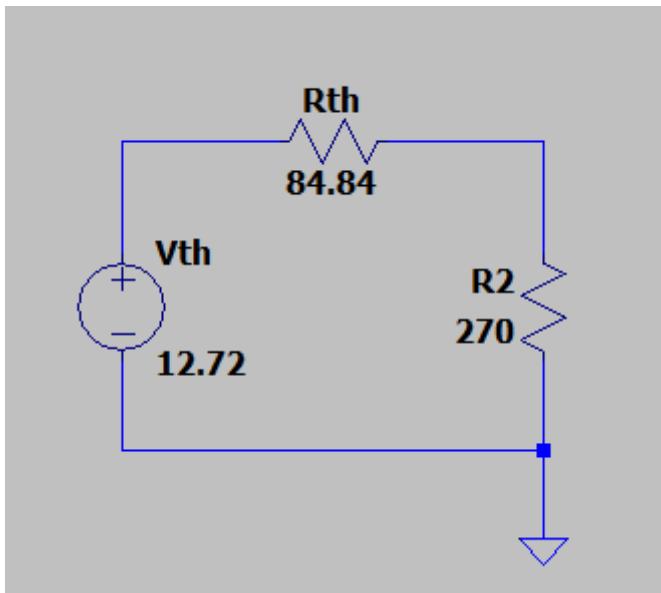


* C:\Program Files\LTC\LTspiceXVII\Draft1.asc

--- Operating Point ---

V(n001) :	84.8485	voltage
I(I1) :	1	device_current
I(R2) :	0.151515	device_current
I(R1) :	0.848485	device_current

6. Make the connections as per the circuit diagram. Determine the current across the Load Resistor. Obtain the value of current from the output window.



 * C:\Program Files\LTC\LTspiceXVII\Draft1.asc

--- Operating Point ---

```
V(n001) : 12.72 voltage
V(n002) : 9.67873 voltage
I(R2) : 0.0358471 device_current
I(R1) : -0.0358471 device_current
I(V1) : -0.0358471 device_current
```

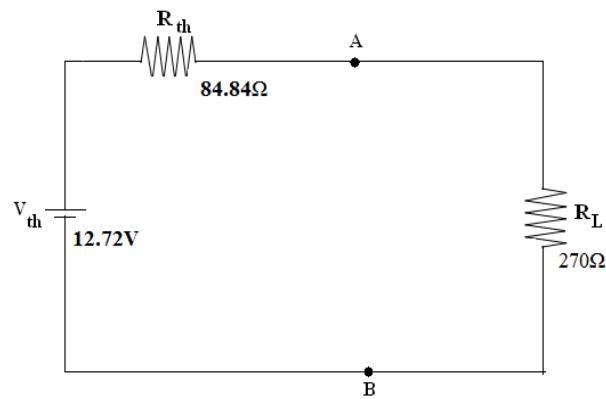
Observation Table:

S. No	V _s (V)	V _{TH} (V)	(R _{th}) (Ω)	Current through Load Resistance I _L (mA)			
				Practical Value	Theoretical Value		
1	15	12.72	84.84	Main circuit	0.0358668	Main circuit	0.0358471
2	15	12.7273	84.8485	Thevenin's circuit	0.0358669	Thevenin's circuit	0.0358669

B. Maximum Power Transfer Theorem

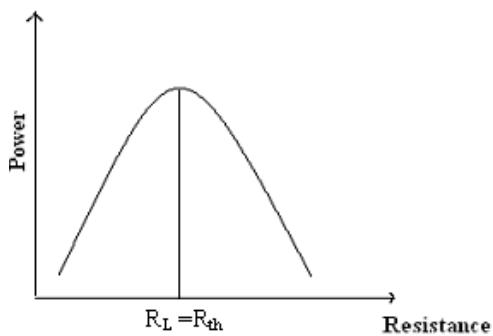
Theory & Circuit Diagram

The maximum power transfer theorem states that maximum power is delivered from a source to a load when the load resistance is equal to source resistance



For finding the Thevenin equivalent circuit steps 1 to 6 is followed. Then as per the maximum power transfer theorem, maximum power will be delivered to the load when the load resistance is equal to the internal or Thevenin's resistance of the network.

Model Graph:



Condition for maximum power transfer:

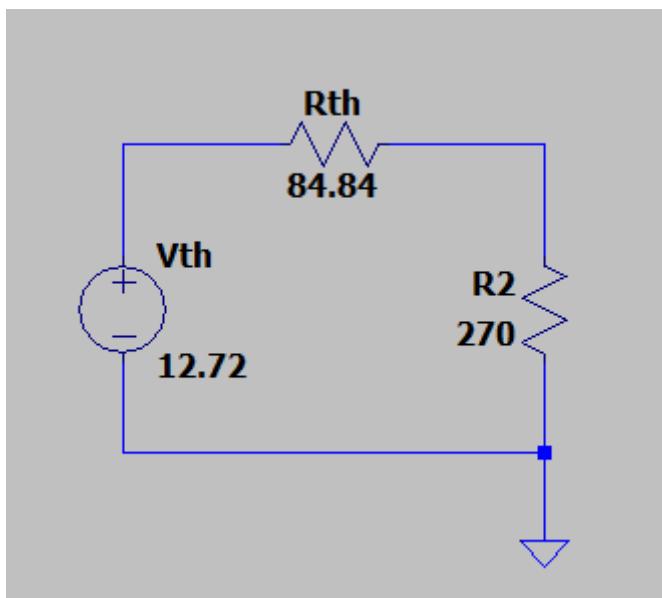
$$R_L = R_{Th}$$

Maximum power transferred:

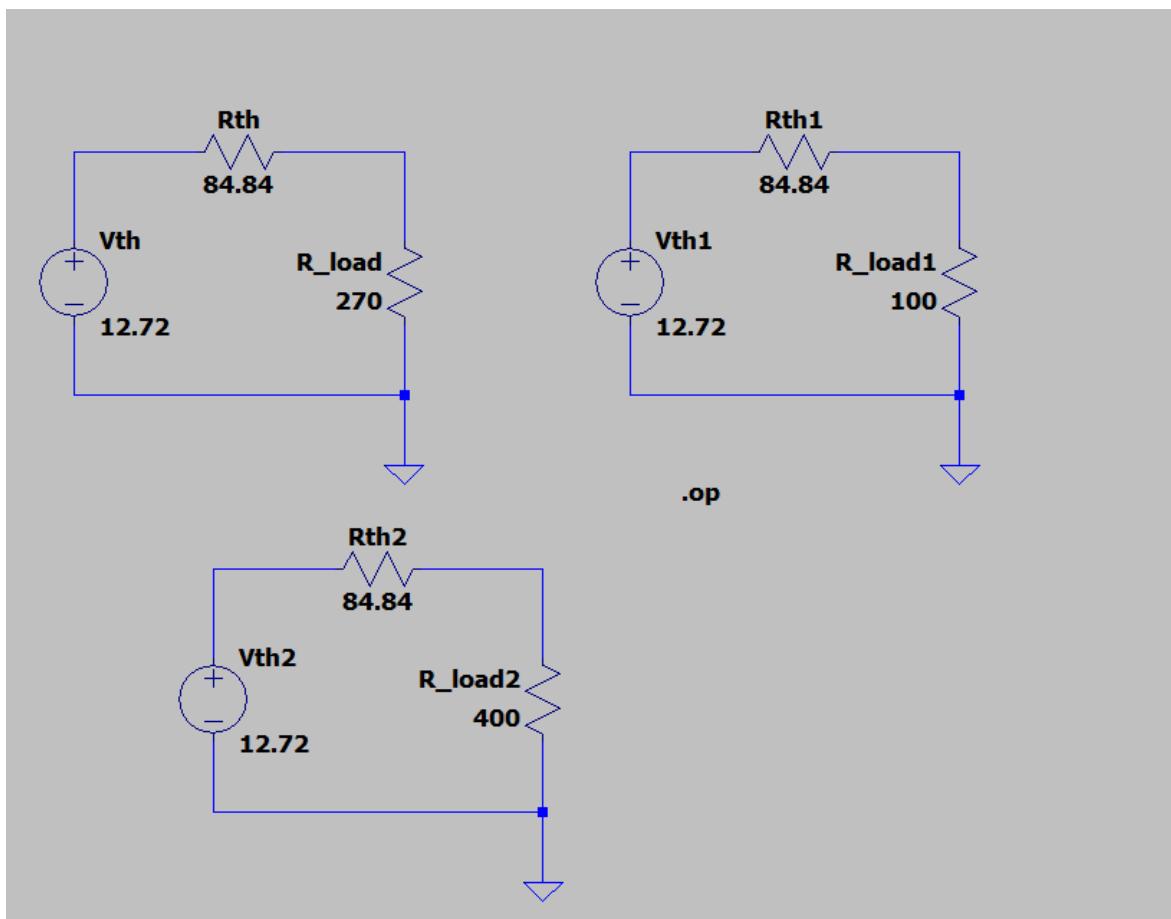
$$P_{max} = \frac{V_{Th}^2}{4R_{Th}}$$

Procedure:

1. Take the Thevenin's Equivalent circuit from the previous experiment.



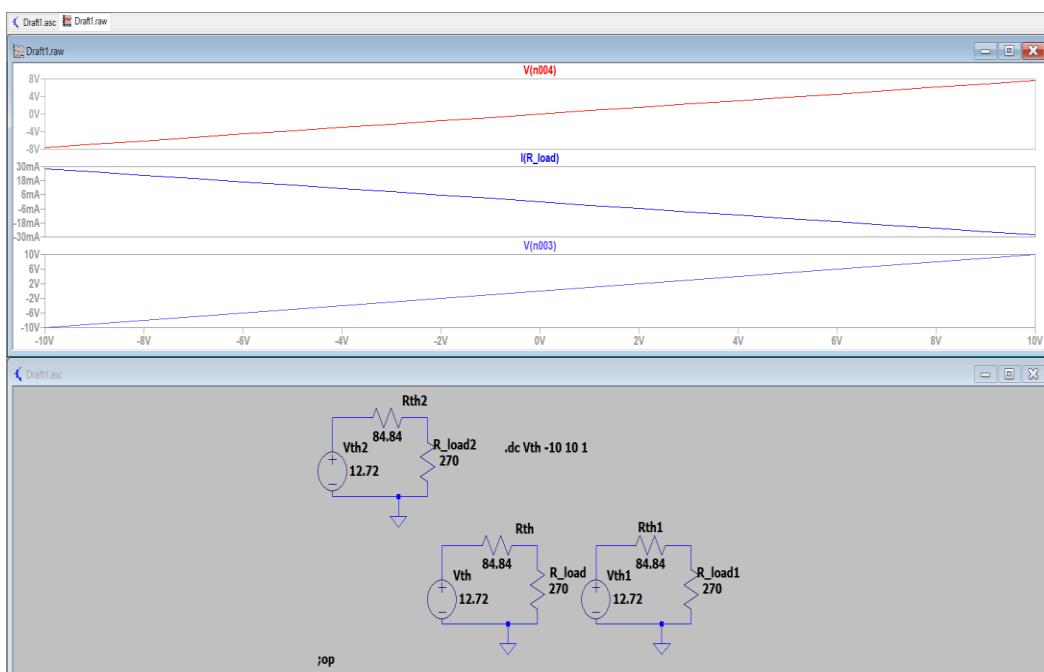
2. Take three values for the load resistance. One equal to R_{th} , one greater and one smaller. Click on edit simulate command under simulate section then select DC op pnt. Run the simulation by clicking on the run command and obtain the output.



* C:\Program Files\LTC\LTspiceXVII\Draft1.asc

--- Operating Point ---

```
V(n003) : 12.72      voltage
V(n004) : 9.67873    voltage
V(n005) : 12.72      voltage
V(n006) : 9.67873    voltage
V(n001) : 12.72      voltage
V(n002) : 9.67873    voltage
I(R_load2) : -0.0358471 device_current
I(Rth2) : -0.0358471 device_current
I(Rth1) : -0.0358471 device_current
I(R_load1) : -0.0358471 device_current
I(R_load) : -0.0358471 device_current
I(Rth) : -0.0358471 device_current
I(Vth2) : -0.0358471 device_current
I(Vth1) : -0.0358471 device_current
I(Vth) : -0.0358471 device_current
```



Observation Table :

S.No.	$R_L (\Omega)$	$R_{TH} (\Omega)$	$I_L(mA)$	$P_L=I_L^2 R_L(mW)$
1	100	84.84	0.0688163	0.473568315
2	270	84.84	0.0358471	0.346953936
3	350	84.84	0.0292521	0.299489874
4	560	84.84	0.0197258	0.217900024



Result & Inferences:

Thus the Thevenin's and Maximum power transfer theorem have been verified in the given circuit.

Practical Applications:**Impedance Matching Transformers**

In cases requiring impedance matching, impedance matching transformers come into play.

Impedance matching transformers are designed to provide maximum power transfer from source to load, altering circuit impedances to allow for necessary matching. By applying an appropriate turns ratio to the ratio of load impedance to output impedance, these devices translate resistance on one side of the circuit into the required value on the other side.

Course Outcomes:

- CO1.** Solve basic electrical circuit problems using various laws and theorems
CO6. Design and conduct experiments to analyze and interpret data

Student Learning Outcomes (SLO):

- SLO9.** Having problem solving ability- solving social issues and engineering problems

Study of the characteristics of PN junction

Diode

(Rectifier Application)

EXP 2 -

Aim:

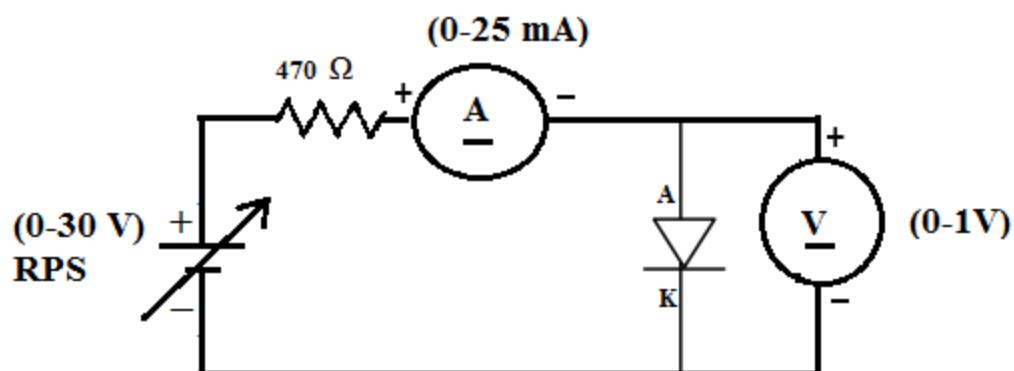
To study the VI characteristics of PN junction.

Software Required:

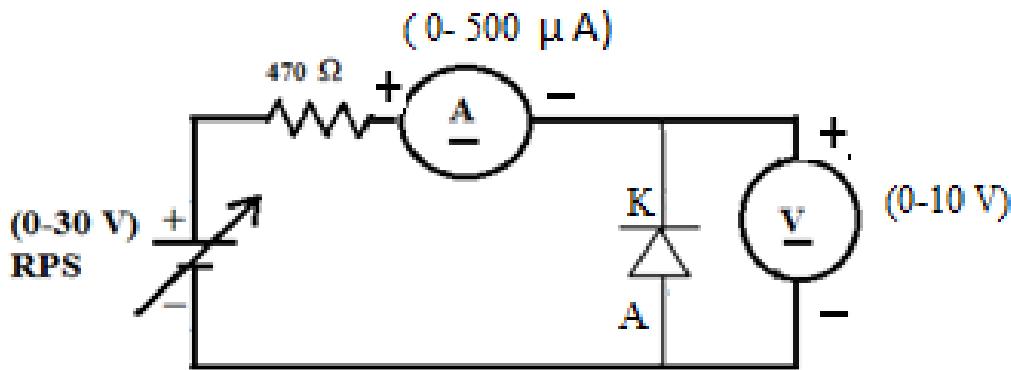
LTS spice Software

Circuit Diagram:

The Forward Bias of PN junction diode:



The Reverse Bias of PN junction diode:



Theory:

PN junction diode:

A PN junction is a piece of semiconductor material in which part of the material is p-type and part is n-type. When a junction is formed between p-type and n-type semiconductor materials, the resulting device is called a semiconductor diode. This component offers extremely low resistance to current flowing in one direction and extremely high resistance to current flowing in the other. Various types of diodes are available for different applications. These include rectifier diodes for use in power supplies, Zener diodes for use as voltage reference sources, light-emitting diodes, etc. The connection to the p-type material is referred to as the anode while that to the n-type material is called the cathode. The circuit symbol of the PN junction diode is shown in Figure 1.



Figure 1. The circuit symbol of PN junction diode

PN junction diode in forward bias:

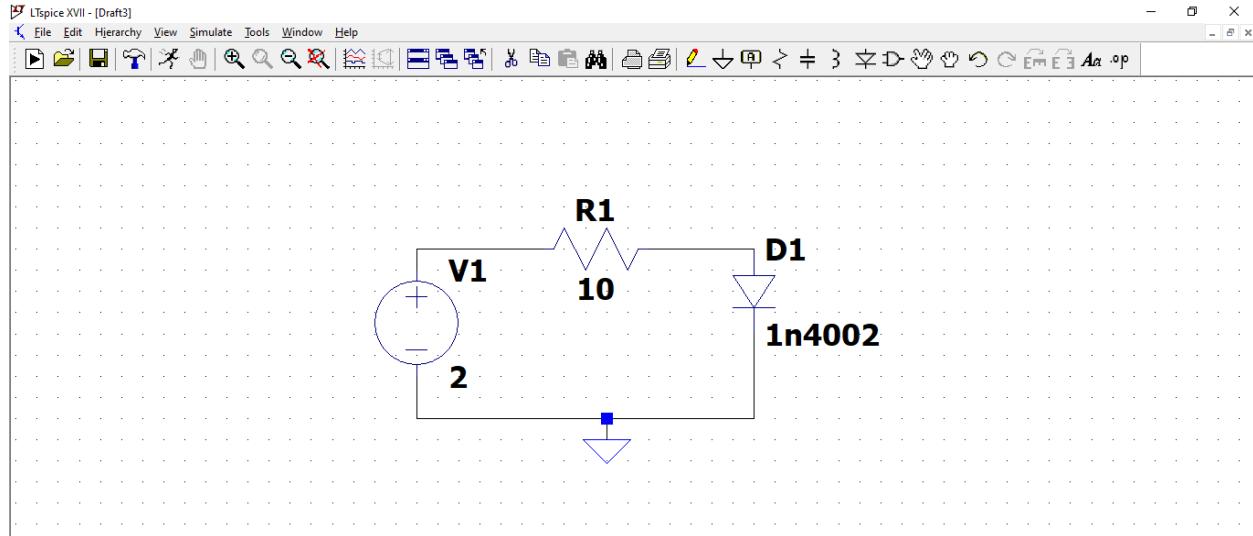
When an external voltage is applied to a p-n junction making the p-type material positive with respect to the n-type material, the p-n junction is forward biased. The applied voltage opposes the contact potential, and, in effect, closes the depletion layer. Holes and electrons can now cross the junction and current flows. An increase in the applied voltage above that required to narrow the depletion layer (about 0.3 V for germanium and 0.7 V for silicon), results in a rapid rise in the current flow. The voltage at which the diode starts conducting is called knee voltage or threshold voltage or barrier cut-in voltage. The applied voltage should not be increased beyond a certain safe limit; otherwise, the diode is likely to burn out.

PN junction diode in reverse bias:

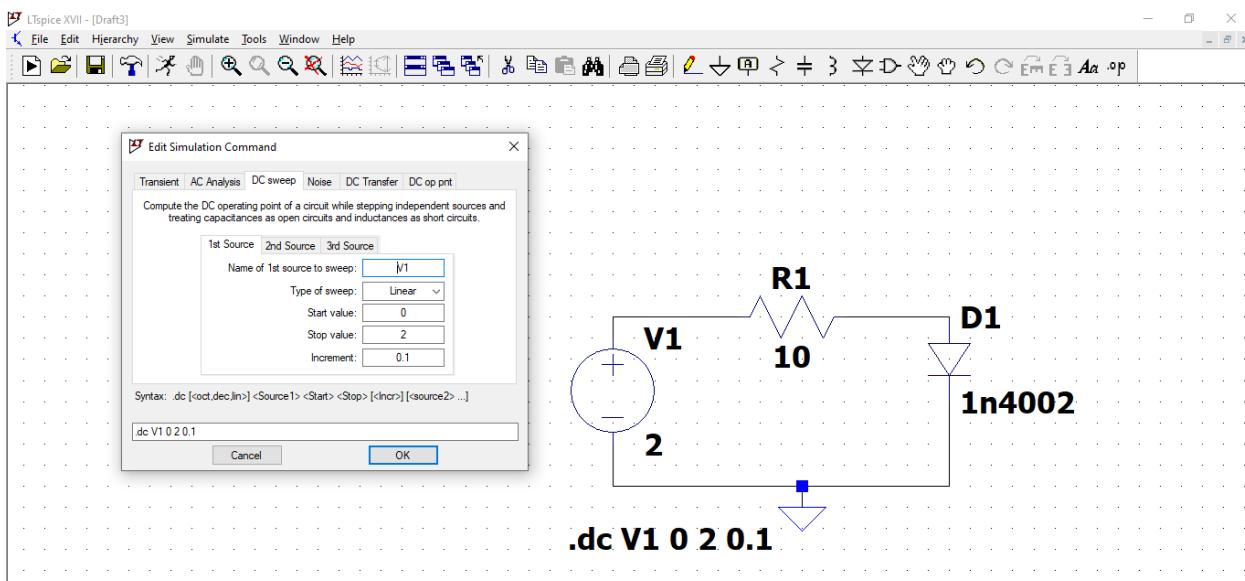
When an external voltage is applied to a p-n junction making the p-type material negative with respect to n-type material, the p-n junction is reverse biased. The applied voltage is now in the same sense as the contact potential and opposes the movement of holes and electrons due to the opening up of the depletion layer. Thus, in theory, no current flows. However, at normal room temperature, certain electrons in the covalent bond lattice acquire sufficient energy from the heat available to leave the lattice, generating mobile electrons and holes. This process is called electron-hole generation by thermal excitation. The electrons in the p-type material and holes in the n-type material caused by thermal excitation are called minority carriers and these will be attracted by the applied voltage. Thus, in practice, a small current of a few microamperes for germanium and less than one microampere for silicon, at normal room temperature, flows under reverse bias conditions.

Procedure:

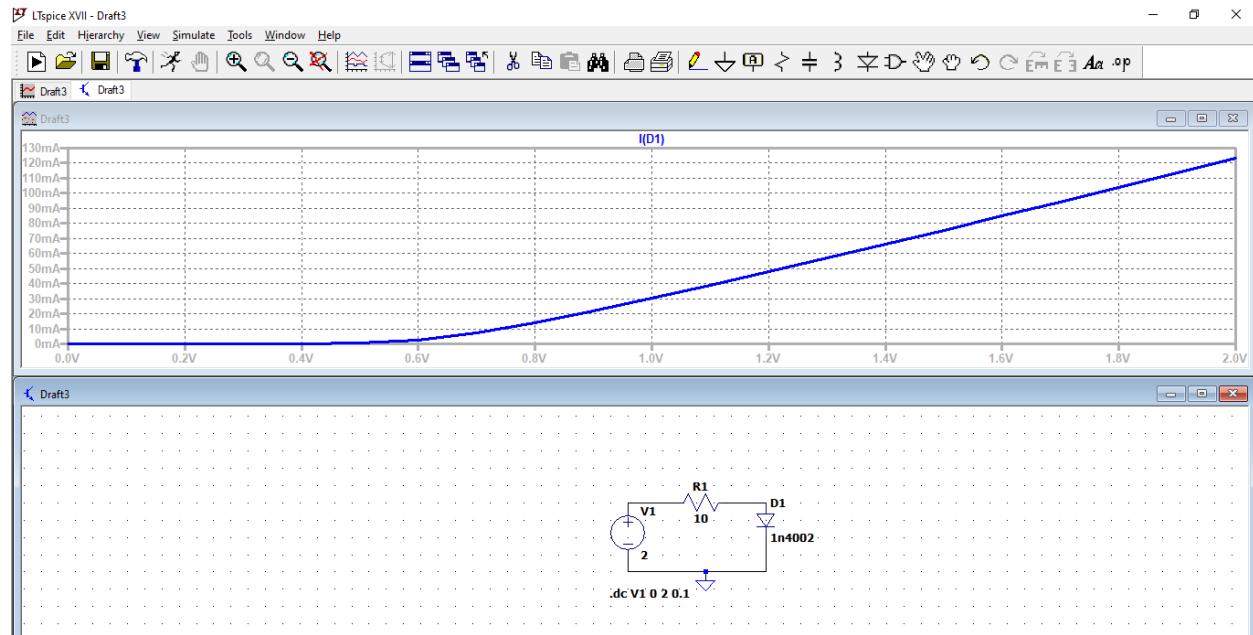
LT Spice Circuit for PN Junction Diode during Forward Biased Condition



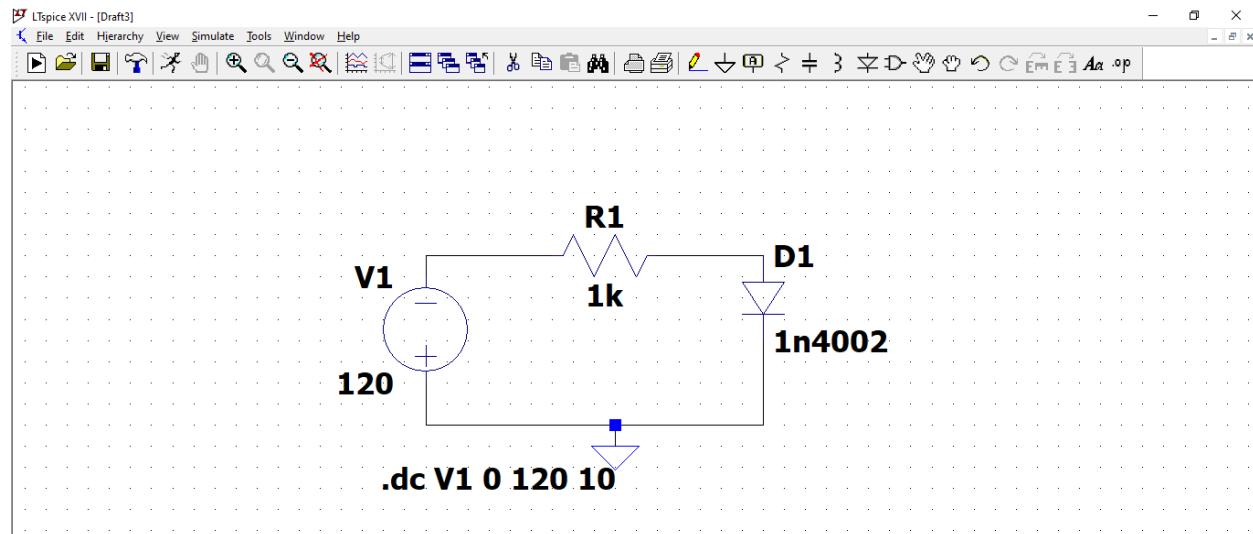
Go to -> RUN --> DC Sweep (Put the values as mentioned)



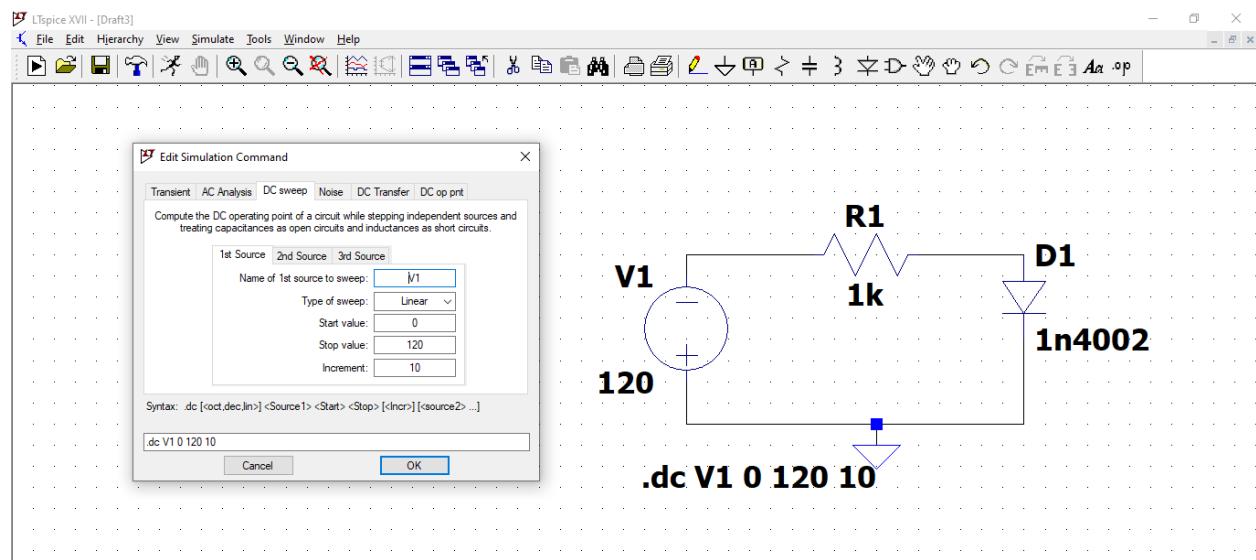
Place the Ammeter to the measure the diode current by clicking on to the diode



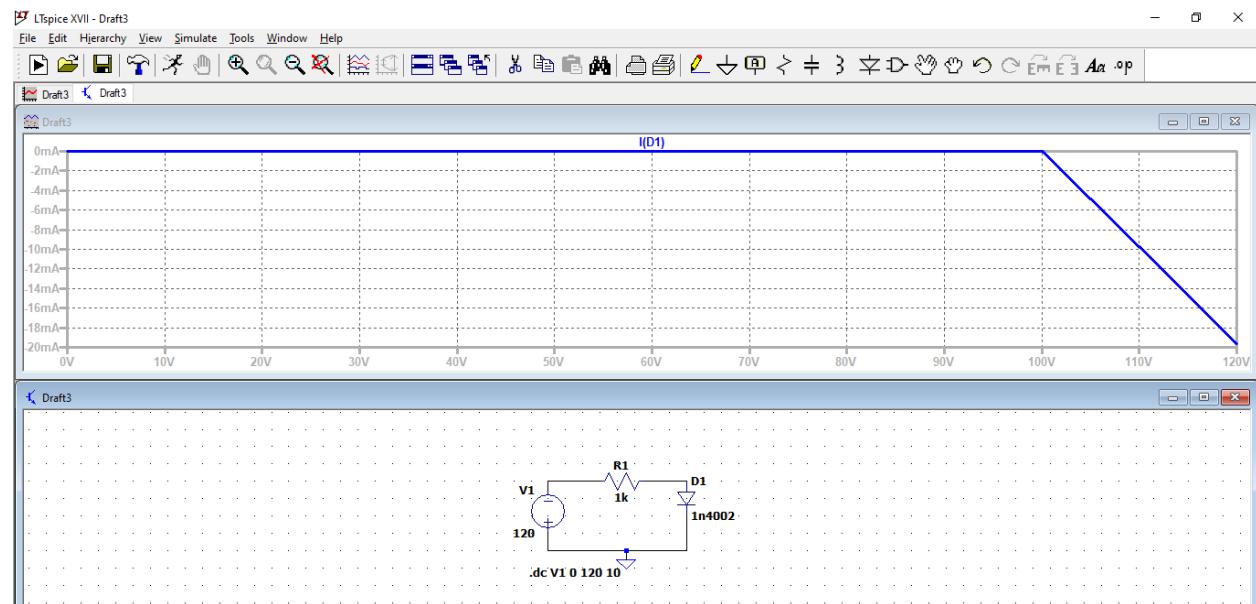
LT Spice Circuit for PN Junction Diode during Reversed Biased Condition

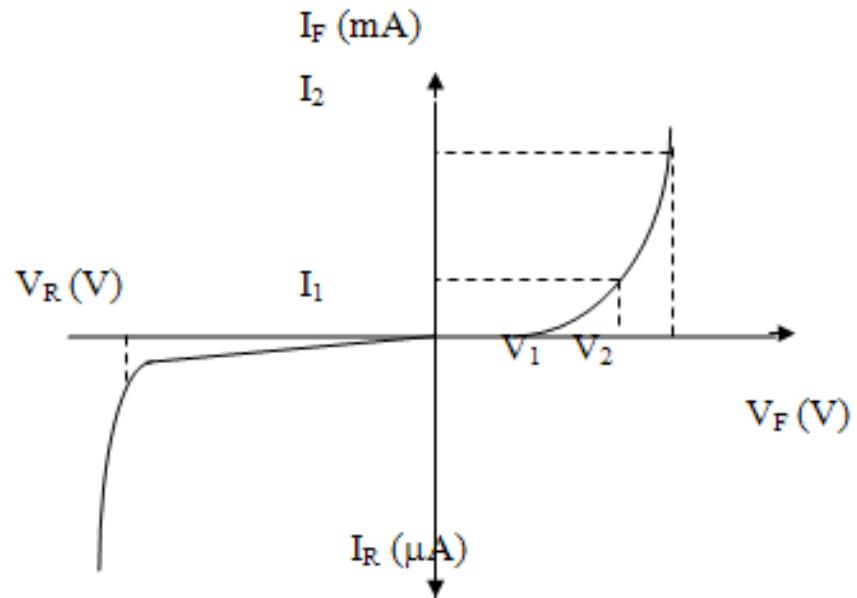


Go to -> RUN --> DC Sweep (Put the values as mentioned)

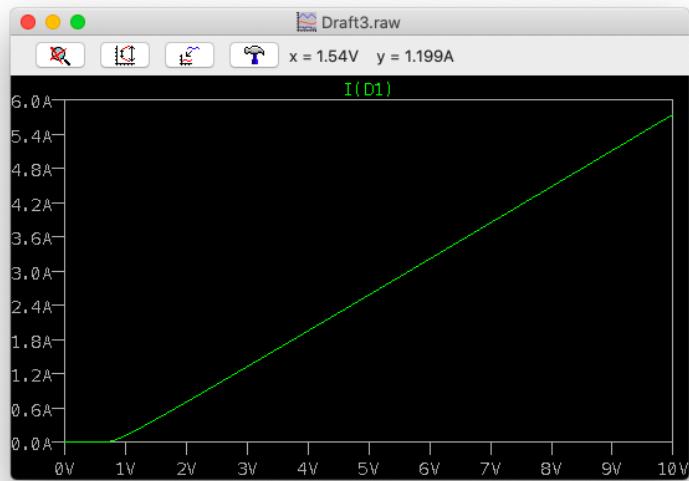


Place the Ammeter to the measure the diode current by clicking on to the diode



Model Graph:**VI characteristics of PN junction diode:****Observation:****PN Junction Diode:****Forward bias:**

V	R	Diode	Breakdown V
10	1	1N4148	0.631
	1	MMSD4148	0.617
	1	1N5819	0.243
50	1	1N4148	0.622
	1	MMSD4148	0.581
	1	1N5819	0.171
100	1	1N4148	0.567
	1	MMSD4148	0.541
	1	1N5819	0.149



Reverse bias:

V	R	Diode	Breakdown V
10	1	1N4148	2.9
	1	MMSD4148	0.206
	1	1N5819	0.3
50	1	1N4148	2.98
	1	MMSD4148	0.301
	1	1N5819	0.28
100	1	1N4148	0.302
	1	MMSD4148	0.294
	1	1N5819	0.29



Result & Inferences:

Thus, the VI characteristics of the PN junction diodes is studied.

Practical Applications:

PN junction Diodes are used

- in clipping circuits as wave shaping circuits in computers, radios, radars, etc.
- as switches in digital logic designs.
- in detector and demodulator circuits.
- in clamping circuits in TV receivers as well as voltage multipliers.
- as rectifiers in DC power supply manufacturing.

Zener diodes are used

- as a Voltage Regulator or Stabilizer,
- as a Meter Protector
- as a WaveShaper

Course Outcomes:

CO5. Analyze the characteristics of semiconductor devices and comprehend the various modulation techniques in communication engineering

Student Learning Outcomes (SLO):

SLO2. Having a clear understanding of the subject related concepts and of contemporary issues

Voltage Regulator using Zener Diode

(*Battery charging application*)

EXP 3 -

Aim:

To design a voltage regulator circuit to provide a 12V stabilized power supply from 30V DC power source.

Software Required:

LT Spice Software

Theory:

Zener diode acts as normal PN junction diode during forward biased condition. During reverse biasing as reverse voltage reaches breakdown voltage, diode starts conducting. A simple voltage regulator circuit can be designed using a Zener diode to maintain a constant DC output voltage across the load, inspite of variations in the input voltage or changes in the load current. The zener voltage regulator consists of a current limiting resistor R_S connected in series with the input voltage V_S with the zener diode connected in parallel with the load R_L in this reverse biased condition. The stabilised output voltage is always selected to be the same as the breakdown voltage V_Z of the diode.

The stabilized output voltage V_{out} is taken across the Zener diode. With no load connected to the circuit, the load current will be zero, ($I_L = 0$), and all the circuit current passes through the zener diode which in turn dissipates its maximum power. Also, a small value of the series resistor R_S results in a greater diode current when the large load resistance R_L is connected. As this increase the power dissipation requirement of the diode, care must be taken while selecting the appropriate value of series resistance so that the zener's maximum power rating is not exceeded under this no-load or high-impedance condition.

The load is connected in parallel with the zener diode, so the voltage across R_L is always the same as the zener voltage, ($V_R = V_Z$). There is a minimum Zener current for which the stabilisation of the voltage is effective and the Zener current must stay above this value operating under load within its breakdown region at all times. The upper limit of current is dependent upon the power rating of the device. The supply voltage V_S must be greater than V_Z .

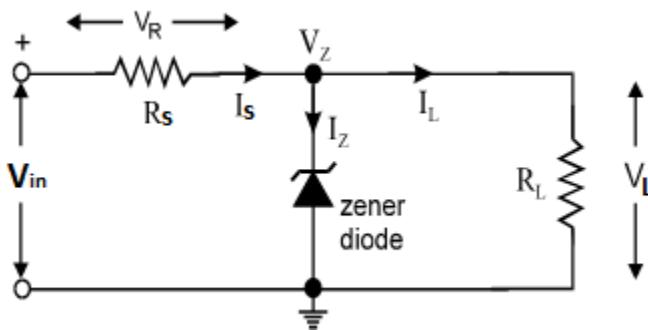


Fig.1 Zener Voltage regulator

4.Design a Voltage Regulator:

The maximum current through Zener diode is given as

$$I_{\max} = \frac{\text{Power}}{\text{zener voltage}}$$

I_{\max} - Maximum current for Zener diode

V_Z - Zener Diode standard voltage

V_{in} - Input voltage (it is known)

V_s - Voltage across series resistance

V_L - Voltage across the load resistance

I_s - Current passing through the series resistance

I_Z - Current passing through the Zener diode

I_L - Current passing through the load resistance

(Note: When selecting the zener diode, be sure that its maximum power rating is not exceeded.)

Calculation voltage and current:

The total current drawn from the source is the same as that through the series resistor (R_s)

$$I_s = \frac{V_s}{R_s}$$

The current through the load resistor (R_L) is

$$I_L = \frac{V_L}{R_L}$$

and the zener diode current is

$$I_Z = I_s - I_L$$

If the voltage source is $V_s = V_{in} - V_L$ greater than V_Z , and $V_L = V_Z$

If the voltage source is less than V_Z

$$V_s = \frac{R_s * V_{in}}{(R_s + R_L)} \quad \text{and} \quad V_L = \frac{R_L * V_{in}}{(R_s + R_L)}$$

Basically, there are two type of regulations such as:

- a. **Line Regulation:** In this type of regulation, series resistance and load resistance are fixed, only input voltage is changing. Output voltage remains the same as long as the input voltage is maintained above a minimum value.

$$\text{Percentage of Line regulation} = \left[\frac{\Delta V_L}{\Delta V_{in}} \right] \times 100$$

- b. **Load Regulation:** In this type of regulation, input voltage is fixed and the load resistance is varying. Output voltage remains same, as long as the load resistance is maintained above a minimum value.

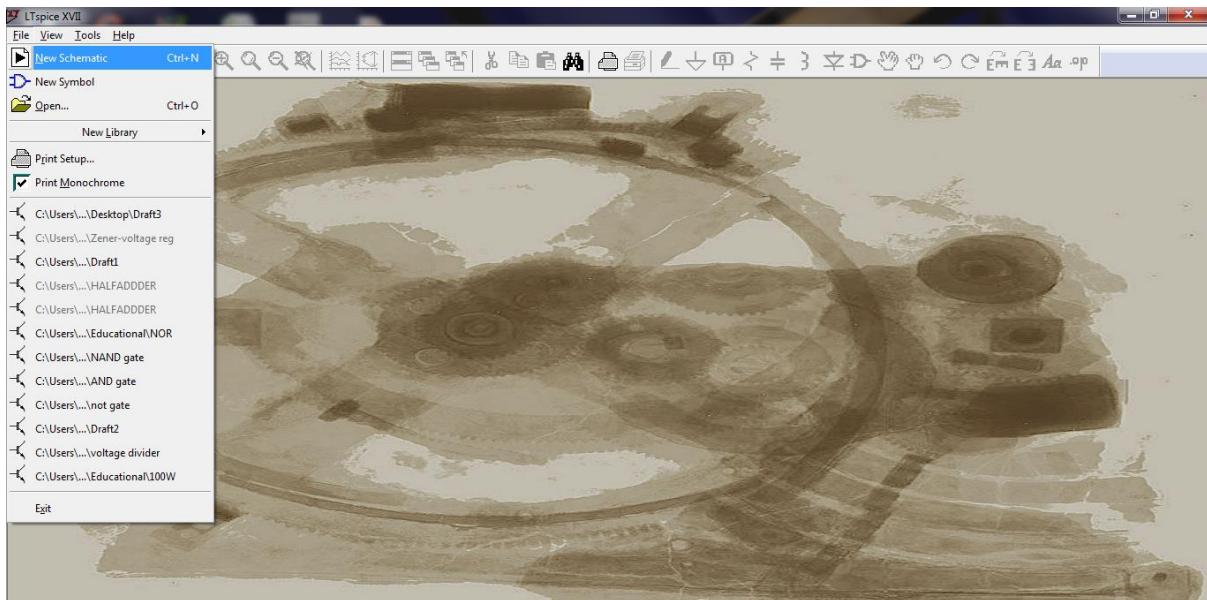
Let us consider V_{NL} is the output voltage when there is no load resistance (ideally $V_{NL} = \text{Zener voltage}$) and V_{FL} is the output voltage when load resistance is maximum.

$$\text{Percentage of Load regulation} = \left[\frac{V_{NL}-V_{FL}}{V_{NL}} \right] \times 100$$

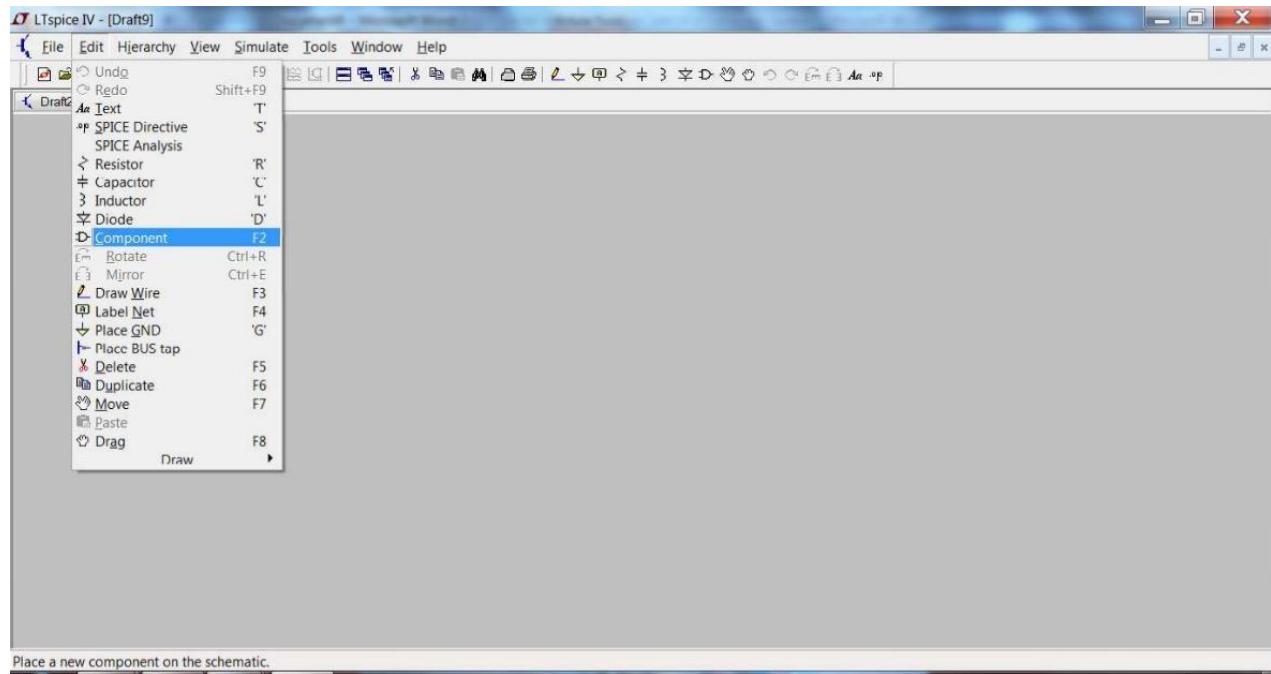
Note: This is an ideal circuit. For a real circuit, there will be small variations in output voltage with varying input voltage or load resistance.

Procedure for Simulation:

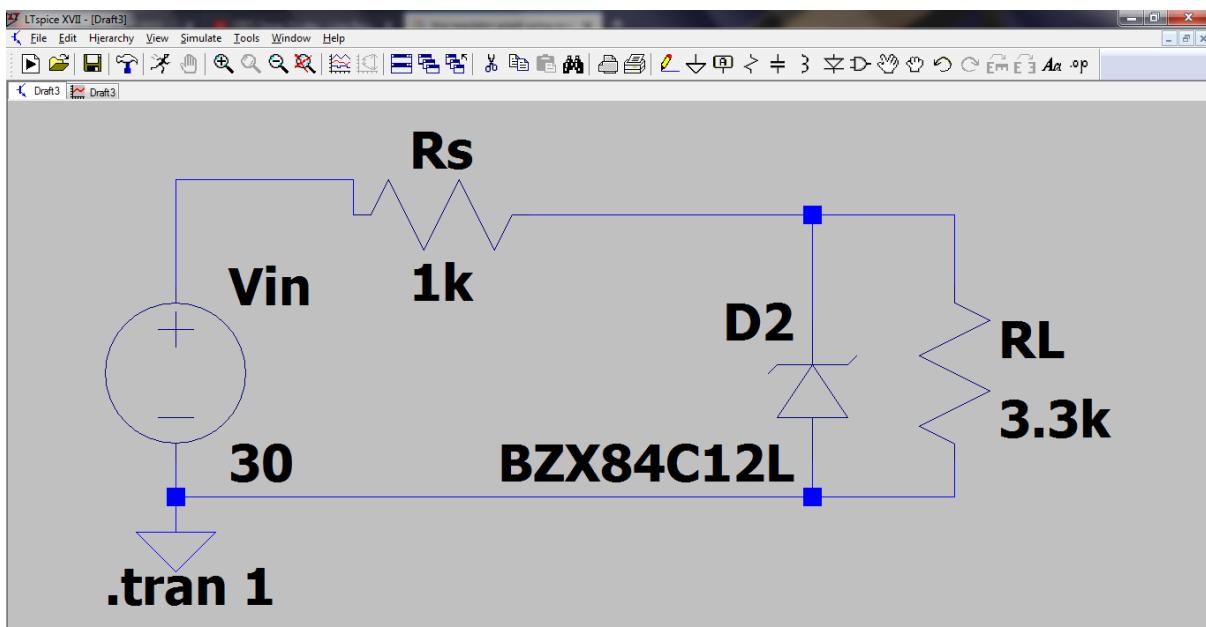
1. Open LTspice. Go to File _New Schematic.



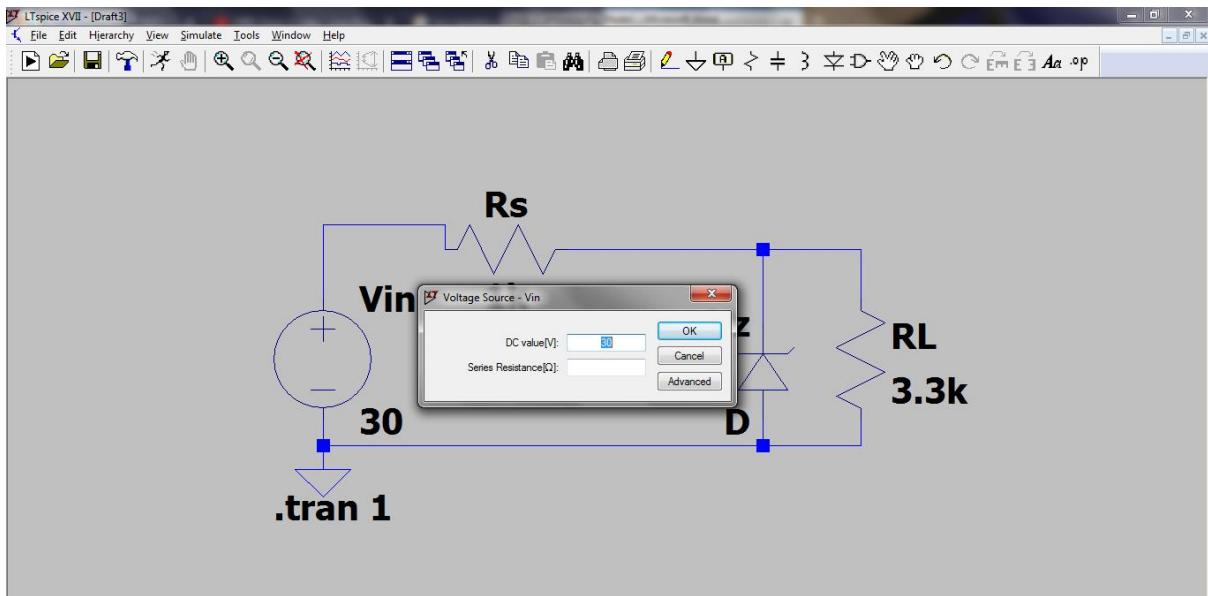
2. On the File Menu, click on Edit -Component.



3. Place the voltage source, series resistance, Zener diode, load resistance and ground on to schematic and make necessary connections as shown in the Figure.

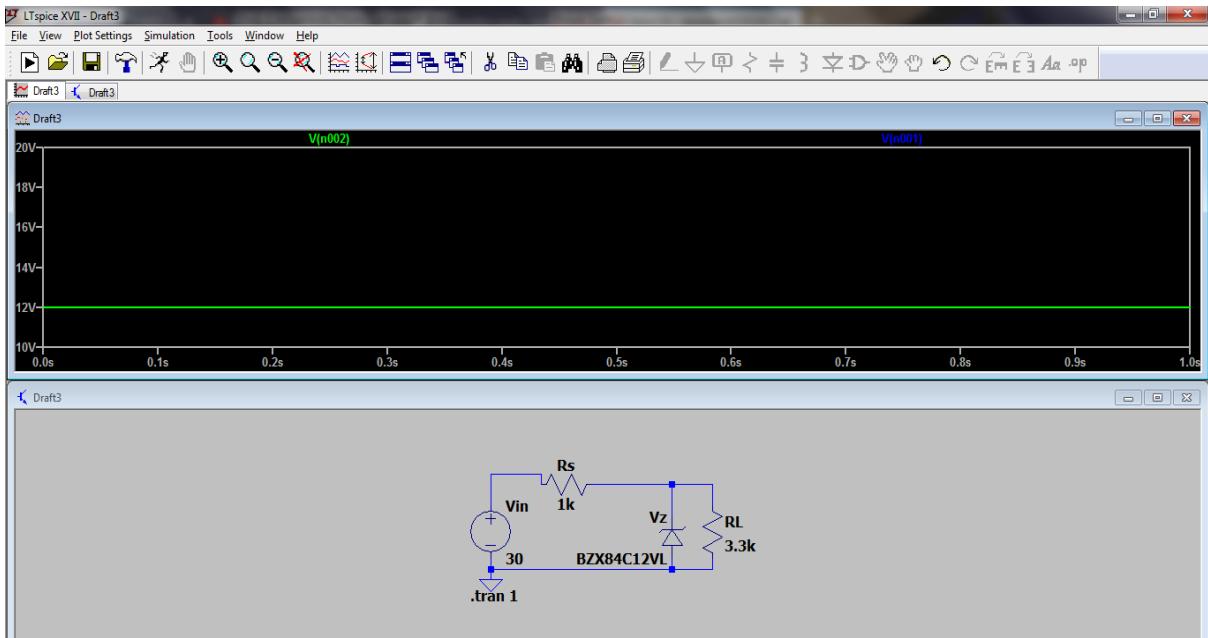


4. As shown in the figure below, Right click on the voltage sources and vary the values for line regulation.

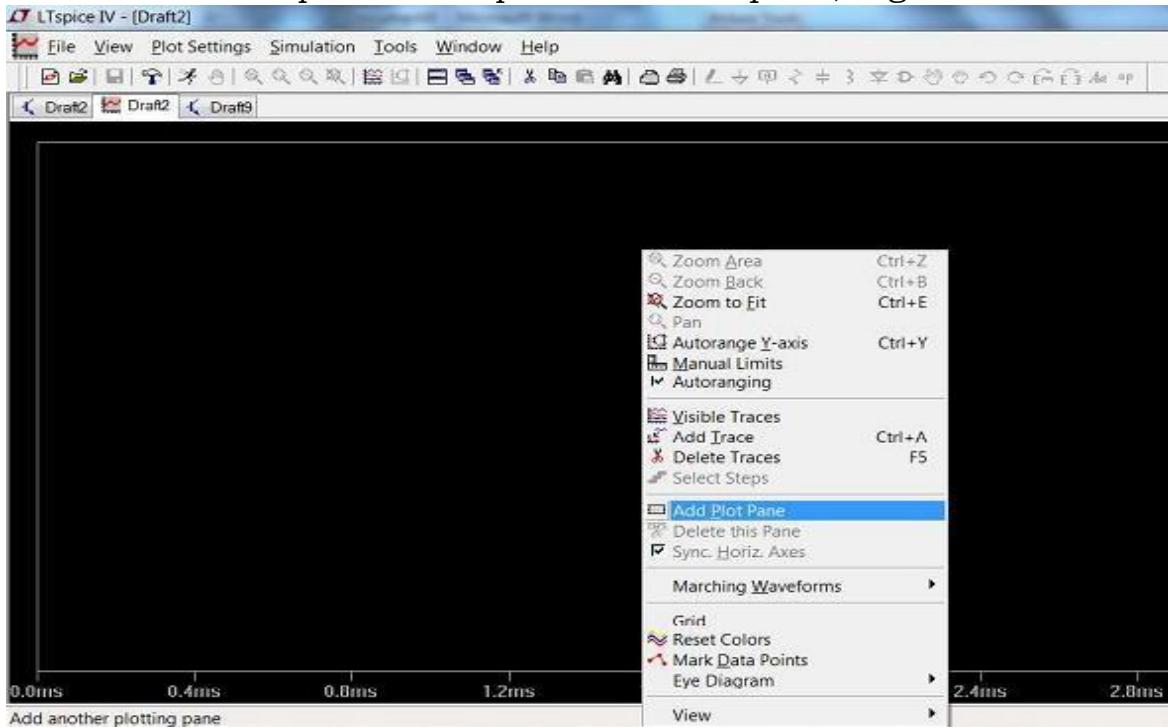


5. Go to Edit SPICE analysis.

Set the stop time to 1 ms in Transient command and run the simulation (run symbol on menu bar).

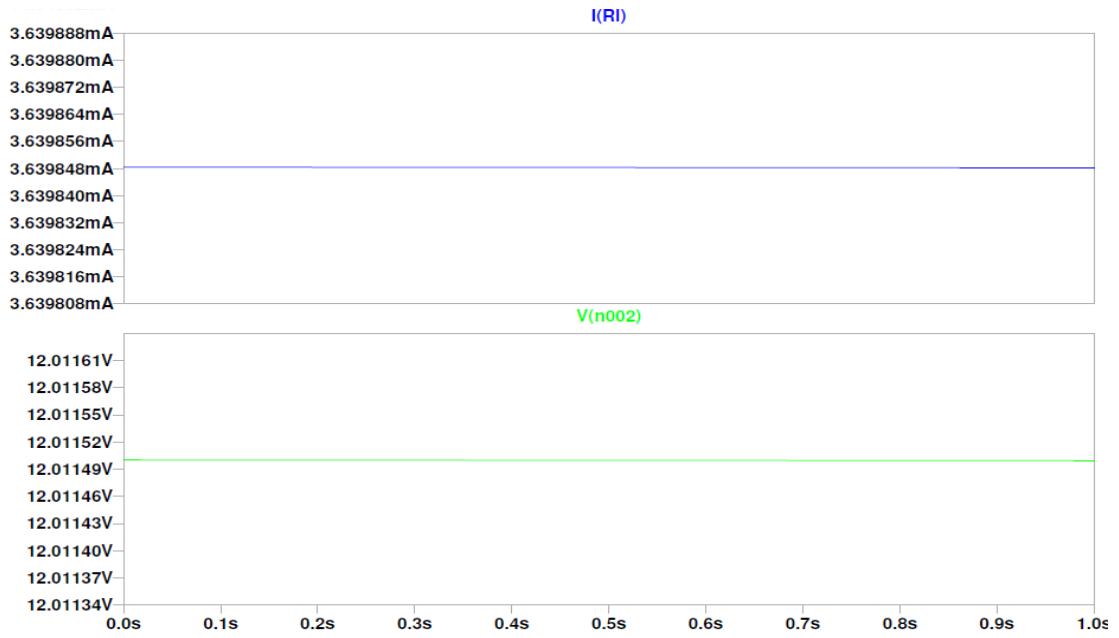


6. To view the results, right click ---> Add Plot Pane, add plot panes to view the input and output. For each pane, right click ---> Add

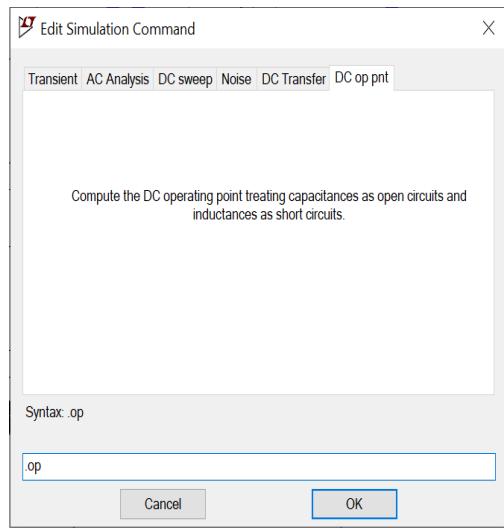


Trace ---> Select V (<<respective node>>). (nodes correspond to input and output).

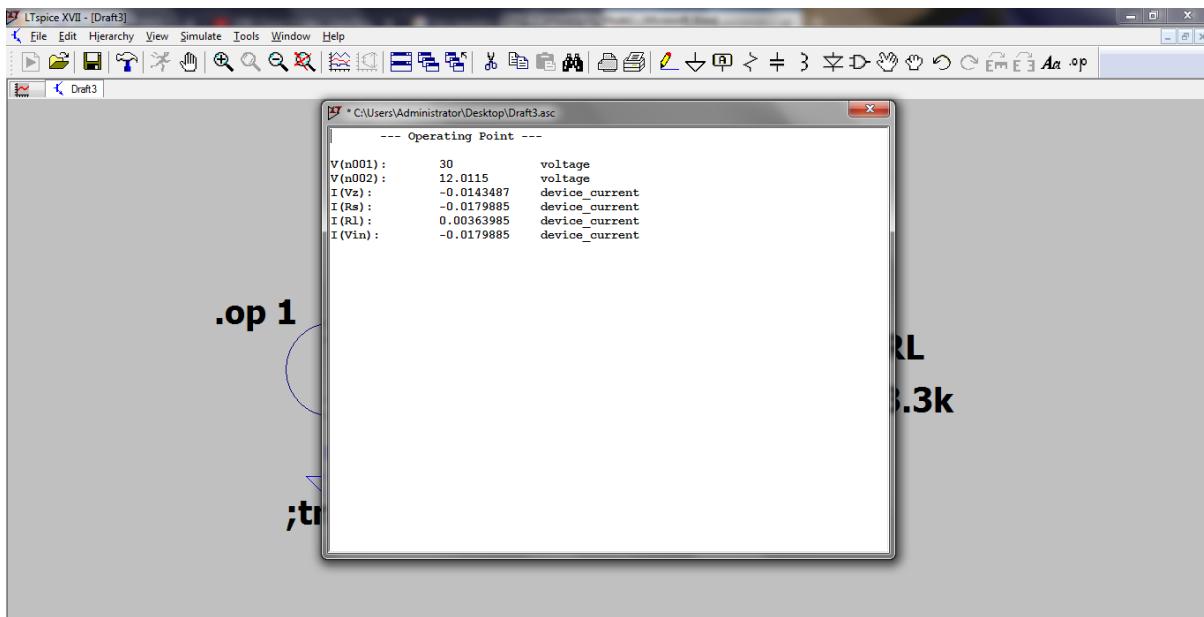




7. To view the output voltage and input voltage value, Go to Edit → SPICE analysis.



8. The node voltages shown in Figure below should be entered in the observation table.

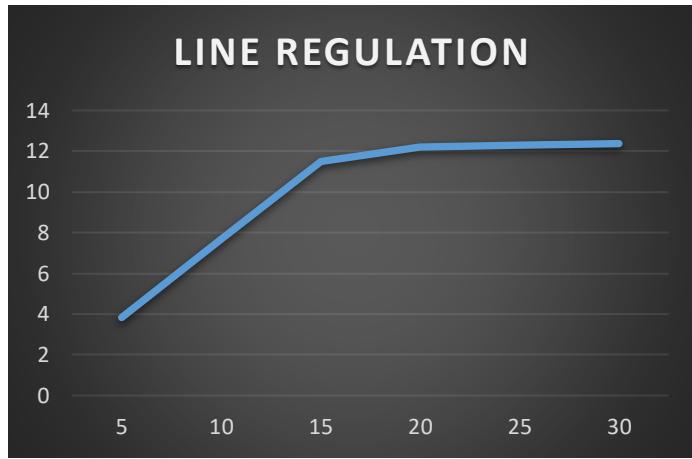


Observation Table

a. Line regulation

1. Choose the zener diode (number....) and connect the circuit as shown in Fig.
2. Vary the supply voltage from in steps of 1 volt from (0- 15) volts.
3. Note down the corresponding input voltage and output voltage and tabulate it.
4. Plot the graph between V_{in} and V_L taking V_{in} on x-axis V_L on y-axis.

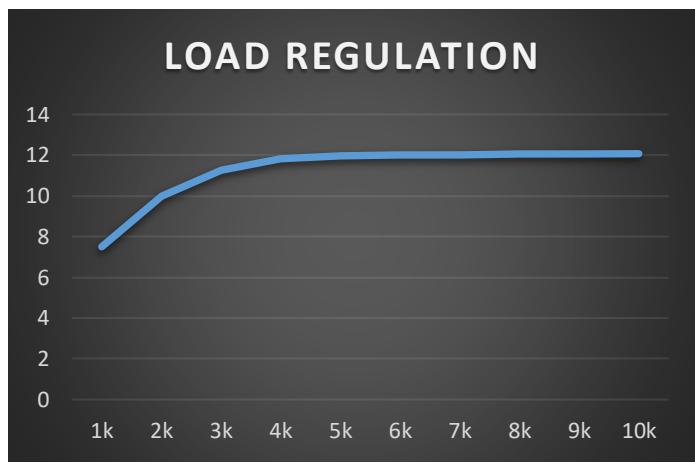
Trial No	V_{in}, in Volt	V_L, in Volt
1	5	3.83
2	10	7.67
3	15	11.49
4	20	12.185
5	25	12.28
6	30	12.37



b. Load Regulation

1. Connections are given as per the circuit diagram.
2. Fix the supply voltage at 15 V.
3. Without connecting the load R_L , note down the No-load voltage (V_{NL}).
4. Change the load Resistance with the interval of $1\text{k}\Omega$ from $1\text{k}\Omega - 10\text{k}\Omega$ up to maximum range.
5. Note the reading and tabulate it.
6. Plot the graph between V_L along x-axis and R_L along y-axis.

Trial No	R_L in Ohms	V_L , in Volt
1	1k	7.5
2	2k	10
3	3k	11.24
4	4k	11.813
5	5k	11.947
6	6k	12



7. GRAPH

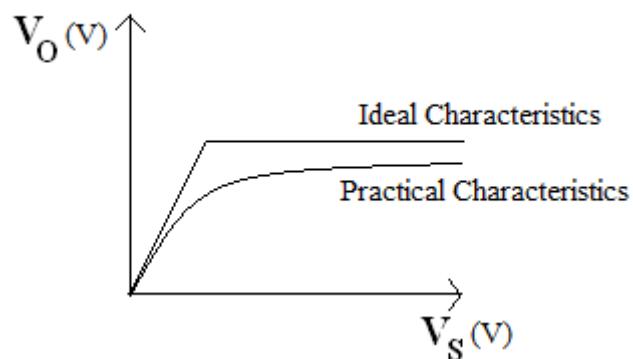


Fig.2 Line regulation

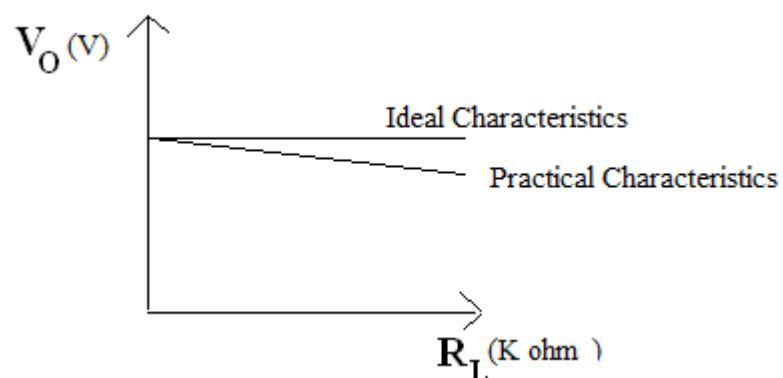


Fig. 3 Load regulation

8. INFERENCES:

9. RESULT:

Result & Inferences:

Thus, the Zener diode as a voltage regulator is designed to provide a stabilized output voltage and the circuit is analyzed for the line regulation and load regulation.

Practical Applications:

Regulated Power Supply for battery charging applications.

Course Outcome:

CO5. Analyze the characteristics of semiconductor devices and comprehend the various modulation techniques in communication engineering

CO6. Design and conduct experiments to analyze and interpret data

Student Learning Outcomes (SLO):

SLO2. Having a clear understanding of the subject related concepts and of contemporary issues

Sinusoidal Steady State Response of RLC circuit (Series Band pass filter using passive components)

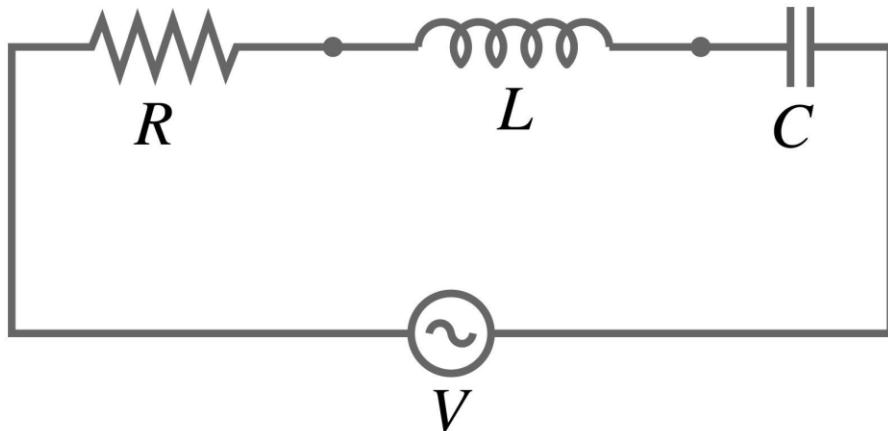
Aim:

To study the sinusoidal steady-state response of the given RLC circuit which can be used in a series bandpass filter.

Software Required:

LTspice software

Theory & Circuit Diagram:



The Series RLC circuit is shown in the above figure. The RLC series circuit can be used as a series bandpass filter by placing a series LC circuit in series with the load resistor. In the series RLC circuit, larger reactance determines the net reactance of the circuit.

If $X_L > X_C$ the circuit behaves like an inductive circuit and the current lags the voltage and if $X_C > X_L$, the circuit behaves like a capacitive circuit and the

current leads the voltage. The magnitude and Phase angle of the current, I in the series RLC circuit is obtained using the following equation,

$$I = \frac{V}{Z} = \frac{V}{\sqrt{R^2 + (X_L - X_C)^2}}$$

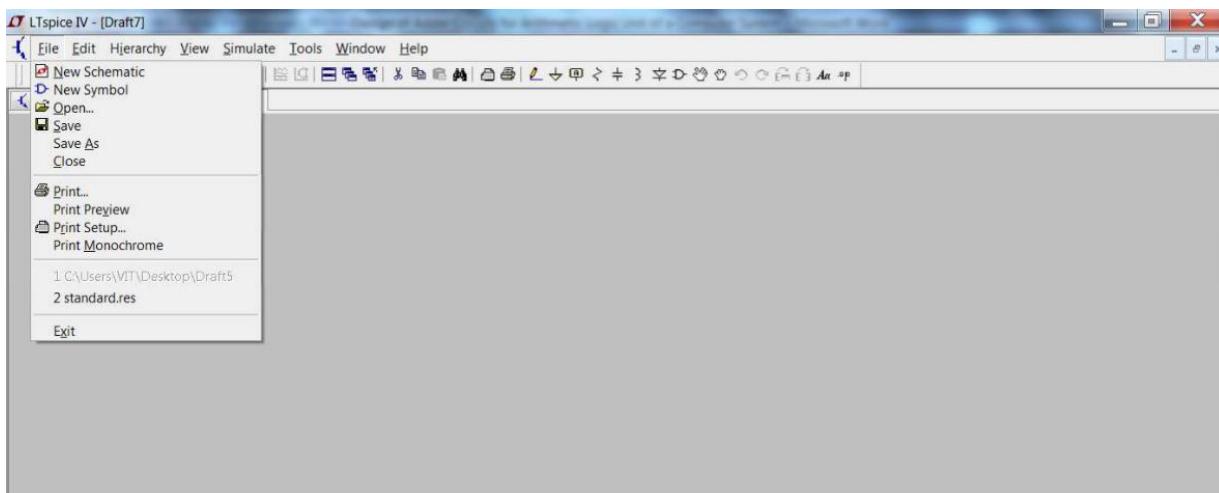
$$\varphi = \frac{\tan^{-1}(X_L - X_C)}{R}$$

For RLC circuit with $R = 10 \Omega$, $L = 1mH$, $C = 1 \mu F$ and $V_m = 100 V$, $f = 50 \text{ Hz}$, $X_L = \omega L = 2\pi fL = 0.314 \Omega$, $X_C = (1/\omega C) = (1/2\pi fC) = 3184 \Omega$, $I_m = 0.0314 A$, $\Phi = 89.82^\circ$.

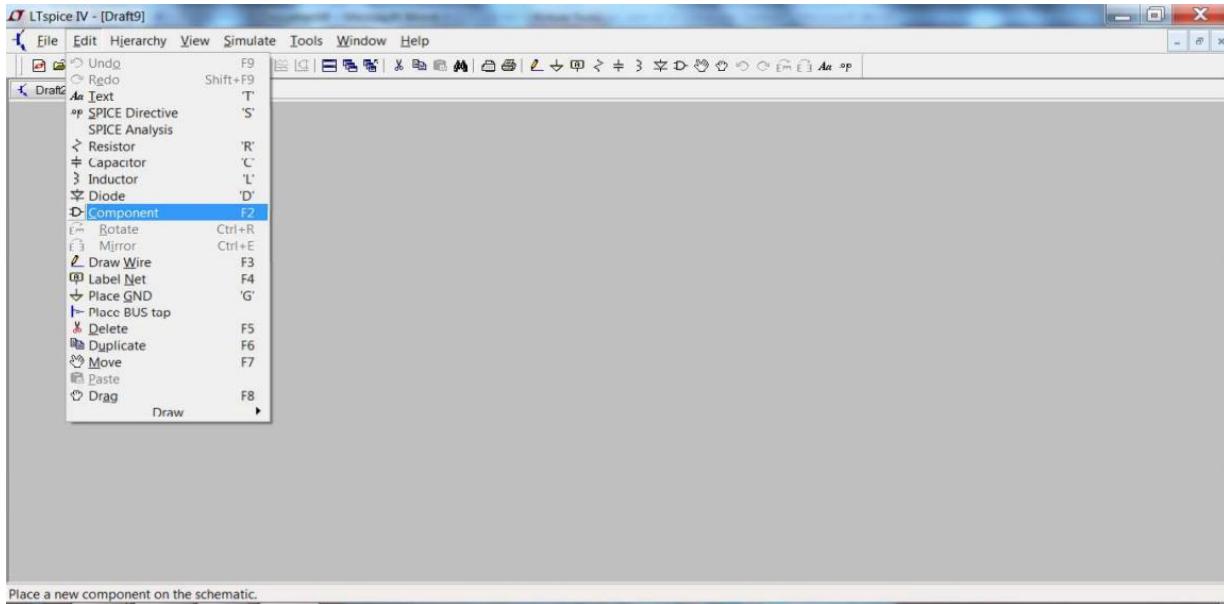
In this example, since $X_C > X_L$, Current leads the voltage.

Procedure:

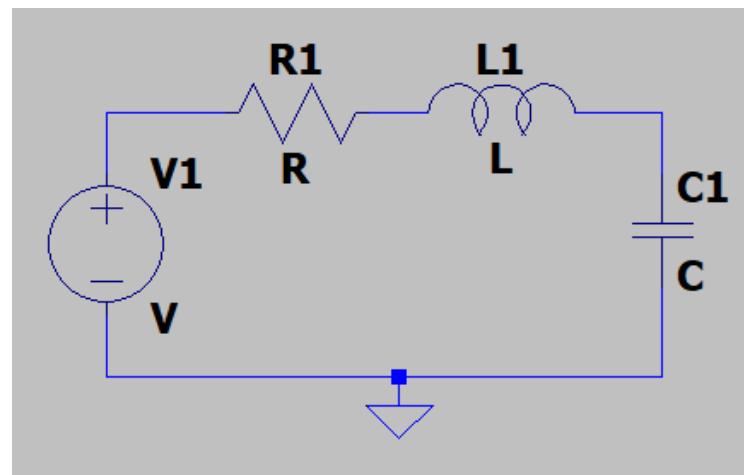
7. Open LTspice. Go to File New Schematic.



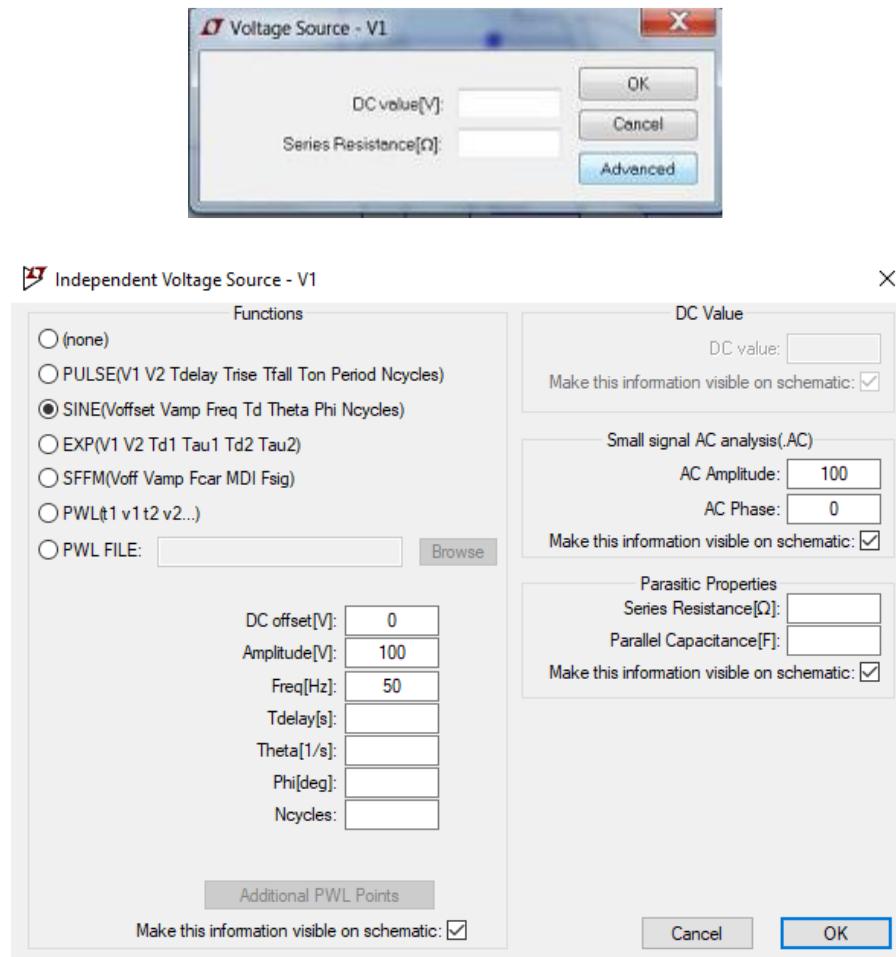
8. On the File Menu, click on Edit Component.



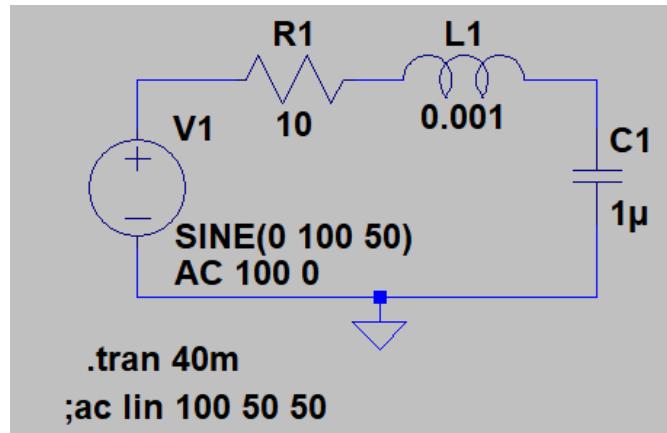
9. Place the voltage sources, resistor, inductor , capacitor and ground on to schematic and make necessary connections as shown in the Figure.



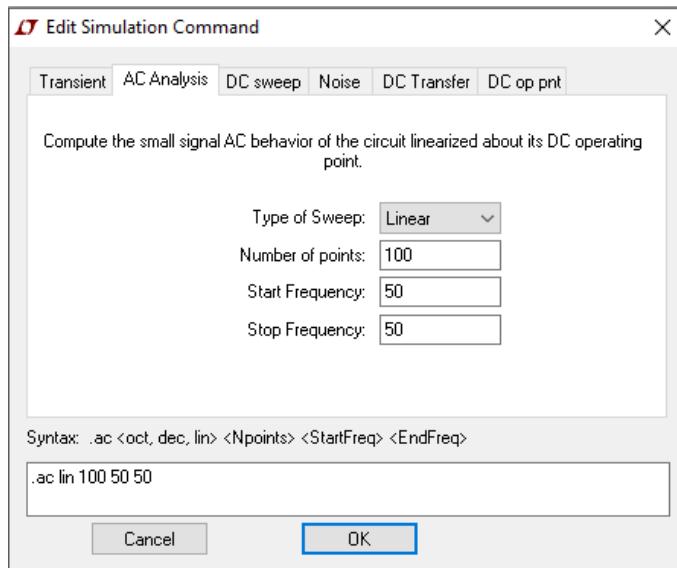
10. As shown in the figures below, Right click on the voltage source V1 and click Advanced option and then Select SINE (Voffset Vamp Freq Td Theta Phi Ncycles) and Set the values as (DC offset = 0, Amplitude =100, Freq = 50).



11. As shown in the figure below, Right click on the resistor, inductor and capacitor and set the value as 10Ω , 0.001 H and $1 \mu\text{F}$ respectively



12. Go to Edit → SPICE analysis. Set the type of sweep to Linear, Number of points to 100 and start and stop frequency to 50 each in the AC Analysis command as shown in the figure below and run the simulation. (run symbol on the menu bar).

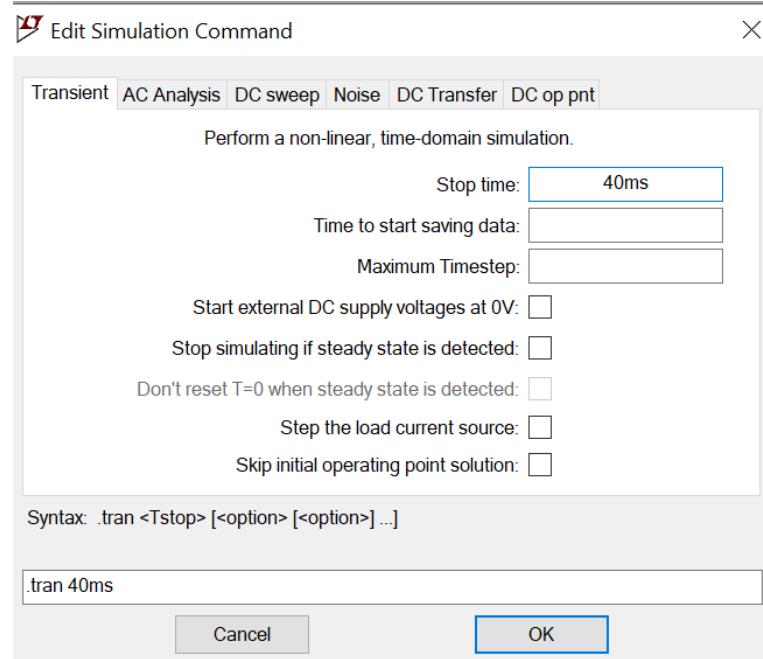


13. Observe the peak value of the current and phase angle from the obtained output window below and note it in the “Theoretical Value” column of the observation table.

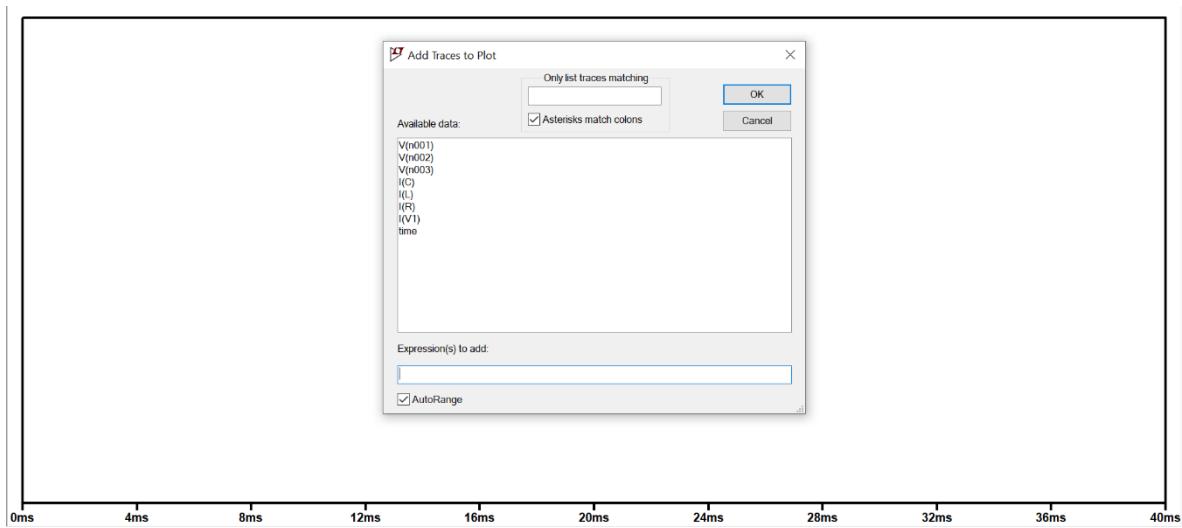
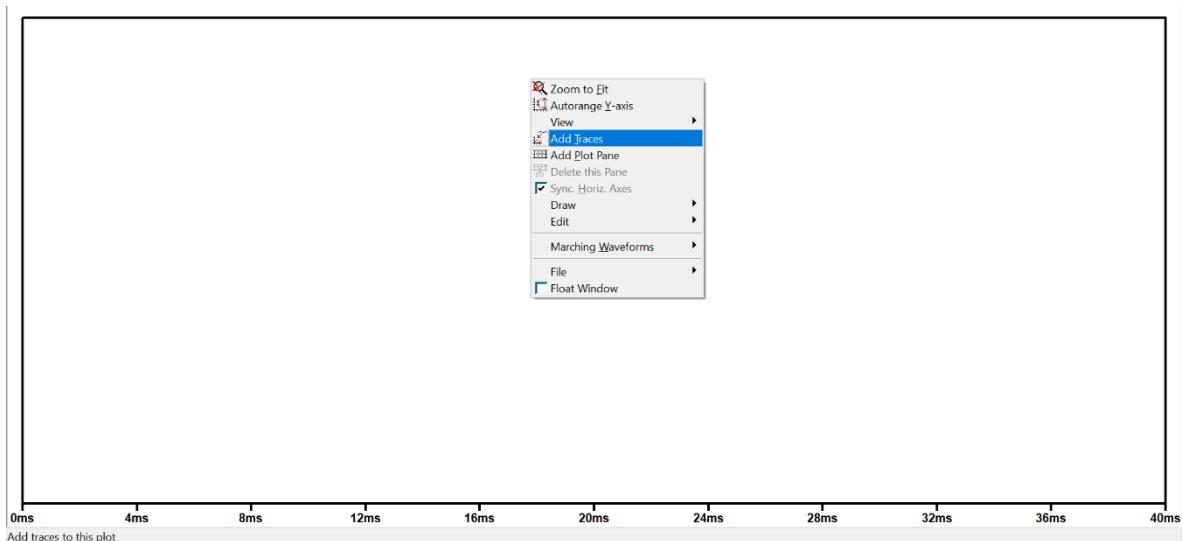
```
* * H:\RLC.asc
--- AC Analysis ---

frequency:      50          Hz
V(n002):        mag:    99.9995 phase: -0.180017°      voltage
V(n001):        mag:    100 phase: 0°                  voltage
V(n003):        mag:    100.009 phase: -0.180035°      voltage
I(C1):          mag: 0.0314189 phase: 89.82°      device_current
I(L1):          mag: 0.0314189 phase: 89.82°      device_current
I(R1):          mag: 0.0314189 phase: -90.18°      device_current
I(V1):          mag: 0.0314189 phase: -90.18°      device_current
```

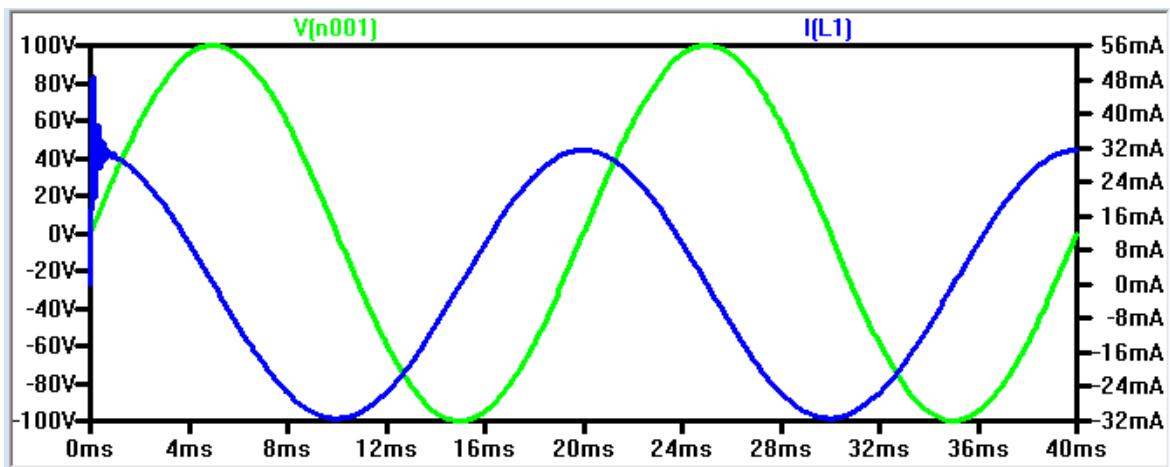
14. **For waveforms:** Go to Edit → SPICE analysis. Set the stop time to 40ms in Transient command as shown in the figure below and run the simulation. (run symbol on the menu bar).



15. To view the results, right click → Add Trace → Select V (<<input node>>) and I (L1).



16. Observe the waveforms, change the appropriate colors for proper visibility using color preferences and control panel tool. Sample figure shown below.

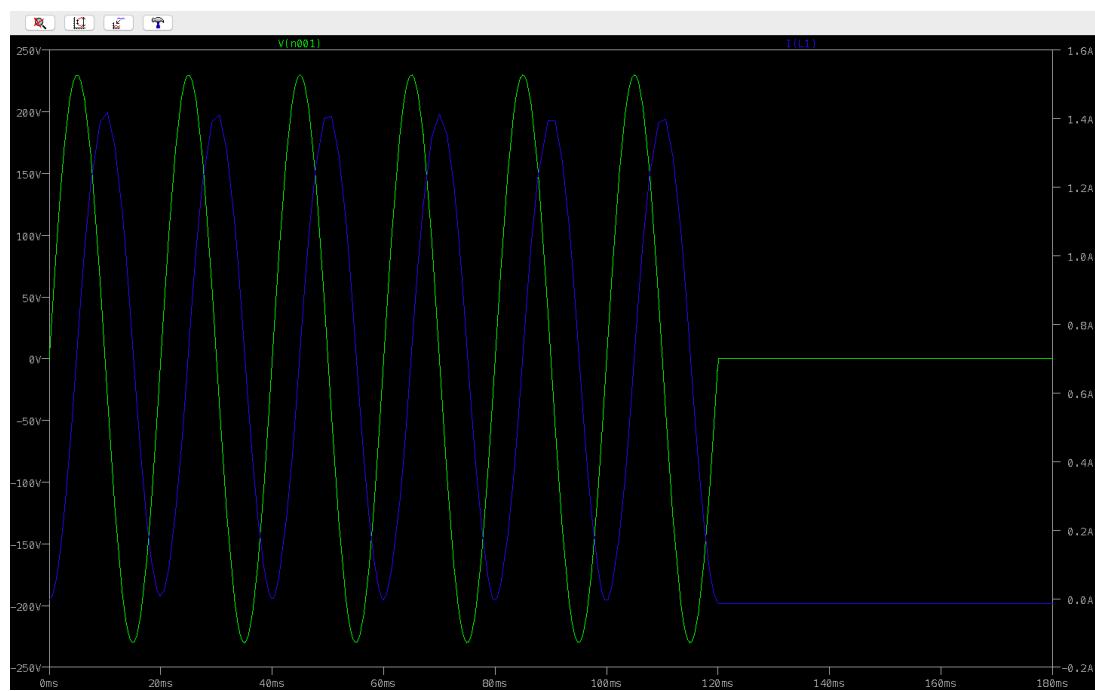


Observation table:

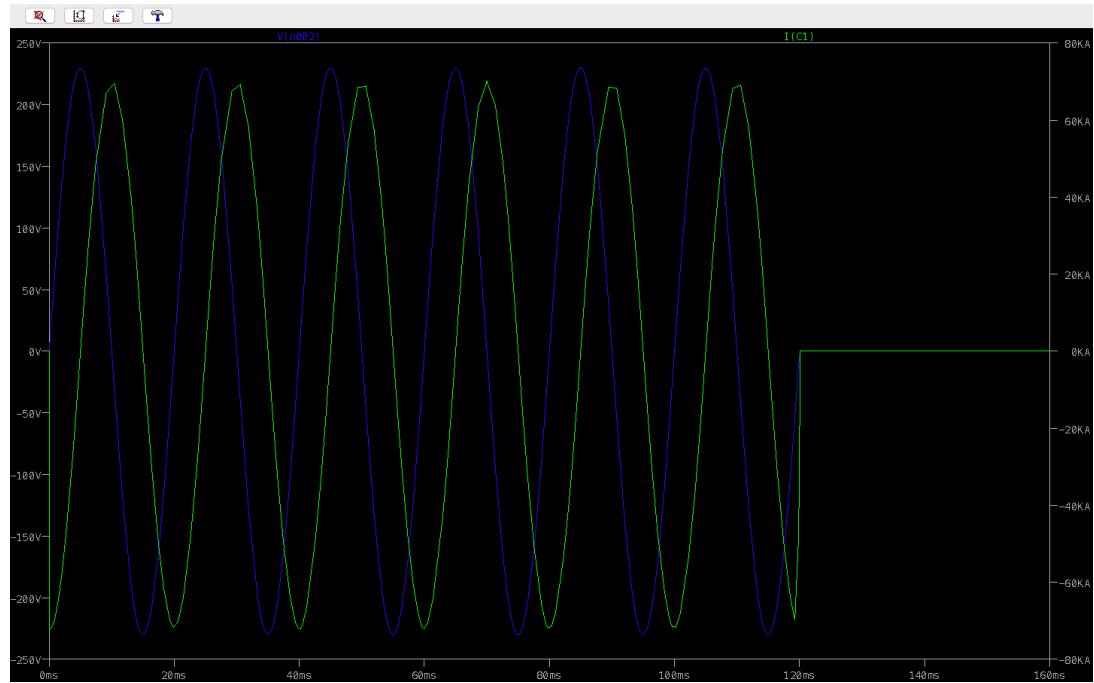
S. No.	Parameter	Theoretical Value	Observed Value
1.	I (Peak value)	0.03156 A	0.0314 A

2.	Phase angle	90.1 Deg	89.82 Deg
----	-------------	-----------------	------------------

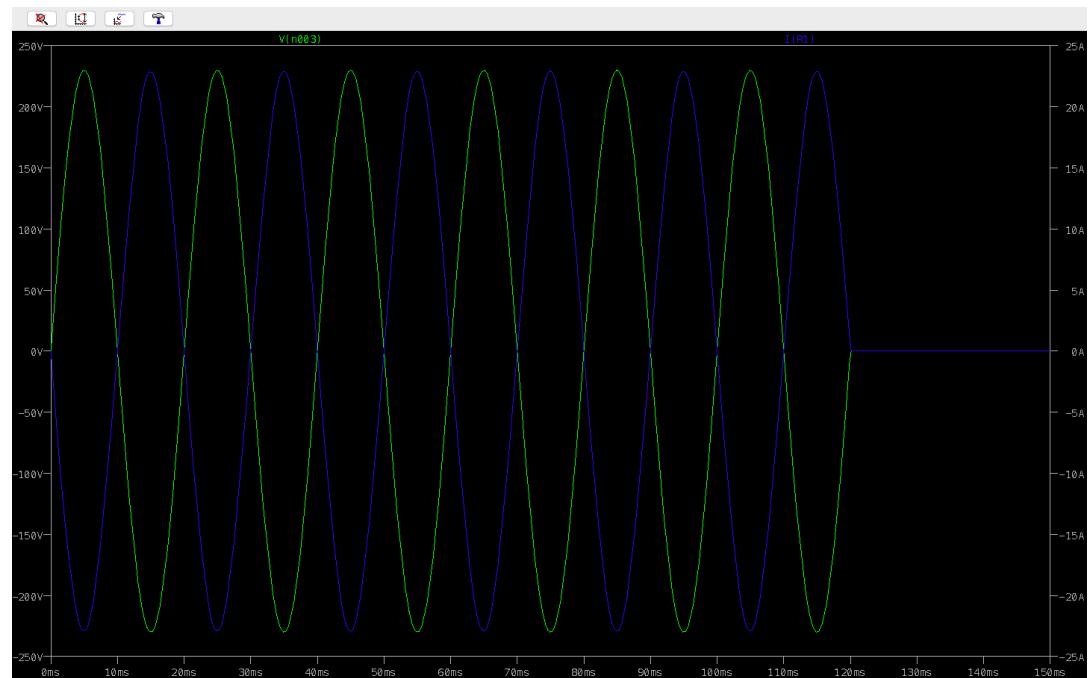
L-Circuit :



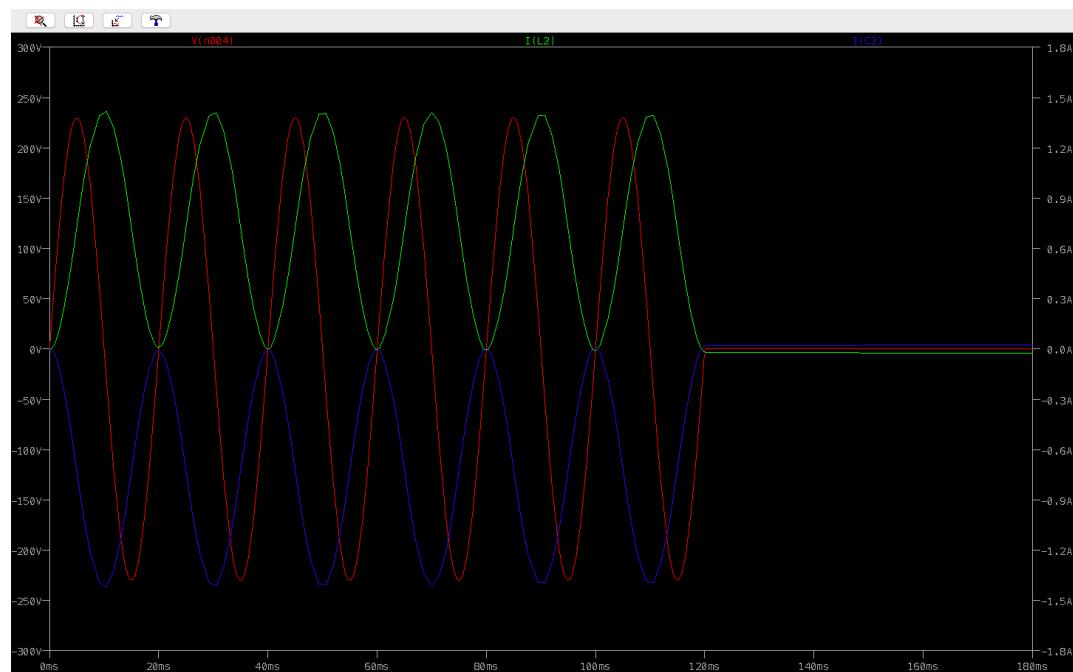
C-Circuit :



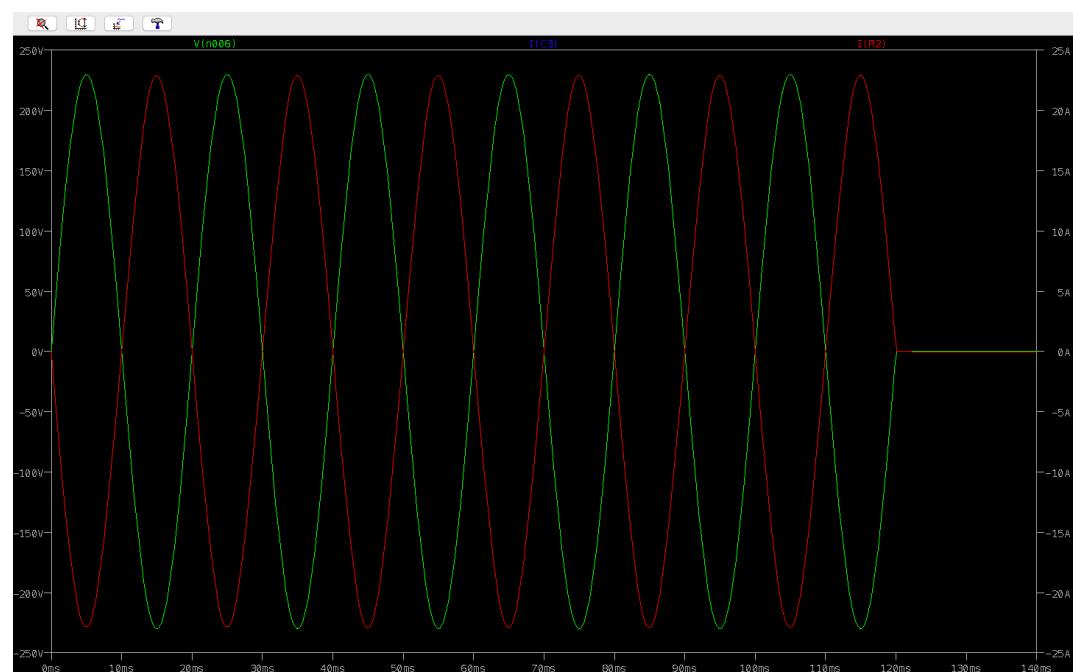
R-Circuit :



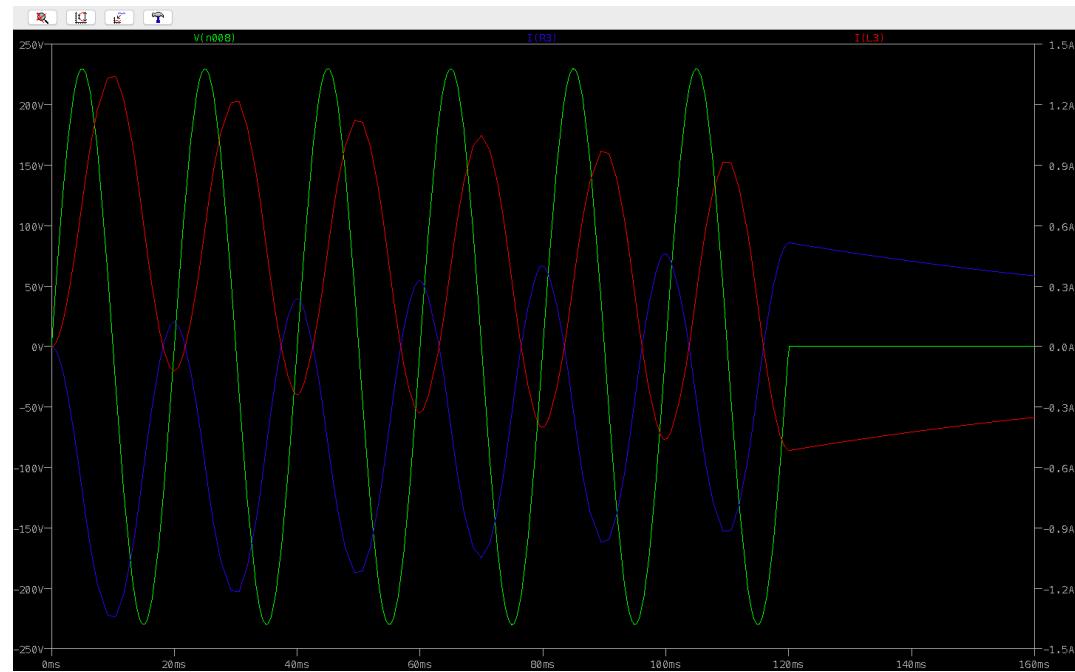
LC-Circuit :



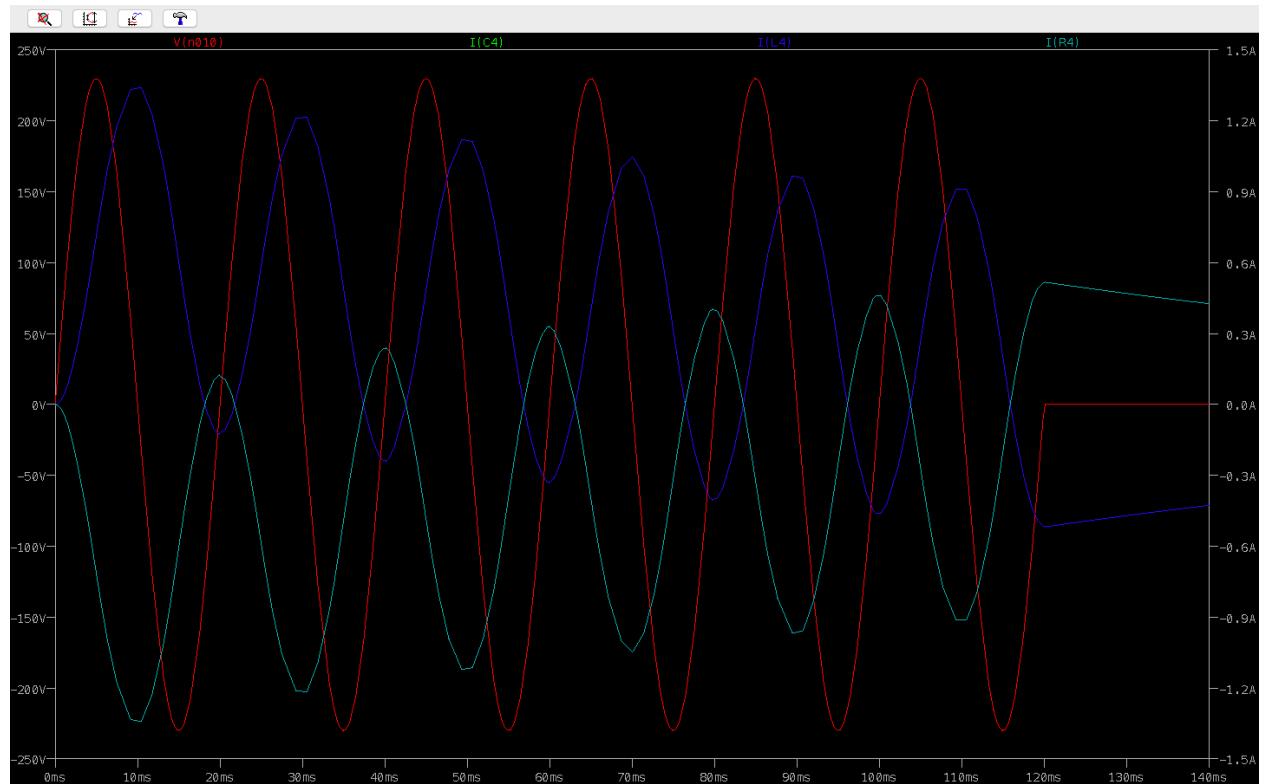
CR-Circuit :



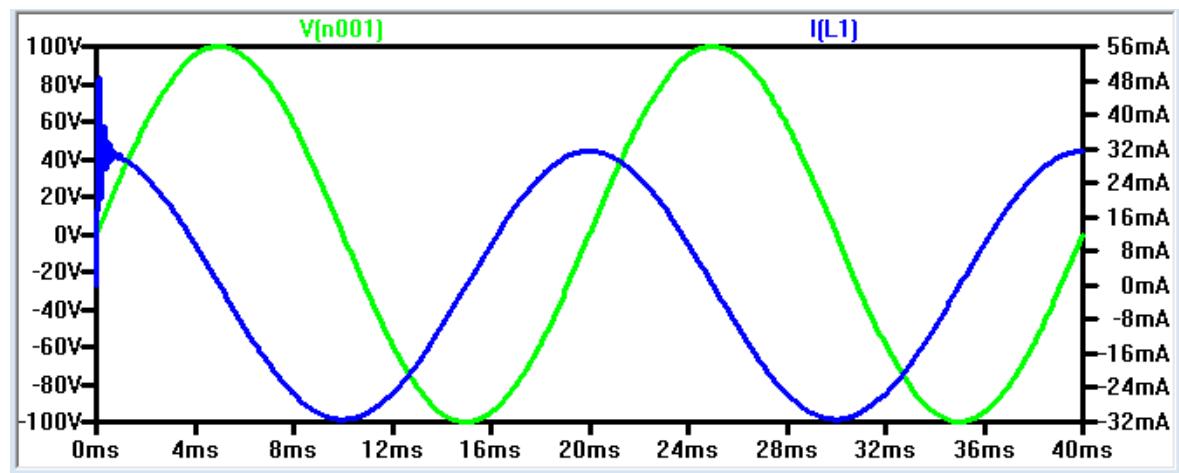
LR-Circuit :



LCR-Circuit :



Waveforms:



Result & Inferences:

Thus, a series RLC circuit has been designed and implemented in LTspice software, and the current amplitude and phase angle is observed as 0.0314 A and 89.82° respectively which is matching with Theoretical Values. From the waveforms, it is also observed that the current leads the voltage.

Practical Applications:

The three circuit elements, R, L, and C can be combined in several different topologies by connecting them in series or parallel. RLC circuits have many applications as follows:

- Variable tuned circuit
- Filters - Band-pass filter, Band-stop filter, Low-pass filter or High-pass filter
- Oscillator
- Voltage multiplier
- Pulse discharge circuit

Course Outcome:

CO2. Analyze AC power circuits and networks, its measurement and safety concerns

CO6. Design and conduct experiments to analyze and interpret data

Student Learning Outcomes (SLO):

SLO1. Having an ability to apply mathematics and science in engineering applications

SLO9. Having problem-solving ability- solving social issues and engineering problems

Verification of Truth tables for Logic gates *(Alarm or Buzzer Application)*

Aim:

To study about logic gates and verify its truth tables.

Software Used:

LTspice software

Theory and Circuit Diagram:

The circuit that takes the logical decision and the process is called logic gates. Each gate has one or more input and only one output. OR, AND and NOT are basic gates. NAND and NOR are known as universal gates. Basic gates are formed from these gates.

AND Gate:

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

OR Gate:

The OR gate performs a logical addition commonly known as the OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low.

NOT GATE:

The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high.

NAND GATE:

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the inputs is low. The output is low level when both inputs are high.

NOR GATE:

The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

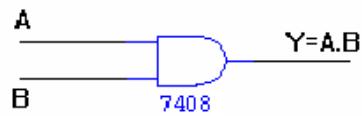
XOR GATE:

The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

Circuit Diagram:

AND Gate:

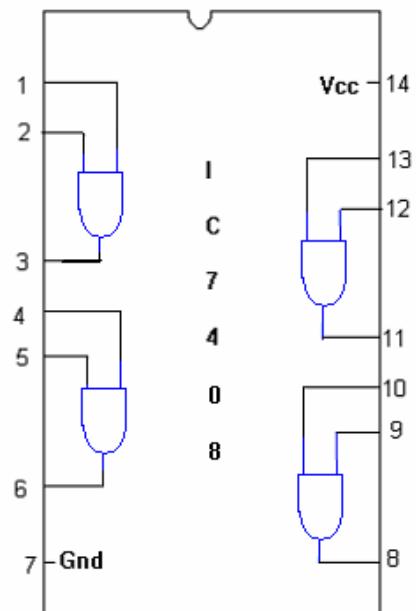
SYMBOL:



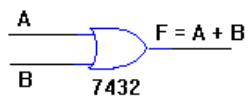
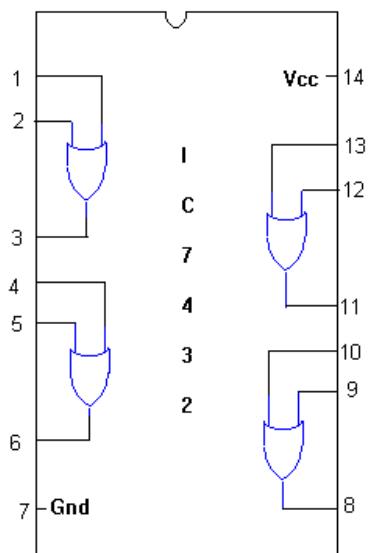
TRUTH TABLE

A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

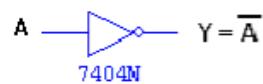
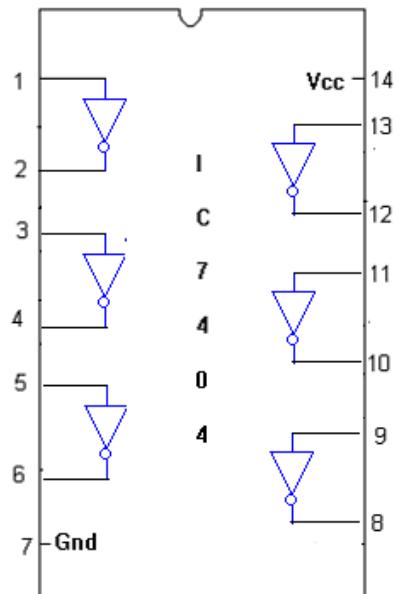
PIN DIAGRAM:



OR GATE:

SYMBOL :**PIN DIAGRAM :****TRUTH TABLE**

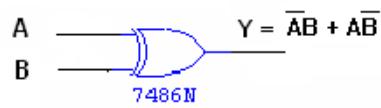
A	B	$A+B$
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE:**SYMBOL:****PIN DIAGRAM:****TRUTH TABLE :**

A	\bar{A}
0	1
1	0

X-OR GATE :

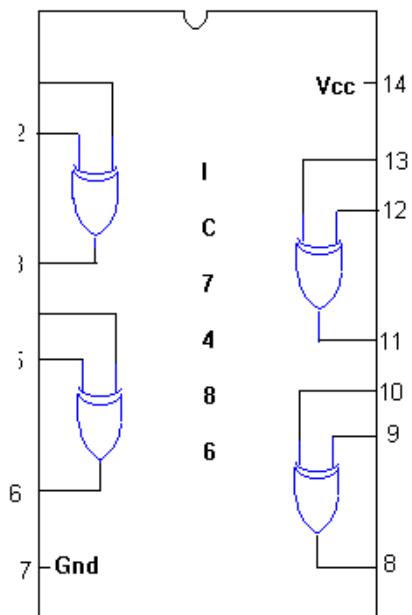
SYMBOL :



TRUTH TABLE :

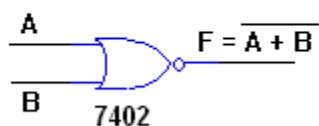
A	B	$\overline{AB} + \overline{A}\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

PIN DIAGRAM :



NOR GATE:

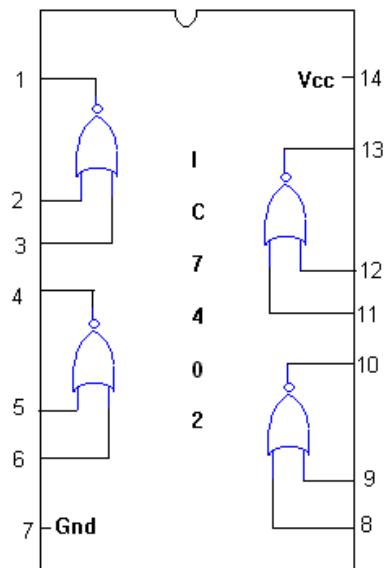
SYMBOL :



TRUTH TABLE

Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	0

PIN DIAGRAM :



NAND

gate

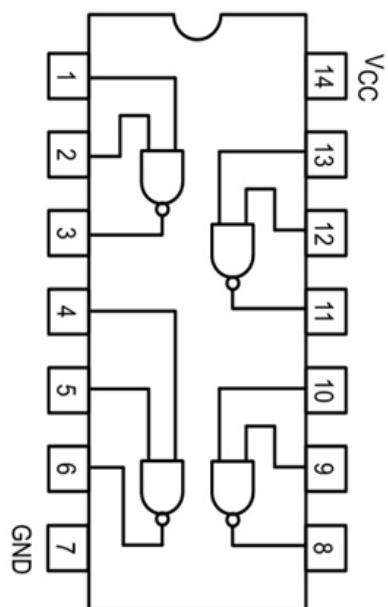
SYMBOL :



TRUTH TABLE

Input A	Input B	Output
0	0	1
0	1	1
1	0	1
1	1	0

PIN DIAGRAM :



X-NOR gate

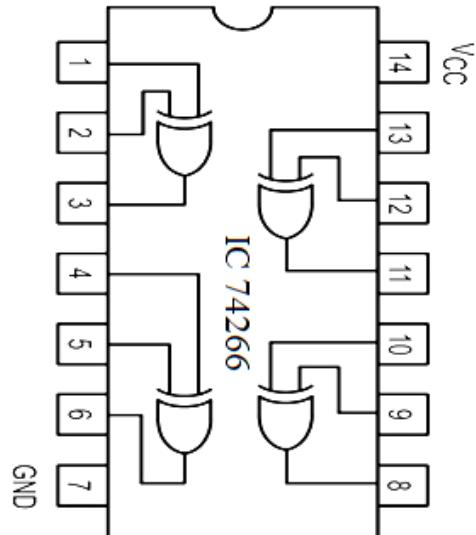
SYMBOL :



TRUTH TABLE

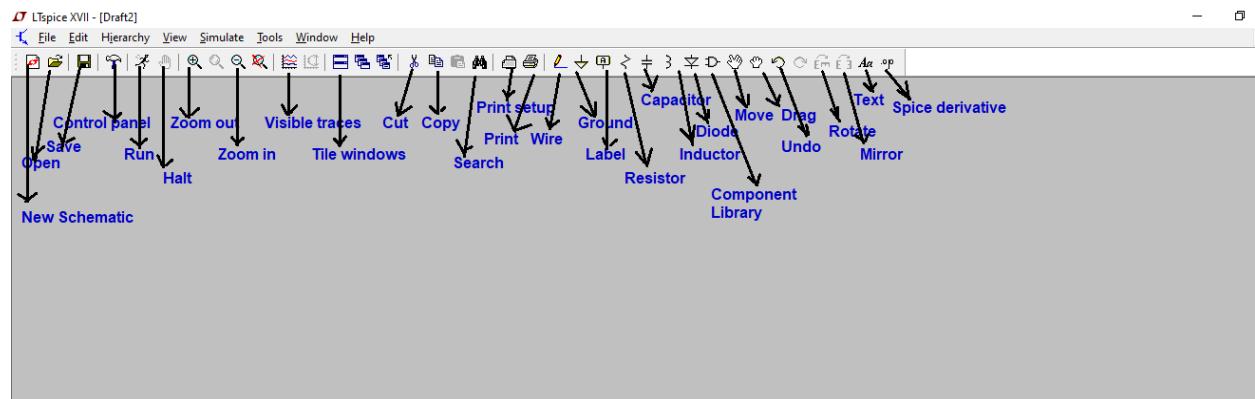
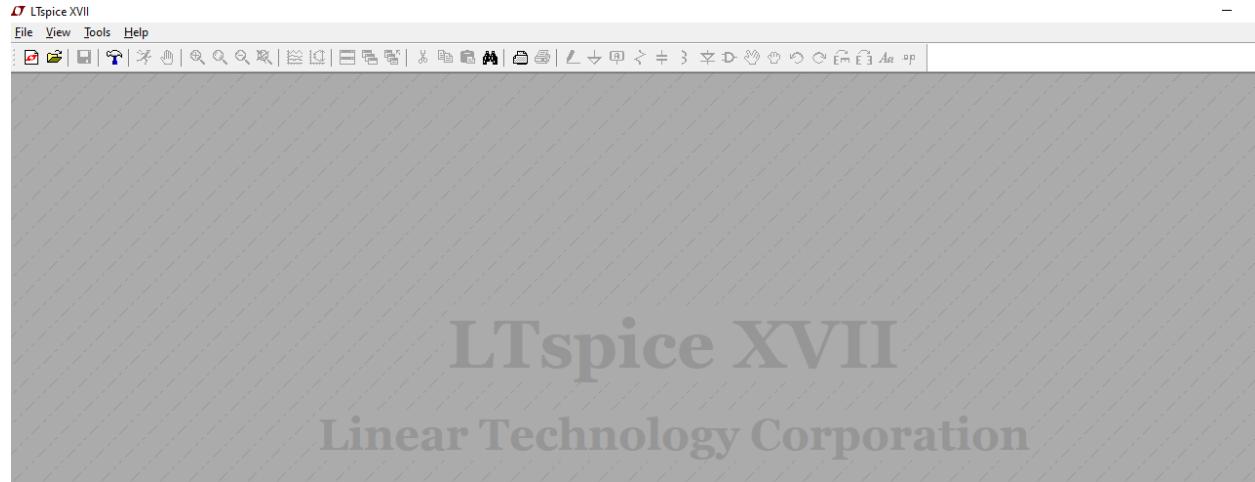
Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	1

PIN DIAGRAM :

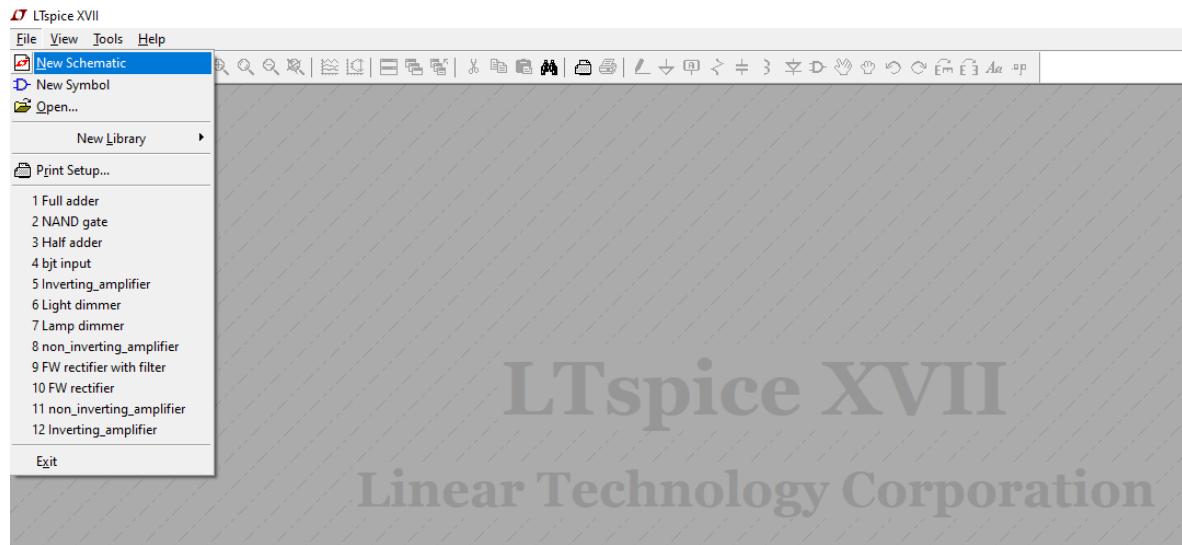


Procedure, Observation Table, and Waveforms:

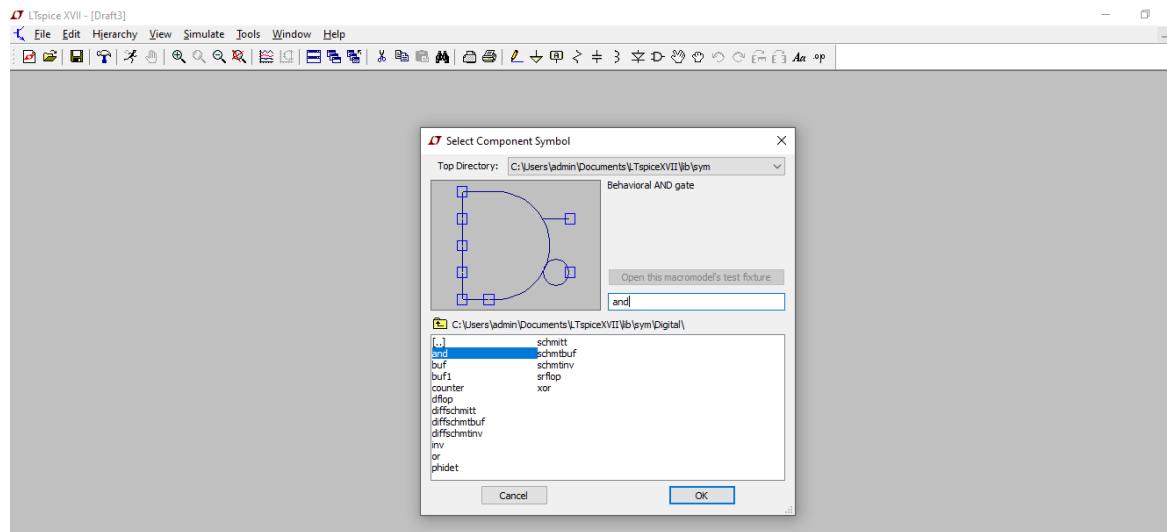
Step 1: Open LTspice software.



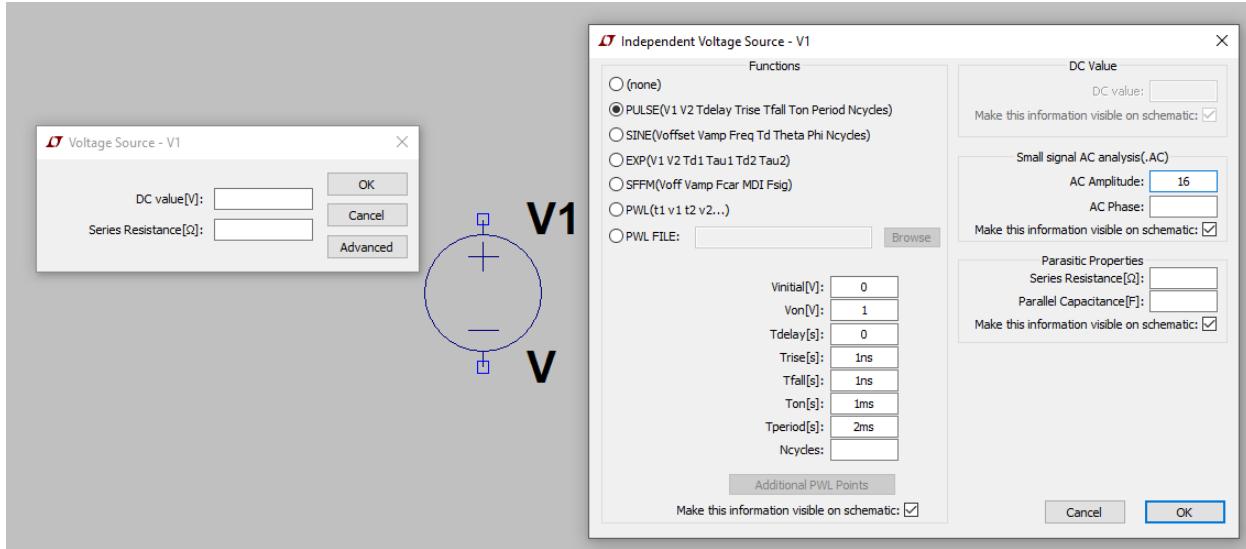
Step 2: Go to File→ New schematic



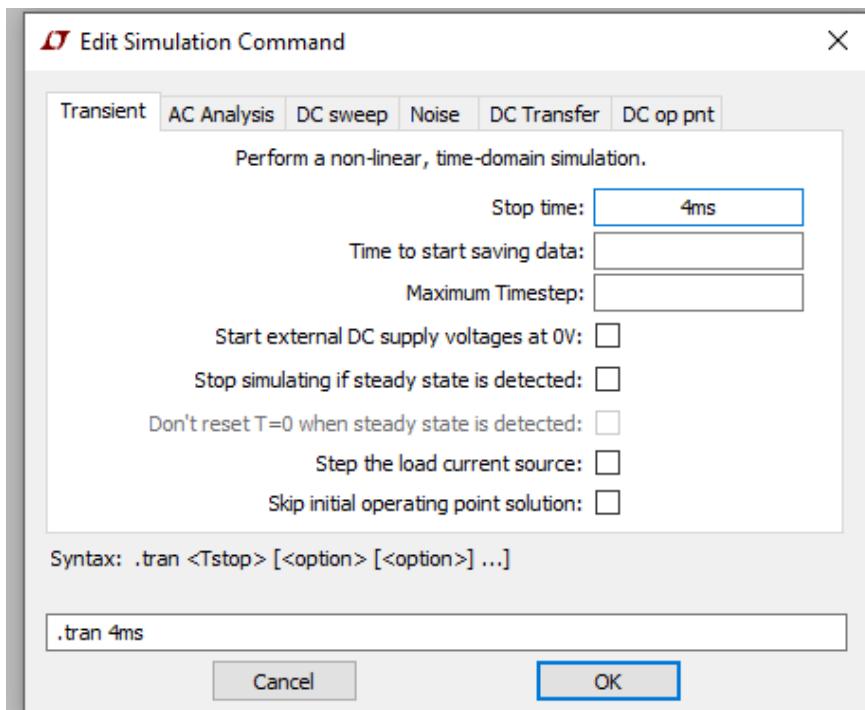
Step 3: Once new schematic file is created, go to component library and choose AND gate as shown below.



Step 4: Similarly, choose the voltage in the library and press the advanced option. Choose pulse and enter the given values as shown in the figure.

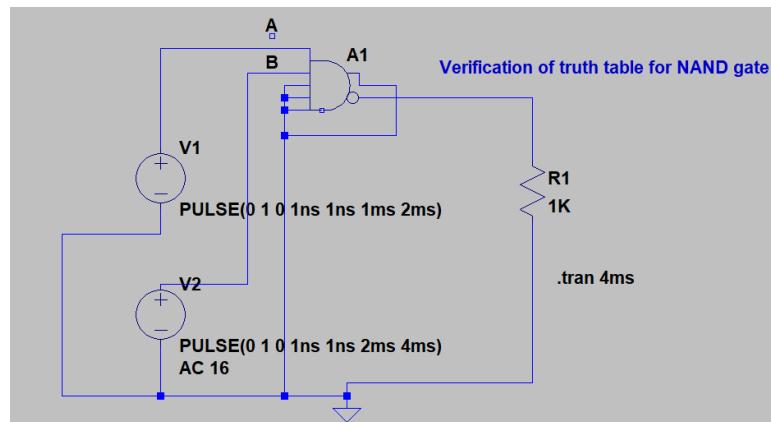


Step 5: Choose resistor, ground, and make connections using wire.
Then go to the simulation icon in the toolbar and choose edit simulation command. Give the stop time of the simulation.



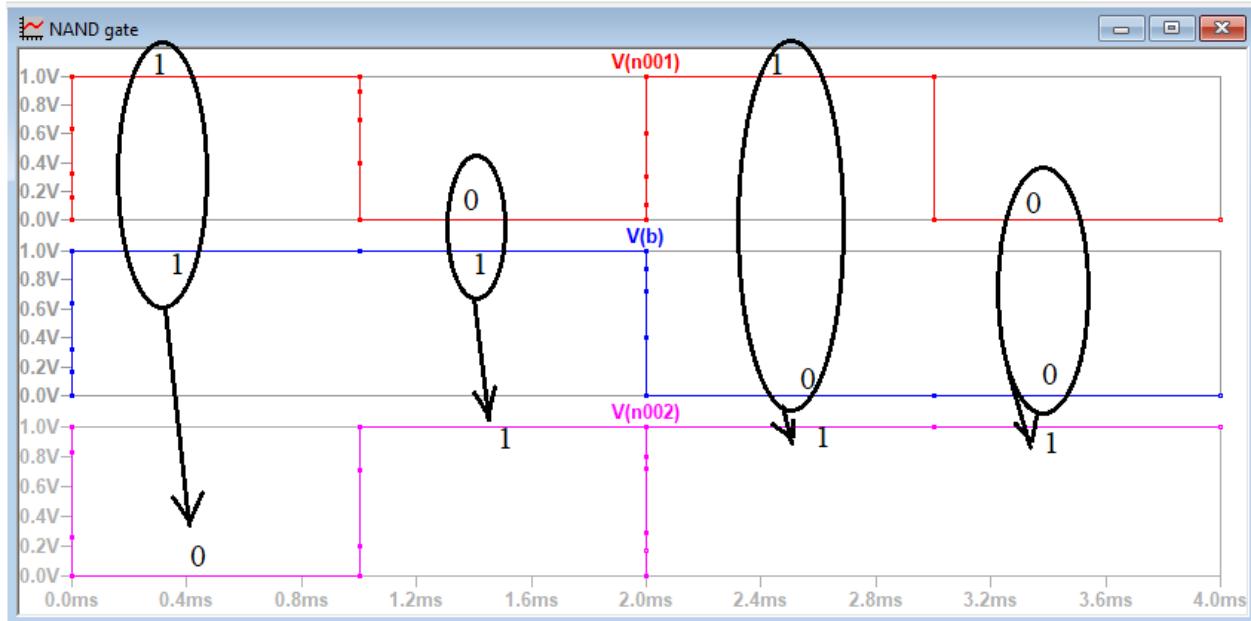
Step 6: For the AND gate element, if the output is directly taken, it will give you AND logic. Otherwise, if the output is taken from the inverted element (with a circle), it is the NAND logic as shown in figure.

NAND gate



Step 7: After giving the simulation command, run the file. And find the graph results by placing the cursor at the terminals of the inputs A, B and the output terminal.

A input- $V(001)$, B input $-V(b)$ and the output- $V(002)$.

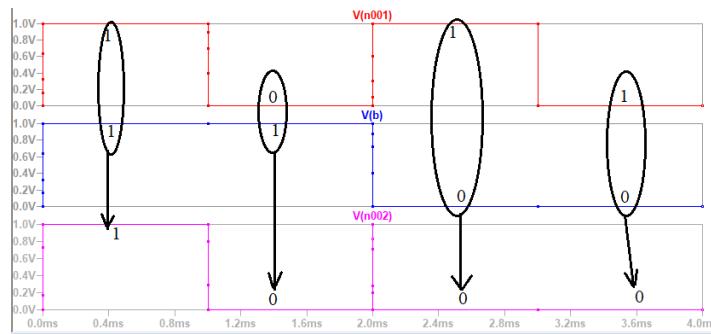
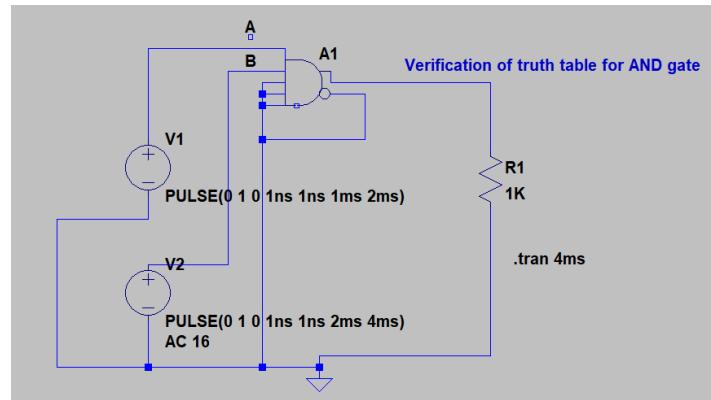


Step 8: We can observe that the results are matched with the truth table as shown below.

Input A	Input B	Output
0	0	1
0	1	1
1	0	1
1	1	0

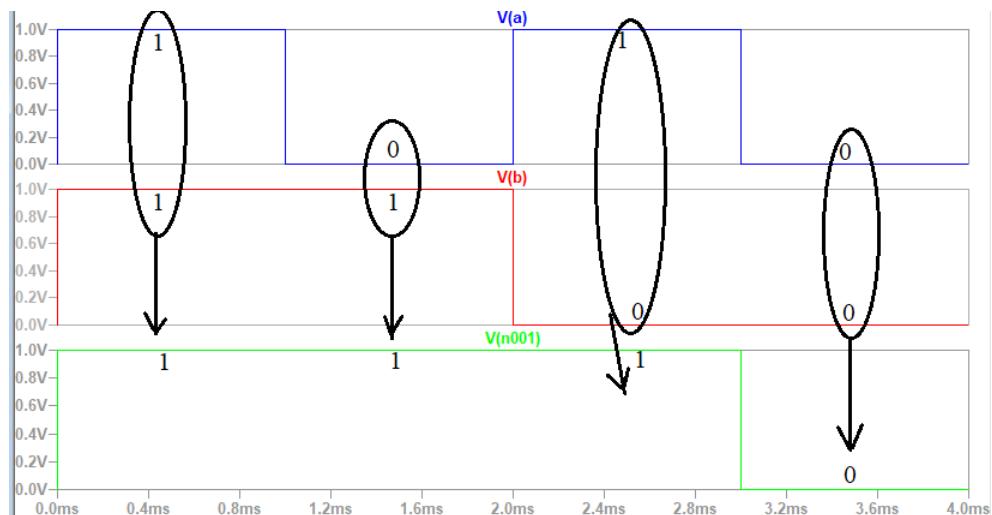
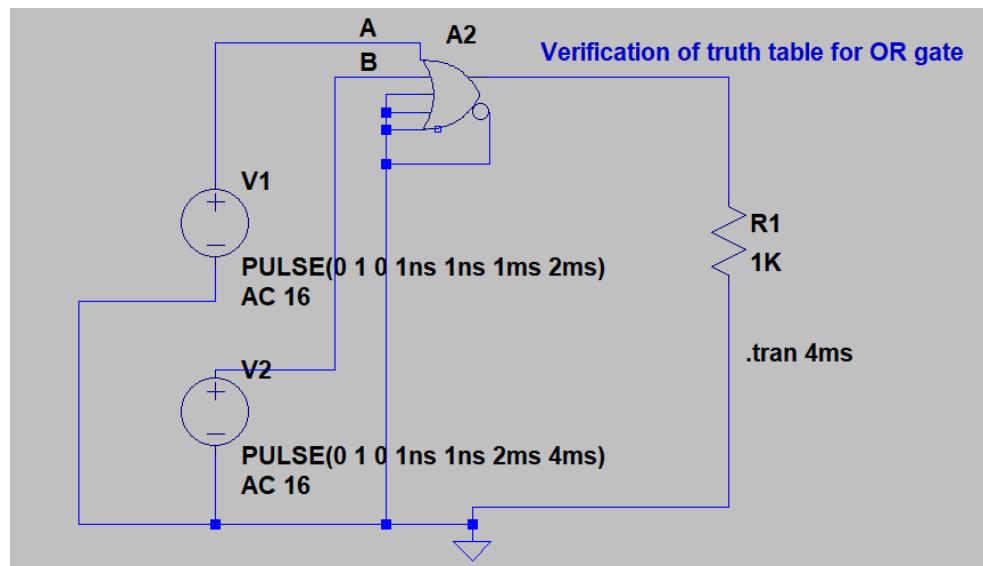
Step 9: In similar way, we can obtain the results for the remaining logic gates as shown below.

AND gate



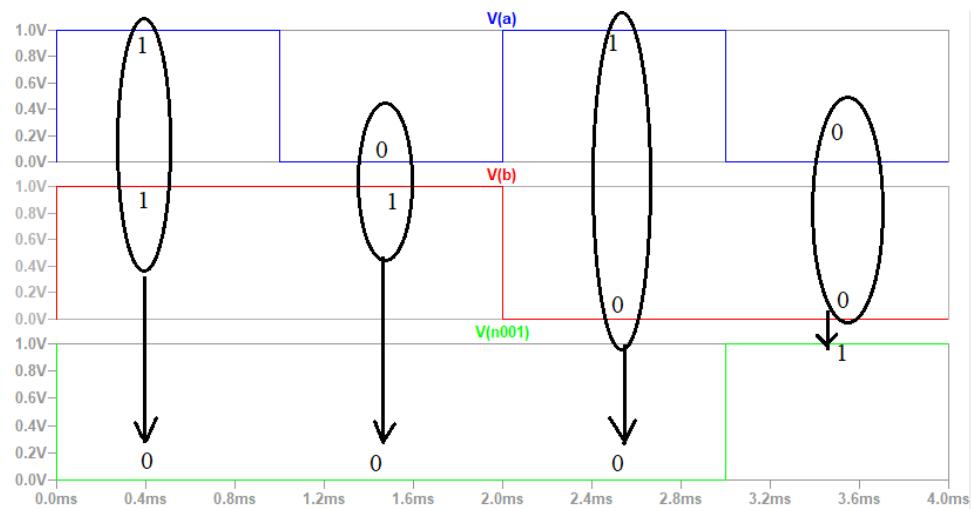
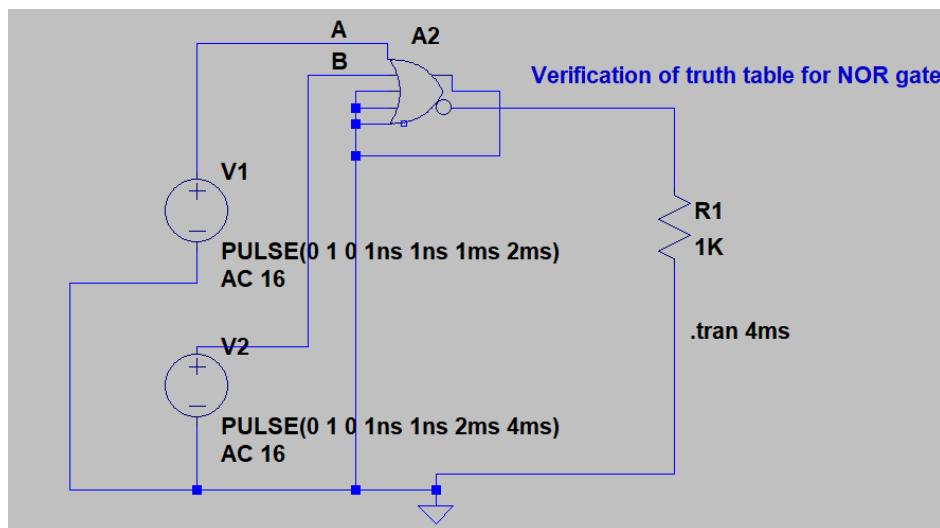
Input A	Input B	Output
0	0	0
0	1	0
1	0	0
1	1	1

OR gate



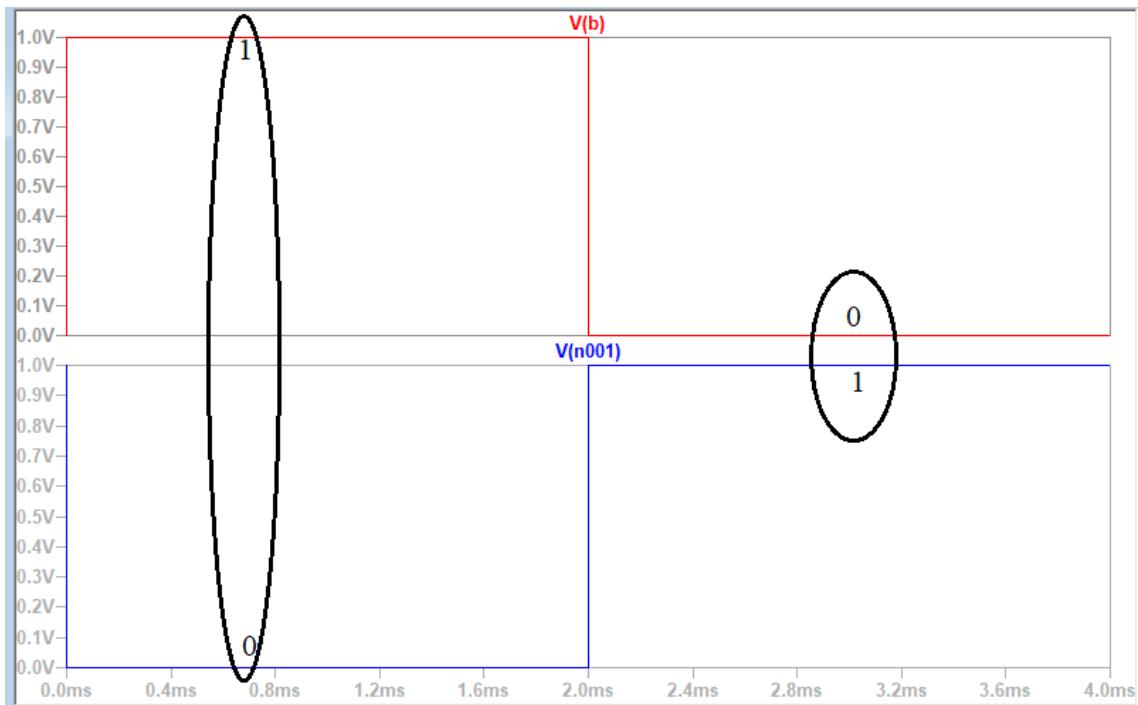
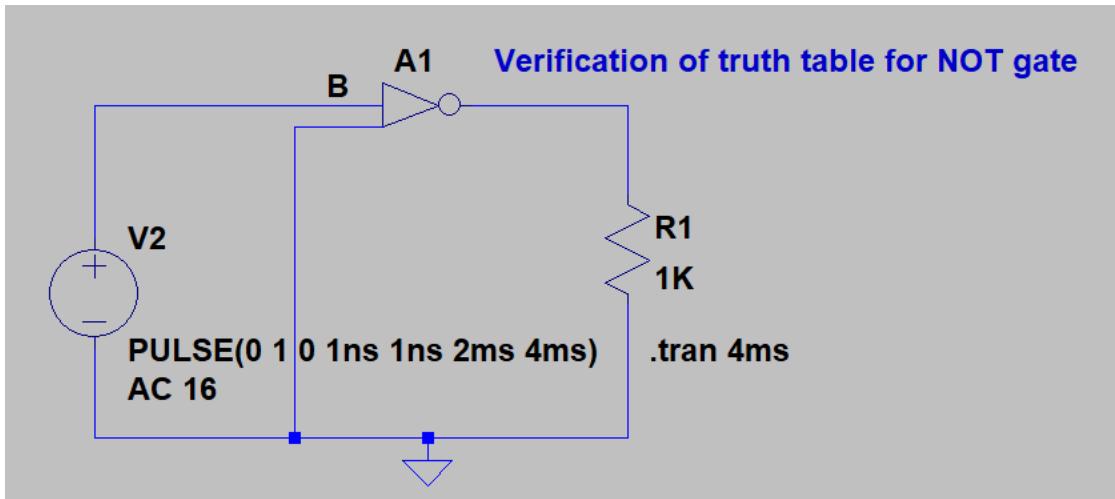
Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	1

NOR gate



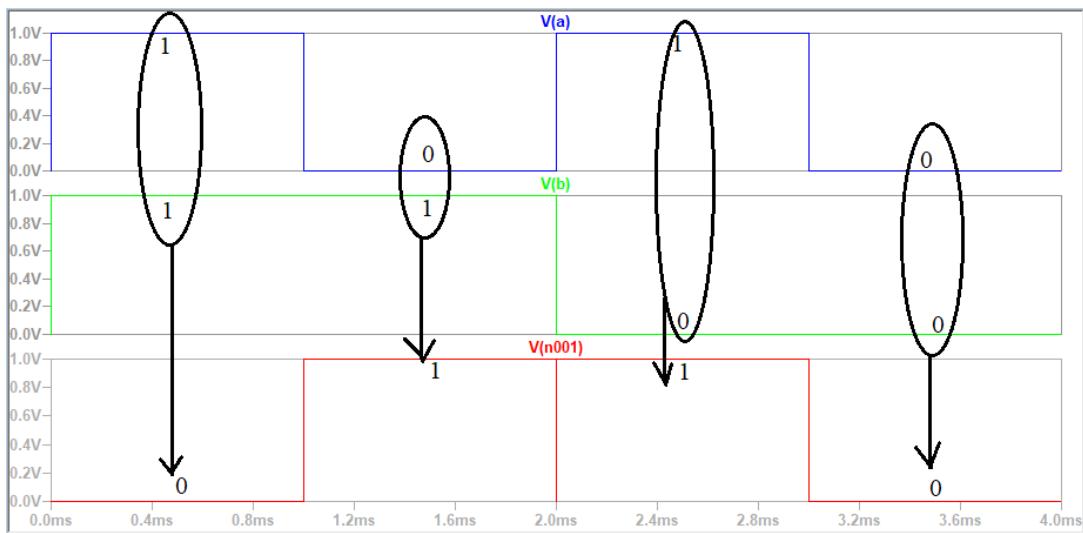
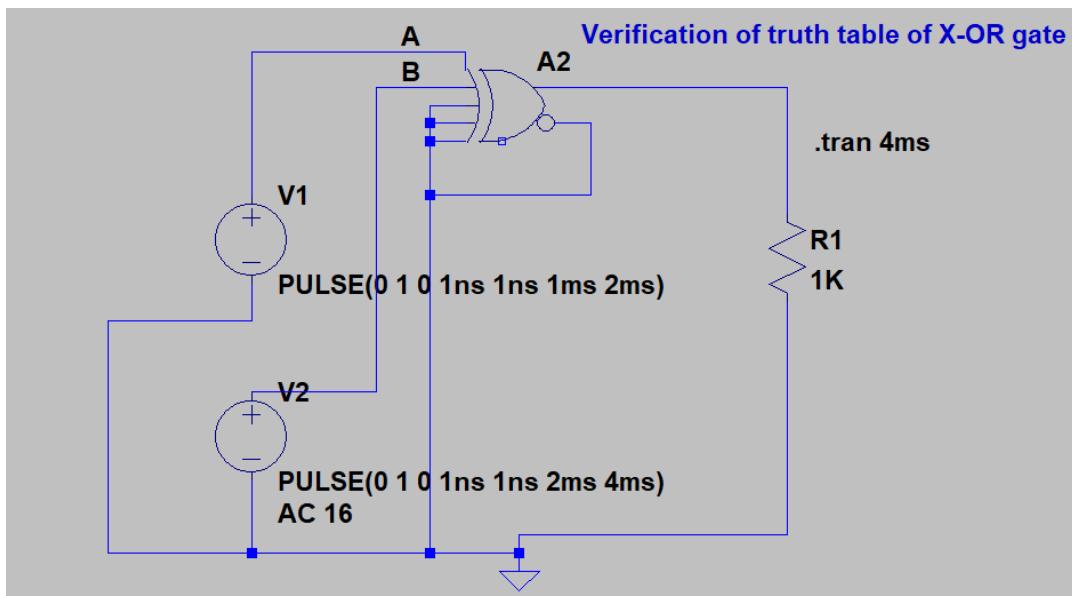
Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	0

NOT gate



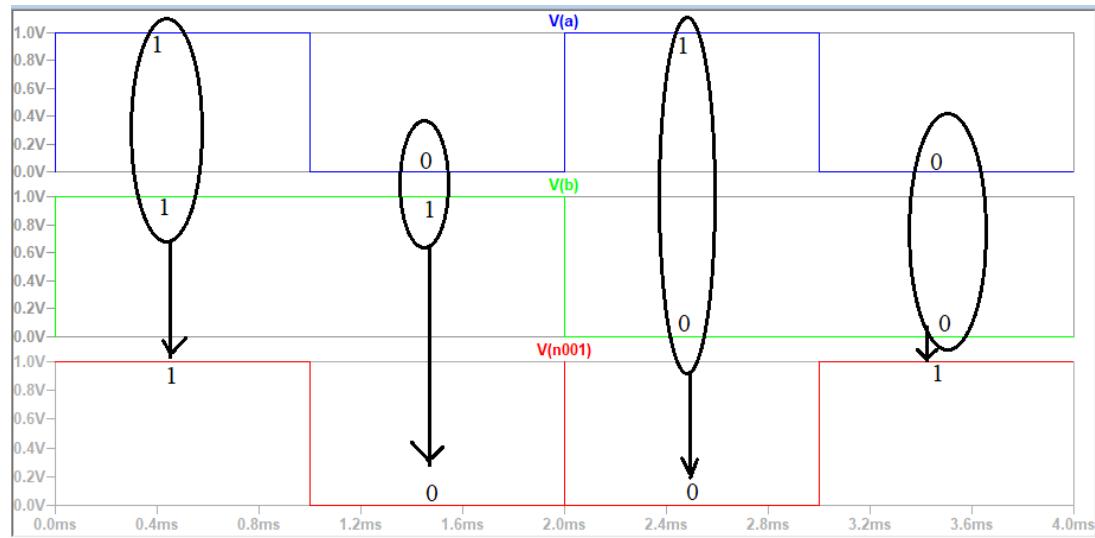
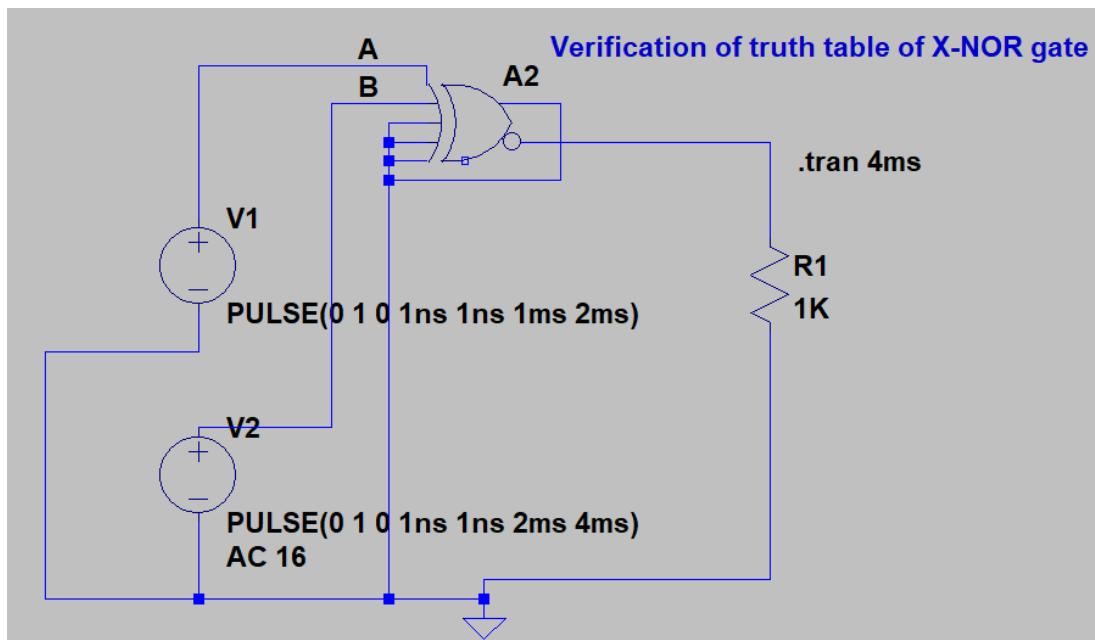
Input A	Output
0	1
1	0

X-OR gate



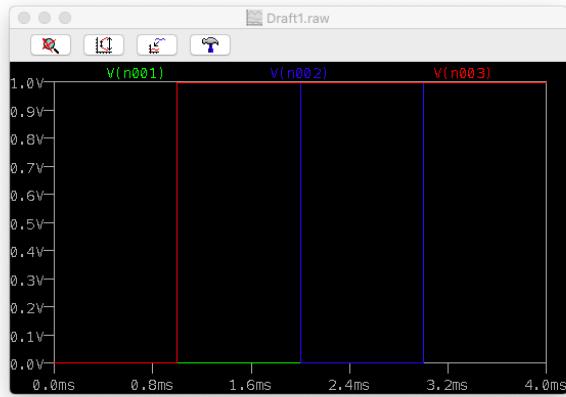
Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	0

X-NOR gate



Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	1

OR



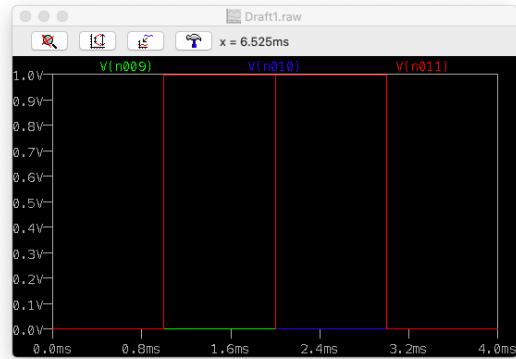
AND



NOT



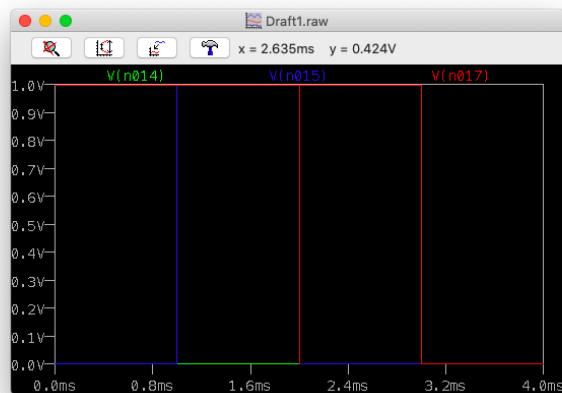
XOR



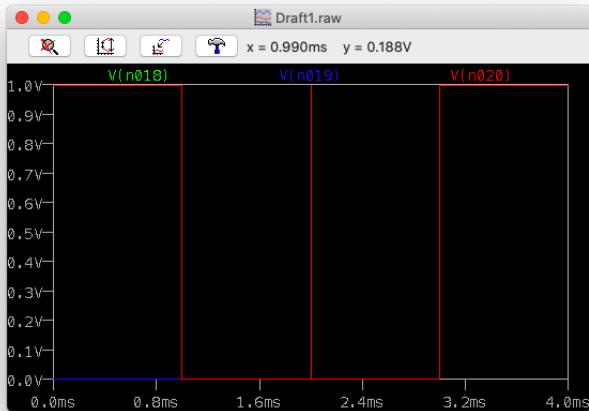
NOR



NAND



XNOR



Results and Inferences:

Thus, the circuit connections for various gates are constructed using LTspice software and its truth table for all the logic gates are verified with obtained waveforms.

Practical Applications

1. In hospitals, babies sometimes need to be kept warm in incubators for a period of time after birth. Design a system that will sound an alarm if the incubator gets too cold.

Solution: Input(s): Thermistor

Output: Buzzer

Process: Inverter

The Thermistor will send a positive result when it is warm, we want a positive result when it is cold...thus the solution would be to 'reverse' the default output of the Thermistor so that the buzzer will turn 'on' when the Thermistor 'reads' cold.

2. Ornithology deals with the study of birds. When photographing these creatures, one needs to be very careful not to scare them. Design a remote

camera shutter release that will be activated when the birds land on a feeding table. The camera should only work during daylight hours.

Solution: Input(s): Photocell and Push Button Switch

Output: Camera

Process: 'AND' Gate

Photocell	Push Button Switch	'AND' Gate results	'Or' Gate Results	'XOR' Gate results	What I want
No light(0)	On (1)	Off	On (wrong answer)	On (wrong answer)	Off
No light (0)	Off (0)	Off	Off	Off	Off
Light (1)	On (1)	On	On	Off (wrong answer)	On
Light (1)	Off (0)	Off	On (wrong answer)	On (wrong answer)	Off

Course Outcome

CO4: Design and implement various digital circuits

Student Learning Outcomes (SLO):

SLO9. Having problem solving ability- solving social issues and engineering problems

Design of Arithmetic Logic Circuit using IC's-Half Adder

(Data Processing in Micro-controller Applications)

Aim:

To design, simulate, and verify a half adder used in the Arithmetic logic circuit, using ICs.

Software required:

LTspice software

Theory:

Adders form a core component of the Arithmetic Logic Unit (ALU) and play a major role in calculating memory addresses, table indices, etc.

A half adder is the simplest digital adder. It is a combinational circuit that performs the addition of two binary digits. It takes in two input bits, A (addend) and B (augend), and produces two output bits, the sum, and the carry. The truth table for adding two binary digits A and B is shown below:

Truth Table for Half Adder:

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

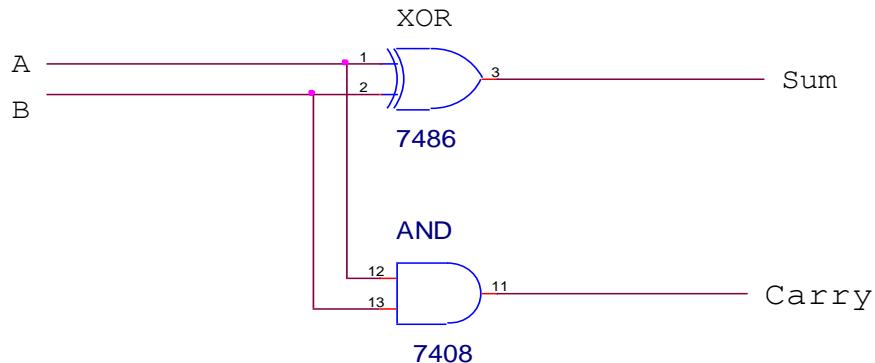
The simplified Boolean functions from the truth table are:

$$\text{SUM} = \bar{A}B + A\bar{B}$$

$$\text{CARRY} = AB$$

Boolean expressions can be implemented in different ways. Below example shows the implementation of Half Adder using EX-OR and AND logic gates:

Implementation of Half Adder using EX-OR and AND logic gates

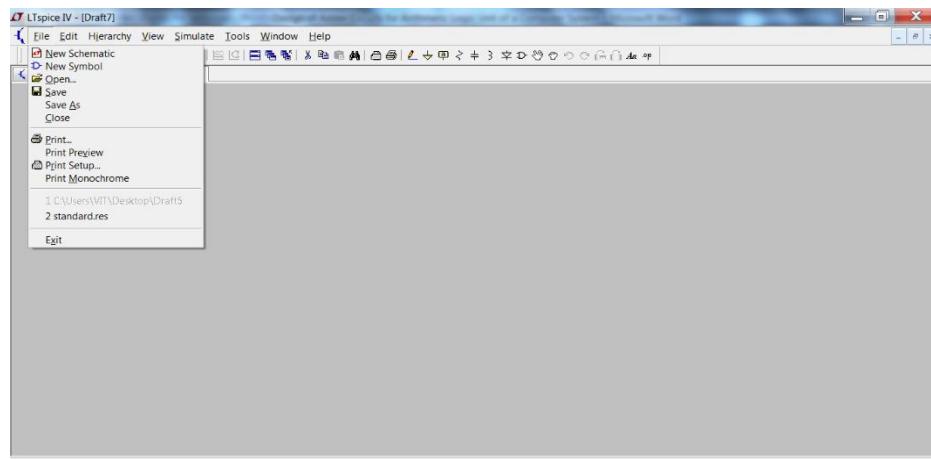


Note: can try alternative ways to implement a Half Adder by

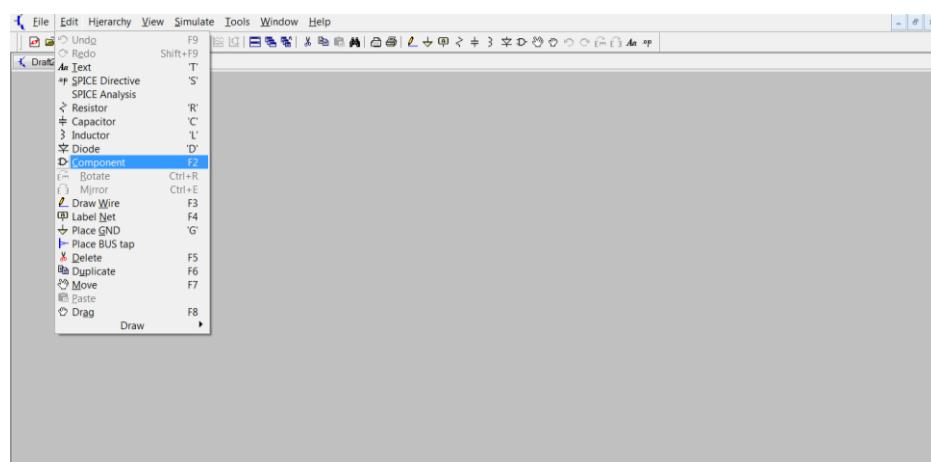
- a) Using AND-NOR-NOR configuration
- b) Using only AND, OR, and NOT logic

Procedure

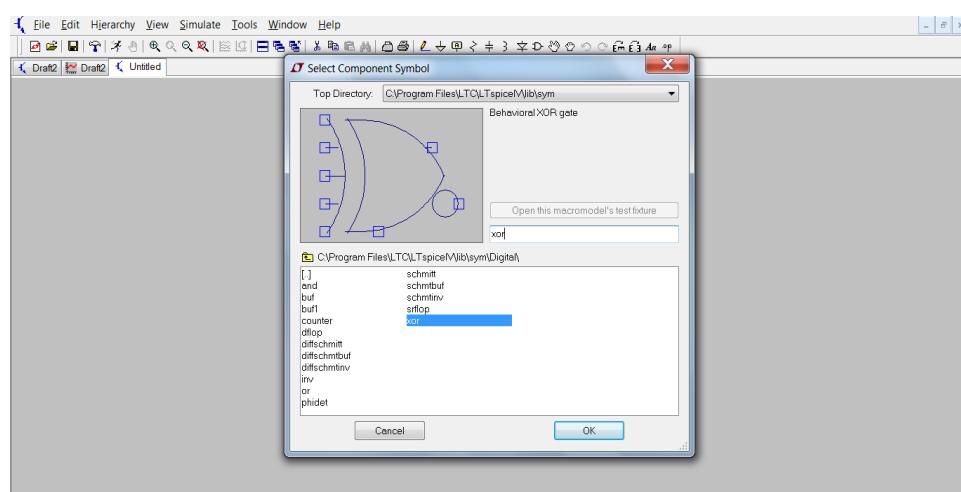
- 1) Open LTspice. Go to File – New Schematic.

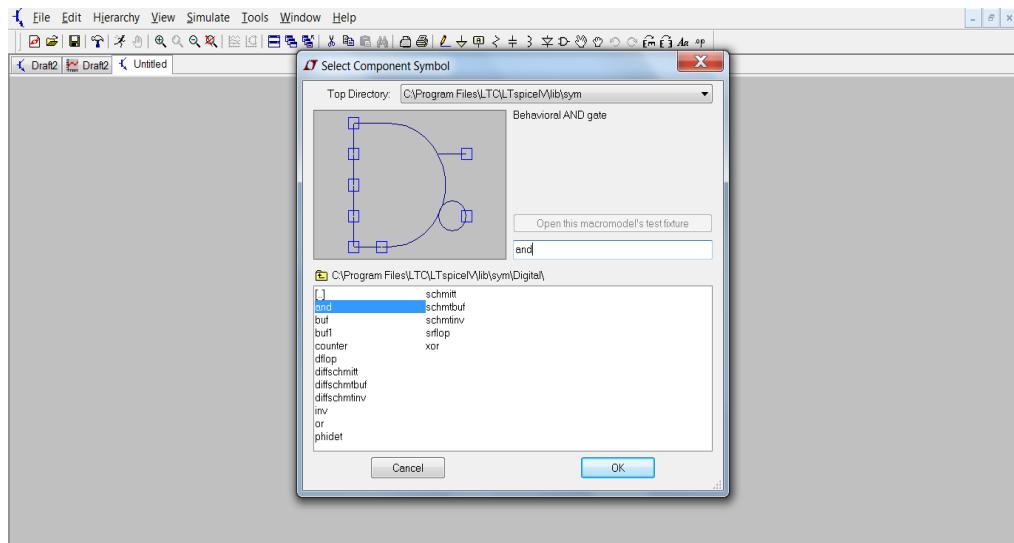


2) On the File Menu, click on Edit – Component.

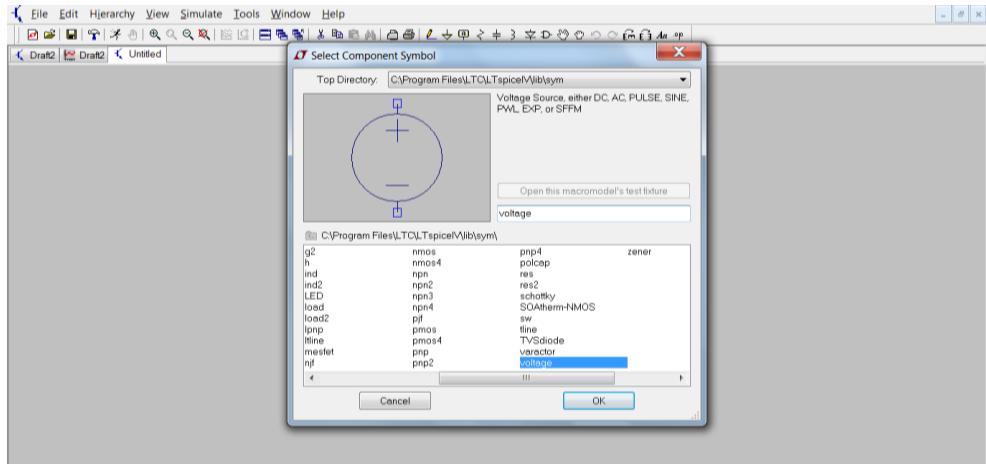


3) Place XOR gate, AND gate, two resistors, and ground on to schematic.

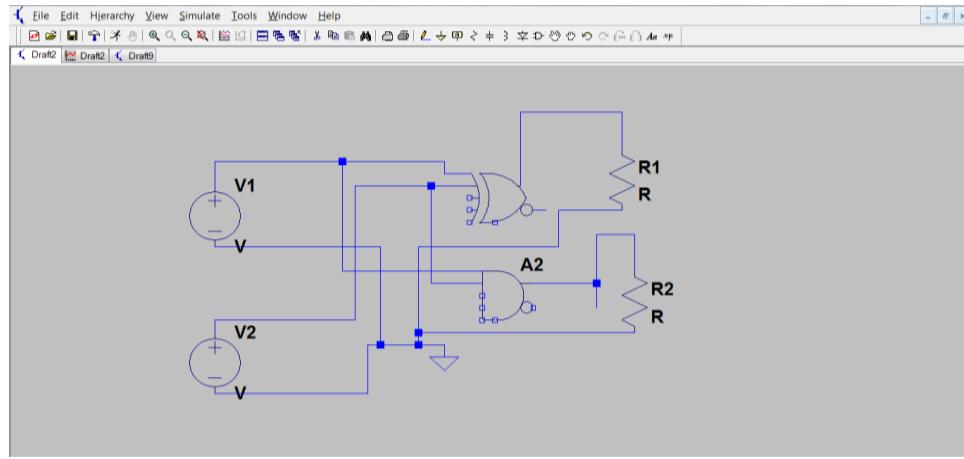




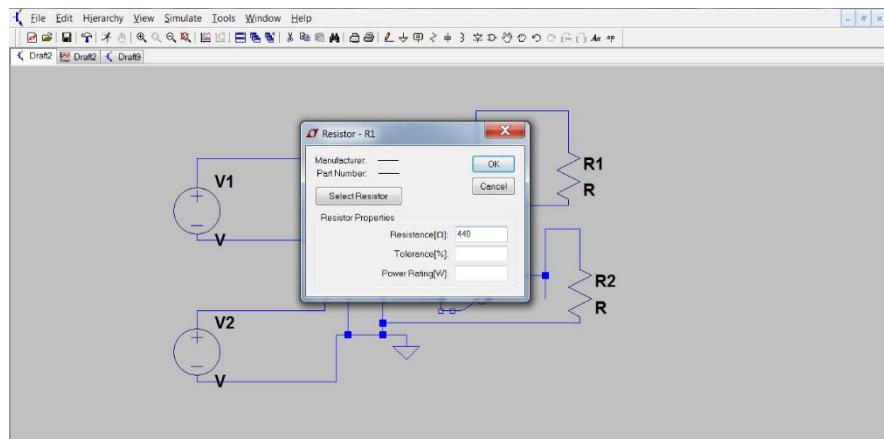
- 4) Place two voltage sources for the two inputs on the schematic.



- 5) Make necessary connections as per the circuit diagram. The first resistance is connected to the XOR output. The second resistance is connected to the AND gate output. Common terminal of both resistances are to be grounded. Voltage source 1 – positive terminal acts as 1st input, the other terminal is to be grounded; Voltage source 2 – positive terminal acts as 2nd input, the other terminal is to be grounded.



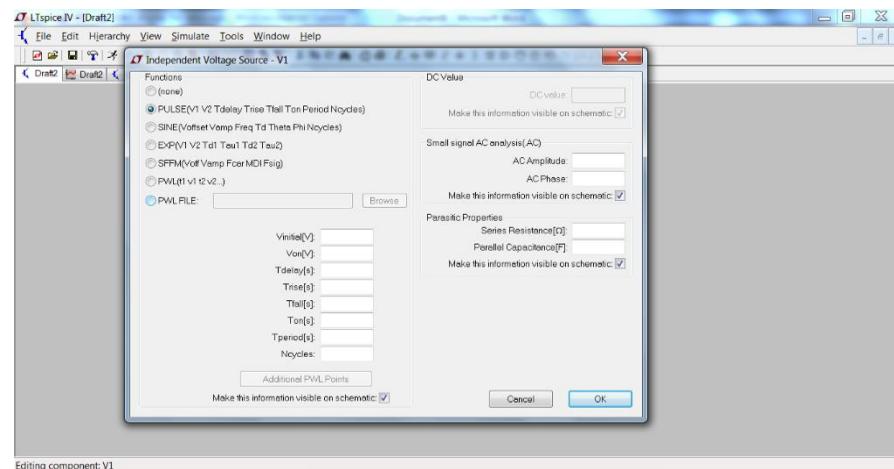
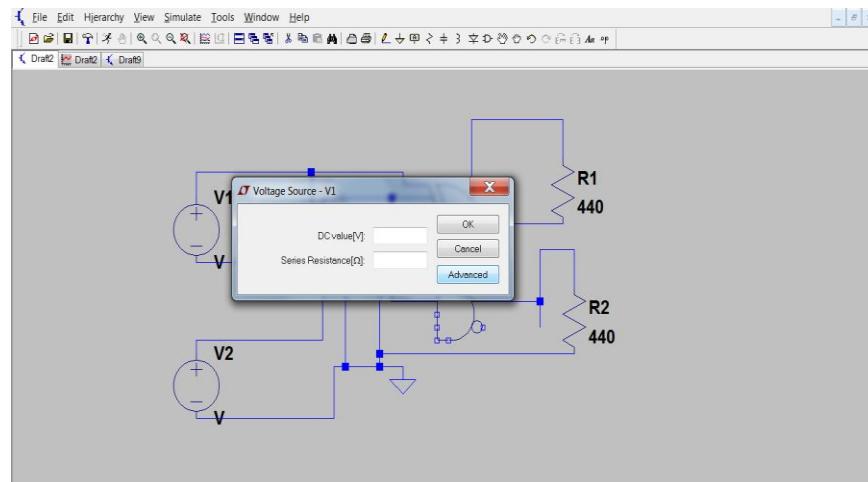
- 6) Right-click on the resistance and change its value to 440Ω . Repeat the step for the other resistance also.



- 7) Provide input to the XOR gate. Right click on the first voltage source.

Select PULSE (V1 V2 Tdelay Trise Tfall Ton Period Ncycles).

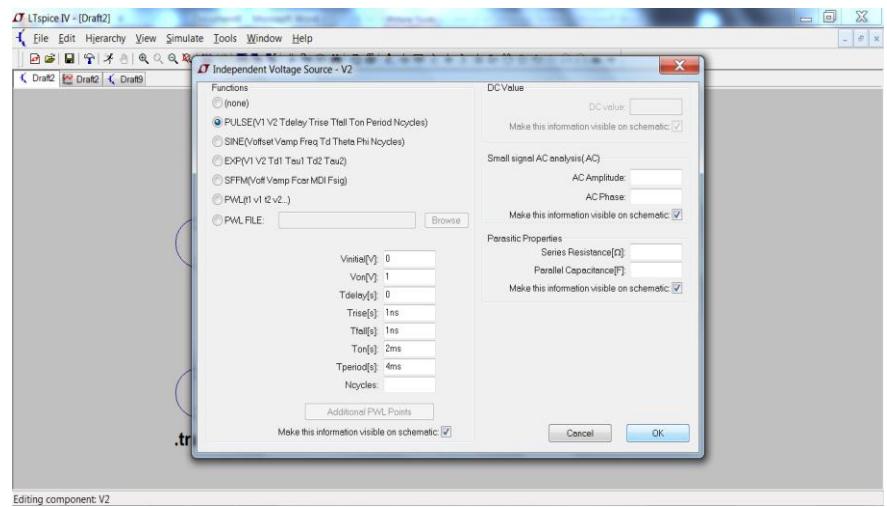
Set the values as (0, 1, 0, 1ns, 1ns, 1ms, 2 ms).



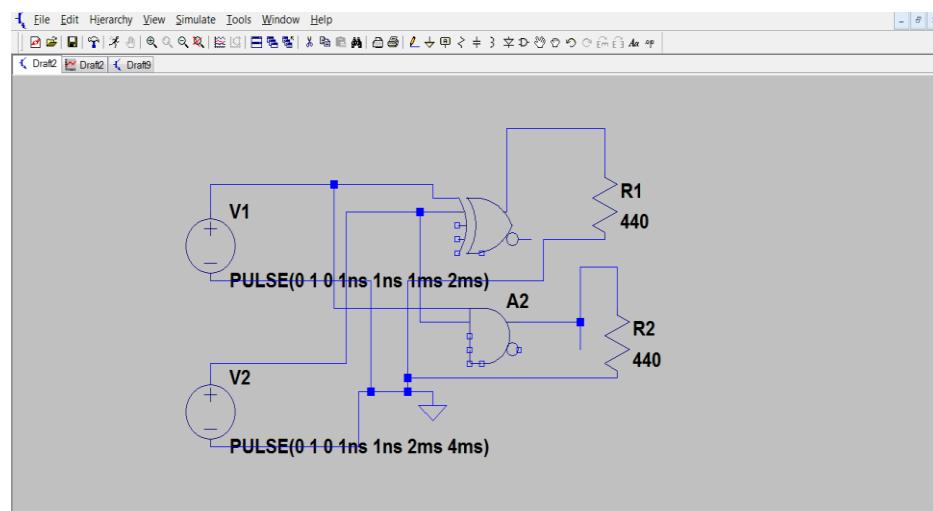
- 8) Provide input to the AND gate. Right-click on the first voltage source.

Select PULSE (V1 V2 Tdelay Trise Tfall Ton Period Ncycles).

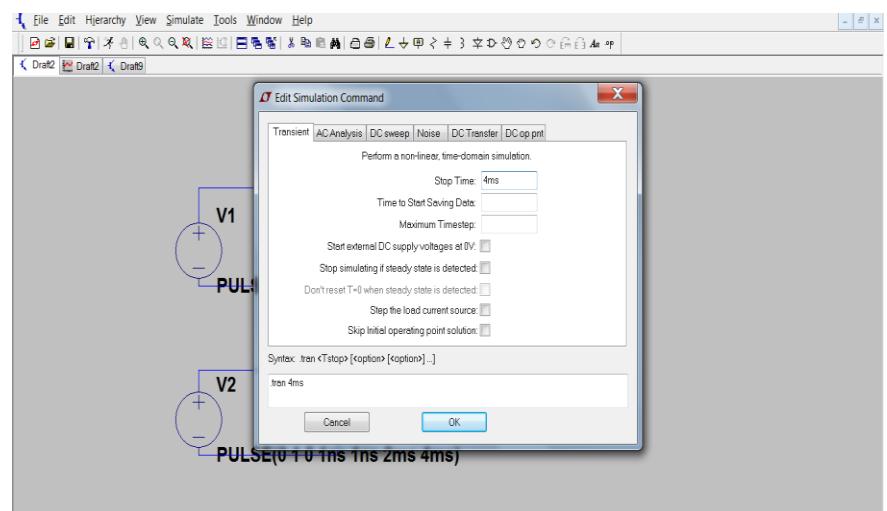
Set the values as (0, 1, 0, 1ns, 1ns, 2ms, 4ms).



Editing component: V2



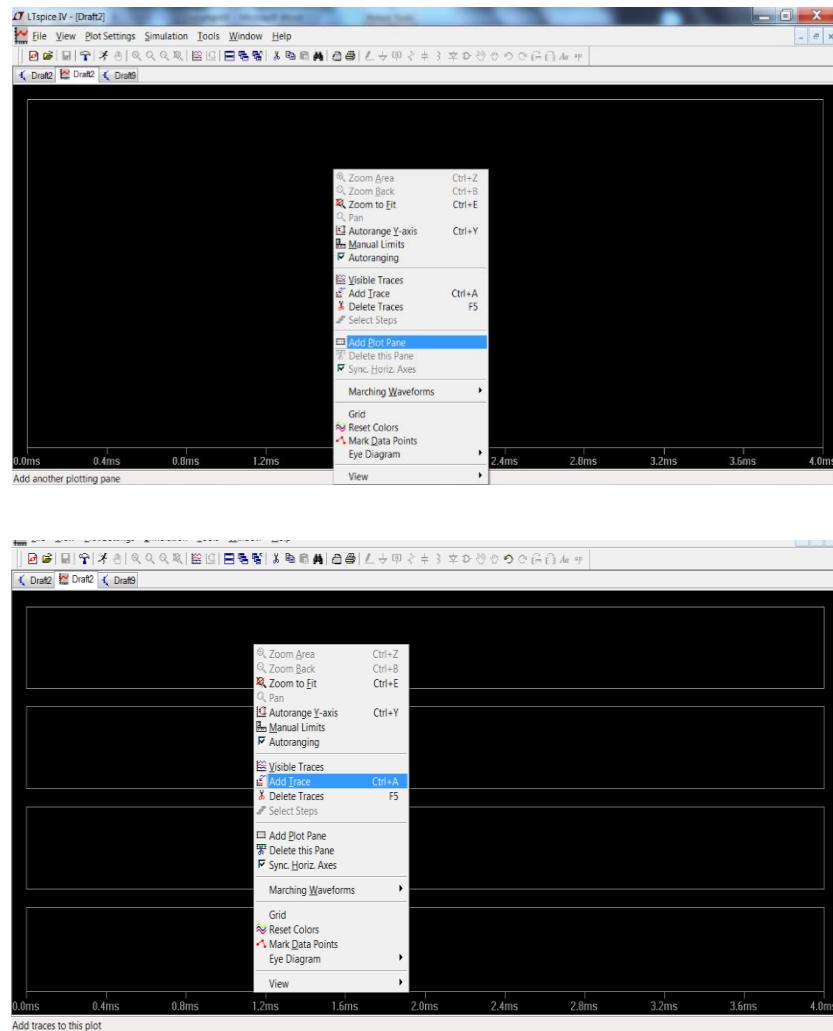
9) Go to Edit – SPICE analysis. Set the stop time to 4 ms



- 10) Run the simulation (run symbol on menu bar).
- 11) To view the results, right click – Add Plot Pane (add 4 plot panes to view the two inputs, sum and carry).

For each pane, right click – Add Trace – Select V(<<respective node>>).

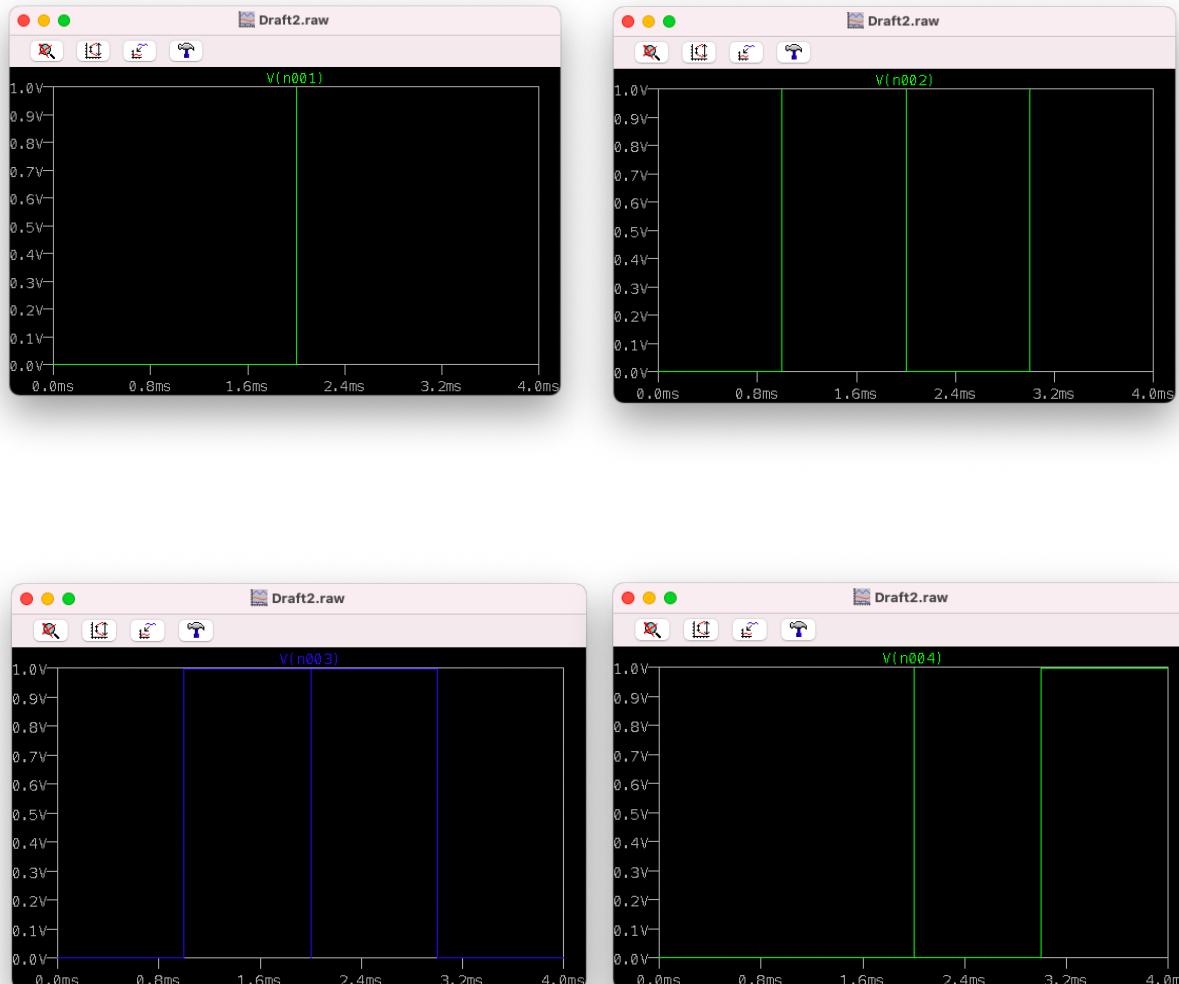
(nodes correspond to input 1, input 2, sum and carry)



- 12) Observe the waveforms and verify the truth table.



GRAPHS :



Results and Inferences:

Thus, a half adder circuit to implement addition operation in the ALU circuit using Exclusive-OR and AND gates is designed and implemented.

Practical Applications:

Data processing in micro-controller.

Course Outcome:

CO4. Design and implement various digital circuits

Student Learning Outcomes (SLO):

SLO2. Having a clear understanding of the subject related concepts and of contemporary issues

Design of arithmetic logic circuit using IC's Full adder

(Data processing in Micro-controller based applications)

Aim:

To design and verify the truth table of the Full Adder circuit using Integrated Circuits (ICs) with the open-source software LTSPICE

Components Used in Simulation:

S. No.	Name of the Apparatus	Range	Quantity
1.	LTSpice XVII Software	-	-
2.	AND gate	IC 7408	3
3.	OR gate	IC 7432	1
4.	EX-OR gate	IC 7486	2
5.	Connecting wires	-	-

Theory:

A	B	SUM (S)	CARRY (C)
0	0	0	0
0	1	1	0
1	0	1	0

1	1	0	1
---	---	---	---

Consider the problem of adding two single-bit numbers, A and B, resulting in a single two-bit answer. The truth table for this operation is shown above.

The two output functions are labeled ‘C’ and ‘S’, where ‘S’ stands for ‘sum’ is the low order bit of the output. The ‘C’ stands for ‘carry’, and is the high order bit of the output. The functions for S and C can be written as the two Minimum Sum of Products (MSOP) form as per equations below:

$$C = AB \text{ (A Logical AND with B)}$$

$$S = A'B + AB' \text{ (Logical OR of A-Complement with B and B-complement with A)}$$

A circuit that implements these two functions is known as a half adder. We can build a half adder circuit with one logical AND gate and one Logical OR gate ICs. This adder is referred to as a half adder because it only solves half the general problem of adding numbers with more than one bit. Let's take a look at an example of what happens when we add two 8-bit numbers:

Carry (C)	1 0 1 1 1 0 0 0
Input-1 (A)	1 0 1 1 1 0
	0 1
Input-2 (B)	1 0 1 0 1 1
	0 0
Sum(S)	0 1 1 0 0 1
	0 1

Note that, except for the right most column, we are actually adding three bits: a bit from each of the 2 numbers and a carry bit from the bits immediately to the right. Note also that each addition produces 2 bits - the result bit (S), and the carry bit (C). Now, let's make a truth table for this addition process. The truth table will have three variables, one bit from each of the numbers A and

B, and a carry in bit(C_{in}), which represents the carry from the previous position. The two outputs are the sum bit and the carry out bit (C_{out}), which will be used in the next position.

C_{in}	A	B	SUM (S)	CARRY (C_{out})
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

We'll use Karnaugh maps to simplify the two functions in the table above into MSOP form:

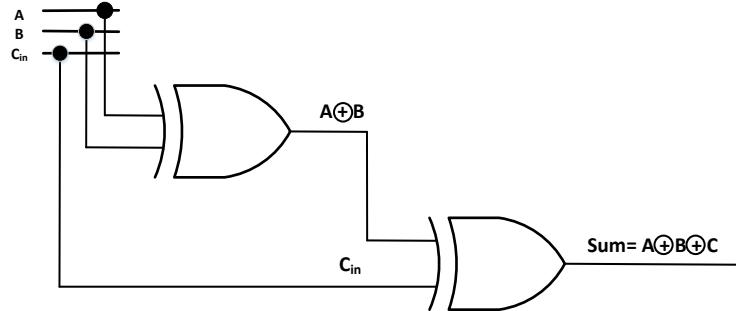
AB		00	01	11	10
C_{in}	0	0	0	1	0
1	0	1	1	1	1
Carry (C_{out}) =					
$A \cdot B + B \cdot C_{in} + C_{in} \cdot A$					

AB		00	01	11	10
C_{in}	0	0	1	0	1
1	1	0	1	1	0
Sum (S) = $A'B'C_{in} + AB'C_{in}' + A'B'C_{in}' + AB'C_{in}$					
= $A \oplus B \oplus C_{in}$					

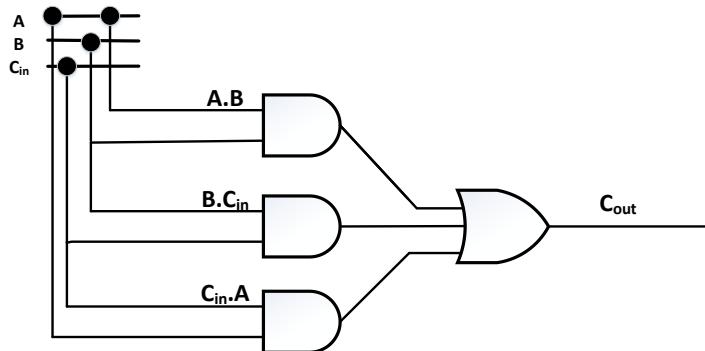
We can implement the function for $Carry(C_{out})$ and $Sum (S)$ in a straightforward manner, as shown below in logical circuit diagram.

Logical Diagram and Truth Table

1. Logical Diagram for Realizing a Sum:



2. Logical Diagram for Realizing a Carry:

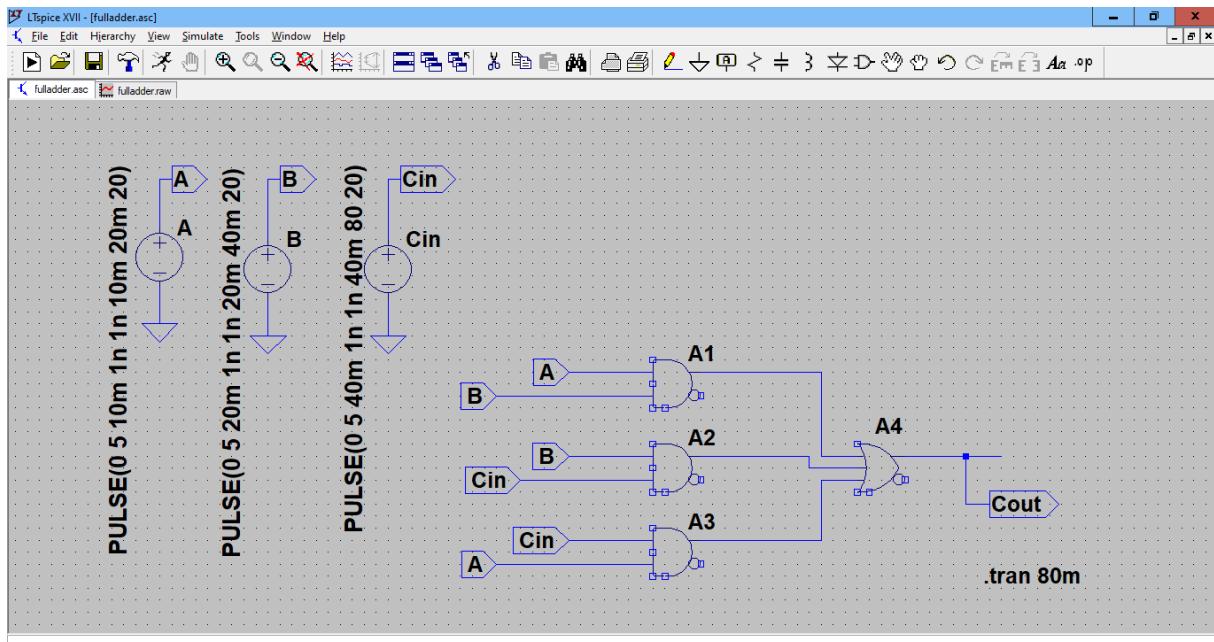


3. Observation Truth Table of Full adder:

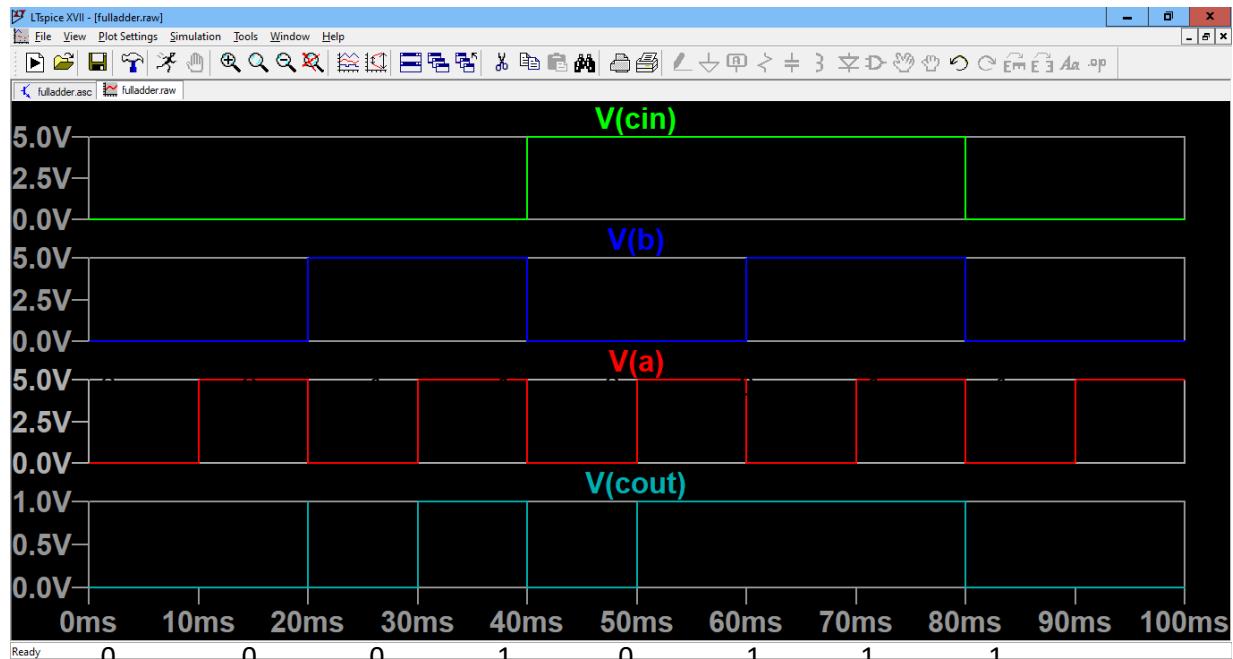
C_{in}	A	B	SUM (S)	CARRY (C_{out})
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

LTSPICE diagram and Waveforms

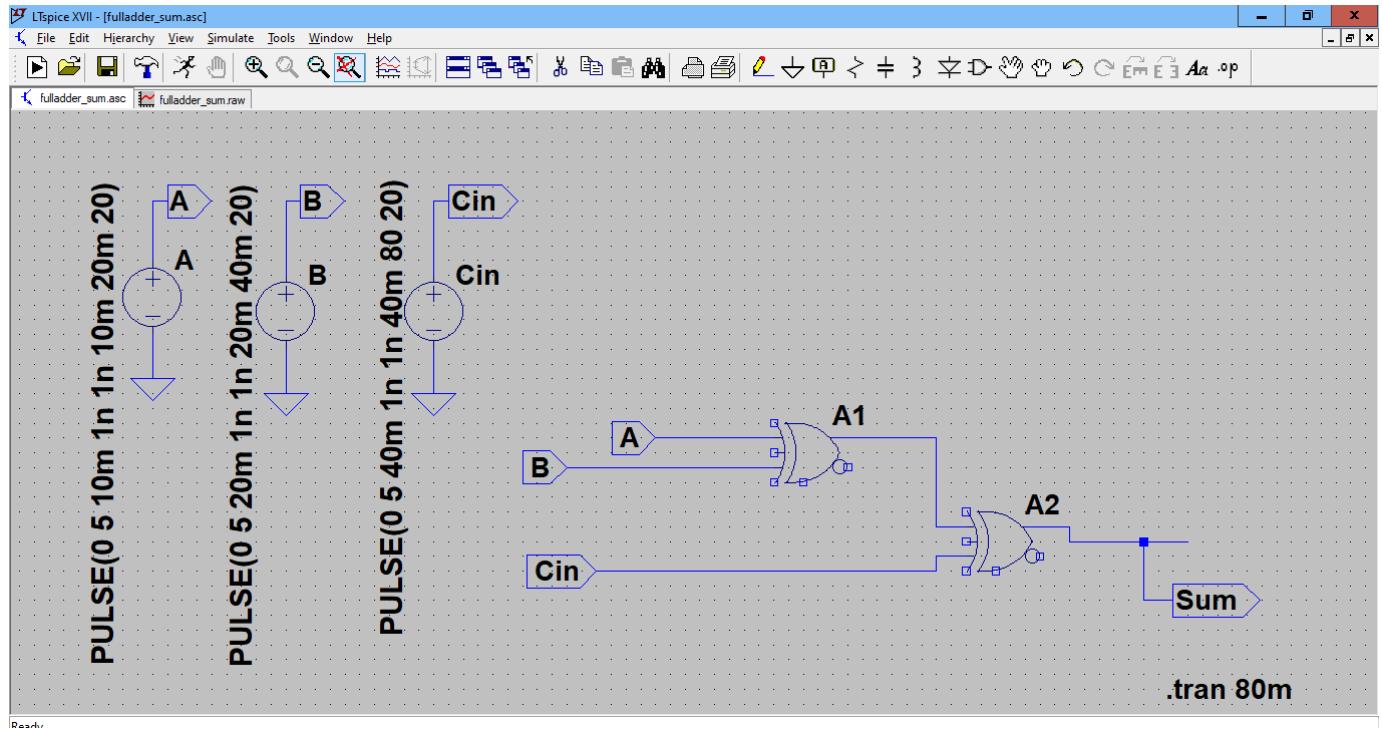
4. LTSPICE Window to realize C_{out}



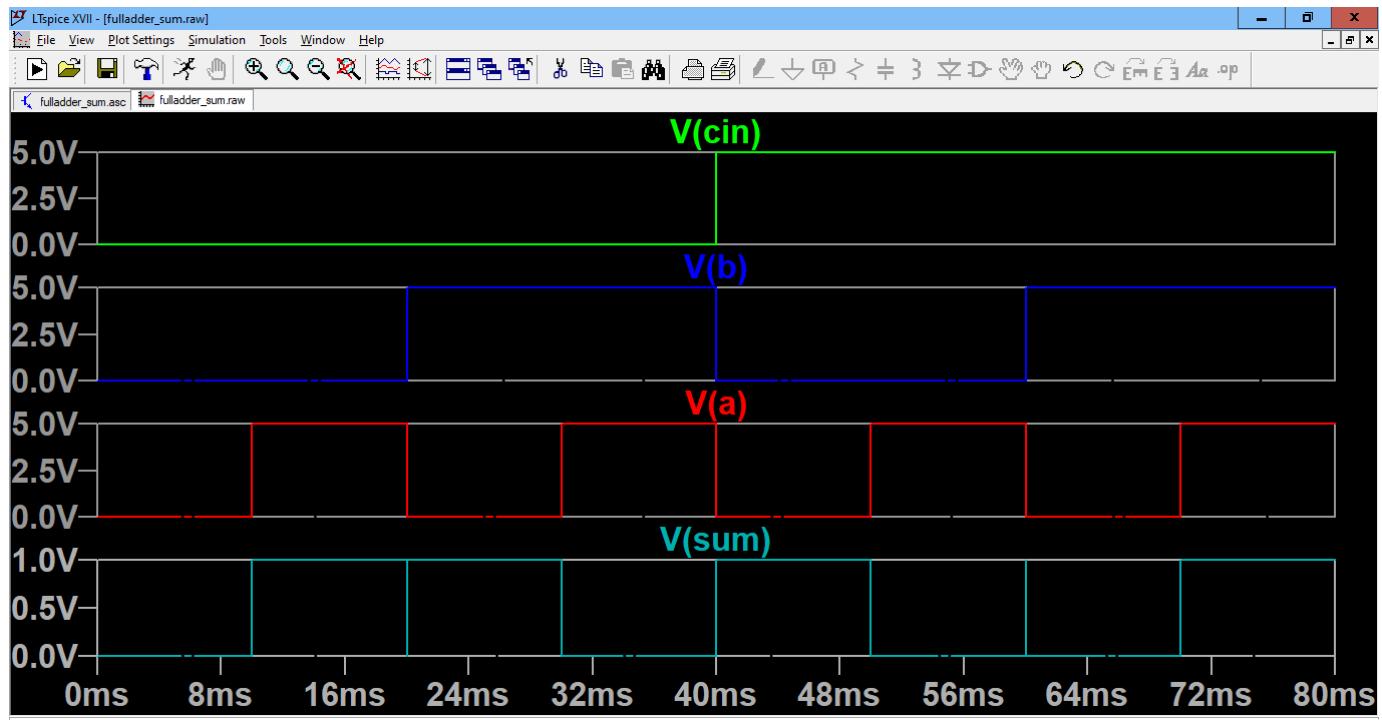
5. LTSPICE Window to realize C_{out} waveform.



6. LTSPICE Window to realize Sum(S)

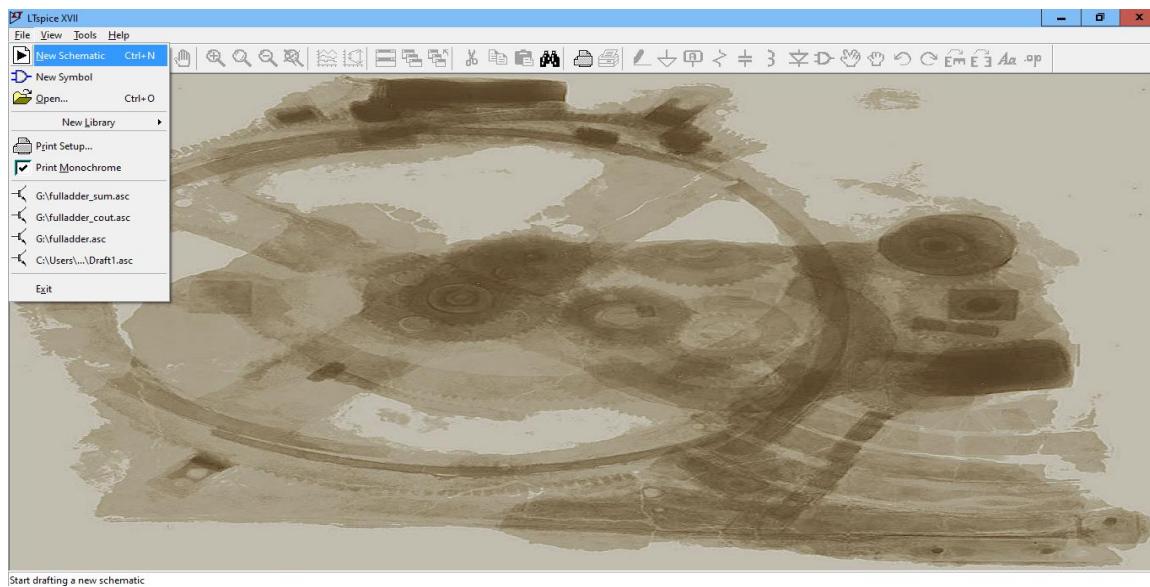


7. LTSPICE Window to realize Sum waveform.

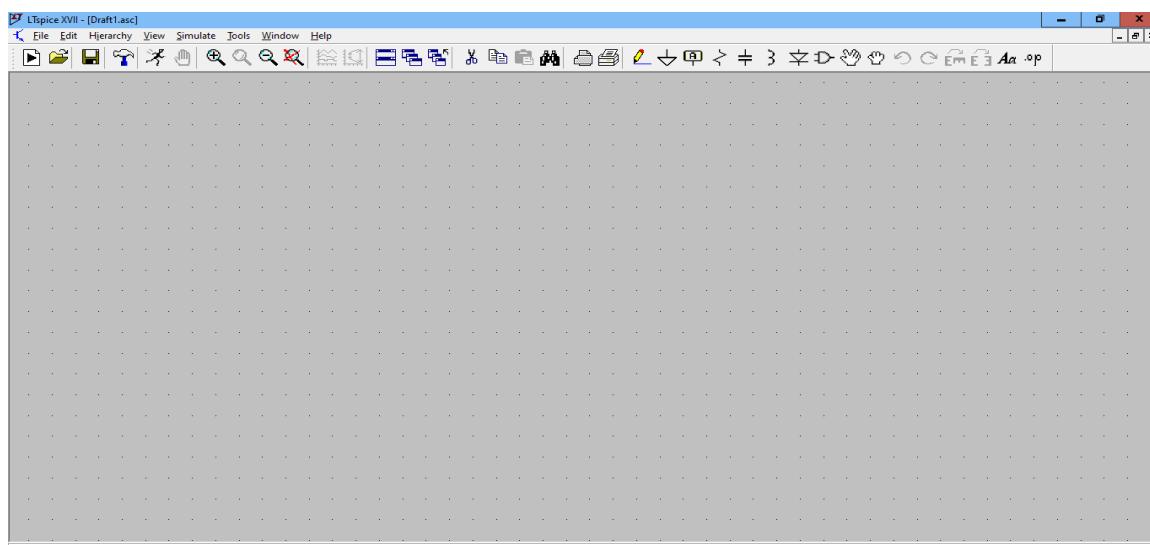


Procedure

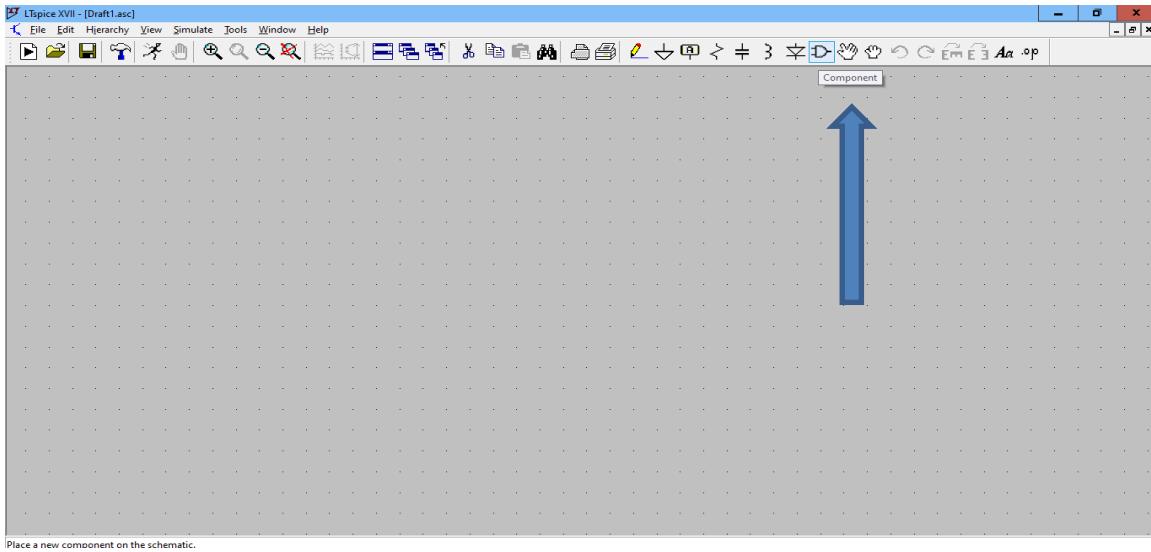
1. Open the LTSPICE .exe to get the new schematic.



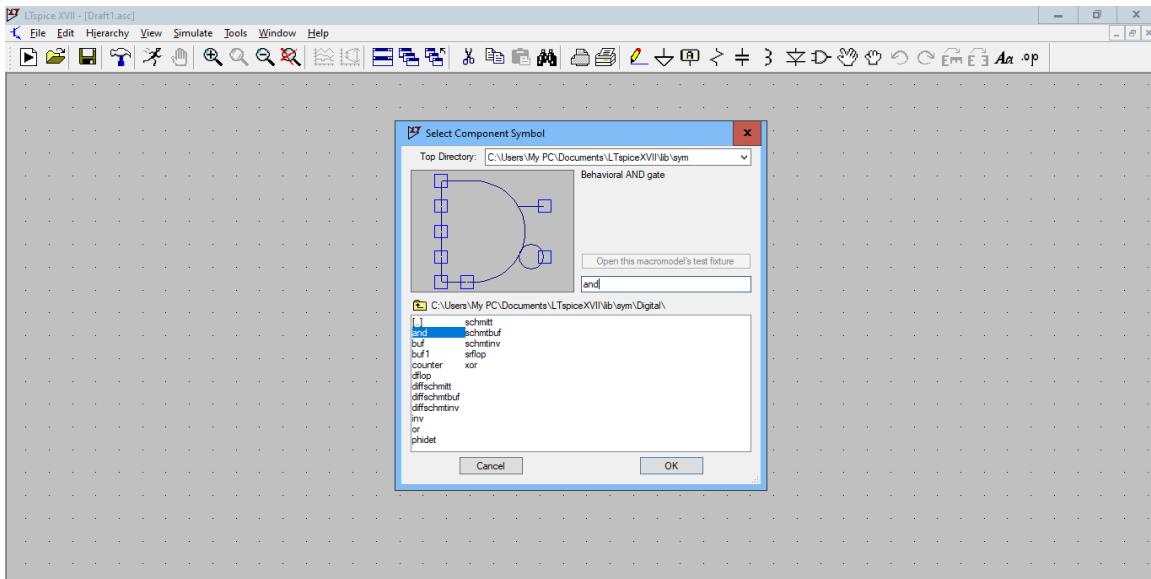
2. A New Draft1.asc schematic is opened



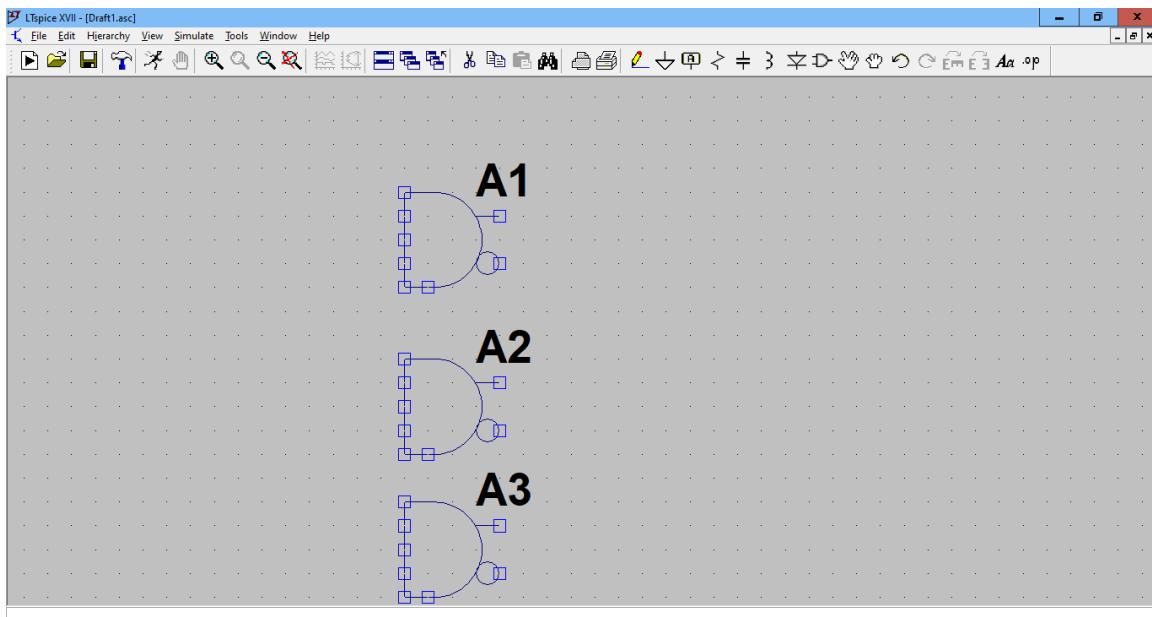
3. Click the component Menu



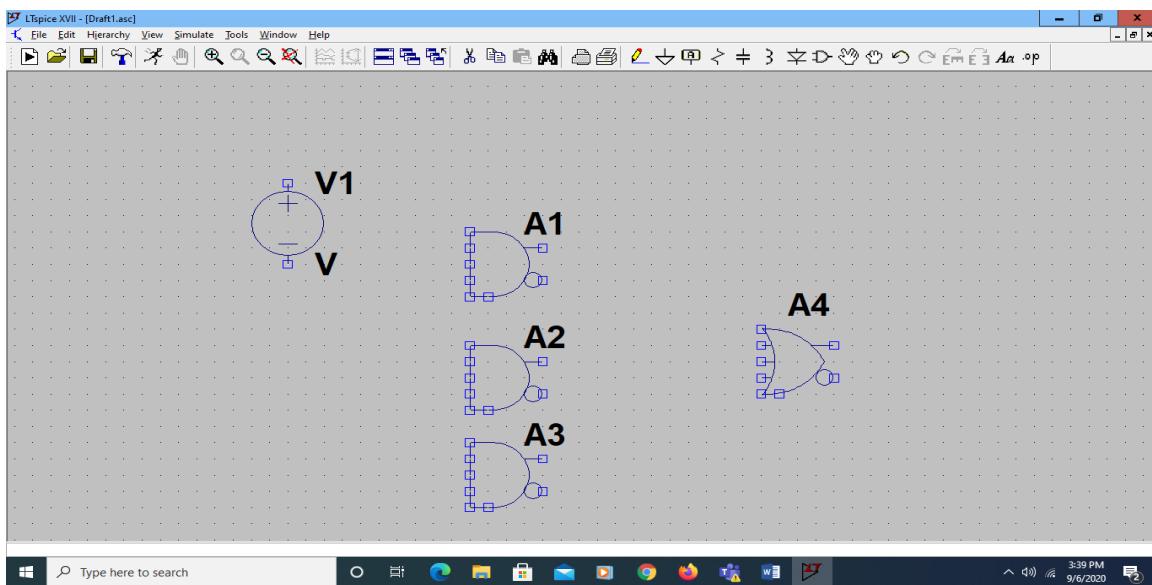
4. Type in the “Select Component Symbol” as AND to get the AND gate .Click Ok



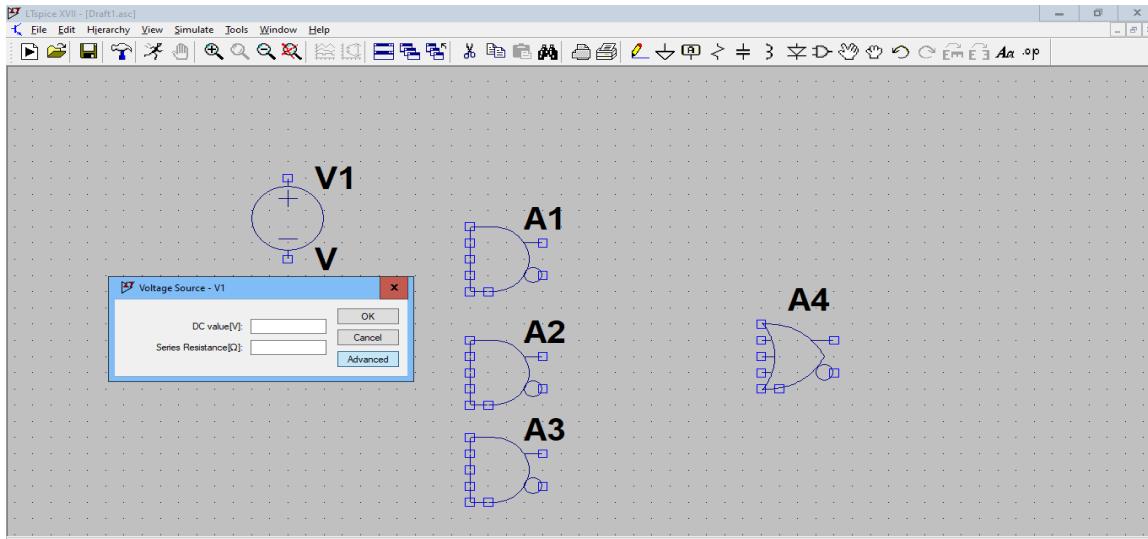
5. Drag it to the Schematic window. Each click in the Schematic will duplicate one component (AND Gate): A1,A2 and A3



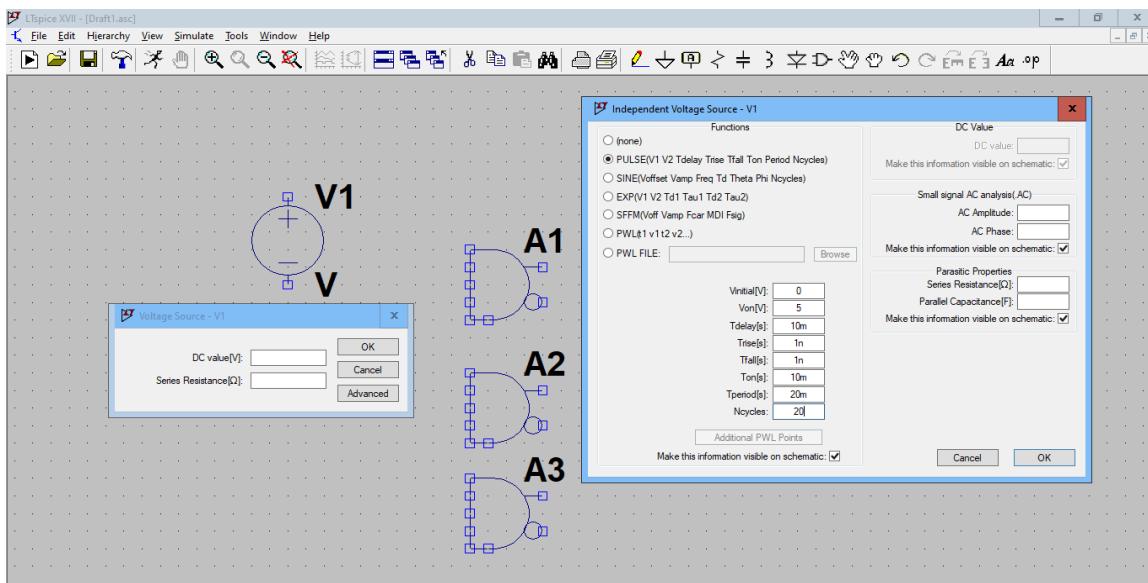
6. Similarly drag the OR gate (A4) and voltage source (V1)



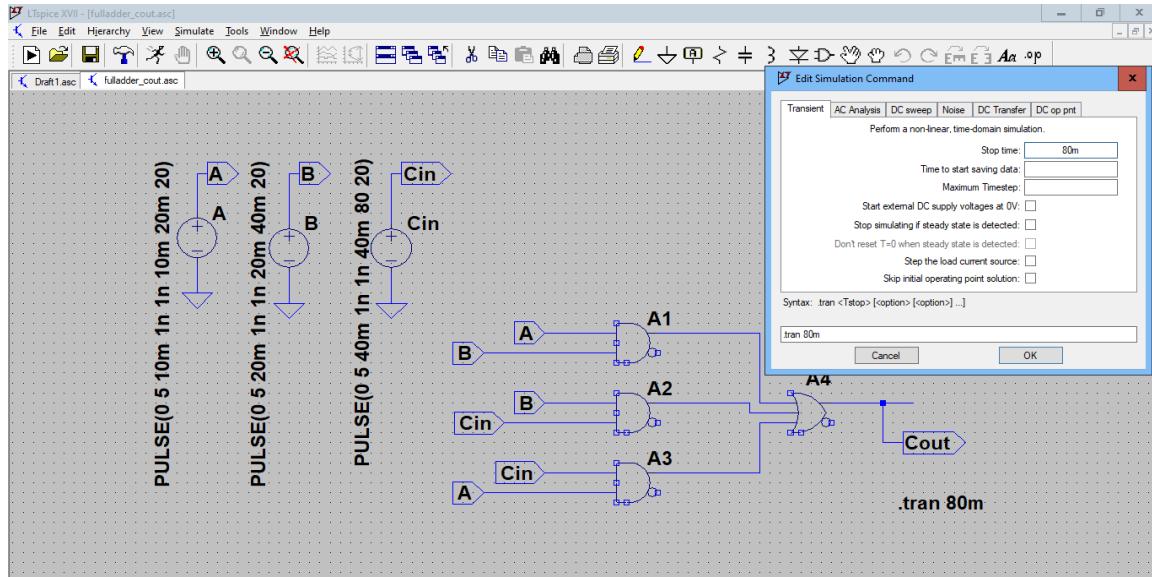
7. Right-click the voltage source(V1) and click the Advanced icon to configure it.



8. Select the Pulse Function and the initial values as shown below

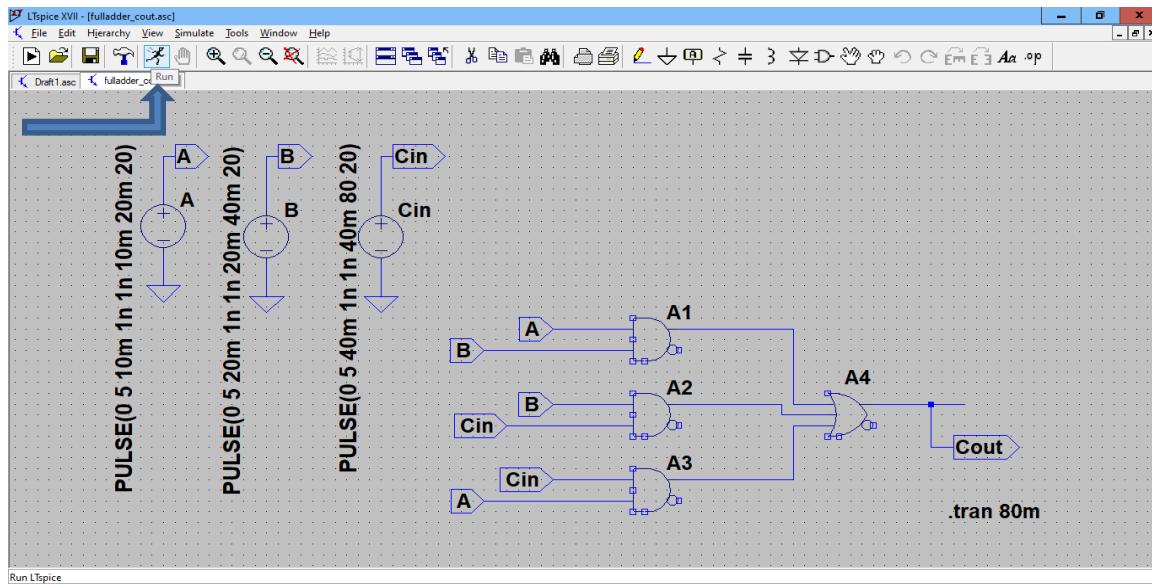


9. Connections are given as per the logic diagram Fig.4. LTSPICE Window to realize Cout . Click Simulate-----> Edit Simulation Cmd to set the simulation configuration as shown below. Set the

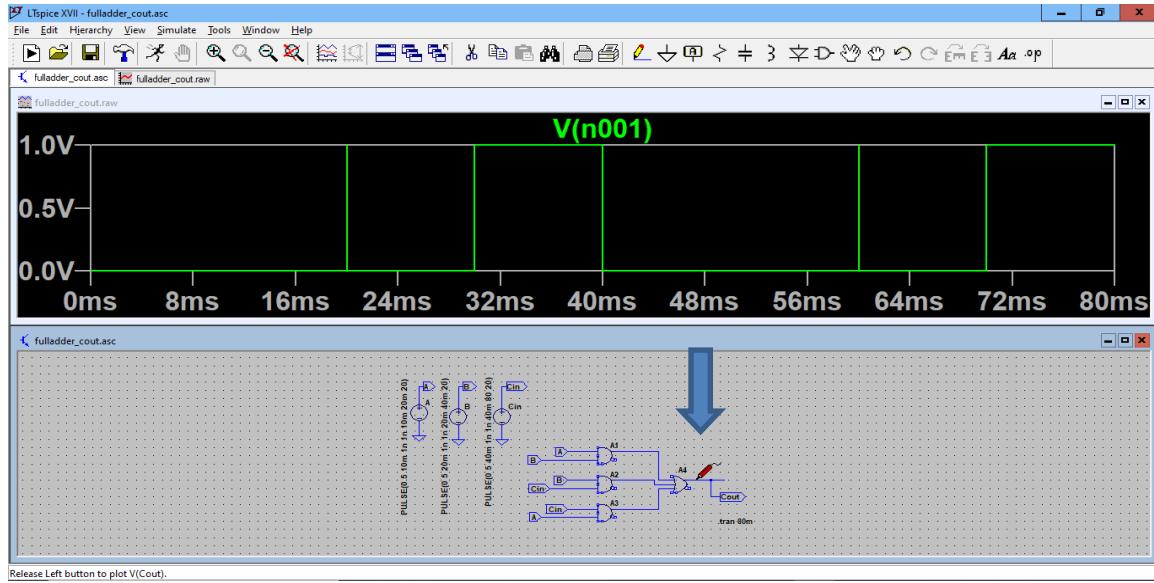


transient menu→ Stop time as 80m in seconds

10. Click the Run icon to start the simulation.

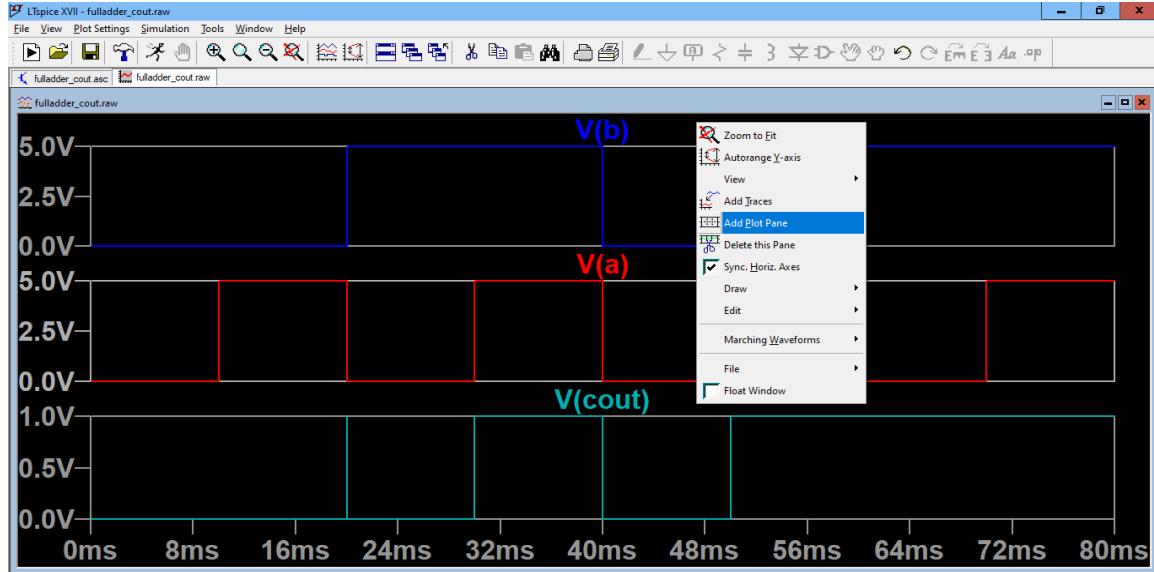


11. Click on the plot plane and simulate icon to get the voltage probe



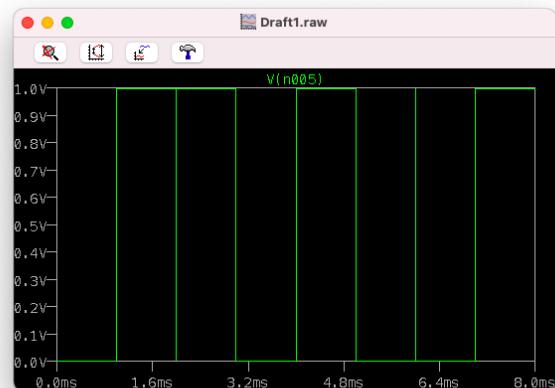
(red colour).

12. Include more plot pane as follows.



13. Apply the inputs and verify the truth table for the full adder circuit as shown in figure 4, Figure 5, Figure 6 and Figure 7.

GRAPH :



Results and Inferences:

Thus the design and verification of the truth table for the Full Adder circuit using Integrated circuits with open source software LTSPICE were done.

Practical Applications:

1. It is used in Digital Processors
2. ALU in computers and varieties of calculators
3. Different IC and microprocessor chips in PCs and laptops
4. In Ripple counters
5. An important tool in DSP (Digital Signal Processing)
6. The 74LS83 is a practical high-speed 4-bit full adder IC with carry out feature.

Course Outcome:

CO4. Design and implement various digital circuits

CO6. Design and conduct experiments to analyze and interpret data

Student Learning Outcomes (SLO):

SLO2. Having a clear understanding of the subject related concepts and of contemporary issues

Full Wave Rectifier With And Without Filter (SMPS Application)

Aim:

To examine the input and output waveforms of full wave bridge rectifier without filter and with capacitor filter

Software Used:

LTSPICE Software

Theory and Circuit Diagram;

The bridge rectifier circuit consists of 4 diodes D1, D2, D3, and D4. The circuit diagram of the bridge rectifier is shown in Figures 1 and 2. During the positive half cycle of the input voltage, diodes D1 and D2 are forward biased and diodes D3 and D4 are reverse biased. Therefore, current flows through the diode D1, load resistor R, and diode D2. During the negative half-cycle, D3 and D4 are forward biased and diodes D1 and D2 are reverse biased. Therefore, current flows through the diode D3, Load resistor R, and D4. During both the half-cycles, the current flows through the load resistor in the same direction. The peak value of the output voltage is less than the peak value of the input voltage due to the voltage drop across two diodes.

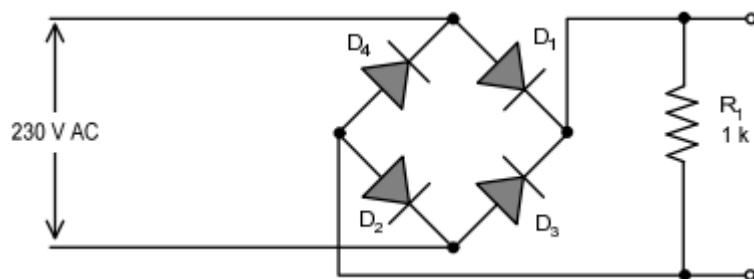


Figure 1. Bridge Rectifier circuit diagram without capacitor filter

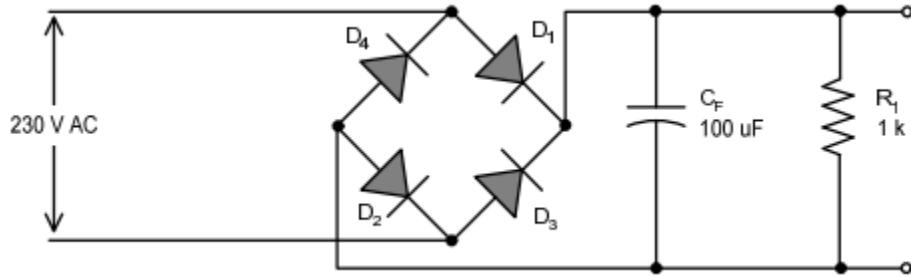


Figure 2. Bridge Rectifier circuit diagram with capacitor filter

All rectifier outputs contain a considerable amount of ripple in addition to the DC component. To avoid AC components, a filter is connected to the output of the rectifier. Capacitor input filter, choke input filter, RC, CRC, LC, and CLC filters are the usually used filters. The capacitor input filter is the simplest and cheapest. A high-value capacitor C is connected in shunt with the load resistor R. Capacitor charges to peak voltage when the half-cycle appears at the output. After the peak value is passed, the capacitor discharges through the load resistor slowly since the diode is reverse biased by the capacitor voltage. Before the capacitor voltage drops substantially, the next output cycle arrives and the capacitor recharges to the peak.

The RMS value of the filtered output is calculated assuming that the wave as a triangular wave and it is

$$V_{rms} = \frac{V_{pp}}{2\sqrt{3}}$$

where V_{pp} is the peak to the peak value of the ripple voltage.

$$V_{dc} = V_m - \frac{V_{pp}}{2}$$

$$\text{Ripple factor } r = \frac{V_{rms}}{V_{dc}}$$

Ripple factor is also given by the expression, $r = \frac{1}{4\sqrt{3}fRC}$,

where f is the mains supply frequency 50 Hz

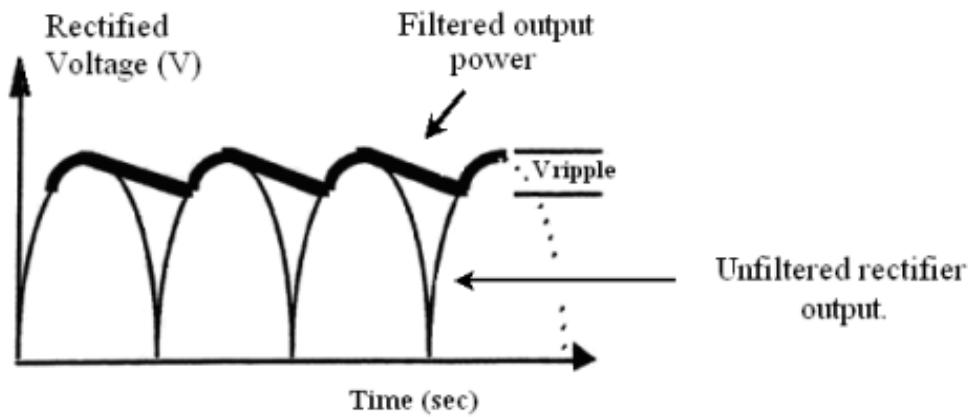
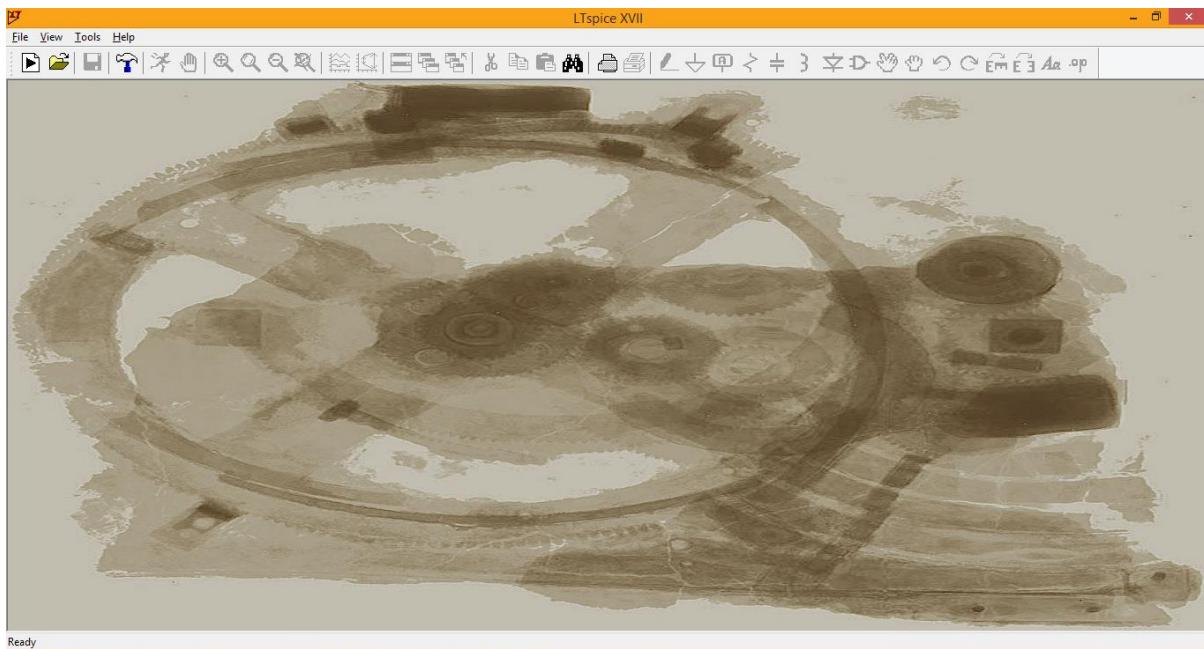


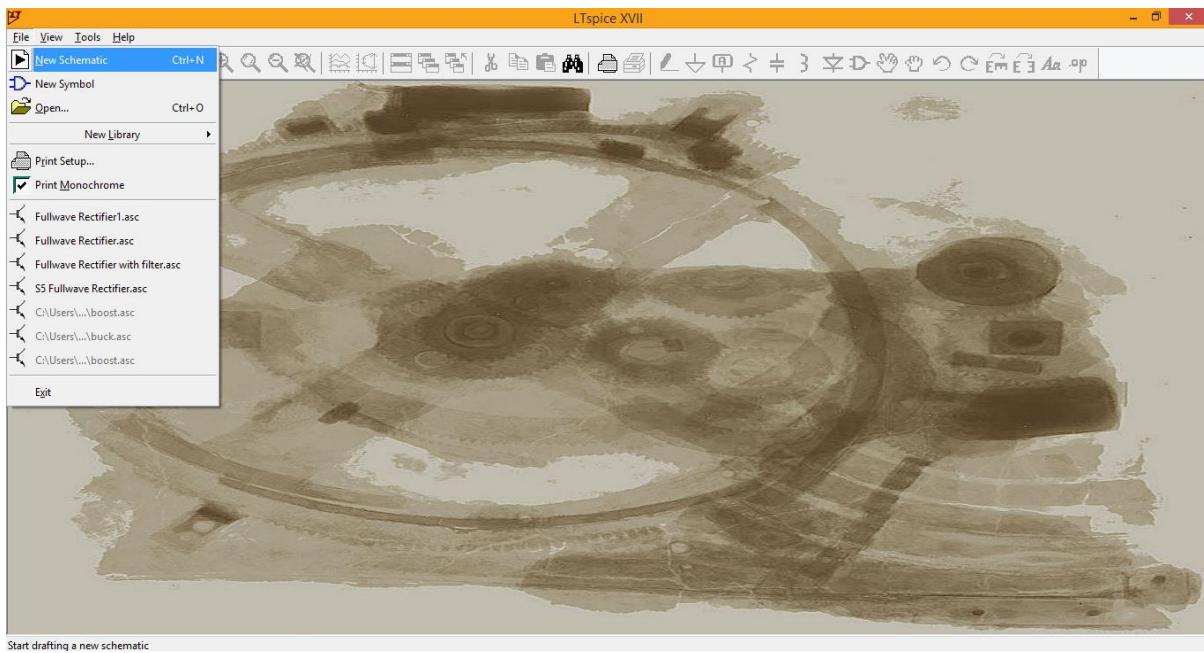
Figure 3. Bridge Rectifier output waveform (Dark line is filtered output and thin line is unfiltered output)

Procedure:

1. Open LTSPICE software.

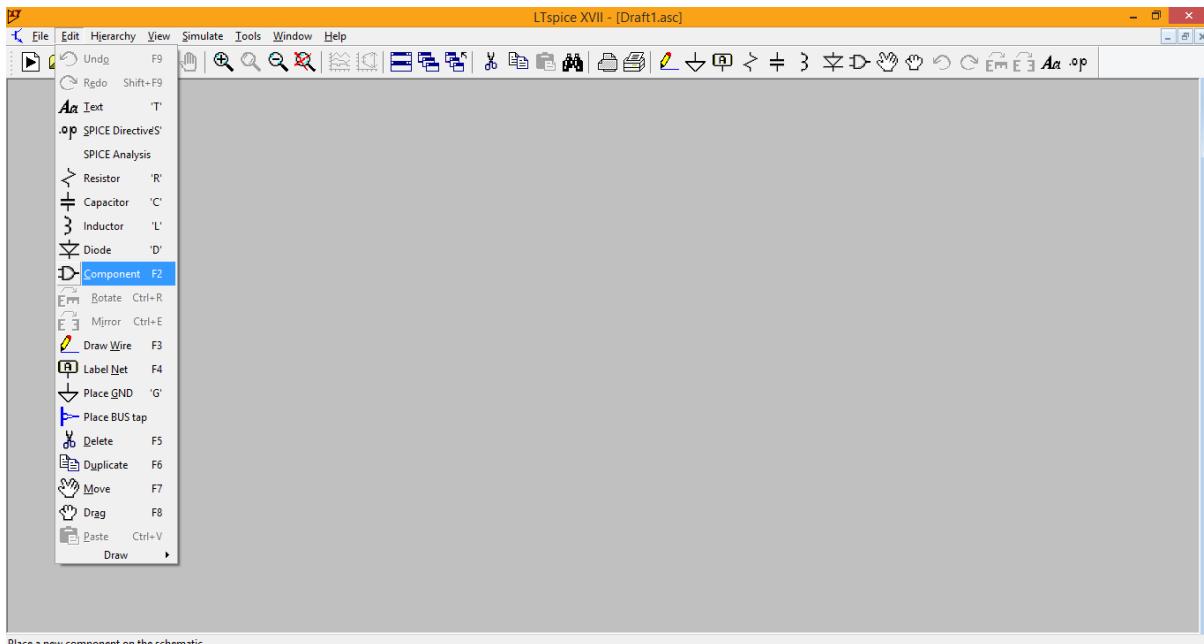


2. In the file menu click the new schematic and open the new schematic file.



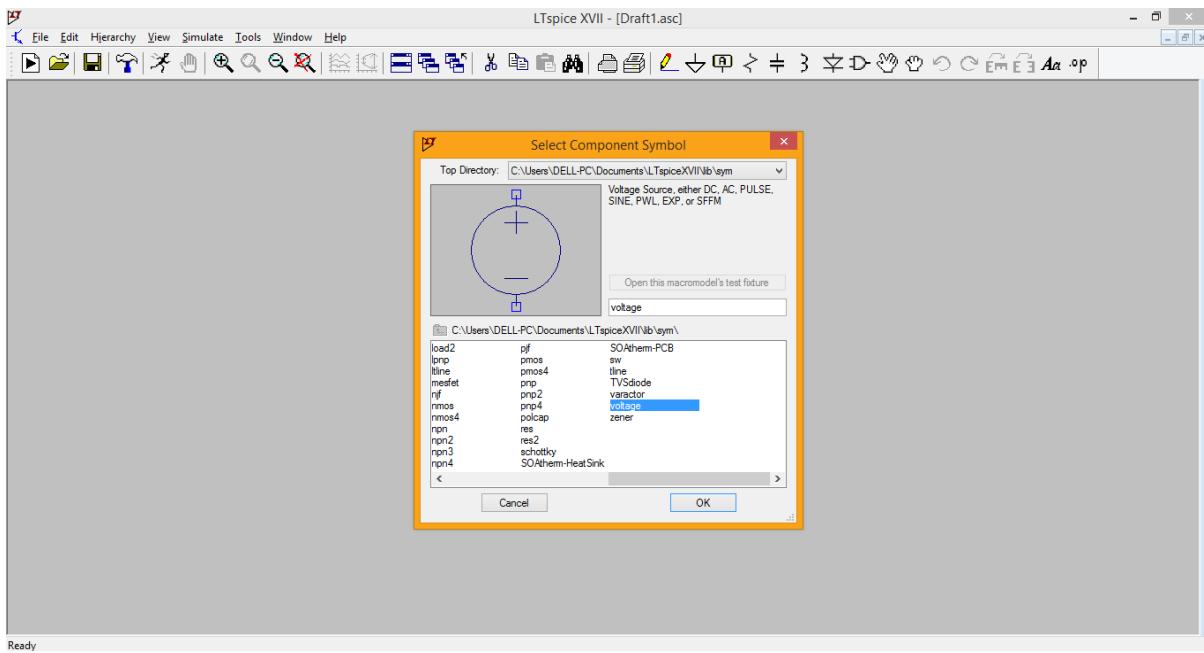
Start drafting a new schematic

3. In the edit menu click the component and open the components tab.

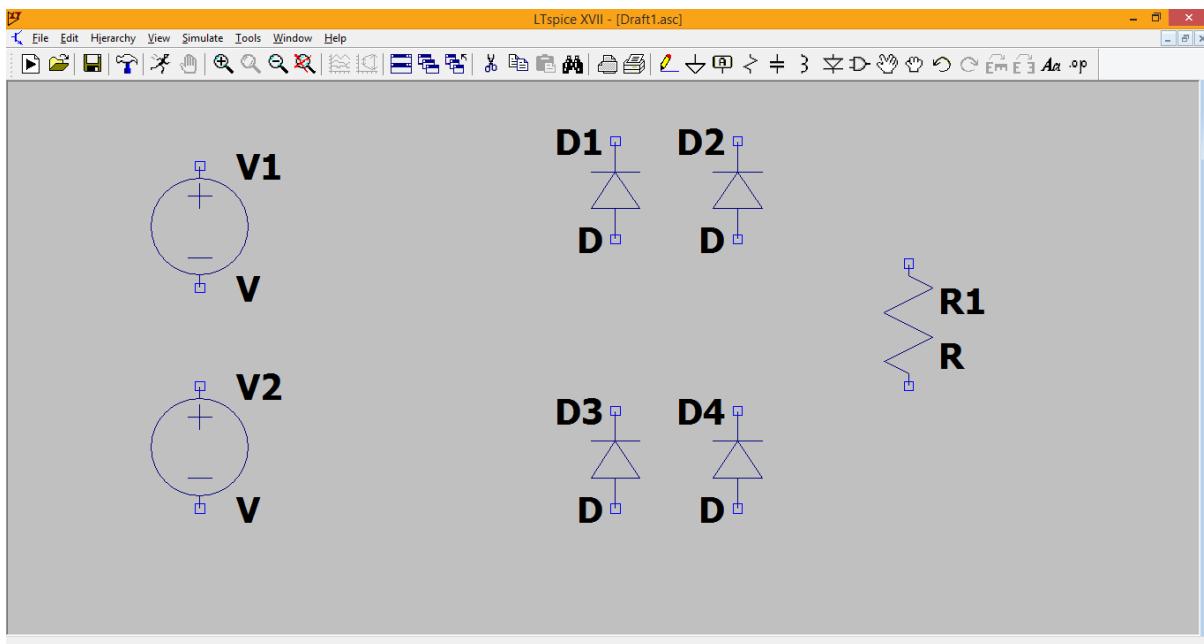


Place a new component on the schematic.

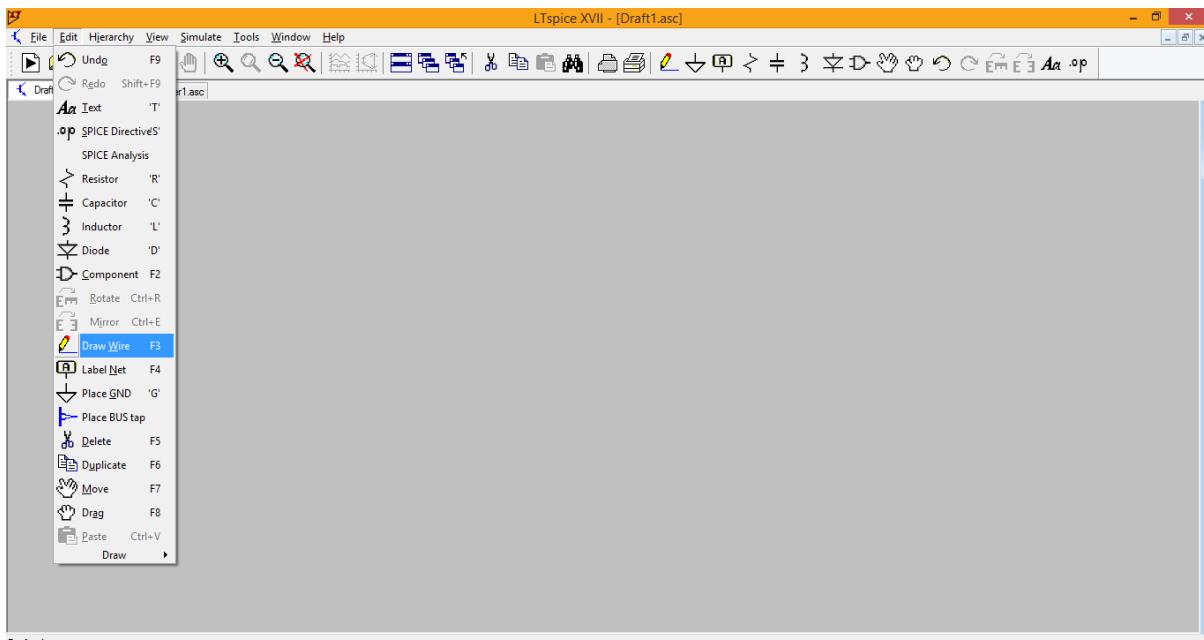
4. Select the voltage component for voltage source and press ok.



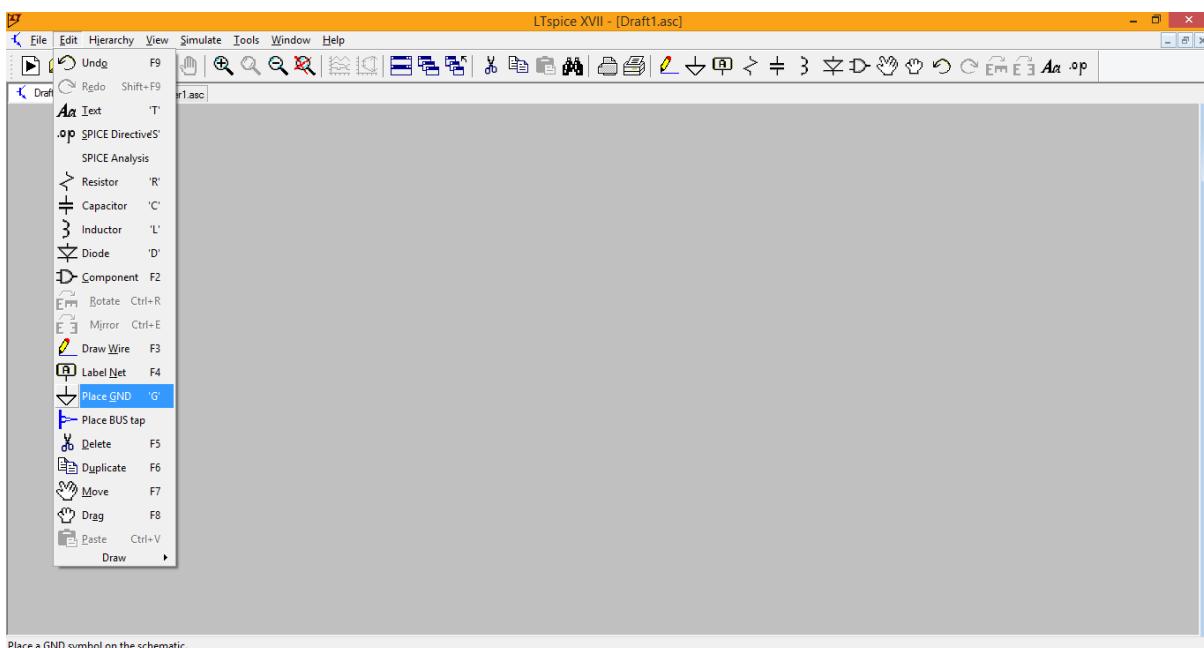
5. Similarly by opening the components tab select the other component required (Diode, Resistance, and Capacitance).



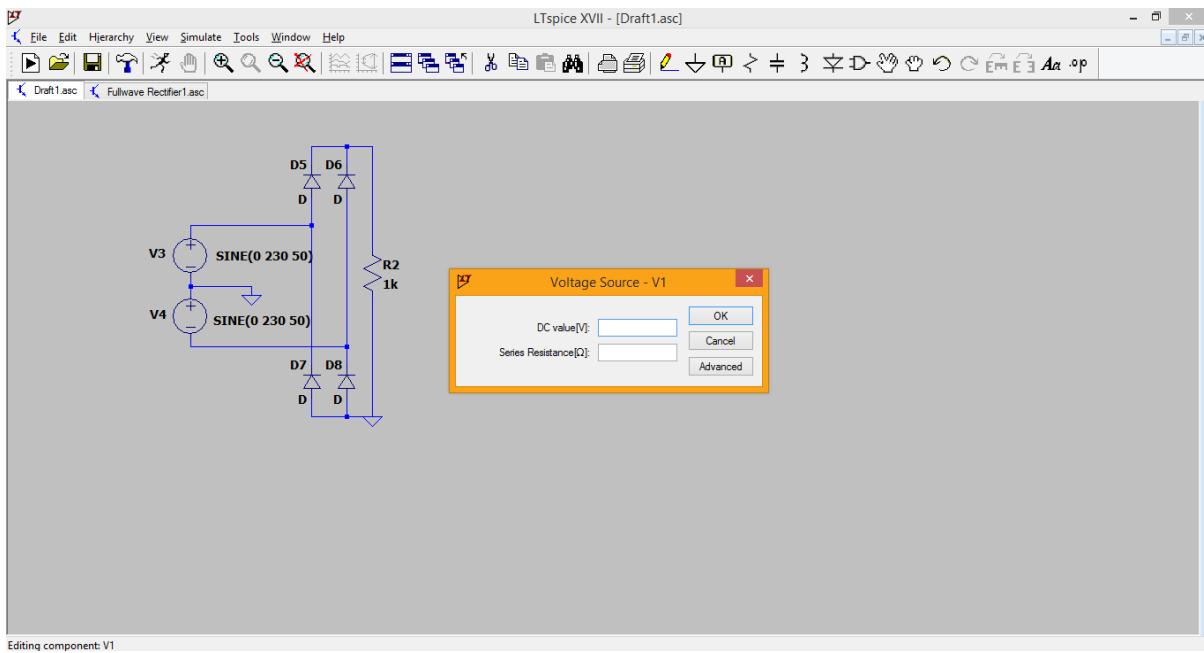
6. Connect the components by using the draw wire in the menu bar or draw wire in the edit menu.



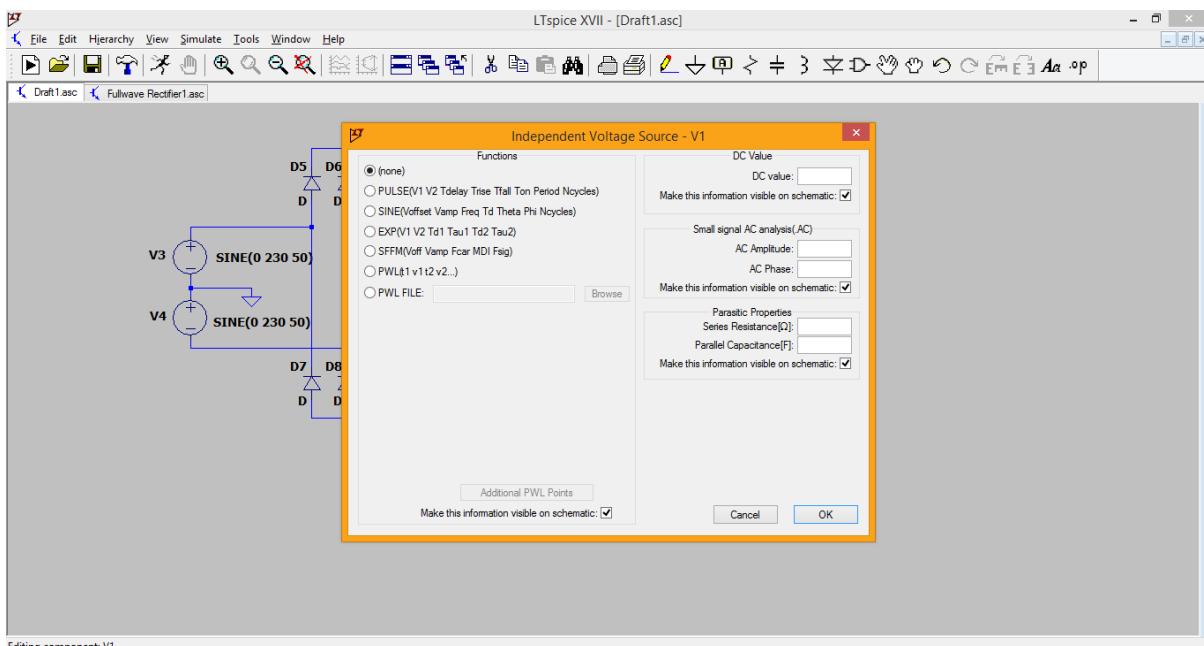
7. Connect the ground to the circuit from the menu bar or place ground in the edit menu.



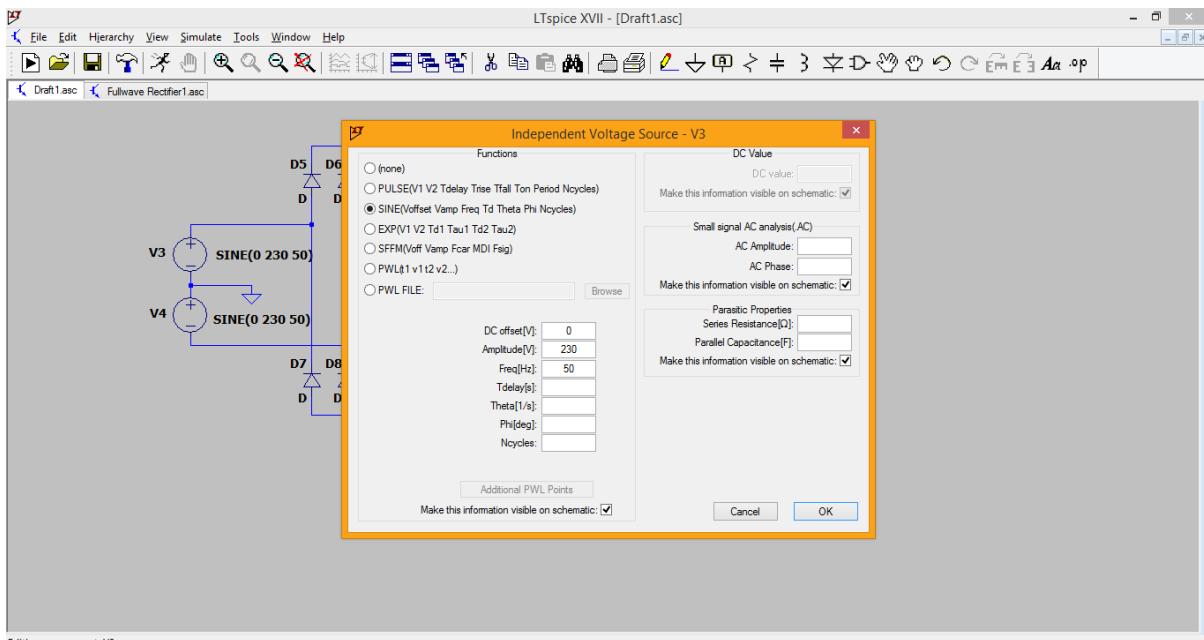
8. Place the cursor on the voltage source and the cursor will look like a hand pointing.
9. Right click the voltage source and new tab opens.



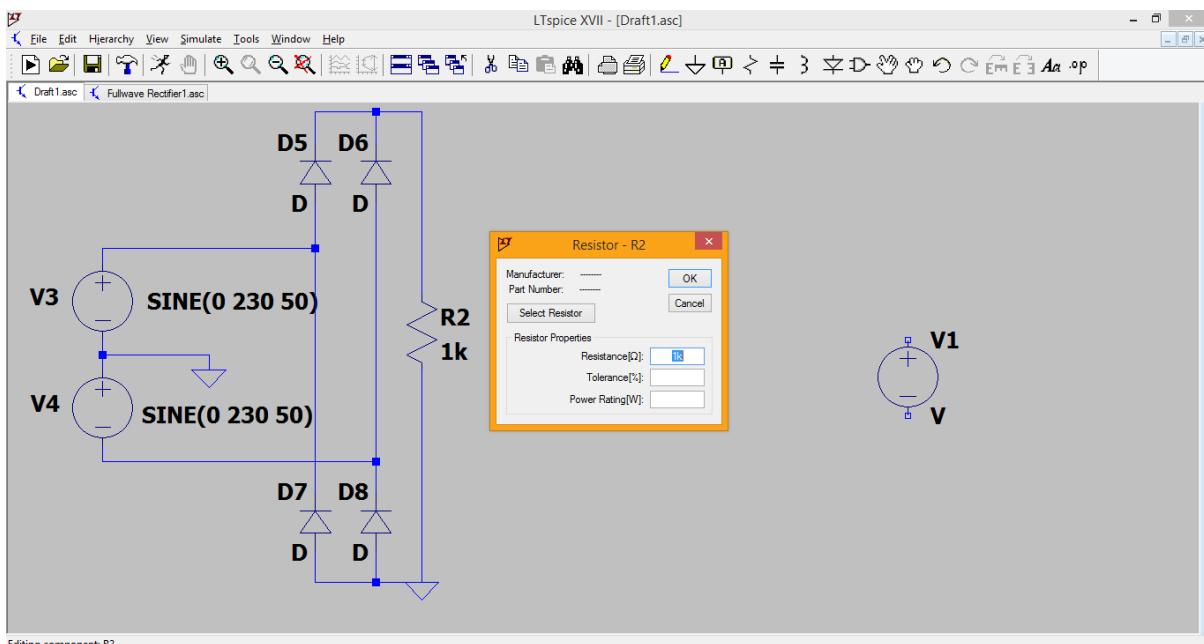
10. Click advanced tab and a new tab opens.



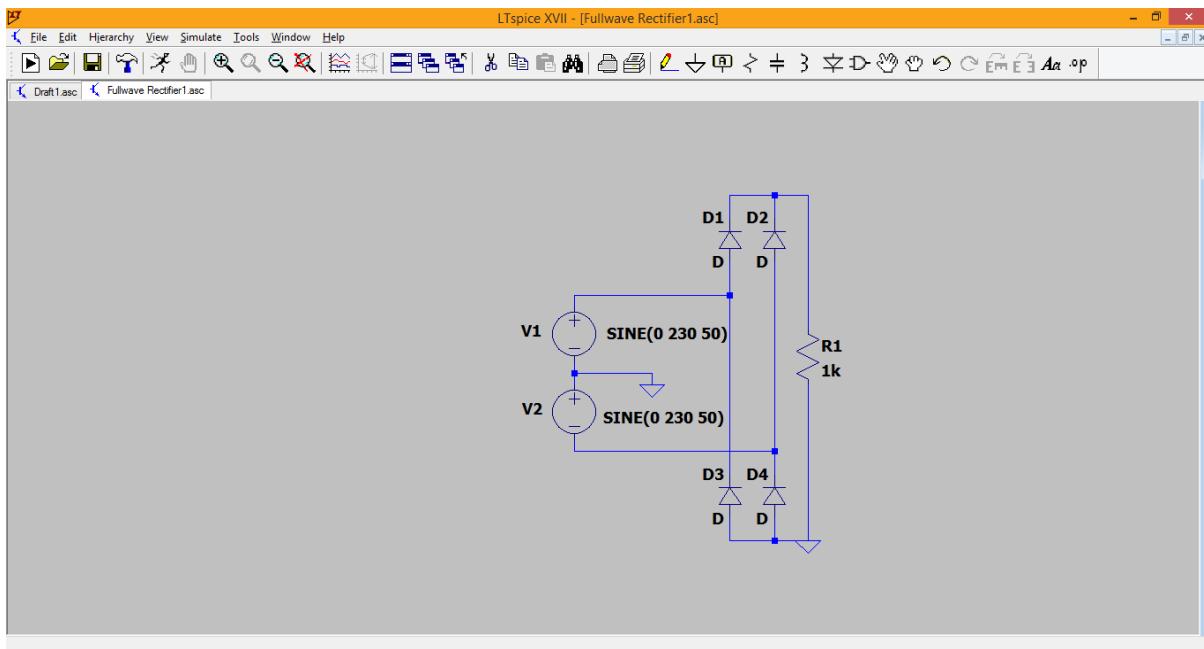
11. Select the sine option and enter the value for voltage amplitude, dc offset and frequency.



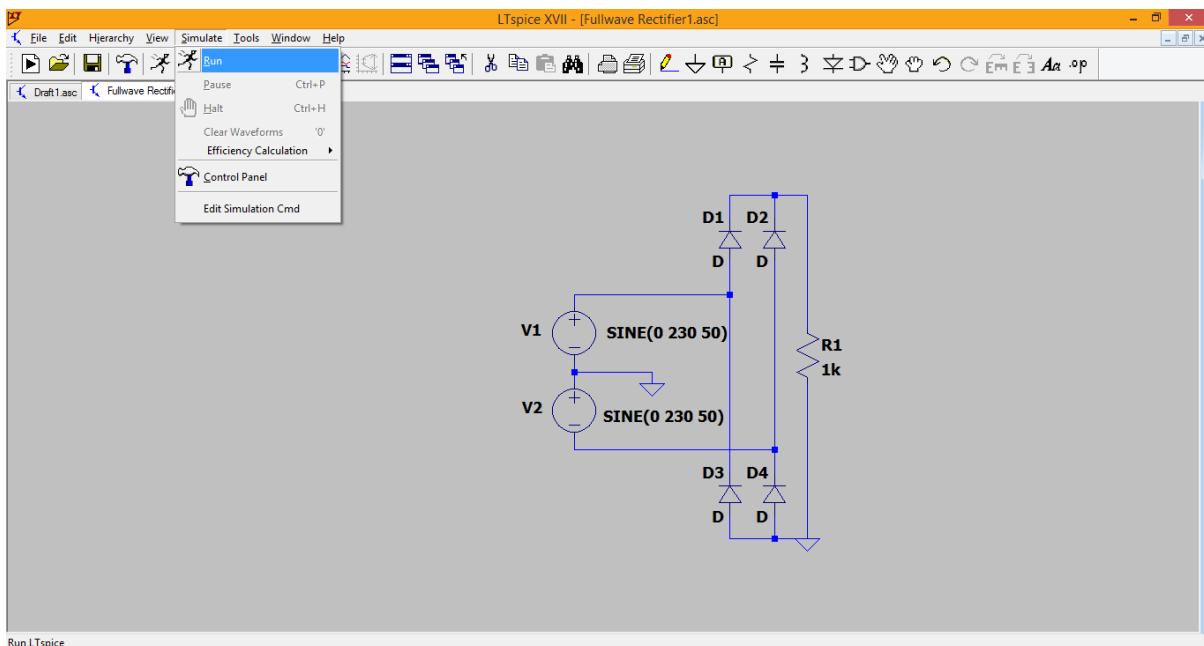
12. Right click the resistance and enter the value of the resistance.



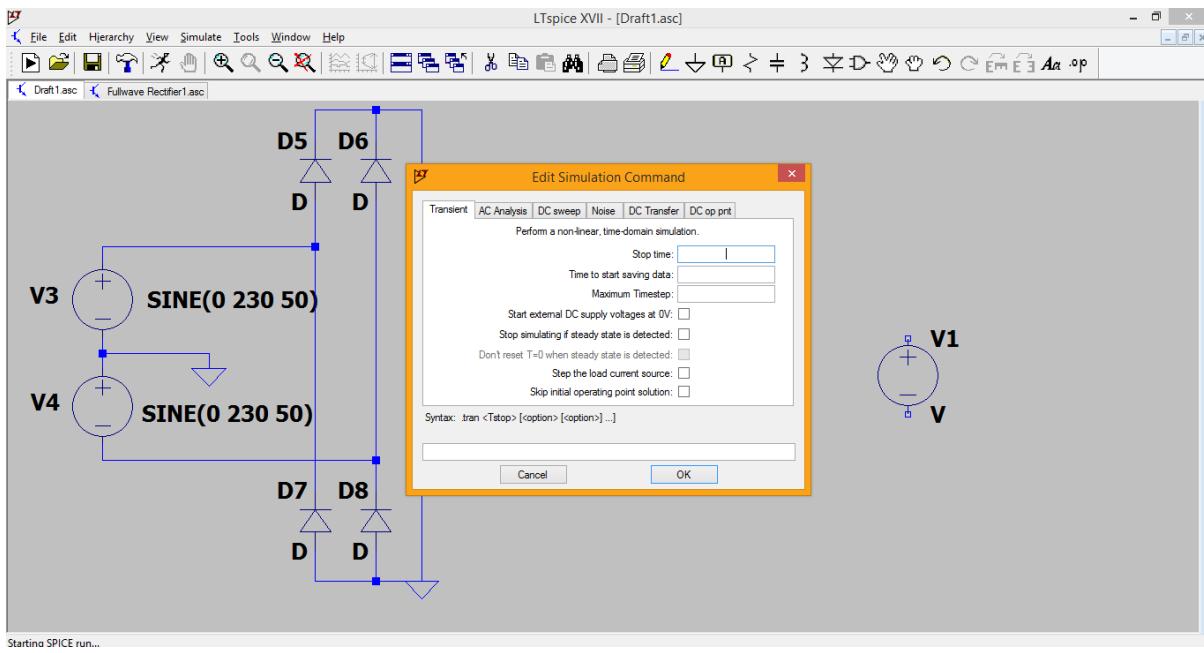
13. After connecting the components and entering the values save the file.



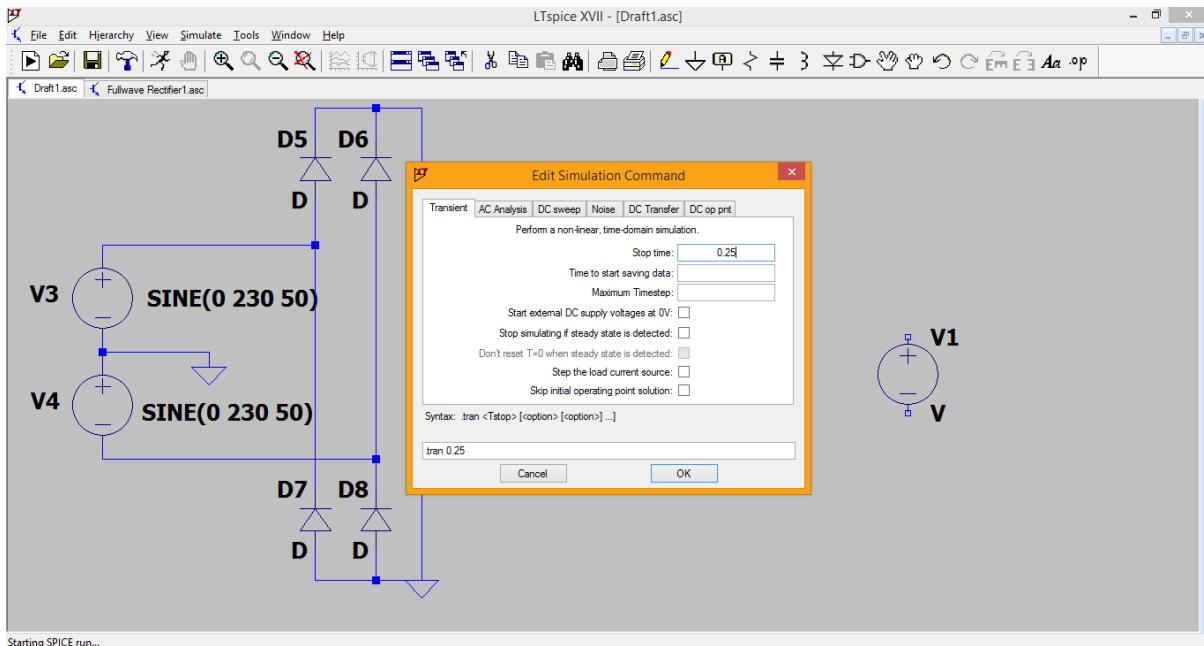
14. The file can be executed using the run button in the menu bar or the run option in simulate menu.



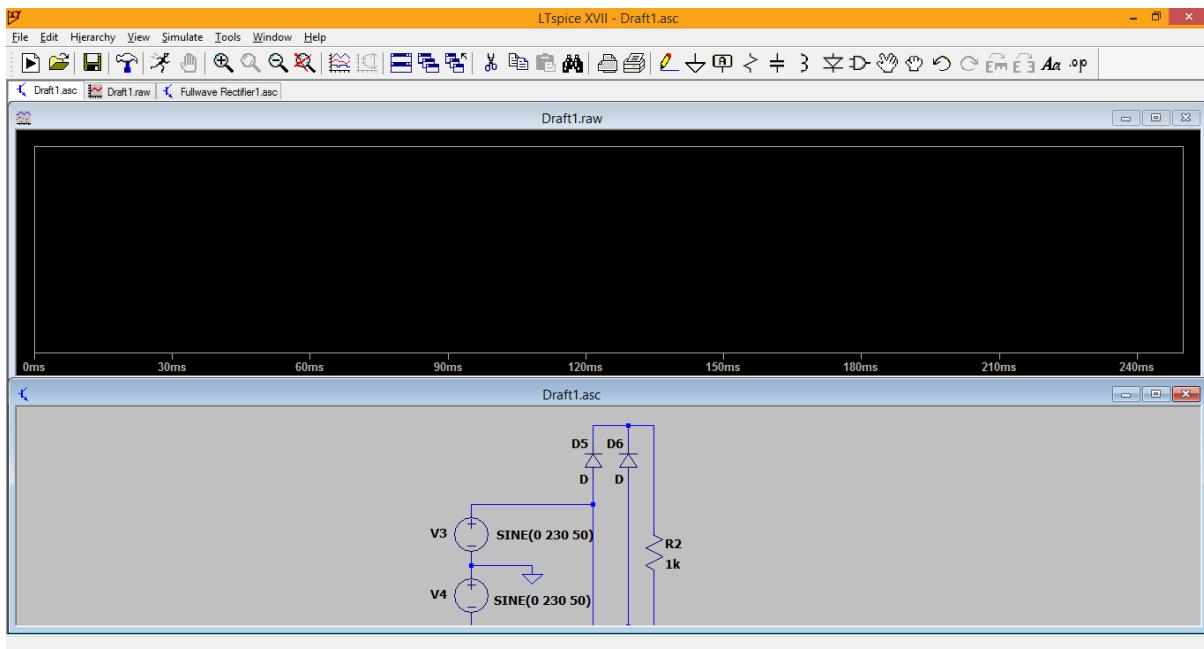
15. The edit simulation command tab opens.



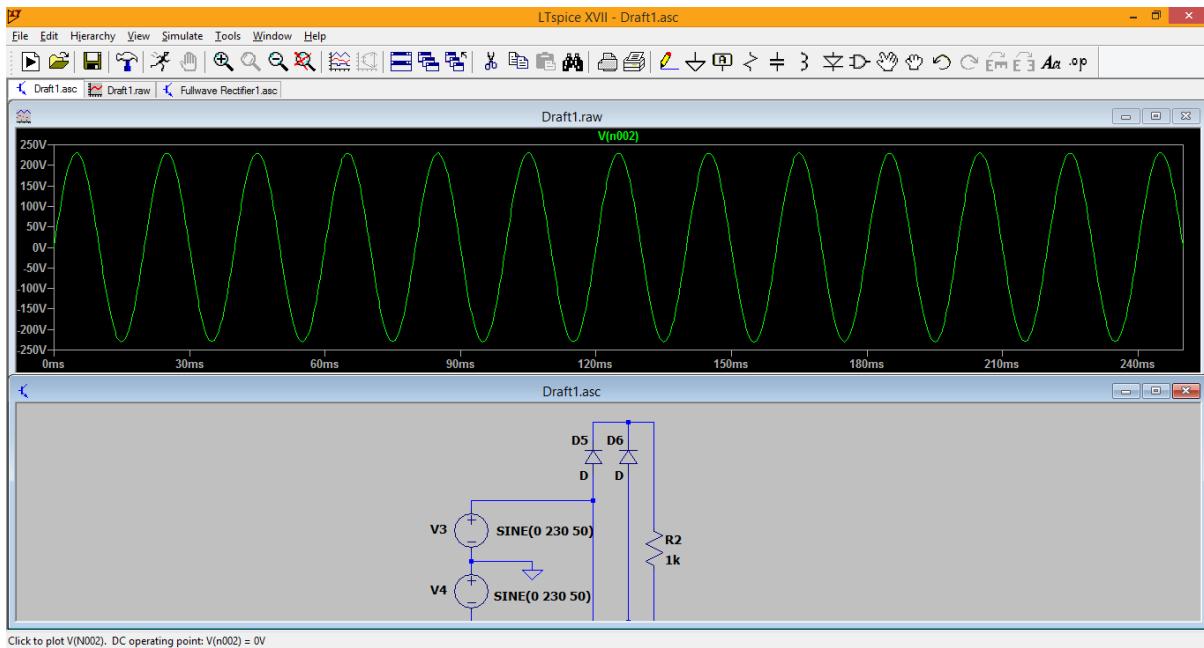
16. Select transient tab and enter the value for stop time.



17. The run command executes and the plot pane opens.

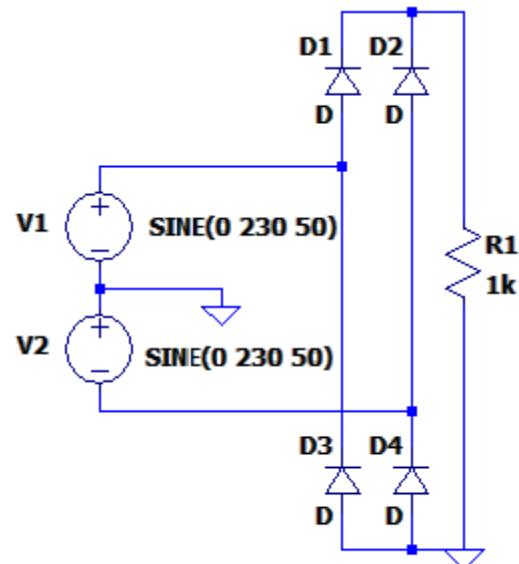


18. Place the cursor near the source to get the probe and left click to get the source voltage graph displayed.



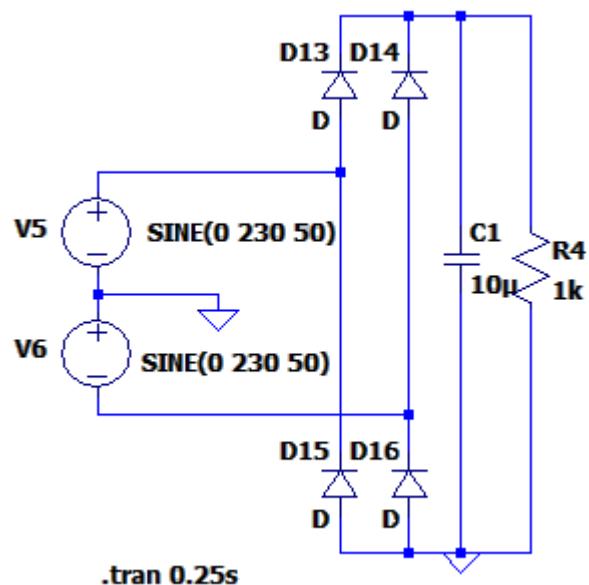
19. Add the plot pane and check the graphs for output voltage.

The LTSPICE circuit for rectifier without filter and with filter is as shown below.



.tran 0.25s

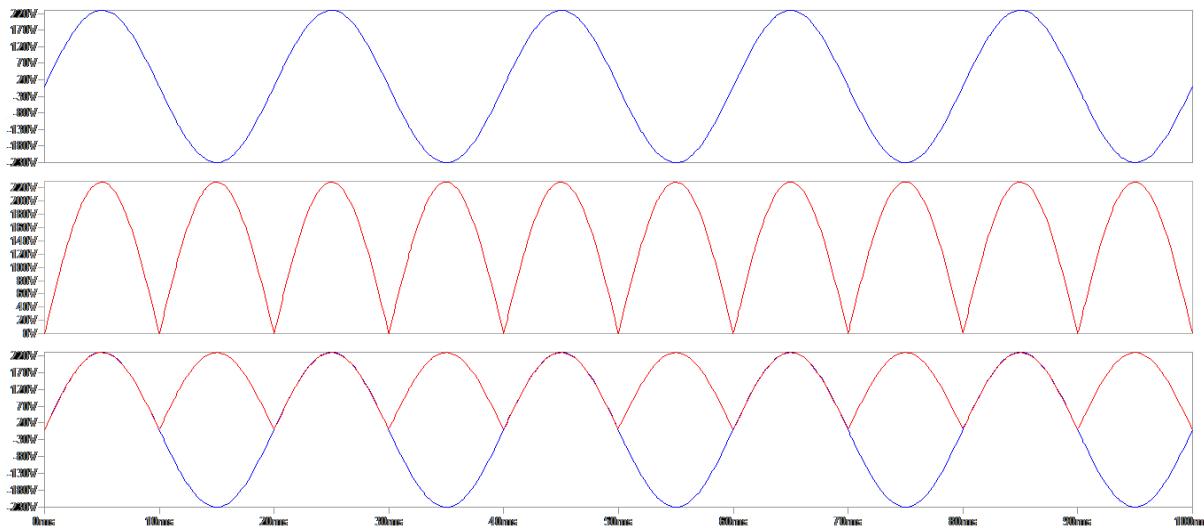
Bridge Rectifier circuit diagram without capacitor filter



.tran 0.25s

Bridge Rectifier circuit diagram with capacitor filter

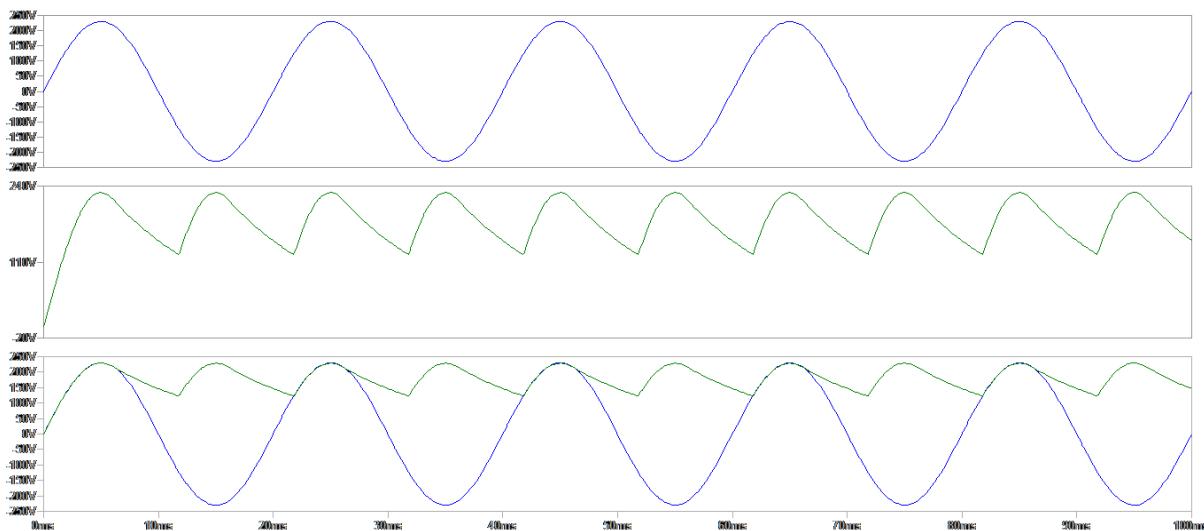
Observation Table and Waveforms



Bridge Rectifier output without capacitor filter

(First graph – Source Voltage, Second graph – Output Voltage,

Third graph – Input and output voltage)



Bridge Rectifier output with capacitor filter

(First graph – Source Voltage, Second graph – Output Voltage,

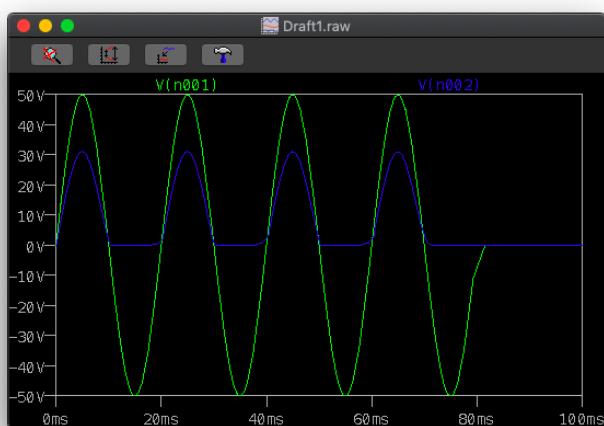
Third graph – Input and output voltage)

Tabular Column

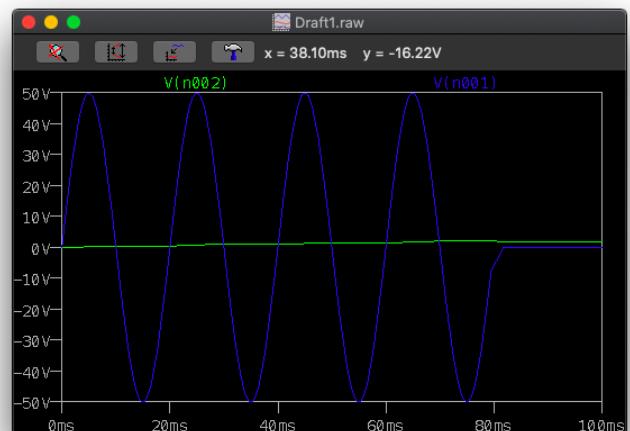
Without Filter					
S.No	Vm	Vrms = Vm/v2	Vdc=2Vm/π	r=V(Vrms/Vdc)^2-1	
1	50	35.355	31.847	0.4833	
2	100	70.7106	63.661	0.4834	
3	230	162.63	146.42	0.4834	
With Filter					
S.No	Vm	Vpp	Vrms = Vpp/2v3	Vdc=Vm-Vpp/2	r=Vrms/Vdc
1	50	50	14.433	25	0.57732
2	100	100	28.867	50	0.57734
3	230	230	66.395	115	0.57734

GRAPH :

Without --



With --



Results and Inferences:

Thus the input and output waveforms of full-wave bridge rectifier without filter and with capacitor filter are examined.

Practical Applications:

1. **Bridge rectifier** circuits are also used to supply steady and polarized DC voltage in electric welding.
2. **Full Wave Bridge Rectifier** is used to detect the amplitude of the modulating radio signal.

Course Outcome:

CO2. Analyze AC power circuits and networks, its measurement and safety concerns

Student Learning Outcomes (SLO):

- SLO1.** Having an ability to apply mathematics and science in engineering applications
- SLO9.** Having problem-solving ability- solving social issues and engineering problems

Characteristics of MOSFET

(Circuits for Motor Control Application)

Aim:

The objectives of this experiment are

1. To study the drain characteristics and transfer characteristics of enhancement type n-channel MOSFET.
2. To plot the characteristics curve I_D vs V_{DS} (drain characteristics) and I_D vs V_{GS} (transfer characteristics) of n-channel E-MOSFET using LTSpice software.

Software Used:

LTSpice

Theory:

FET's are similar in operation to that of BJT's but complementary in their working principle. BJTs are current-controlled devices whereas FETs are voltage controlled. It is a majority carrier device, where the conduction is due to either electron or due to holes. Hence FET forms a class of unipolar transistor/switch. The source terminal acts as an input terminal for the majority carriers, the drain terminal acts as the output terminal, and the gate as a control terminal that regulates the charge carrier flow through the substrate/channel in the device.

FETs are broadly classified into two major groups namely Junction Field Effect Transistor (JFET) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The gate is conductively coupled to the substrate in JFET forming a *PN*-junction, whereas it is capacitively coupled in MOSFET. This is the most significant difference between both the groups of FETs. JFETs in turn are classified into n-channel and p-channel based on the conduction channel.

MOSFETs are classified into enhancement type and depletion type in addition to the type of channel.

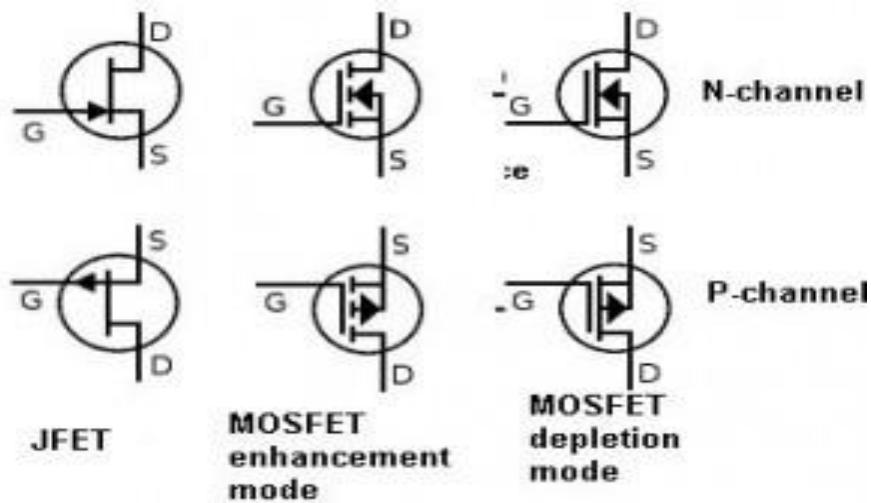


Figure 1 – Circuit symbols of JFET and MOSFET and its types

Experiment:

The circuit diagram to study the characteristics of enhancement type n-channel MOSFET is shown in figure 1. It requires two variable dc supplies to energize the drain-source and gate-source circuit. The power supply powering drain-source circuit is labeled as V_{DS} and the supply powering gate-source circuit is labeled as V_{GS} . For both the circuits, the source terminal is common and hence the configuration is referred to common source configuration.

In n-channel MOSFET, electrons are the majority carriers that flows from source to drain terminal within the device. To ensure this, the drain terminal is connected to +ve terminal of V_{DS} with respect to source. To regulate the charge flow inside the device, a channel of negative ions to be induced on the substrate by powering the gate with positive voltage with respect to source. Hence the gate terminal is connected to +ve terminal of V_{GS} with respect to source.

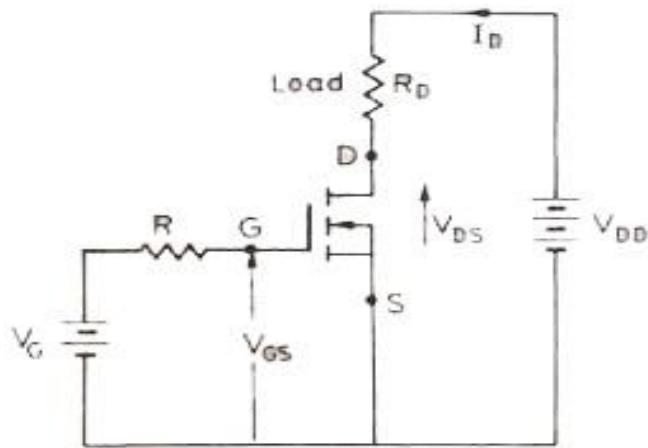


Figure 2 – Circuit to study characteristics of MOSFET

Transfer Characteristics:

It is the plot of drain current as a function of V_{GS} at constant drain-to-source voltage (V_{DS}). In this characteristic, the drain current is plotted as a function of gate-to-source voltage (V_{GS}). As long V_{GS} is equal to a threshold value V_{GST} , the drain current is zero, since no channel is established between source and drain for the charges to flow. At V_{GST} , a minimum channel is established between source and drain resulting in charge carrier flow from source to drain resulting in a small drain current. As V_{GS} increases, the width of the channel increases resulting in more charge flow from source to drain, decided by V_{DS} and drain-to-source resistance (R_{DS}). The transfer characteristics of enhancement MOSFET is shown in figure.

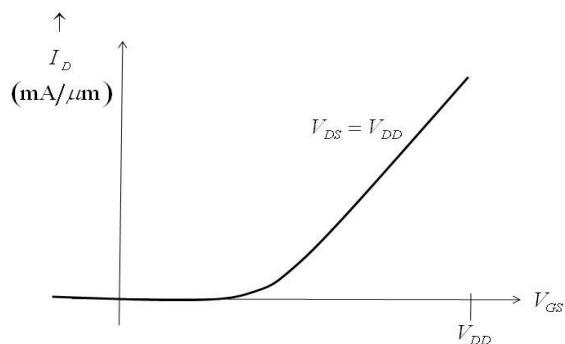


Figure 3 – Transfer characteristics of enhancement type MOSFET

Drain Characteristics:

It is the plot of drain current I_D as a function of V_{DS} with V_{GS} as constant. It is the set of characteristics plotted for various values of V_{GS} . It reveals the output characteristics of MOSFET. It has three significant operating regions namely cut-off region, saturation region and ohmic region.

Cut-off region is for which I_D is zero for any value of applied drain-to-source voltage V_{DS} . In this region, the MOSFET works as an “OPEN” switch. In saturation region, the drain current is limited by V_{GS} and is fairly constant for any value of V_{DS} applied. The MOSFET has the ability to work as amplifier in this region. Under ohmic region, the drain current I_D increases linearly even for a small change in V_{DS} . MOSFET works as “CLOSED” switch in this region.

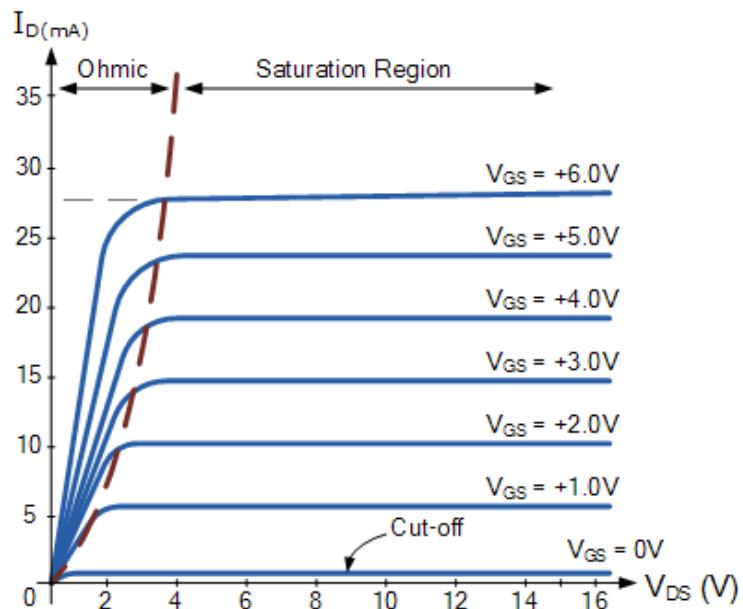
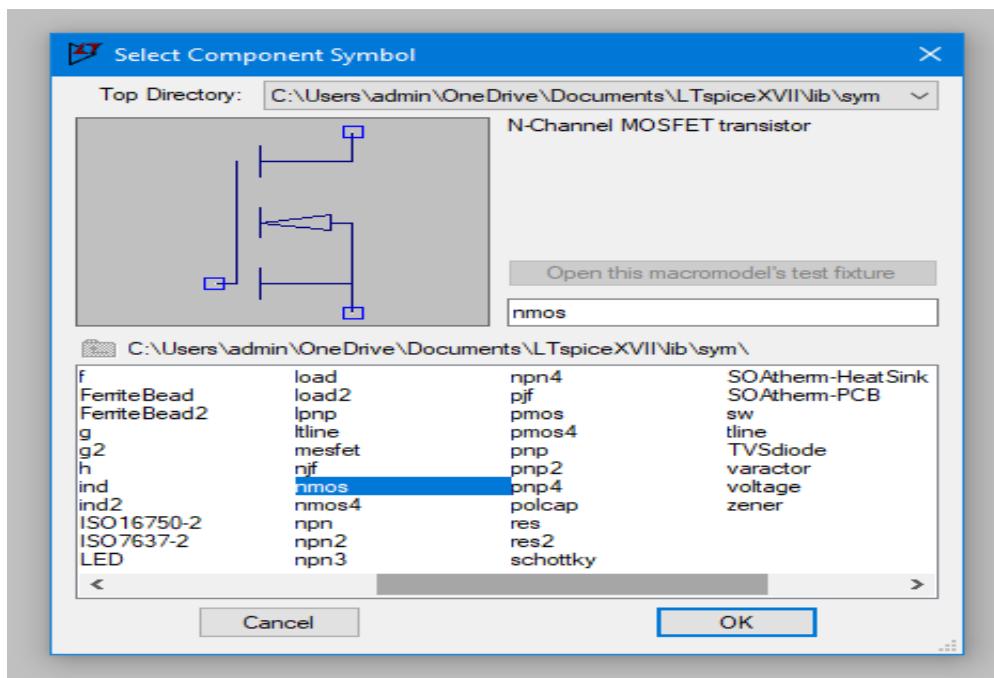


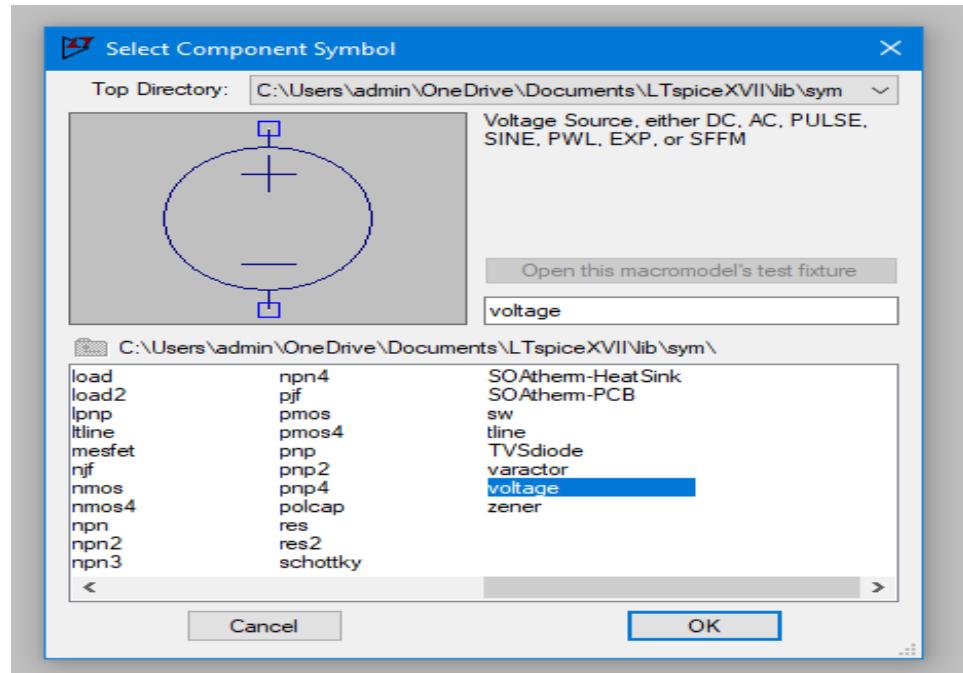
Figure 4 – Drain characteristics of enhancement type MOSFET

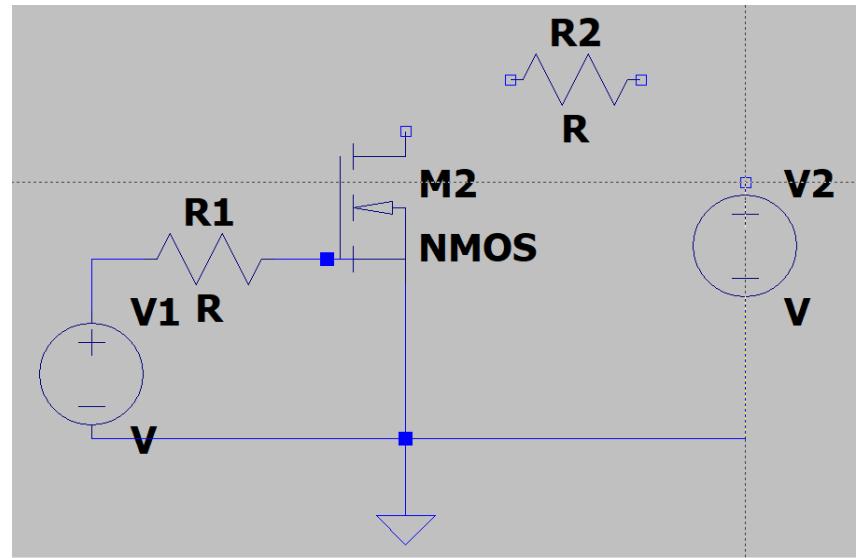
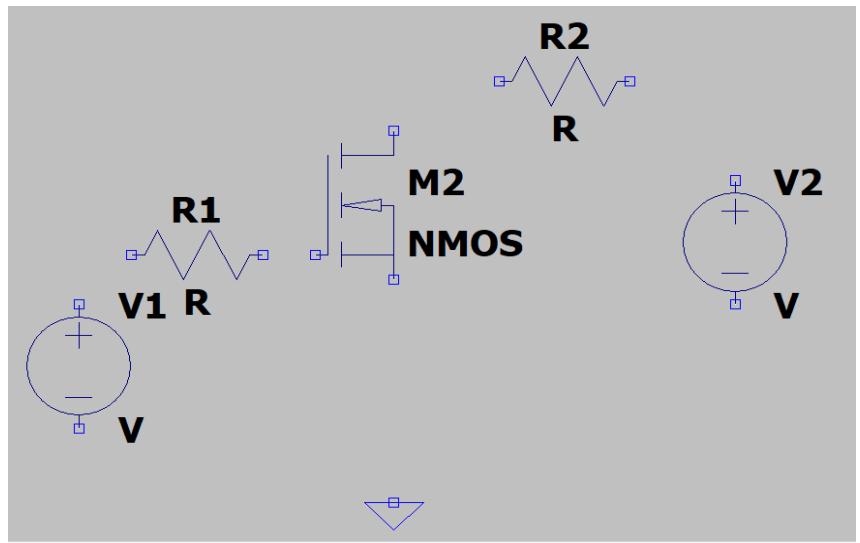
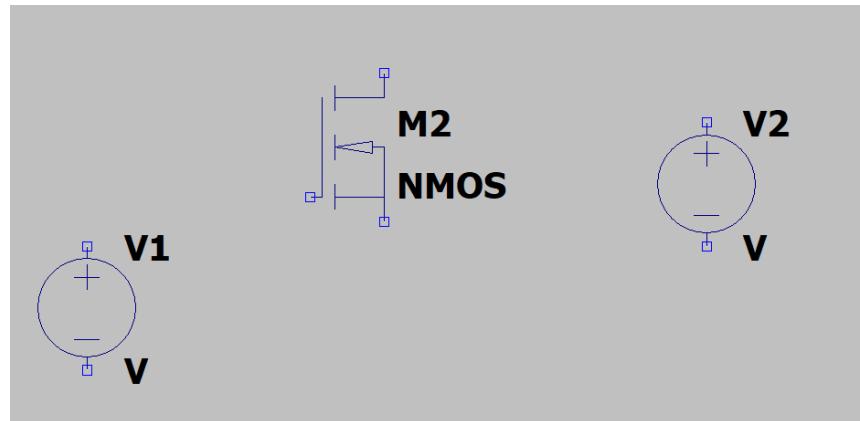
Procedure:

1. Open LTSpice software and create a new file.
2. Click on “ADD COMPONENTS” icon and search for ‘nmos’ in the component search dialog box.

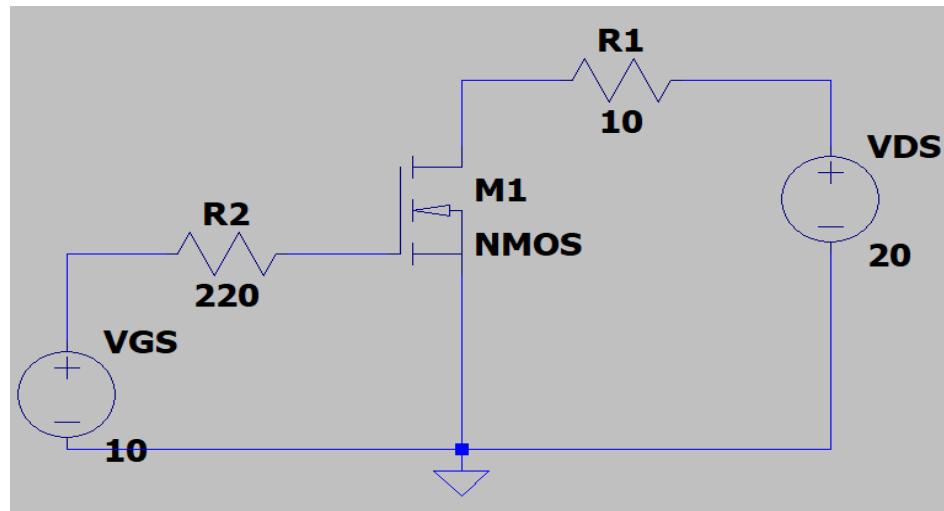


3. Add required components based on the circuits to the new file.

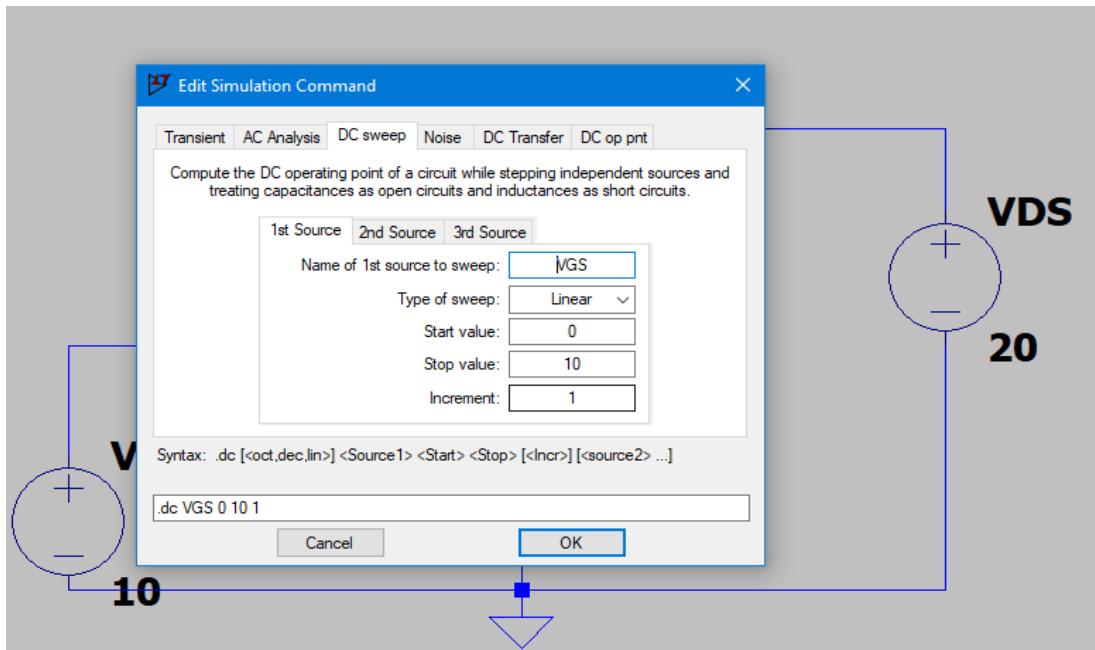
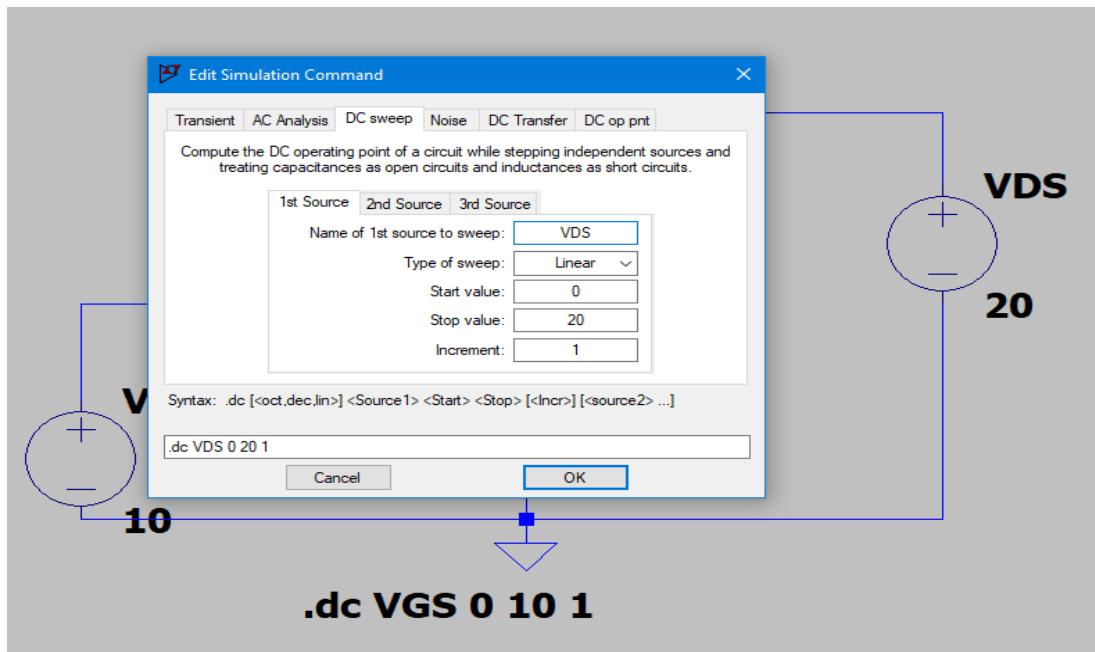


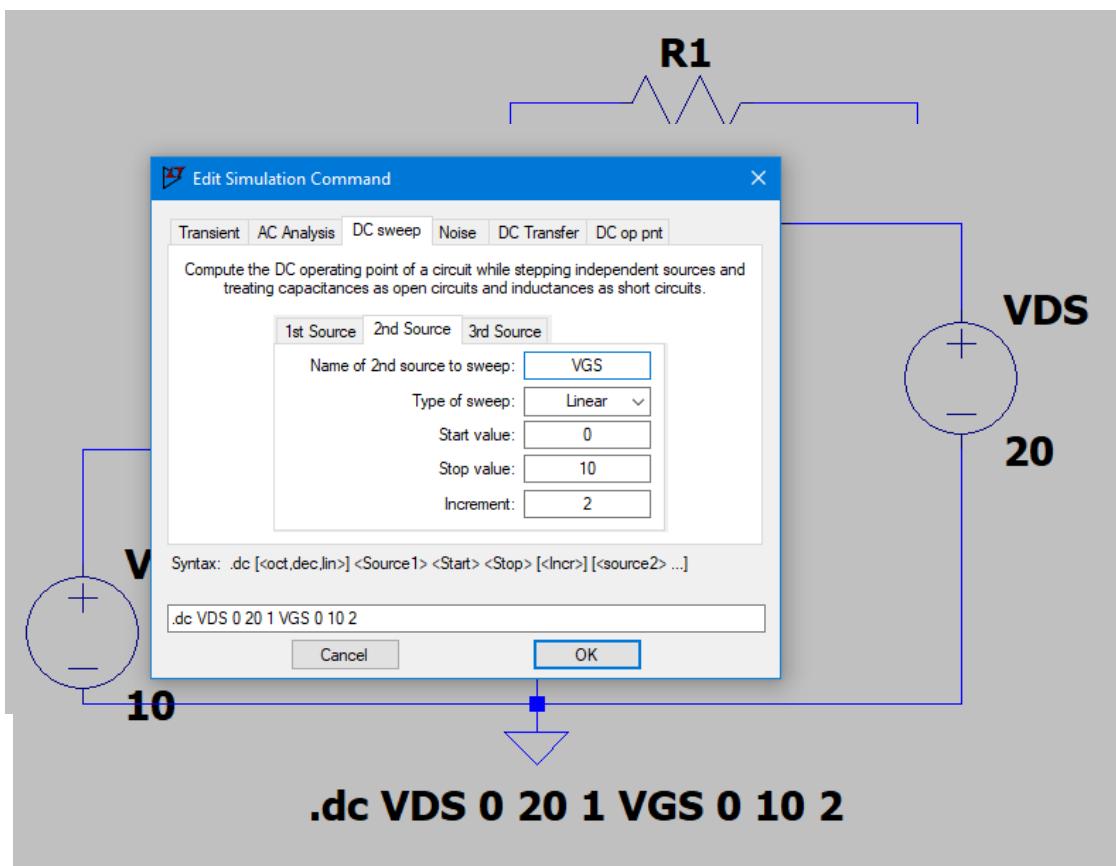


4. Configure the power sources and components following the guidelines in video.



5. Configure the simulation command for transient response characteristics.
a) For Drain characteristics

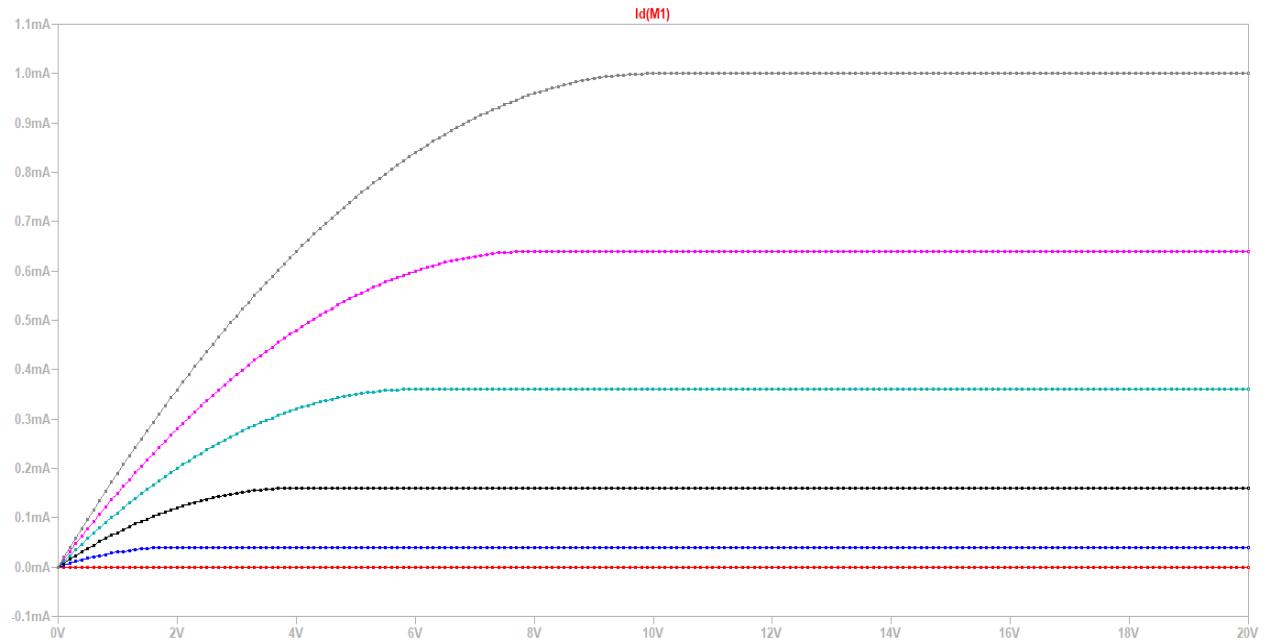




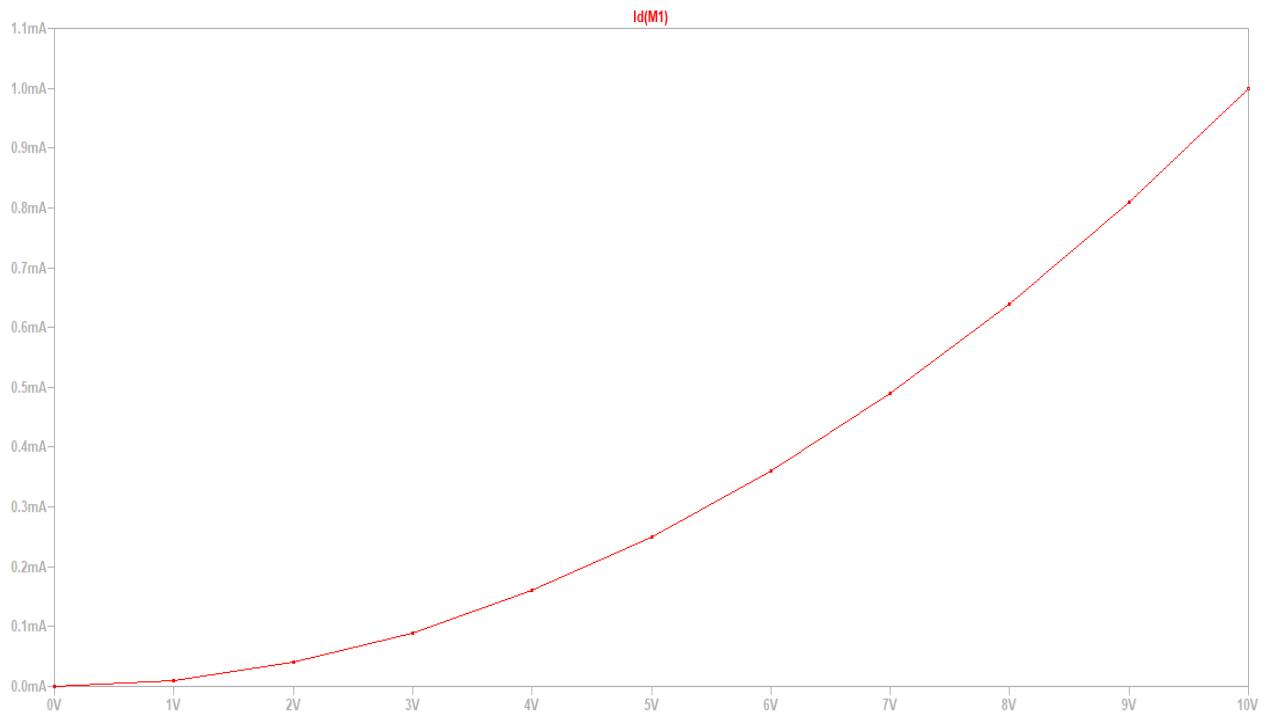
b) Transfer Characteristics:

6. Simulate by clicking the “RUN” icon.

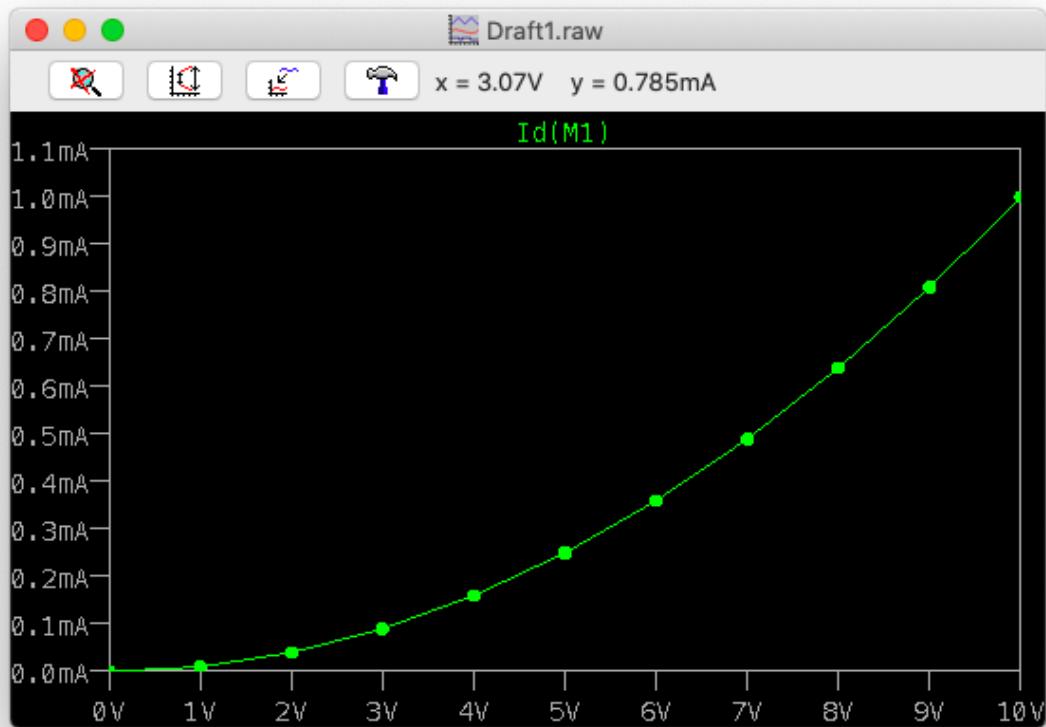
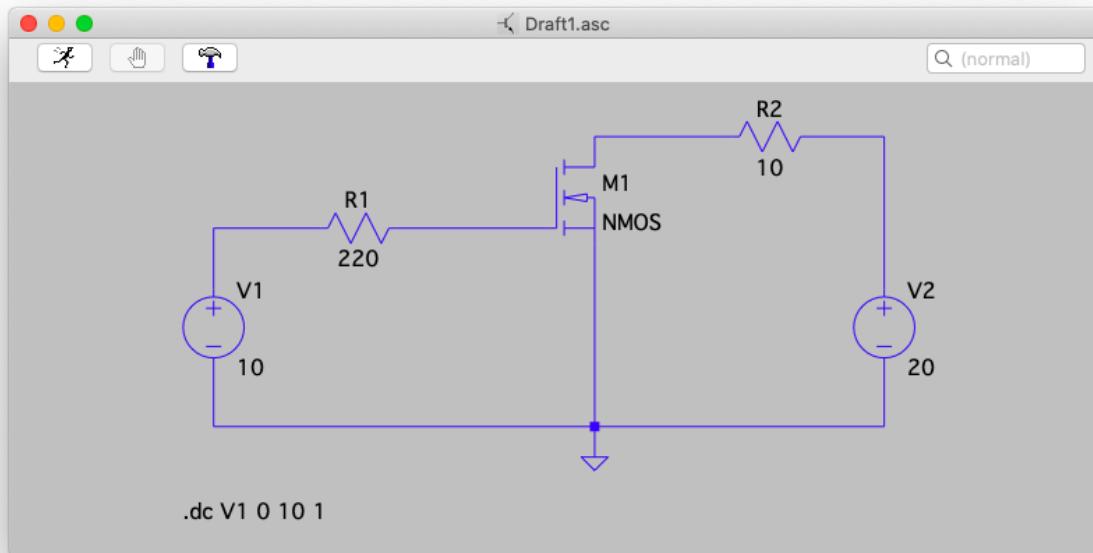
a) Drain Characteristics:

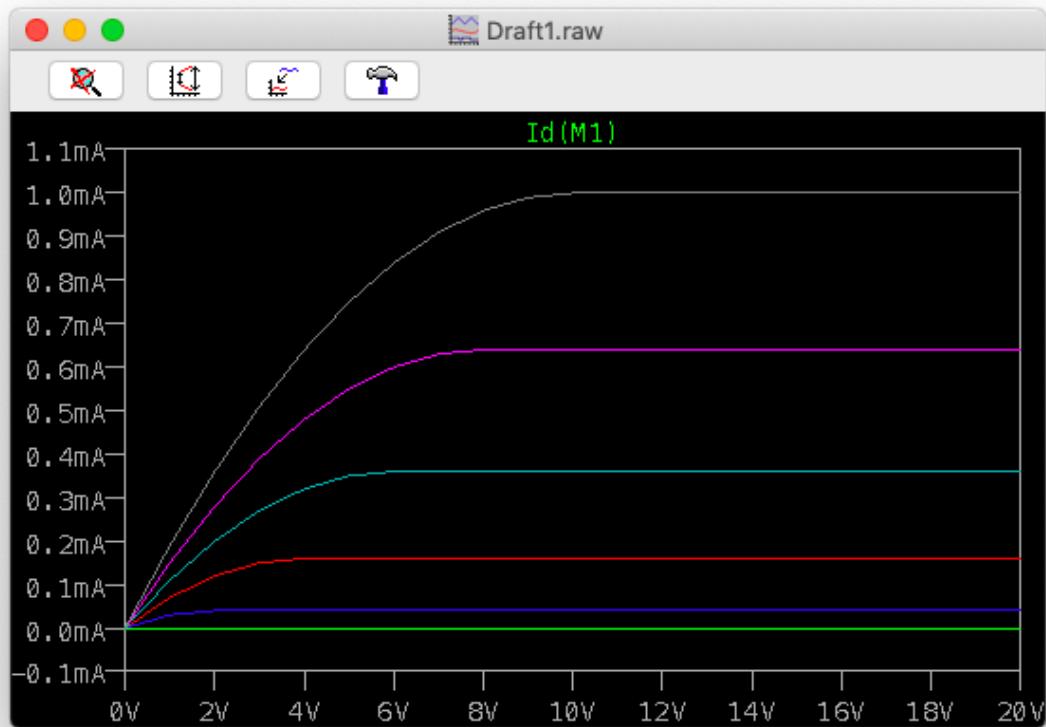
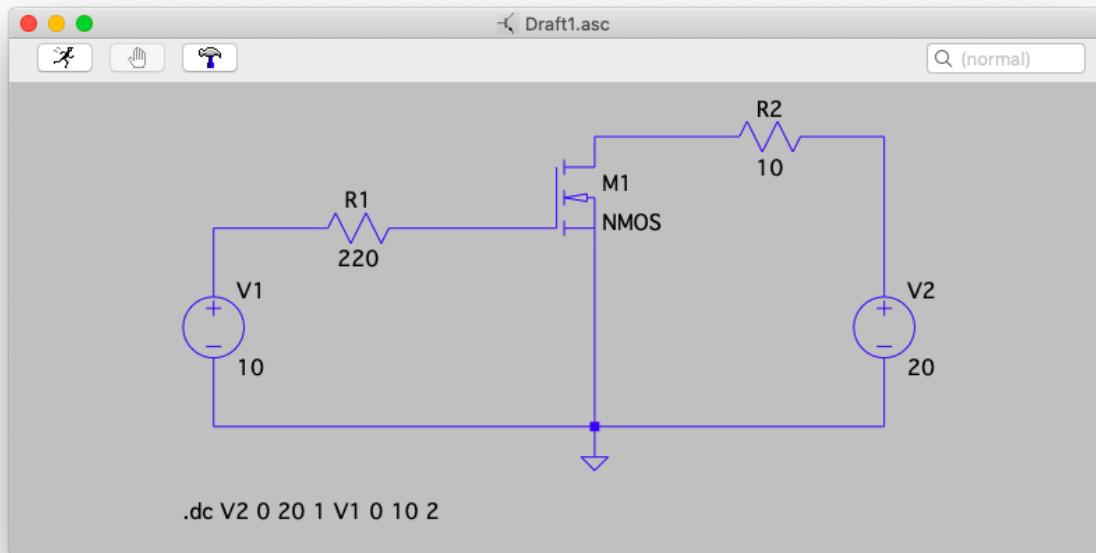


b) Transfer Characteristics:



RESULT :





Results and Inferences:

In this experiment, the characteristics of enhancement type n-channel MOSFET is studied theoretically and using LTSpice software. The transfer and drain characteristics of MOSFET were plotted using LTSpice.

Practical Applications:

MOSFETS are majorly used in switching applications from milliwatts to Megawatt power levels.

It is used in switched-mode power supplies, dc-dc converters, microinverters etc.

Course Outcome:

CO5. Analyze the characteristics of semiconductor devices and comprehend the various modulation techniques in communication engineering

Student Learning Outcomes (SLO):

SLO2. Having a clear understanding of the subject related concepts and of contemporary issues

Video Link:

Characteristics of MOSFET using LTSpice:

<https://youtu.be/ErpKbG7HCG0>

Power Factor Improvement In Single Phase Ac System

(PF Correction circuit in Rolling Mills)

Aim:

To calculate the capacitor value required to improve the Power Factor (PF) of a given single-phase AC system.

Software used:

LTS defense

THEORY:

The majority of the loads present in the industry are motors, lights, and computers. The current drawn by these loads are made up of real and reactive components. Loads such as a heater require the supply of only the real component of current. Some loads, such as an induction motor, require both real and reactive currents.

The real current is that component that is converted by the equipment into useful work such as the production of heat through a heater element. The unit of measurement of this current is ampere (A) and of power (voltage x real current) is watts (W).

The reactive current is that component that is required to produce the flux necessary for the functioning of induction devices. The current is measured in ampere (A) and the reactive power (voltage x reactive current) in VARs.

The total current is the algebraic sum of the real and reactive current, measured in amperes.

$$\text{Total Current} = \sqrt{(\text{Real current})^2 + (\text{Reactive current})^2}$$

The relation between the real, reactive, and total current is shown in Figure 1.

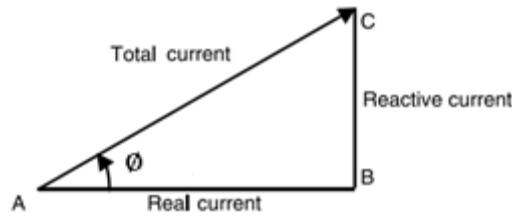


Figure 1

The power factor may be expressed as the ratio of the real current to the total current in a circuit. Alternatively, the power factor is the ratio of kW to total kVA:

$$\text{Power Factor} = \frac{\text{Real Current}}{\text{Total Current}} = \frac{kW}{kVA} = \frac{AB}{AC}$$

The angle ϕ is called the power factor angle. This is the angle included between the total current and the real current. The cosine of this angle ($\cos\phi$) is the power factor.

The concept of lagging PF:

The inductive load and its phasor diagram are shown in Figure 2. From the Figure 2, it is clear that both Watts and VARs are delivered from the source. The power factor angle in this case is negative, and therefore the power factor is lagging.

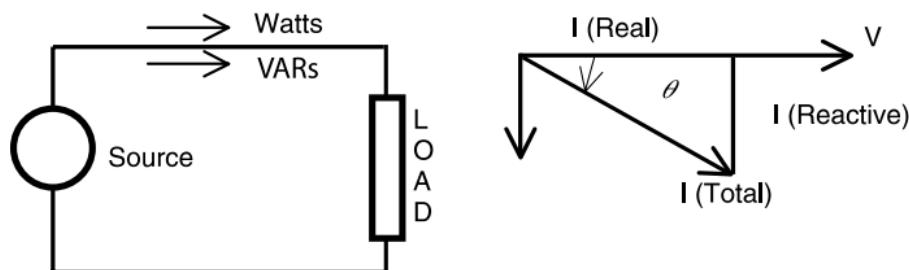


Figure 2. Inductive load and its phasor diagram

The Concept of Leading Power Factor:

Consider a capacitive load and its phasor diagram as shown in Figure 3. In this circuit, the watts are delivered from the source. The reactive power (VARs) is delivered from the load to the source. The power factor angle in this case is positive, and therefore the power factor is leading.

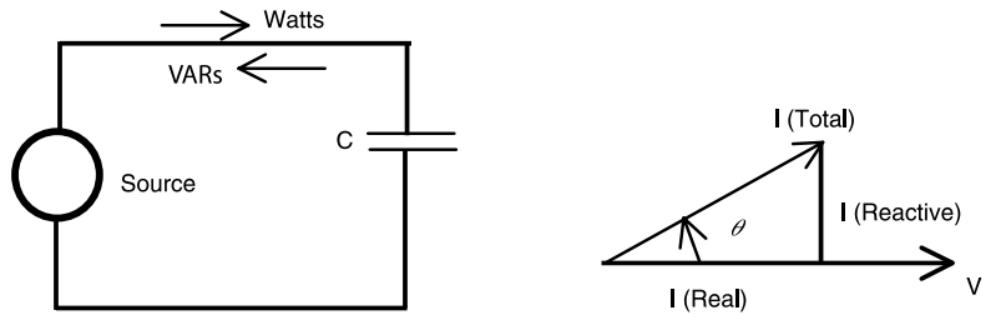
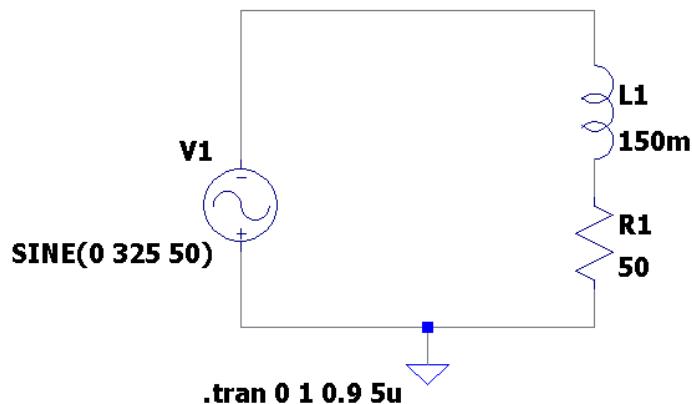


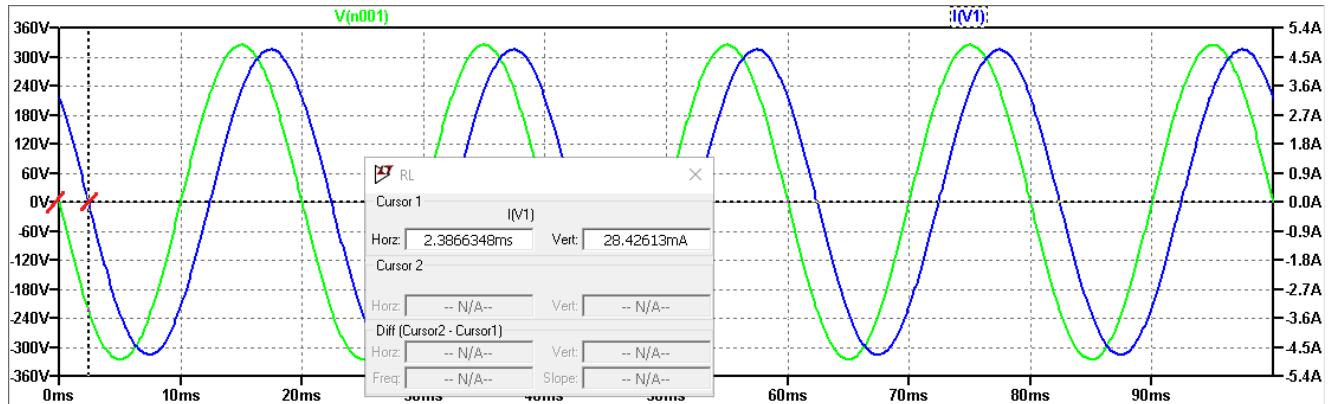
Figure 3. Capacitive load and its phasor diagram

Many utilities prefer a power factor of the order of 0.95. Since industrial equipment such as an induction motor operates at a much lower power factor, the overall power factor of the industrial load is low. In order to improve the power factor, capacitors are used. The shunt capacitors provide kVAR at leading power factor and hence the overall power factor is improved.

Calculation:

RL Circuit:





PF calculation of RL circuit from the observed reading:

The steps for calculating the PF of the RL circuit are as follows:

The time difference between voltage and current waveform = 2.4 ms (approx.)

Angular displacement between voltage and current waveform, $\phi = \omega t$ radians

$$\phi = \omega t$$

$$\phi = 2\pi ft$$

$$\phi = 2 \times 3.14 \times 50 \times 2.4 \times 10^{-3} \text{ radians}$$

$$\phi = 0.7536 \text{ radians}$$

$$\phi = 0.7536 \times (180/\pi) \text{ degrees}$$

$$\phi = 43.2 \text{ degrees}$$

Power factor of the RL circuit from the observed reading, $\cos\phi = \cos 43.2 = 0.728$
lagging

Actual PF of the RL circuit:

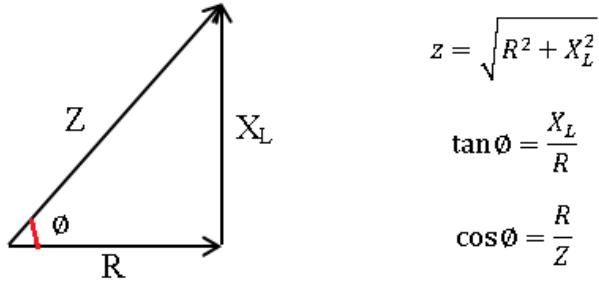
Inductive Reactance $X_L = 2\pi fL$, Ω

$$X_L = 2 \times 3.14 \times 50 \times 150 \times 10^{-3} = 47.1 \Omega$$

$$R = 50 \Omega$$

$$Z_{RL} = \sqrt{R^2 + X_L^2} = 68.69\Omega; \quad Z_{RL}=50+j47.1 \Omega; Z_{RL}=68.69 \angle 43.289^\circ$$

Impedance Triangle

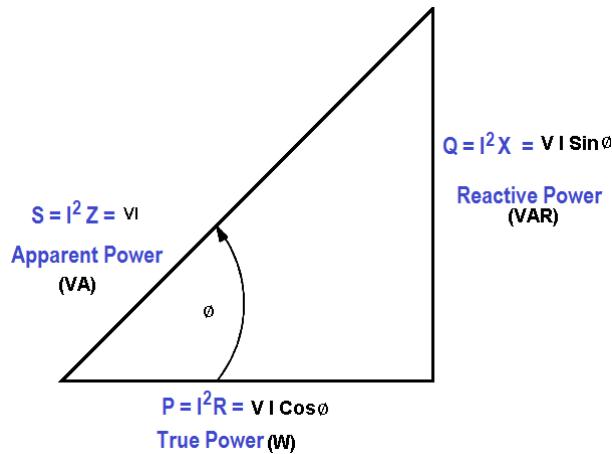


$$z = \sqrt{R^2 + X_L^2}$$

$$\tan \phi = \frac{X_L}{R}$$

$$\cos \phi = \frac{R}{Z}$$

Power triangle



The angular displacement between voltage and current waveform $\phi = \tan^{-1} \left(\frac{X_L}{R} \right)$

$$\phi = \tan^{-1} \left(\frac{47.1}{50} \right)$$

$$\phi = 43.28 \text{ degrees}$$

$$\cos \phi = 0.728 \text{ lagging}$$

(or)

$$I = \frac{V}{Z_{RL}} = \frac{230}{68.69} = 3.348 \text{ A}$$

True Power (P) = $VI\cos\phi=230\times3.348\times0.728=560.58$ W

Apparent Power(S)= $VI=230\times3.348=770.04$ VA

Power Factor=True Power/Apparent Power= $560.58/770.04=0.728$ lagging

PF verification of the RL circuit

PF of the RL Circuit	Observed	Actual
	$\cos\phi= 0.728$ lagging	$\cos\phi = 0.728$ lagging

From the above table it is clear that, the PF of RL circuit is low and to improve the PF it is necessary to include capacitor across the series combination of RL elements.

PF improvement:

Calculation of the capacitor value required to improve the PF

From the above power triangle

$$\text{Apparent Power } S = \frac{V^2}{Z}$$

$$S = \frac{230^2}{\sqrt{R^2 + X_L^2}}$$

$$S = \frac{230^2}{\sqrt{50^2 + 47.1^2}}$$

$$S = 770.12 \text{ VA}$$

$$X_C = \frac{V^2}{Q} = \frac{230^2}{VI\sin\phi} = 100.195 \Omega$$

$$C = \frac{1}{2\pi f X_C} = 31.785 \mu\text{F}$$

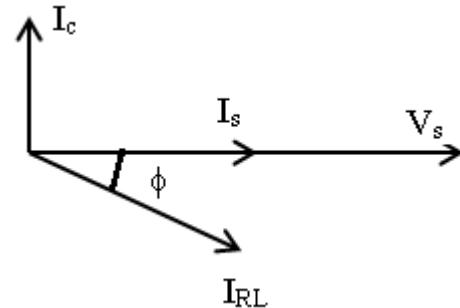
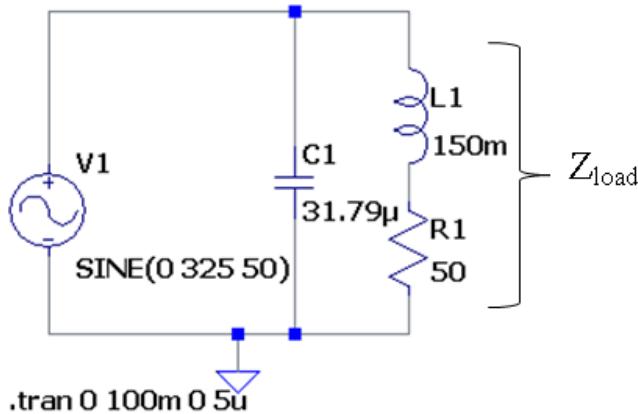
(or)

$$I_{RL} = \frac{230\angle 0}{Z_{RL}} = \frac{230\angle 0}{68.69\angle 43.289} = 3.34\angle -43.289 A = 2.4312 - j2.29 A$$

2.4312 A=Real Current; 2.29A = Reactive current

$$X_C = \frac{V}{I_C} = \frac{230}{2.29} = 100.43 \Omega; C = 31.71 \mu F$$

Alternate way of calculating Capacitor value required:



$$\frac{1}{Z_{eq}} = \frac{1}{Z_{load}} + \frac{1}{Z_c}$$

$$\frac{1}{Z_{eq}} - \frac{1}{Z_c} = \frac{1}{Z_{load}} = \frac{1}{R + j\omega} = \frac{R - j\omega}{(R + j\omega)(R - j\omega)}$$

$$\frac{1}{Z_{eq}} - \frac{1}{Z_c} = \frac{1}{Z_{load}} = \frac{R}{(R^2 + \omega^2 L^2)} - j \frac{\omega L}{(R^2 + \omega^2 L^2)}$$

Equating imaginary components

$$-\frac{1}{Z_c} = -j \frac{\omega L}{(R^2 + \omega^2 L^2)}$$

$$j\omega C = j \frac{\omega L}{(R^2 + \omega^2 L^2)}$$

$$C = \frac{L}{(R^2 + \omega^2 L^2)}$$

$$C = 31.79 \mu F$$

PF of compensated system:

Total impedance of the system $Z = \frac{Z_{RL} * Z_C}{Z_{RL} + Z_C}$

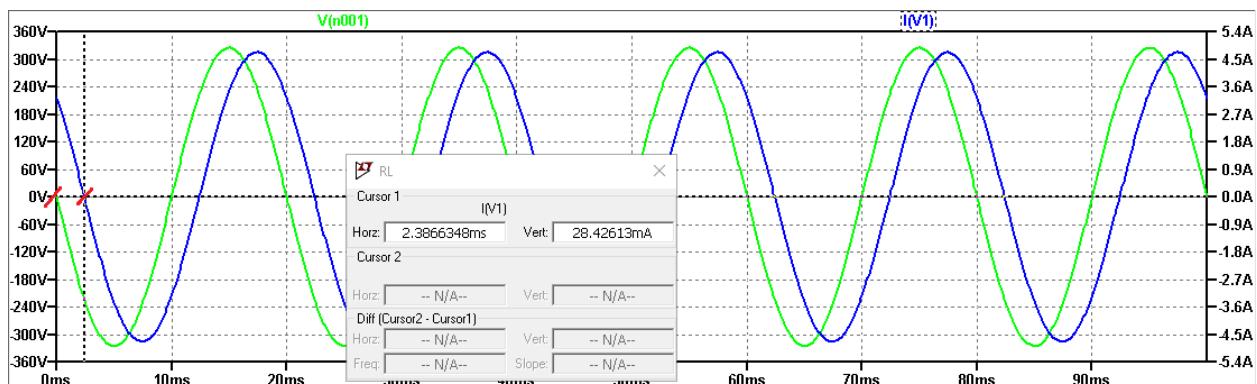
$$Z=94.36+j0.231; \quad Z=94.36\angle 0.1407$$

$$\text{Impedance angle } \phi=0.1407$$

$$\cos (0.1407) = 0.99$$

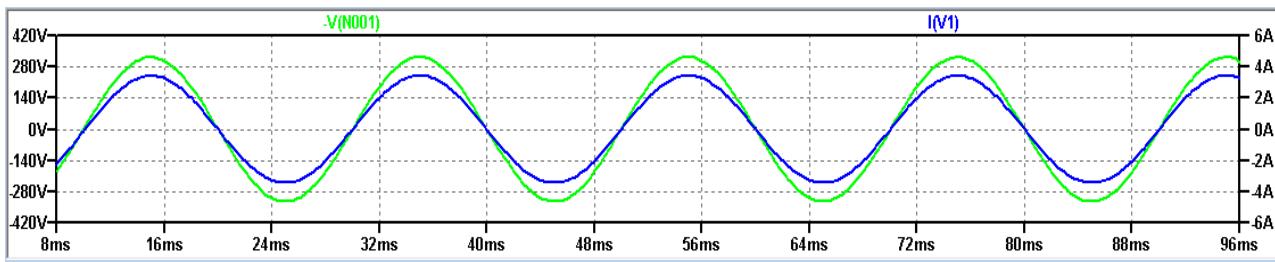
SIMULATION RESULTS:

Before PF improvement:



$$\cos \phi = 0.728$$

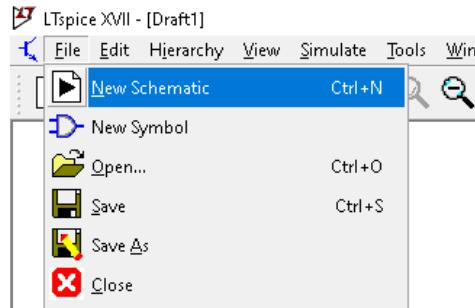
After PF improvement:



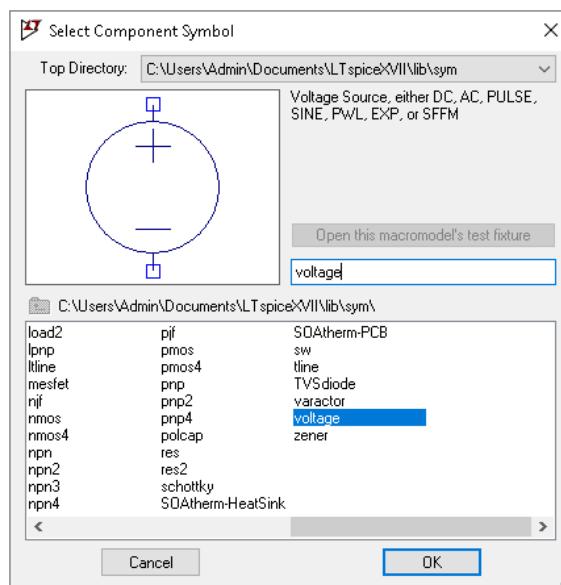
$$\cos \phi = 0.99$$

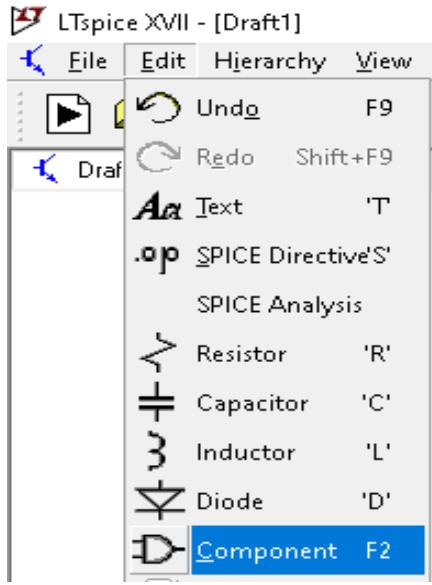
PROCEDURE

1. Open LTspice. Go to File menu and click on New Schematic.

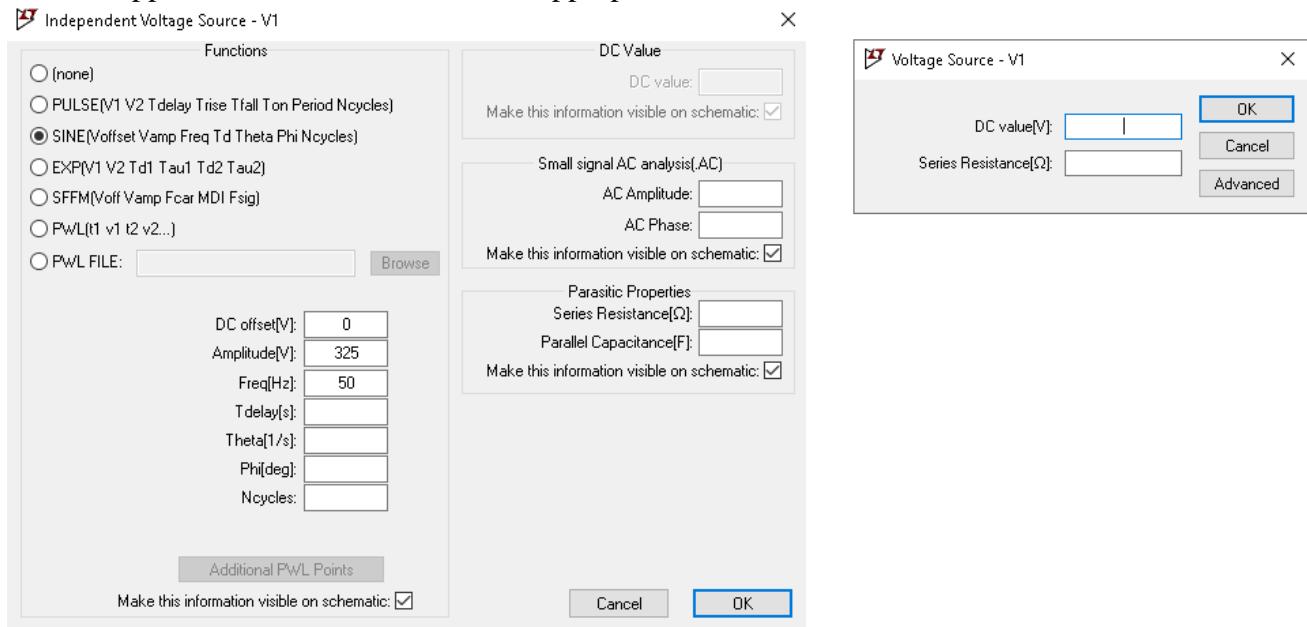


2. Go to Edit menu and click on component. Select voltage source and place it in the work area.

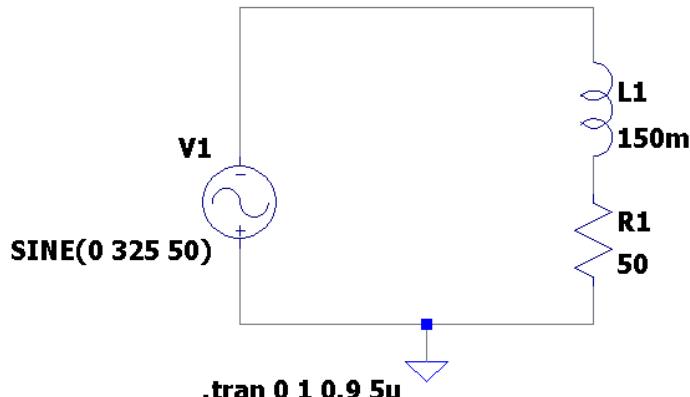




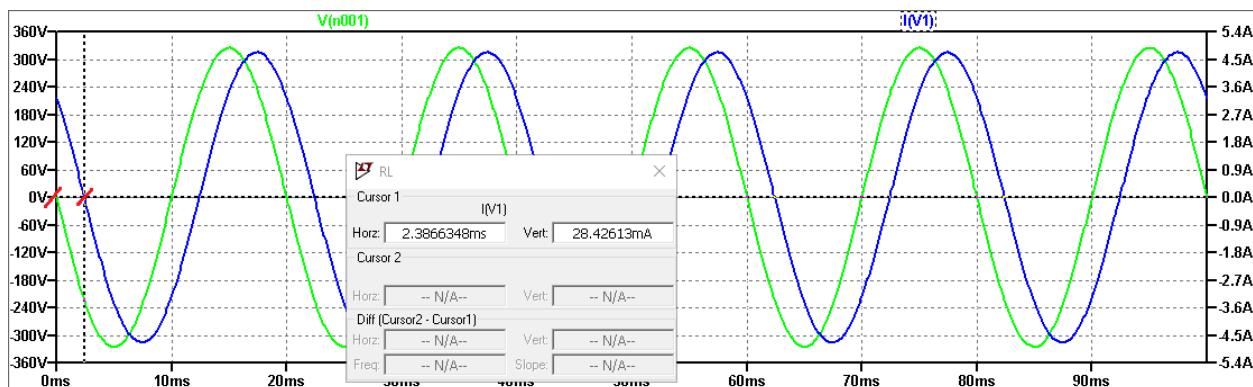
3. Right click on the voltage source block(V1) and click on advanced option. The following window appears, select SINE and fill the appropriate fields as shown below.



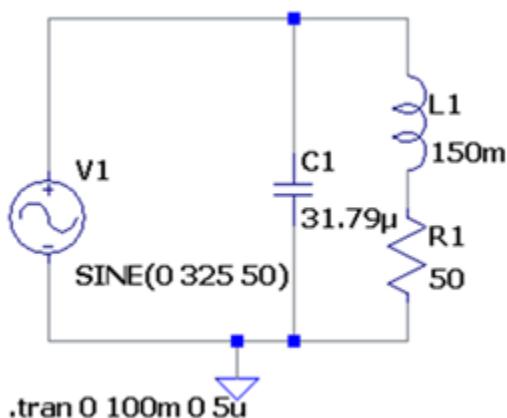
4. Similarly place the Resistor and Inductor in the work area either from the edit menu or from the tool bar present below the menu bar. Assign value to Resistor and Inductor by right clicking on it. Connect the components using wire and construct a circuit as shown below.



5. Run the circuit and display both source voltage and current waveforms on the same window. Click on $I(V1)$ get cursor and place it on the zero crossing to obtain the time difference between voltage and current waveforms as shown below.



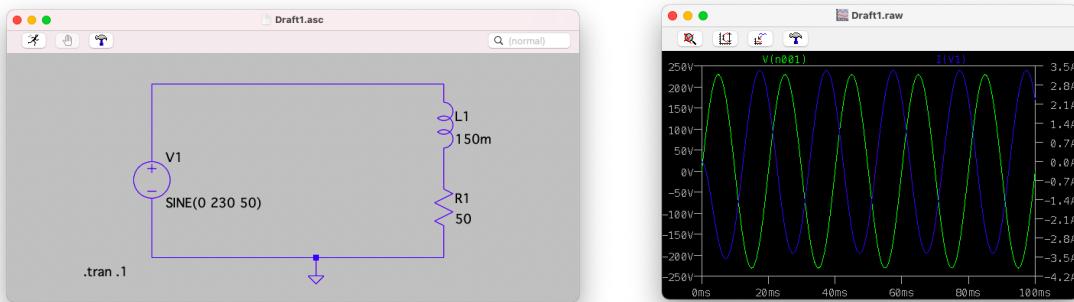
6. Follow the procedure given in calculation section to calculate the PF of uncompensated system and capacitor value required to improve the PF. Place the capacitor across the series combination on RL branch as shown below.



7. Run the circuit and verify the improvement in the PF value by following the steps given in calculation section.

Result:

Without Filter -



Time difference between the peaks of the voltage and the current wave forms = (25.01-17.46) ms

$$= 7.55 \text{ ms}$$

Angular displacement between voltage and current wave form, ϕ

$$= \omega t = 2\pi f t \text{ radians}$$

$$= 2 \times 3.14 \times 50 \times 7.55 \times 10^{-3} \text{ rad}$$

$$= 2.3707 \text{ rad}$$

$$\sim 2.4 \text{ rad}$$

$$= 137.57^\circ$$

Power factor = -0.738

Inductive reactance (X_L)

$$= 2\pi f L \Omega$$

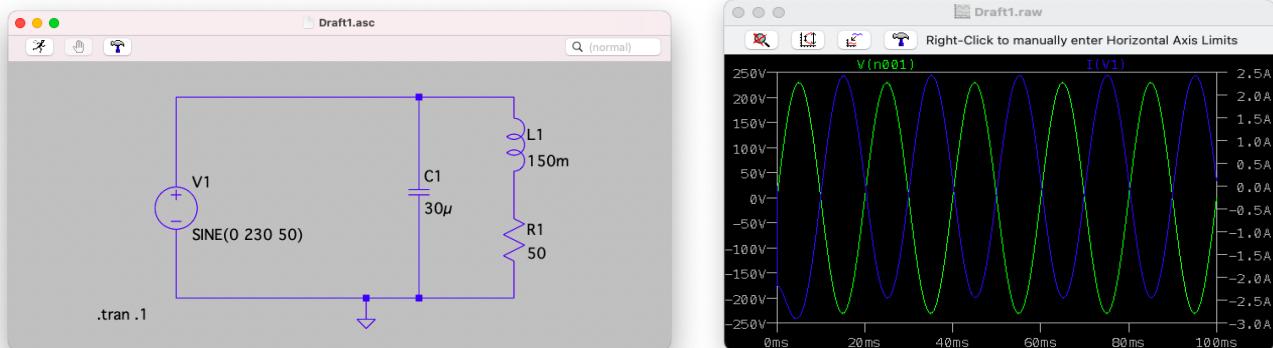
$$= 2 \times 3.14 \times 50 \times 150 \times 10^{-3} \Omega = 47.1 \Omega$$

Resistance = 50 Ω

$$Z_{RL} = \sqrt{(X_L^2 + R^2)} = 68.69 \angle 43.289^\circ$$

$$\text{Power factor} = \cos(\tan^{-1}(\frac{X_L}{R})) = 0.728 \text{ (lagging)}$$

With Filter –



Results and Inferences:

Practical Applications:

Used for PF correction in Industry

Course Outcome:

CO2. Analyze AC power circuits and networks, its measurement and safety concerns

Student Learning Outcomes (SLO):

SLO2. Having a clear understanding of the subject related concepts and of contemporary issues

SLO9. Having problem solving ability- solving social issues and engineering problems