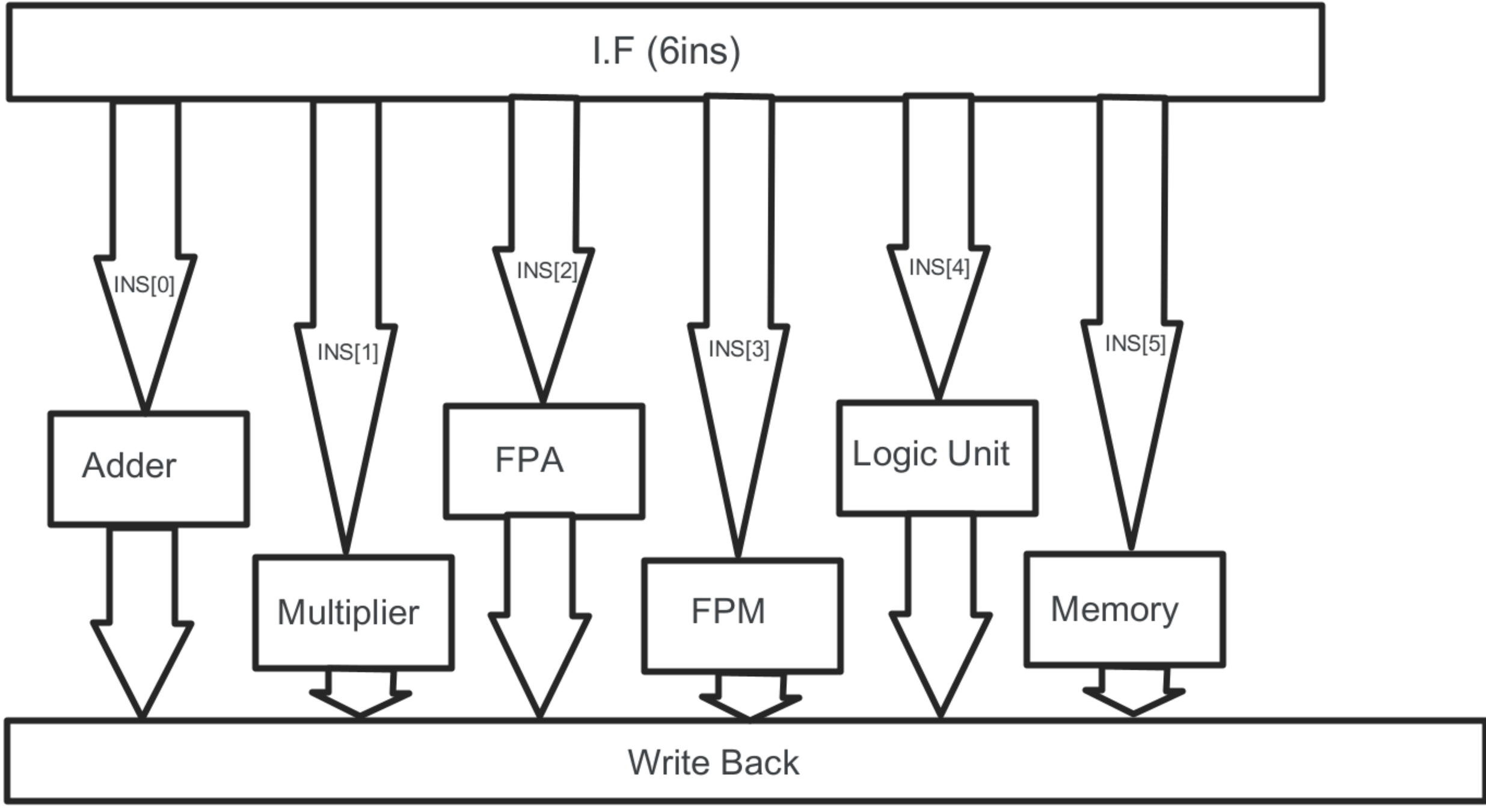
I.F (6ins)
INS[0]
INS[1]
INS[2]
INS[3]
INS[4]
INS[5]
Adder
Multiplier
FPA
FPM
Logic Unit
Memory
Write Back

Features

--> 3 Stage pipeline
--> 6 Instructions per cycle
--> 6 Functional units (IntAdd,IntMul,FPAdd,FPMul,LogicUnit,MemoryUnit)
--> All the units except Memory use register based addressing. Memory instructions use immediate operands only.
--> No Jump/Branch instruction is supported
--> Memory has been split into Instruction memory (6kB) and Data memory (4Kb)