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NAND Flash Interface Interoperability

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NAND FLASH INTERFACE INTEROPERABILITY

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NAND FLASH INTERFACE INTEROPERABILITY

(From JEDEC Board Ballot JCB-22-09, formulated under the cognizance of the JC-42.4 Subcommittee on Nonvolatile Memory Devices, item numbers 1863.02 and 1767.58).

1 Scope

This standard was jointly developed by JEDEC and the Open NAND Flash Interface Workgroup, hereafter referred to as ONFI. This standard defines a standard NAND flash device interface interoperability standard that provides means for system be designed that can support Asynchronous SDR, Synchronous DDR and Toggle DDR NAND flash devices that are interoperable between JEDEC and ONFI member implementations.

2 Terms, Definitions, Abbreviations, and Conventions

2.1 Terms and Definitions

address: A character or group of characters that identifies a register, a particular part of storage, or some other data source or destination. (Ref. ANSI X3.172 and JESD88.)

NOTE 1 In a nonvolatile memory array, the address consists of characters, typically hexadecimal, to identify the row and column location of the memory cell(s).

NOTE 2 For NAND nonvolatile memory devices, the row address is for a page, block, or logical unit number (LUN); the column address is for the byte or word within a page.

NOTE 3 The least significant bit of the column address is zero for the source synchronous data interface.

asynchronous: Describing operation in which the timing is not controlled by a clock.

NOTE For a NAND nonvolatile memory, asynchronous also means that data is latched with the WE_n signal for the write operation and the RE_n signal for the read operation.

block: A continuous range of memory addresses. (Ref. IEC 748-2 and JESD88.)

NOTE 1 The number of addresses included in the range is frequently equal to 2^n, where n is the number of bits in the address.

NOTE 2 For nonvolatile memories, a block consists of multiple pages and is the smallest addressable memory segment within a memory device for the erase operation.

column: In a nonvolatile memory array, a series of memory cells whose sources and/or drains are connected via a bit line.

NOTE 1 Depending on the nonvolatile memory array, the bit line is accessed via the column select transistor, the column address decoder, or other decoding scheme.

NOTE 2 In nonvolatile memory device, a column decoder accesses a bit (x1), byte (x8), word (x16), or Dword (x32) either individually or within a page.

NOTE 3 In a typical schematic of a memory array, the column is in the vertical direction.

2.1 Terms and Definitions (cont'd)

Dword (x32): A sequence of 32 bits that is stored, addressed, transmitted, and operated on as a unit within a computing system.

NOTE 1 A Dword may be represented as 32 bits, as two adjacent words, or as four adjacent bytes. When shown as bits, the least significant bit is bit 0 and the most significant bit is bit 31; the most significant bit is shown on the left. When shown as words, the least significant word (lower) is word 0 and the most significant (upper) word is word 1. When shown as bytes, the least significant byte is byte 0 and the most significant byte is byte 3.

NOTE 2 See Figure 2.5-1 for a description of the relationship between bytes, words, and Dwords.

latching edge: The rising or falling edge of a waveform that initiates a latch operation.

NOTE 1 For a NAND nonvolatile memory, the latching edge is the edge of the CK or DQS signal on which the contents of the data bus are latched for the source synchronous data interface.

NOTE 2 For a NAND nonvolatile data cycle, the latching edge is both the rising and falling edges of the DQS signal.
NOTE 3 For a NAND nonvolatile command and address cycle, the latching edge for the source synchronous interface is the rising edge of the CK signal.

NAND defect area: A designated location within the NAND memory where factory defects are identified by the manufacturer.

NOTE 1 The location is a portion of either the first page and/or the last page of the factory-marked defect block, this defect area in each page is defined as (# of data bytes) to (# of data bytes + # of spare bytes -1).

NOTE 2 For an 8-bit data access NAND memory device, the manufacturer sets the first byte in the defect area of the first or last page of the defect block to a value of 00h.

NOTE 3 For a 16-bit data access NAND memory device, the manufacturer sets the first word in the defect area of the first or last page of the defect block to a value of 0000h.

NAND nonvolatile memory device: The packaged NAND nonvolatile memory unit containing one or more NAND targets.

NOTE This is referred to as "device" in this standard.

NAND row address: An address referencing the LUN, block, and page to be accessed.

NOTE 1 The page address uses the least significant row address bits.

NOTE 2 The block address uses the middle row address bits.

NOTE 3 The LUN address uses the most significant row address bits.

page: The smallest nonvolatile memory array segment, within a device, that can be addressed for read or program operations.

page register: A register used to transfer data from a page in the memory array for a read operation or to transfer data to a page in the memory array for a program operation.

read request (for a nonvolatile memory): A data output cycle request from the host that results in a data transfer from the device to the host.

source synchronous (for a nonvolatile memory): Describing an operation in which the strobe signal (DQS) is transmitted with the data to indicate when the data should be latched.

NOTE The strobe signal (DQS) is similar in concept to an additional data bus bit.

2.1 Terms and Definitions (cont'd)

status register (SR[x]): A register within a particular LUN containing status information about that LUN.

NOTE SR[x] refers to bit "x" within the status register.

target: A nonvolatile memory component with a unique chip enable (CE_n) select pin.

word (x16): A sequence of 16 bits that is stored, addressed, transmitted, and operated on as a unit within a computing system.

NOTE 1 A word may be represented as 16 bits or as two adjacent bytes. When shown as bits, the least significant bit is bit 0 and the most significant bit is bit 15; the most significant bit is shown on the left. When shown as bytes, the least significant byte (lower) is byte 0 and the most significant byte is byte 2.

NOTE 2 See Figure 2.5-1 for a description of the relationship between bytes, words, and Dwords.

2.2 Abbreviations

DDR: Abbreviation for "double data rate".

LUN (logical unit number): The minimum memory array size that can independently execute commands and report status.

N/A: Abbreviation for "not applicable". Fields marked as "na" are not used.

O/M: Abbreviation for Optional/Mandatory requirement. When the entry is set to "M", the item is mandatory. When the entry is set to "O", the item is optional.

2.3 Conventions

2.3.1 Active-low Signals

While the preferred method for indicating a signal that is active when low is to use the over-bar as in $\overline{CE}$, the difficulty in producing this format has resulted in several alternatives meant to be equivalents. These are the use of a CE reverse solidus (\ ) or the trailing underscore (_) following the signal name as in CE\ and CE_. In this publication "_n" is used to indicate an active low signal (i.e., an inverted logic sense).

2.3.2 Signal Names

The names of abbreviations, initials, and acronyms used as signal names are in all uppercase (e.g., CE_n). Fields containing only one bit are usually referred to as the "name bit" instead of the "name field". Numerical fields are unsigned unless otherwise indicated.

2.3.3 Precedence in Case of Conflict

If there is a conflict between text, figures, state machines, timing diagrams, and/or tables, the precedence shall be state machine, timing diagrams, tables, figures, and text.

2.4 Keywords

Several keywords are used to differentiate between different levels of requirements or suggestions.

mandatory: A keyword indicating items to be implemented as defined by a standard. Users are required to implement all such mandatory requirements to ensure interoperability with other products that conform to the standard.

may: A keyword that indicates flexibility of choice between stated alternatives or possibly nothing with no implied preference.

optional: A keyword that describes features that are not required by the specification. However, if any optional feature defined by the specification is implemented, that feature shall be implemented in the way defined by the specification.

reserved: A keyword indicating reserved bits, bytes, words, fields, and opcode values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this or other specifications. A reserved bit, byte, word, or field may be cleared to zero or in accordance with a future extension to this publication. A host should not read/use reserved information.

shall: A keyword indicating a mandatory requirement.

should: A keyword indicating flexibility of choice with a strongly preferred alternative. This is equivalent to the phrase "it is recommended".

2.5 Byte, Word, and Dword Relationships

Figure 2.5-1 illustrates the relationship between bytes, words, and Dwords

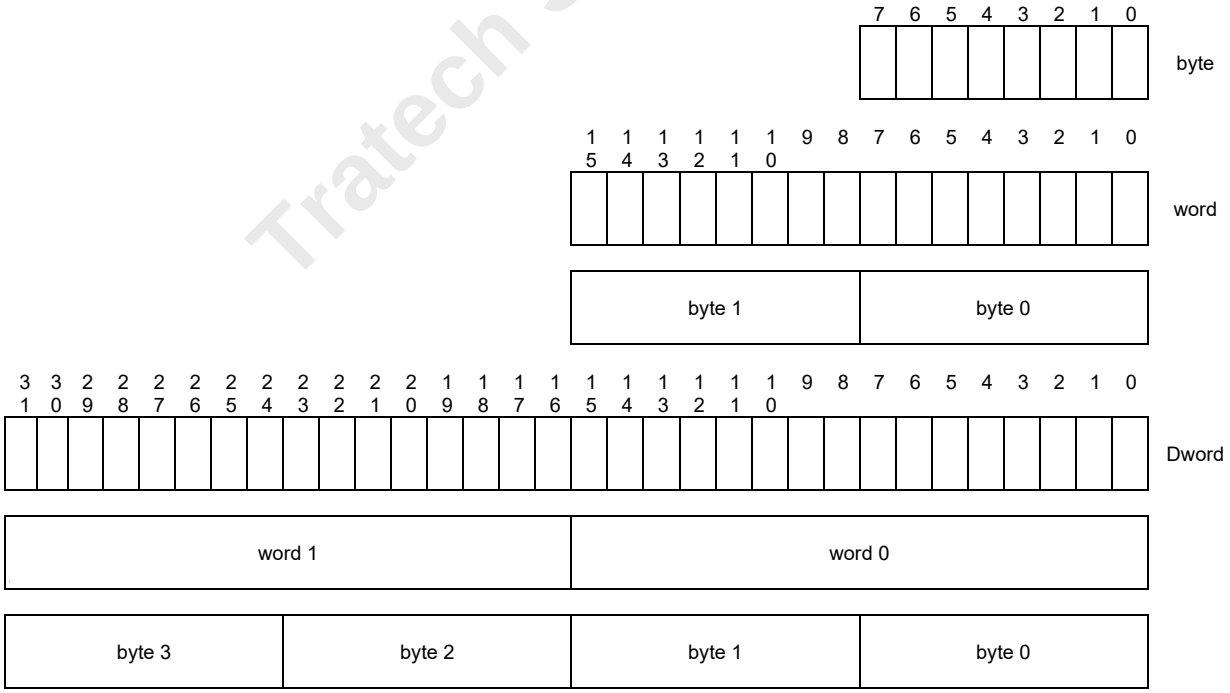


Figure 2.5-1 — Byte, Word, and Dword Relationships

2.6 Pin Description

Table 2.6-1 — Pin Description

Name	Input/ Output	Description
IO0 ~ IO7(~ IO15) DQ0 ~ DQ7 DQ0_x ~ DQ7_x	I/O	DATA INPUTS/OUTPUTS These signals are used to input command, address and data, and to output data during read operations. The signals float to high-z when the chip is deselected or when the outputs are disabled. IO0 ~ IO15 are used in a 16-bit wide target configuration. With multi channel support, IO0_0~IO7_0 and IO0_1~IO7_1 are used for IOs of channel 0 and IOs of channel 1 respectively. Also known as DQ0~DQ7 for Toggle DDR and Synchronous DDR. The number after the underscore represents the channel. For example, DQ0_0 indicates DQ0 of channel-0 and DQ0_1 does DQ0 of channel-1.
CLE_x	I	COMMAND LATCH ENABLE The CLE_x signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data).
ALE_x	I	ADDRESS LATCH ENABLE The ALE_x signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data).
CEx_x_n	I	CHIP ENABLE The CEx_x_n input is the target selection control. When CEx_x_n is high and the target is in the ready state, the target goes into a low-power standby state. When CEx_x_n is low, the target is selected.
WE_x_n	I	WRITE ENABLE The WE_x_n input controls writes to the I/O port. For Asynchronous SDR Data, commands, addresses are latched on the rising edge of the WE_x_n pulse. For Toggle DDR commands, addresses are latched on the rising edge of the WE_x_n pulse.
R/B_x_n	O	READY/BUSY OUTPUT The R/B_x_n output indicates the status of the target operation. When low, it indicates that one or more operations are in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
RE_x_n (RE_x_t)	I	READ ENABLE The RE_x_n input is the serial data-out control. For Asynchronous SDR Data is valid tREA after the falling edge and for Toggle DDR Data is valid after the falling edge and rising edge of RE_x_n which also increments the internal column address counter by each one.
RE_x_c	I	Complement of Read Enable This is the complementary signal to Read Enable
DQS_x (DQS_x_t)	I/O	Data Strobe The data strobe signal that indicates the data valid window for Toggle DDR and Synchronous DDR data interface. Output with read data, input with write data. Edge-aligned with read data, centered in write data.
DQS_x_c	I/O	Complement of Data Strobe This is the complementary signal to Data Strobe.
DBI_x	I/O	Data Bus Inversion Optional pin/function for NAND device to reduce power consumption and power/noise during data input/output. The device supporting DBI shall have DBI pin to designate if the DQ signals are inverted by transmitter side or not.

Table 2.6-1 — Pin Description (cont'd)

Name	Input/ Output	Description
W/R_x	I	Write/Read Direction The Write/Read Direction signal indicates the owner of the DQ bus and DQS signal in the Synchronous DDR data interface. This signal shares the same pin as RE_x_n in the asynchronous data interface.
CK_x	I	Clock The Clock signal is used as the clock in Synchronous DDR data interface. This signal shares the same pin as WE_x_n in the asynchronous data interface.
WP_x_n[3,4]	I	WRITE PROTECT The WP_x_n disables the Flash array program and erase operations.
ODT_x_n[3,4]	I	ODT (On Die Termination) Pin This signal enables and disables termination on the NAND DQ, DQS, RE bus according to the specified set feature settings.
Vcc	I	POWER VCC is the power supply for device.
VccQ	I	I/O POWER The VccQ is the power supply for input and/or output signals.
Vss	I	GROUND The Vss signal is the power supply ground.
VssQ	I	I/O GROUND The VssQ signal is the ground for input and/or output signals
VSPx	n/a	Vendor Specific The function of these signals is defined and specified by the NAND vendor. Any VSP signal not used by the NAND vendor shall not be connected internal to the device.
VREFQ	n/a	Reference voltage This is used as an external voltage reference.
V_{PP}	I	High Voltage Power The V_{PP} signal is an optional external high voltage power supply to the device. This high voltage power supply may be used to enhance Erase and Program operations (e.g. improve power efficiency)
RZQ_x	Supply	Reference pin for ZQ calibration This is used on ZQ calibration and RZQ ball shall be connected to Vss through 300ohm resistor
ENi / ENo	I/O	Enumeration pins These pins may be used for ONFI NAND
R	n/a	Reserved. These pins shall not be connected by host.
RFU	n/a	Reserved for Future Use These pins may be assigned for certain functions in the future
NU	n/a	Not Usable A pin that is not to be used in normal applications and that may or may not have an internal connection.
NC	n/a	No (internal) connection A pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device, provided that the voltage applied to this terminal (by means of wiring) does not exceed the highest supply voltage rating of the circuit.

Table 2.6-1 — Pin Description (cont'd)

NOTE 1	All Vcc, VccQ and Vss pins of each device shall be connected to common power supply outputs.
NOTE 2	All Vcc, VccQ, Vss and VssQ shall not be disconnected.
NOTE 3	Some vendor define WP_x_n pin as multi-function. User can use ODT_x_n instead of WP_x_n via set-feature. The default mode of this multi-function pin is WP_x_n.
NOTE 4	WP/ODT mode selection should be set to WP before power-off to make the pin working as Write Protect for protecting against data corruption at power-off.

3 NAND Interface General Information

3.1 NAND Interface Spec Overview

Table 3.1-1 — NAND Interface Comparison Table

Interface Items	Toggle 4.0	ONFI 4.2	JESD230E	JESD230F
VCC	2.5 V/3.3 V (Optional)		2.5 V/3.3 V (Optional)	2.5 V/3.3 V (Optional)
VCCQ	1.2 V/1.8 V (Optional)		1.2 V	1.2 V
DQ (Bus Width)	x8		X8	X8
Max Data Rate	~1.2 Gbps	~1.6 Gbps	~2.4Gbps	~3.6 Gbps[7]
Vref	External VrefQ is Required > 200 Mbps		Internal VrefQ is allowed for CTT[2] > 200 Mbps, External VrefQ is optional for CTT[2] > 200 Mbps, Internal VrefQ is required for LTT[3]	Internal VrefQ is allowed for CTT[2] > 200Mbps, External VrefQ is optional for CTT[2] > 200Mbps, Internal VrefQ is required for LTT[3]
Input Path Topology	Matched DQS		Matched DQS	Matched DQS or Unmatched DQS (see vendor datasheet)
OCD Topology	HSUL[1]/CTT[2]		HSUL/CTT/LTT[1,2,3]	HSUL/CTT/LTT[1,2,3]
ODT[4] Control	ODT (nWP) pin	Matrix Termination	ODT (nWP) pin or Matrix Termination	ODT (nWP) pin or Matrix Termination
Ron CAL	ZQ		ZQ	ZQ
CMD/ADDR IO	SDR (nWE sync, ~100 MHz)	SDR (nWE sync, ~40 MHz)	SDR (nWE sync, ~40 MHz – ~100 MHz)	SDR (nWE sync, ~40 MHz – ~100 MHz)
DBI[5]	N/A		Optional	Optional
Training	Write/Read DQ/DCC[6]		Write/Read DQ/DCC/Internal VrefQ	Write/Read DQ/DCC/ Internal VrefQ WDCA (optional) Write Training Monitor (optional) Per-pin VrefQ Adjustment (optional)
Differential Signaling on Power-up	Disabled		Disabled	Vendor specific (see vendor datasheet)
Equalization	Not Required		Not Required	Optional and Vendor specific
Fast Set/Get Features	Not Supported		Not Supported	Optional

NOTE 1 HSUL: High Speed Unterminated Logic
NOTE 2 CTT: Center Tapped Termination
NOTE 3 LTT: Low Tapped Termination
NOTE 4 ODT: On Die Termination
NOTE 5 DBI: Data Bus Inversion
NOTE 6 DCC: Duty Cycle Correction
NOTE 7 3.6 GT/s is not mandatory, NAND vendors may only support up to 3.2GT/s (see vendor datasheet).

3.2 Supported Features and Operating Conditions Versus Data Transfer Rate

Table 3.2-1 — Supported Features and Operating Conditions Versus Data Transfer Rate

<table>
<tr><th colspan="3" rowspan="2">Feature</th><th>~200 Mbps</th><th>~400 Mbps</th><th>~800 Mbps</th><th>~1200 Mbps,
~1600 Mbps,
~1800 Mbps,
~2000 Mbps,
~2200 Mbps,
~2400 Mbps</th><th>~2800 Mbps,
~3200 Mbps,
~3600 Mbps</th></tr>
<tr><td colspan="5">VccQ</td><td colspan="2">1.2 V</td></tr>
<tr><td rowspan="4">I/O Type</td><td rowspan="2">Single-ended Signaling for DQS and RE[1, 2]</td><td>NAND</td><td>Supported</td><td colspan="4" rowspan="2">Not supported</td></tr>
<tr><td>Host</td><td>Optional</td></tr>
<tr><td rowspan="2">Differential Signaling for DQS and RE</td><td>NAND</td><td colspan="5">Supported</td></tr>
<tr><td>Host</td><td>Optional</td><td colspan="4">Required</td></tr>
<tr><td colspan="3" rowspan="2">ZQ Calibration</td><td>NAND</td><td colspan="5">Supported</td></tr>
<tr><td>Host</td><td colspan="2">Optional</td><td colspan="3">Required</td></tr>
<tr><td colspan="3" rowspan="2">Training (DCC)</td><td>NAND</td><td colspan="3" rowspan="2">Not supported</td><td colspan="2" rowspan="2">Required</td></tr>
<tr><td>Host</td></tr>
<tr><td colspan="3" rowspan="2">Training (Read)</td><td>NAND</td><td colspan="5">Supported</td></tr>
<tr><td>Host</td><td colspan="3">Optional</td><td colspan="2">Required</td></tr>
<tr><td colspan="3" rowspan="2">Training (Write)</td><td>NAND</td><td colspan="5">Supported</td></tr>
<tr><td>Host</td><td colspan="3">Optional for Matched DQS NAND,
Required for Unmatched DQS NAND</td><td colspan="2">Required for both Unmatched DQS and Matched DQS NAND</td></tr>
<tr><td colspan="3" rowspan="2">Training (WDCA)</td><td>NAND</td><td colspan="5">Optional</td></tr>
<tr><td>Host</td><td colspan="5">Optional</td></tr>
<tr><td rowspan="4">On Die (NAND) Termination</td><td rowspan="2">CTT</td><td>NAND</td><td colspan="5">Supported</td></tr>
<tr><td>Host</td><td colspan="5">Optional[3]</td></tr>
<tr><td rowspan="2">LTT</td><td>NAND</td><td colspan="5">Supported</td></tr>
<tr><td>Host</td><td colspan="5">Optional[3]</td></tr>
<tr><td colspan="3" rowspan="2">Equalization</td><td>NAND</td><td colspan="5">Optional and Vendor Specific</td></tr>
<tr><td>Host</td><td colspan="5">Optional and Vendor Specific</td></tr>
</table>

NOTE 1 For CTT mode, the device can be used up to 200 Mbps without Differential Signals. To use high speed over 200 Mbps,
NOTE 2 Differential Signals shall be used and asserted before High-speed setting.
NOTE 3 For LTT mode, Differential Signaling is always required, even below 200 Mbps. Host can enable/disable On Die (NAND) Termination.

3.3 Supported VrefQ Versus Data Transfer Rate

Table 3.3-1 — Supported VrefQ Versus Data Transfer Rate

Feature				~60 Mbps	~80 Mbps	~200 Mbps	> 200 Mbps
VrefQ	CTT[1]	Internal VrefQ (Default Level)	NAND	Supported	Not Supported		
			Host				
		Internal VrefQ (VccQ/2 setting)	NAND	Optional			Optional[2]
			Host	Optional			
		External VrefQ (VccQ/2)	NAND	Optional[2]			
			Host				
	LTT[3]	Internal VrefQ	NAND	Supported			
			Host				
		External VrefQ	NAND	Not Supported			
			Host				

NOTE 1 The host and NAND shall power-up with the CTT interface enabled and with Internal VrefQ. The maximum data rate supported with the default internal VrefQ setting is only up to ~60Mbps and further initialization may be done at a faster data rate (up to ~200Mbps) on the CTT interface, provided that either the Internal VrefQ is configured to VccQ/2 or External VrefQ has been enabled for use on both the NAND and the Host.

NOTE 2 NAND External VrefQ support is optional. In the case where NAND support for External VrefQ has been removed, then NAND shall use Internal VrefQ, and the NAND vendor may recommend an Internal VrefQ setting that shall be used for high speed CTT interface operations or may require CTT interface Internal VrefQ training. If a device does not support >200Mbps operations with Internal VrefQ, then External VrefQ shall be required for >200Mbps operations

NOTE 3 The host shall ensure that the NAND internal VrefQ is within the NAND Minimum Internal VrefQ Allowable Range allowed for the LTT interface prior to enabling the LTT interface, and at any time while the LTT interface is active. External VrefQ shall always be disabled when the device runs in LTT mode.

4 Physical Interface

4.1 Input Specifications

4.1.1 AC/DC Levels

4.1.1.1 Combo Interface Devices

4.1.1.1.1 CTT Interface (1.2 V VccQ) AC/DC Levels

Table 4.1-1 — CTT Interface Single-Ended AC and DC Input Levels for Control and DQ-related Signals

Parameter	Symbol	Up to 1200 Mbps	>1200 Mbps up to 1800 Mbps	2000 Mbps, 2200 Mbps, 2400 Mbps 2800 Mbps, 3200 Mbps	3600 Mbps	Notes	Unit
DC input high for control signals	V_{IH}.CNT(DC)	0.7*VccQ			0.7*VccQ	1	V
DC input low for control signals	V_{IL}.CNT(DC)	0.3*VccQ			0.3*VccQ		
AC input high for control signals	V_{IH}.CNT(AC)	0.8*VccQ			0.8*VccQ		
AC input low for control signals	V_{IL}.CNT(AC)	0.2*VccQ			0.2*VccQ		
DC input high for DQ-related signals w/o V_{REFQ}	V_{IH}.DQrel (DC)	0.7*VccQ			0.7*VccQ	2, 3	
DC input low for DQ-related signals w/o V_{REFQ}	V_{IL}.DQrel (DC)	0.2*VccQ			0.2*VccQ		
AC input high for DQ-related signals w/o V_{REFQ}	V_{IH}.DQrel (AC)	0.8*VccQ			0.8*VccQ		
AC input low for DQ-related signals w/o V_{REFQ}	V_{IL}.DQrel (AC)	0.1*VccQ			0.1*VccQ		
DC input high for DQ-related signals for Data Input w/ V_{REFQ}	V_{IH}.DQrel (DC)	V_{REFQ}+0.100	V_{REFQ}+0.100 (ONFI)	$V_{REF}Q$+0.08	$V_{REF}Q$+0.07	2, 4, 5	
			$V_{REF}Q$+0.08(Toggle)				
DC input low for DQ-related signals for Data Input w/ V_{REFQ}	V_{IL}.DQrel (DC)	V_{REFQ}-0.100	$V_{REF}Q$-0.100 (ONFI)	$V_{REF}Q$-0.08	$V_{REF}Q$-0.07		
			$V_{REF}Q$-0.08(Toggle)				
AC input high for DQ-related signals for Data Input w/ V_{REFQ}	V_{IH}.DQrel (AC)	V_{REFQ}+0.150	$V_{REF}Q$+0.150 (ONFI)	$V_{REF}Q$+0.100	$V_{REF}Q$+0.095		
			$V_{REF}Q$+0.100 (Toggle)				
AC input low for DQ-related signals for Data Input w/ V_{REFQ}	V_{IL}.DQrel (AC)	V_{REEFQ}-0.150	$V_{REF}Q$-0.150 (Toggle)	$V_{REF}Q$-0.100	$V_{REF}Q$-0.095		
			$V_{REF}Q$+0.100 (Toggle)				

Table 4.1-1 — CTT Interface Single-Ended AC and DC Input Levels for Control and DQ-related Signals (cont'd)

NOTE 1 Control signals are CE_n, WE_n, ODT_n/WP_n, ALE, and CLE.
NOTE 2 DQ-related signals are RE_t, RE_n, DQS_t, DQS_c and DQ[7:0] and DBI. For RE_t, RE_n, DQS_t, and DQS_c these are single-ended signal requirements.
NOTE 3 Specs apply to NAND command, address bus cycles and unterminated data input cycles.
NOTE 4 $V_{REF}Q$ may be External VrefQ or Internal VrefQ (if NAND device supports >200 Mbps with Internal VrefQ, see vendor datasheet).
NOTE 5 For DQ signals, at 1600 MT/s these specifications may be replaced by Rx Mask and VIHL_AC specifications (see vendor datasheet), but above 1600MT/s the Rx Mask and VIHL_AC specifications shall be used.

Table 4.1-2 — CTT Interface External Reference Voltage Requirements

Parameter	Symbol	Min	Max	Notes	Unit
External Reference Voltage	VREFQ(DC)	0.49*VccQ	0.51*VccQ	1	V
NOTE 1 See NAND vendor datasheet if External VrefQ is supported for CTT interface.					

Table 4.1-3 — CTT Interface Differential AC and DC Input Levels and Cross-Point

Parameter	Symbol	Up to 1200 Mbps	>1200 Mbps up to 1800 Mbps	2000 Mbps, 2200 Mbps, 2400 Mbps 2800 Mbps, 3200 Mbps	3600 Mbps	Notes	Unit
DC differential input	V_{ID} (DC)	0.200	0.200 (ONFI)	0.160	0.140	1	V
			0.160 (Toggle)				
AC differential input	V_{ID} (AC)	0.300	0.300 (ONFI)	0.200	0.190		
			0.200 (Toggle)				
AC differential input cross-point	V_{IX}	0.5xVccQ±0.120	0.5xVccQ±0.080	0.5xVccQ±0.080	0.5xVccQ±0.068	2	

NOTE 1 VID(DC) and VID(AC) specify the input differential voltage |VTR-VCP| required for switching where VTR is the 'true' input signal while VCP is the 'complementary' input signal. The minimum values are equal to VIH(DC) – VIL(DC) and VIH(AC) – VIL(AC), respectively.
NOTE 2 For CTT, the typical value of V_{IX} is expected to be about 0.5*VccQ of the transmitting device and V_{IX} is expected to track variations in VREFDQ. V_{IX} indicates the voltage at which differential input signals must cross.

4.1.1.1.2 LTT Interface (1.2 V VccQ) AC/DC Levels

Table 4.1-4 — LTT Interface Single-Ended AC and DC Input Levels for Control and DQ-Related Signals

Parameter	Symbol	<1600 Mbps	1600 Mbps, 1800 Mbps	2000 Mbps, 2200 Mbps, 2400 Mbps	2800 Mbps, 3200 Mbps	3600 Mbps	Notes	Unit
DC input high for control signals	V_{IH}.CNT(DC)	0.7*VccQ					1	V
DC input low for control signals	V_{IL}.CNT(DC)	0.3*VccQ						
AC input high for control signals	V_{IH}.CNT(AC)	0.8*VccQ						
AC input low for control signals	V_{IL}.CNT(AC)	0.2*VccQ						
DC input high for DQ-related signals (Unterminated)	V_{IH}.DQrel.unterm (DC)	0.5*VccQ					2, 3, 7	
DC input low for DQ-related signals (Unterminated)	V_{IL}.DQrel.unterm (DC)	0.080						
AC input high for DQ-related signals (Unterminated)	V_{IH}.DQrel.unterm (AC)	0.5*VccQ						
AC input low for DQ-related signals (Unterminated)	V_{IL}.DQrel.unterm (AC)	0.060						
DC input high for DQ-related signals w/ $V_{REF}Q$ (Terminated)	V_{IH}.DQrel (DC)	$Vcent\_DQ_{rel}$ + 0.080				$Vcent\_DQ_{rel}$ + 0.060	2, 4, 5	
DC input low for DQ-related signals w/ $V_{REF}Q$ (Terminated)	V_{IL}.DQrel (DC)	$Vcent\_DQ_{rel}$ - 0.080				$Vcent\_DQ_{rel}$ - 0.060		
AC input high for DQ-related signals w/ $V_{REF}Q$ (Terminated)	V_{IH}.DQrel (AC)	$Vcent\_DQ_{rel}$ + 0.100				$Vcent\_DQ_{rel}$ + 0.085	2, 4, 6	
AC input low for DQ-related signals w/ $V_{REF}Q$ (Terminated)	V_{IL}.DQrel (AC)	$Vcent\_DQ_{rel}$ - 0.100				$Vcent\_DQ_{rel}$ - 0.085		

Table 4.1-4 — LTT Interface Single-Ended AC and DC Input Levels for Control and DQ-Related Signals (cont'd)

NOTE 1 Control signals are CE_n, WE_n, ODT_n/WP_n, ALE and CLE.
NOTE 2 DQ-related signals are RE_t, RE_n, DQS_t, DQS_c, DQ[7:0] and DBI. For RE_t, RE_n, DQS_t and DQS_c these are single-ended signal requirements.
NOTE 3 Termination is disabled during command cycles, address cycles and during data input/output cycles when ODT from the NAND (target and non-target) and the controller are disabled.
NOTE 4 $Vcent\_DQ_{rel}$ shall be regarded as Vcent_RE, Vcent_DQS and Vcent_DQ for RE_t/RE_c, DQS_t/DQS_c, and DQ[7:0] signals, respectively.
NOTE 5 For DQ signals, DC signal requirements are replaced with the Rx Mask
NOTE 6 For DQ signals, AC signal requirements are replaced with the VIHL_AC specification.
NOTE 7 NAND vendors may support a higher VIL.DQrel.unterm or lower VIH.DQrel.unterm specification. See vendor datasheet.

Table 4.1-5 — LTT Interface Differential AC and DC Input Levels and Cross-Point

Parameter	Symbol	Up to 1800 Mbps	2000 Mbps, 2200 Mbps, 2400 Mbps	2800 Mbps, 3200 Mbps	3600 Mbps	Notes	Unit
DC differential input	V_{ID} (DC)	0.160	0.160	0.160	0.120	1	V
AC differential input	V_{ID} (AC)	0.200	0.200	0.200	0.170		
AC differential input cross-point	V_{IX}	VREFDQ ± 0.064	VREFDQ ± 0.064	VREFDQ ± 0.064	VREFDQ ± 0.054	2	

NOTE 1 VID(DC) and VID(AC) specify the input differential voltage |VTR-VCP| required for switching where VTR is the 'true' input signal while VCP is the 'complementary' input signal. The minimum values are equal to VIH(DC) – VIL(DC) and VIH(AC) – VIL(AC) respectively.
NOTE 2 For LTT, the typical value of V_{IX} is expected to be about VREFDQ of the NAND Flash Memory internal setting value by VREF Training and V_{IX} is expected to track variations in VREFDQ. VIX indicates the voltage at which differential input signals must cross.

4.1.1.2 Legacy CTT-only Devices

Table 4.1-6 — Single-Ended AC and DC Input Levels for Control Signals[1] and DQ-related Signals[2]

Parameter	Symbol	Min.	Max.	Unit
DC input high for control signals[1]	VIH.CNT(DC)	$0.7*V_{CCQ}$	V_{CCQ}	V
DC input low for control signals[1]	VIL.CNT(DC)	V_{SSQ}	$0.3*V_{CCQ}$	
AC input high for control signals[1]	VIH.CNT(AC)	$0.8*V_{CCQ}$	Overshoot spec	
AC input low for control signals[1]	VIL.CNT(AC)	Undershoot spec	$0.2*V_{CCQ}$	
DC input high for DQ-related signals[2] without VREFQ	VIH.DQ(DC)	$0.7*V_{CCQ}$	V_{CCQ}	
DC input low for DQ-related signals[2] without VREFQ	VIL.DQ(DC)	V_{SSQ}	$0.3*V_{CCQ}$	
AC input high for DQ-related signals[2] without VREFQ	VIH.DQ(AC)	$0.8*V_{CCQ}$	Overshoot spec	
AC input low for DQ-related signals[2] without VREFQ	VIL.DQ(AC)	Undershoot spec	$0.2*V_{CCQ}$	
DC input high for DQ-related signals[2] with VREFQ (1.8 V VccQ)	VIH.DQ(DC)	Note 3	V_{CCQ}	
DC input low for DQ-related signals[2] with VREFQ (1.8 V VccQ)	VIL.DQ(DC)	V_{SSQ}	Note 3	
AC input high for DQ-related signals[2] with VREFQ (1.8 V VccQ)	VIH.DQ(AC)	Note 3	Note 3	
AC input low for DQ-related signals[2] with VREFQ (1.8 V VccQ)	VIL.DQ(AC)	Note 3	Note 3	
DC input high for DQ-related signals[2] with VREFQ 1.2 V VccQ)	VIH.DQ(DC)	V_{REFQ} +0.1	V_{CCQ}	
DC input low for DQ-related signals[2] with VREFQ (1.2 V VccQ)	VIL.DQ(DC)	V_{SSQ}	V_{REFQ} -0.1	
AC input high for DQ-related signals[2] with VREFQ (1.2 V VccQ)	VIH.DQ(AC)	V_{REFQ} +0.15	Overshoot spec	
AC input low for DQ-related signals[2] with VREFQ (1.2 V VccQ)	VIL.DQ(AC)	Undershoot spec	V_{REFQ} -0.15	

NOTE 1 Control signals are CE_n, WE_n, WP_n, ALE and CLE
NOTE 2 DQ-related signals are RE_n, DQS_n, DQs
NOTE 3 Refer to vendor specification

4.1.1.2 Legacy CTT-only Devices (cont'd)

Table 4.1-7 — Single-Ended AC and DC Output Levels for Control Signals[1] and DQ-related Signals[2]

Parameter	Symbol	Min.	Max.	Unit
DC Output high for control signals	VOH.CNT(DC)	$0.7*V_{CCQ}$	-	V
DC Output low for control signals	VOL.CNT(DC)	-	$0.3*V_{CCQ}$	
AC Output high for control signals	VOH.CNT(AC)	$0.8*V_{CCQ}$	-	
AC Output low for control signals	VOL.CNT(AC)	-	$0.2*V_{CCQ}$	
AC Output high for DQ-related signals (1.2 V VccQ)	VOH.DQ(AC) (w/ termination)	$V_{TT} + 0.1*V_{CCQ}$	-	
AC Output low for DQ-related signals (1.2 V VccQ)	VOL.DQ(AC) (w/ termination)	-	$V_{TT} - 0.1*V_{CCQ}$	

NOTE 1 Control signals are R/B_n
NOTE 2 DQ-related signals are DQS_n, DQs

Table 4.1-8 — Differential AC and DC Input/Output Levels (1.2 V VccQ)

Parameter	Symbol	Min.	Unit
DC differential input[1]	VID(DC)	0.2	V
AC differential input	VID(AC)	0.3	
AC differential output	VOD(AC)	$0.2*V_{CCQ}$	

NOTE 1 VID(AC) specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the "true" input signal and V_{CP} is the "complementary" input signal. The minimum value is equal to $V_{IH}(AC) - V_{IL}(AC)$.

Table 4.1-9 — Differential Signals Cross Point (1.2 V VccQ)

Parameter	Symbol	Min.	Max.	Unit
AC differential input cross point[1]	V_{IX}	$0.5*V_{CCQ} - 0.12$	$0.5*V_{CCQ} + 0.12$	V
AC differential output cross point[2]	V_{OX}	$0.5*V_{CCQ} - 0.15$	$0.5*V_{CCQ} + 0.15$	

NOTE 1 The typical value of V_{IX} is expected to be about 0.5 * V_{CCQ} of the transmitting device and $V_{IX}(AC)$ is expected to track variations in V_{CCQ} . $V_{IX}(AC)$ indicates the voltage at which differential input signals must cross.
NOTE 2 V_{OX} shall be guaranteed only after ZQ calibration completed.

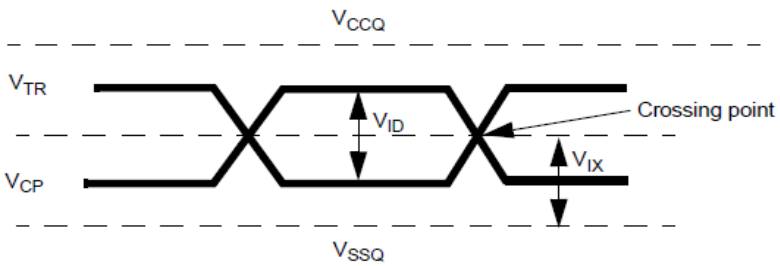


Figure 4.1-1 — Differential Signal Levels

4.1.2 NAND DQ Rx Mask Specifications

The DQ input receiver (Rx) mask defines the area that the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property and is not the valid data-eye. The DQ Rx mask for voltage and timing is shown in the figure below and is applied per individual DQ pin. The DQ Rx mask is evaluated at the die pads.

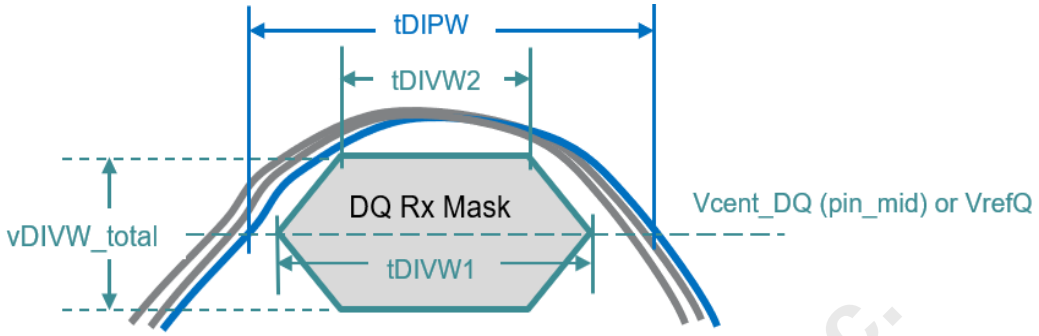


Figure 4.1-2 — DQ Rx Mask Definition

Table 4.1-10 — NAND CTT Interface Rx Mask Specifications

Interface	Parameter	Symbol	<1200 Mbps	1200 Mbps	1600 Mbps, 1800 Mbps	2000 Mbps, 2200 Mbps, 2400 Mbps, 2800 Mbps, 3200 Mbps	3600 Mbps	Unit
CTT	DQ Rx Mask Voltage Total	vDIVW_total	N/A	N/A	200	180	140	mV
	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) or VrefQ[1]	tDIVW1	N/A	N/A	0.48	0.48	0.48	UI
	DQ Rx Mask Timing[2] Window at Vcent_DQ (pin_mid) ± vDIVW_total/2	tDIVW2	N/A	N/A	0.30	0.30	0.30	UI
	DQ Input Pulse Width at Vcent_DQ (pin_mid) or VrefQ	tDIPW	0.62	0.66	0.66	0.66	0.66	UI

NOTE 1 Vcent_DQ (pin_mid) shall be replaced by VrefQ in the case where External VrefQ is used or Internal VrefQ without Vref training is used.
NOTE 2 At 1600Mbps, use of Rx mask specifications is optional, see vendor datasheet whether Rx mask specifications are supported by the device at that data rate.

4.1.2 NAND DQ Rx Mask Specifications (cont'd)

Table 4.1-11 — NAND LTT Interface Rx Mask Specifications

Interface	Parameter	Symbol	<1200Mbps	1200 Mbps, 1600 Mbps, 1800 Mbps	2000 Mbps, 2200 Mbps, 2400 Mbps	2800 Mbps, 3200 Mbps	3600 Mbps	Unit
LTT	DQ Rx Mask Voltage Total	vDIVW_ total	160	160			120	mV
	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid)	tDIVW1	0.48	0.48			0.48	UI
	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) ± vDIVW_total/2	tDIVW2	0.30	0.30			0.30	UI
	DQ Input Pulse Width at Vcent_DQ (pin_mid)	tDIPW	0.62	0.66			0.66	UI

4.1.3 Controller DQ Rx Mask Specifications

The Controller DQ RX Mask specifications in this section are applicable to controllers that support the data rates listed in Table 4.1-12 and Table 4.1-13.

Table 4.1-12 — Controller CTT Interface Rx Mask Specifications[1,2,3]

Interface	Parameter	Symbol	2000Mbps, 2200Mbps, 2400Mbps,	2800Mbps, 3200Mbps	3600Mbps	Unit
CTT	DQ Rx Mask Voltage Total	vDIVW_total	180	180	140	mV
	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) or VrefQ	tDIVW1	0.40	0.40	0.40	UI
	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) ± vDIVW_total/2	tDIVW2	0.25	0.25	0.25	UI
	DQ Input Pulse Width at Vcent_DQ (pin_mid) or VrefQ	tDIPW	0.50	0.50	0.50	UI

NOTE 1 Vcent_DQ (pin_mid) shall be replaced by VrefQ in the case where External VrefQ is used or Internal VrefQ without Vref training is used.
NOTE 2 At 1600Mbps, use of Rx mask specifications is optional, see vendor datasheet whether Rx mask specifications are supported by the device at that data rate.
NOTE 3 System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment.

4.1.3 Controller DQ Rx Mask Specifications (cont'd)

Table 4.1-13 — Controller LTT Interface Rx Mask Specifications[1]

Interface	Parameter	Symbol	2000Mbps, 2200Mbps, 2400Mbps	2800Mbps, 3200Mbps	3600Mbps	Unit
LTT	DQ Rx Mask Voltage Total	vDIVW_total	160	160	120	mV
	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid)	tDIVW1	0.40	0.40	0.40	UI
	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) ± vDIVW_total/2	tDIVW2	0.25	0.25	0.25	UI
	DQ Input Pulse Width at Vcent_DQ (pin_mid)	tDIPW	0.50	0.50	0.50	UI
NOTE 1 System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment.						

4.1.4 Vcent_DQ (pin_mid) Definition

Vcent_DQ (pin_mid) is defined as the midpoint between the largest Vcent_DQ voltage level and the smallest Vcent_DQ voltage level across all DQ pins for a given NAND die.

Each Vcent_DQ is defined by the center (i.e., widest opening) of the cumulative data input eye as depicted in Figure 4.1-3.

Since the DQ Rx mask is centered around Vcent_DQ (pin_mid), any pin-to-pin Vcent_DQ variation must be accounted for in the DQ Rx Mask.

Similarly, Vcent_RE_t, Vcent_RE_c, Vcent_DQS_t, and Vcent_DQS_c are defined by the center of the cumulative data input eye for RE_t, RE_c, DQS_t and DQS_c respectively. Vcent_RE_t and Vcent_RE_c are collectively denoted as Vcent_RE. Vcent_DQS_t and Vcent_DQS_c are collectively denoted as Vcent_DQS.

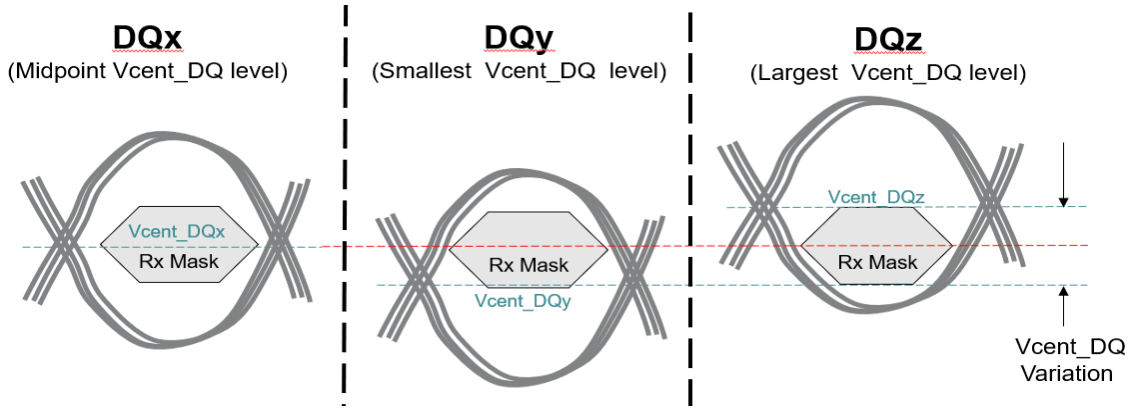


Figure 4.1-3 — Vcent_DQ (pin_mid) Definition

4.1.5 CTT and LTT Interface (1.2 V VccQ) VIHL_AC Definition

The minimum DQ AC input pulse amplitude (pk-pk) is given by the VIHL_AC specification.

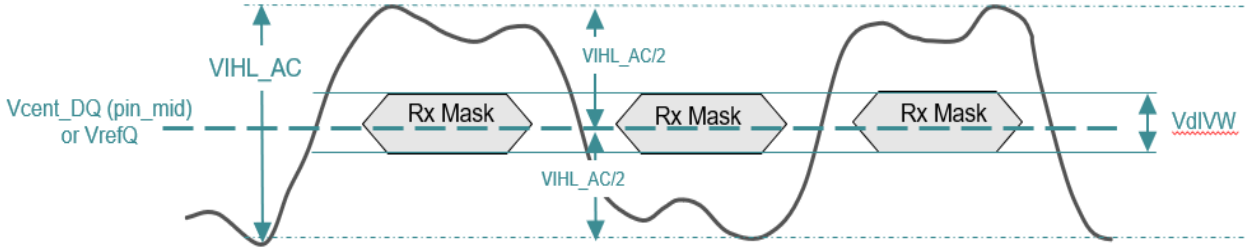


Figure 4.1-4 — VIHL_AC Definition

Table 4.1-14 — VIHL_AC CTT and LTT Interface (1.2 V VccQ) Specifications

Parameter	Symbol	Interface	Up to 1800 Mbps	2000 Mbps, 2200 Mbps, 2400 Mbps	2800 Mbps, 3200 Mbps	3600 Mbps	Notes	Unit
DQ AC input pulse amplitude pk-ok	VIHL_AC_CTT	CTT	220			190	1, 2, 3	mV
	VIHL_AC_LTT	LTT	200			170		

NOTE 1 The DQ only input pulse amplitude must meet or exceed VIHL_AC at any point over the total UI, except when no transitions are occurring for that UI.

NOTE 2 VIHL_AC is centered around Vcent_DQ (pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ (pin_mid). For CTT interface, Vcent_DQ (pin_mid) is replaced by VrefQ as the center reference level in the case where External VrefQ is used or Internal VrefQ without Vref training is used.

NOTE 3 There are no timing requirements above or below VIHL_AC levels.

4.1.6 NAND Minimum Internal VrefQ Allowable Range

Table 4.1-15 — NAND Minimum Internal VrefQ Allowable Range for NAND Devices that Support Internal VrefQ Value1 and Value2 Settings (1.2 V VccQ)

Interface	Parameter	Symbol	Min	Max	Notes	Unit
CTT	Minimum allowable range upper limit	VrefQ_CTT_HI	-	55%	1, 2, 3	VccQ
	Minimum allowable range lower limit	VrefQ_CTT_LO	45%	-		
LTT	Minimum allowable range upper limit	VrefQ_LTT_HI	-	40%		VccQ
	Minimum allowable range lower limit	VrefQ_LTT_LO	160	-		mV

NOTE 1 The host shall not set the NAND internal VrefQ to a setting beyond the allowable range even during Write Training Internal VrefQ training.
NOTE 2 These specs define the allowable range for NAND internal VrefQ settings but do not represent the needed settings for high speed operations. The needed settings for high-speed operations are obtained from either NAND vendor recommendation or through Internal VrefQ Training.
NOTE 3 Some NAND device may offer a wider allowable range. See vendor datasheet.

Table 4.1-16 — NAND Minimum Internal VrefQ Allowable Range for NAND Devices that Support Value3 Settings (1.2 V VccQ)

Interface	Parameter	Symbol	Min	Max	Notes	Unit
CTT	Minimum allowable range upper limit	VrefQ_CTT_HI	-	55%	1, 2, 3	VccQ
	Minimum allowable range lower limit	VrefQ_CTT_LO	45%	-		
LTT	Minimum allowable range upper limit	VrefQ_LTT_HI	-	31.75%		VccQ
	Minimum allowable range lower limit	VrefQ_LTT_LO	160	-		mV

NOTE 1 The host shall not set the NAND internal VrefQ to a setting beyond the allowable range even during Write Training Internal VrefQ training.
NOTE 2 These specs define the allowable range for NAND internal VrefQ settings but do not represent the needed settings for high speed operations. The needed settings for high-speed operations are obtained from either NAND vendor recommendation or through Internal VrefQ Training.
NOTE 3 Some NAND device may offer a wider allowable range. See vendor datasheet.

4.2 Output Specifications

4.2.1 Output Drive and ODT Strengths

4.2.1.1 Combo Interface Devices CTT Drive Strengths

Table 4.2-1— CTT Interface Allowed Pull-Down and Pull-Up Drive Strengths

R_{ONPD}, R_{ONPU}[1,2]	
[ohm]	**Unit**
25	RZQ/12
37.5 (Recommended Default)	RZQ/8
42.9	RZQ/7
50	RZQ/6
60	RZQ/5
75	RZQ/4
100	RZQ/3
150	RZQ/2
300	RZQ/1
NOTE 1 For R_{ONPD} and R_{ONPU} values, 37.5Ω and 50Ω are mandatory while the rest are vendor specific. NOTE 2 With ZQ Calibration, $R_{ONPD\ and}$ R_{ONPU} tolerance from the nominal value (when measured at 0.5*VccQ pad voltage) is ±15%	

4.2.1.2 Legacy CTT-Only Devices Interface Drive Strengths

The device may be configured with multiple driver strengths with 'SET FEATURE' command. There are Underdrive (i.e., 50 Ohm), Nominal (i.e., 35 Ohm or 37.5 Ohm), Overdrive 1(i.e., 25 Ohm) and Overdrive 2 (i.e., 18 Ohm) options. A NAND device supports Nominal and Underdrive as mandatory, and Overdrive1 and Overdrive2 as optional.

Table 4.2-2 — DQ Driver Strength Settings

Setting	Driver Strength
Overdrive 2	18 Ohms (Optional)
Overdrive 1	25 Ohms (Optional)
Nominal	35 Ohms or 37.5 Ohms
Underdrive	50 Ohms

4.2.1.3 LTT Interface Drive Strengths

4.2.1.3.1 LTT Interface Pull-Down

Table 4.2-3 — LTT Interface Allowed Pull-Down Drive Strengths

R_{ONPD}	
[ohm]	**Unit**
25	RZQ/12
37.5 (PDDS Location2 Default)	RZQ/8
42.9	RZQ/7
50 (PDDS Location1 Default)	RZQ/6
60	RZQ/5
75	RZQ/4
100	RZQ/3
150	RZQ/2
300	RZQ/1

NOTE 1 For R_{ONPD} values, 37.5 Ω and 50 Ω are mandatory while the rest are vendor specific.
NOTE 2 With ZQ Calibration, R_{ONPD} tolerance from the nominal value is ±15% (when measured at a pad voltage of VOH_nom).
NOTE 3 The default value when PDDS bit locations are in Location1 (see Feature Address 22h) is 50 Ω while the default value when PDDS bit locations are in Location2 (see Feature Address 10h) is 37.5 Ω.
NOTE 4 Since the default output pull-down drive strength values may be different among NAND vendors, the NAND LTT pull-down shall be configured by the host to the desired value prior to enabling the LTT interface.

4.2.1.3.2 LTT Interface Pull-Up

Table 4.2-4 — Allowable VOH,nom Configurations

VOHpu,nom	VOH,nom (mV) @1.2 V VccQ	Min	Nom	Max	Unit
VccQ/3 (default)	400	0.85	1.0	1.15	VOH,nom
VccQ/2.5 (optional)	480	0.85	1.0	1.15	VOH,nom

NOTE 1 VOHpu,nom = VccQ/3 is mandatory and shall be the default, while VOHpu,nom = VccQ/2.5 is optional.
NOTE 2 VOH,nom accuracy requirements are after ZQ calibration
NOTE 3 VOH,nom accuracy requirements only apply at valid CH_ODT values

4.2.1.3.2 LTT Interface Pull-Up

Table 4.2-5 — Allowable CH_ODT Configurations

Rtt		VOHpu,nom	
[ohm]	Unit	VccQ/3	VccQ/2.5
25	RZQ/12	Valid	Valid
37.5	RZQ/8	Valid	Valid
42.9	RZQ/7	Valid	Valid
50	RZQ/6	Valid (default)	Valid
60	RZQ/5	Valid	Valid
75	RZQ/4	Valid	Valid
100	RZQ/3	Valid	Valid
150	RZQ/2	Valid	Valid
300	RZQ/1	Valid	Valid

NOTE 1 Support for CH_ODT value of 50Ω when VOHpu,nom = VccQ/3 is mandatory and shall be the default setting. Support for other CH_ODT values is vendor specific.

NOTE 2 Support for VOHpu,nom = VccQ/2.5 is optional. When VOHpu,nom = VccQ/2.5 is supported by a device the CH_ODT configurations that are supported as well as the default value are vendor specific.

4.2.1.4 CTT and LTT Interface ODT

Table 4.2-6 — Allowable NAND ODT Rtt Values for CTT and LTT Interfaces

Rtt	
[ohm]	**Unit**
25	RZQ/12
37.5	RZQ/8
42.9	RZQ/7
50	RZQ/6
60	RZQ/5
75	RZQ/4
100	RZQ/3
150	RZQ/2
300	RZQ/1
Disabled (Default)	N/A
NOTE 1 The default value of ODT Rtt = Disabled is mandatory, while the ODT Rtt values supported by a device is vendor specific.	

Table 4.2-7 — ODT Accuracy Specifications

Interface	VOUT	Min	Nom	Max	Notes	Unit
CTT	VIL(AC) to VIH(AC)	0.85	1.0	1.67	1,2,3	RZQ/n
LTT	0.1*VccQ	0.75	1.0	1.15	3	
	0.33*VccQ	0.85	1.0	1.15		
	0.5*VccQ	0.85	1.0	1.35		

NOTE 1 On CTT interface, for data rates where Rx mask is not used, VIL(AC) = VIL.DQrel (AC) and VIH(AC) = VIH.DQrel (AC)
NOTE 2 On CTT interface, for data rates where Rx mask is used, VIL(AC) = Vcent_DQ(pin_mid) – VIHL_AC/2, and VIH(AC) = Vcent_DQ(pin_mid) + VIHL_AC/2.
NOTE 3 All values are after ZQ Calibration.

4.2.2 Output Levels for Unterminated Single-Ended DQ-Related Signals

Table 4.2-8 — Single-Ended AC and DC Output Levels for Unterminated DQ-Related Signals

Interface	Parameter	Symbol	Min	Max	Notes	Unit
LTT	DC Output High DQ-related signals (Unterminated)	$V_{OH.DQrel.unterm}$ (DC)	0.5*VccQ	-	1, 2, 3	V
	DC Output Low DQ-related signals (Unterminated)	$V_{OL.DQrel.unterm}$ (DC)	-	0.080		
	AC Output High DQ-related signals (Unterminated)	$V_{OH.DQrel.unterm}$ (AC)	0.5*VccQ	-		
	AC Output Low DQ-related signals (Unterminated)	$V_{OL.DQrel.unterm}$ (AC)	-	0.060		

NOTE 1 DQ-Related signals are DQS_t/DQS_c and DQs
NOTE 2 Evaluated using Output Timing Reference Load for Unterminated Channel, with default PDDS and CH_ODT settings
NOTE 3 These specs shall be met when tRC(avg) ≥ 30 ns.

4.2.3 Output Timing Reference Loads

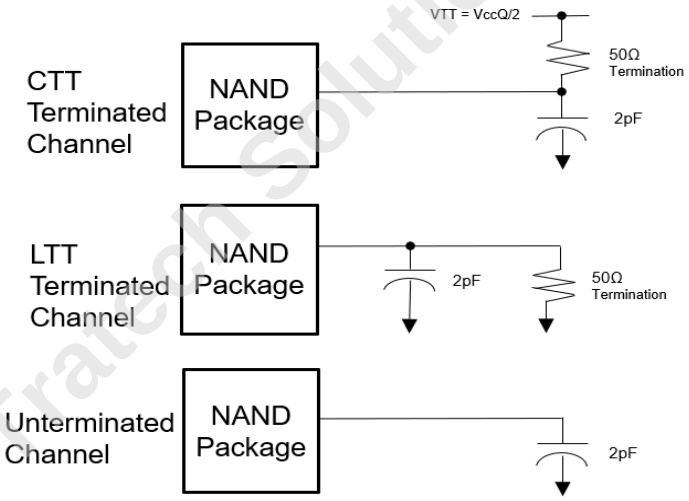


Figure 4.2-1 — Output Timing Reference Loads

The Output Timing Reference Loads are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to their system environment.

4.2.4 Single-Ended Output Slew Rate

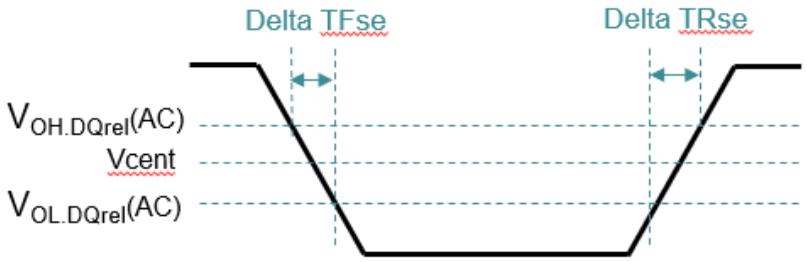


Figure 4.2-2 — Output Slew Rate Measurement

Table 4.2-9 — Single-Ended Output Slew Rate Measurement Levels for Terminated DQ-Related Signals

Description	Measured From	Measured To	Defined By
Single-ended output slew rate for falling edge	$V_{OH.Dqrel}$ (AC)	$V_{OL.Dqrel}$ (AC)	[$V_{OH.DQrel}$(AC) -$V_{OL.DQrel}$(AC)] / Delta TFse
Single-ended output slew rate for rising edge	$V_{OL.Dqrel}$ (AC)	$V_{OH.Dqrel}$ (AC)	[$V_{OH.DQrel}$(AC) - $V_{OL.DQrel}$(AC)] / Delta TRse
NOTE 1 The default value of ODT Rtt = Disabled is mandatory, while the ODT Rtt values supported by a device is vendor specific.			

Table 4.2-10 — Single-Ended Output Slew Rate Measurement Levels for Terminated DQ-Related Signals

Interface	Parameter	Symbol	Level	Unit
CTT	AC Output high for DQ-related signals for slew rate measurements (With Output Ref Load)	$V_{OH.Dqrel}$ (AC)	VTT + 0.1*VccQ	V
	AC Output low for DQ-related signals for slew rate measurements (With Output Ref Load)	$V_{OL.Dqrel}$ (AC)	VTT - 0.1*VccQ	
LTT	AC Output high for DQ-related signals for slew rate measurements (With Output Ref Load)	$V_{OH.Dqrel}$ (AC)	0.8*VOH,nom	
	AC Output low for DQ-related signals for slew rate measurements (With Output Ref Load)	$V_{OL.Dqrel}$ (AC)	0.2*VOH,nom	
NOTE 1 The default value of ODT Rtt = Disabled is mandatory, while the ODT Rtt values supported by a device is vendor specific. NOTE 2 Measured with Output Timing Reference Load for Terminated Channel				

4.2.5 AC Differential Cross-Point

Table 4.2-11 — AC Differential Output Cross-Point Specifications

Parameter	Symbol	CTT (1.2 V VccQ)		LTT (1.2V VccQ)		Unit
		Min	Max	Min	Max	
AC differential output cross point voltage	V_{OX}	0.5*VccQ – 0.15	0.5*VccQ + 0.15	-	-	V
NOTE 1 Applicable to DQS_t/DQS_c after ZQ calibration NOTE 2 Measured with Output Timing Reference Load for Terminated Channel						

4.2.6 Output Specifications for R/B# Signal

Table 4.2-12 — AC/DC Specifications for R/B# Signal

Parameter	Symbol	1.2 V VccQ CTT	1.2V VccQ LTT	Notes	Unit
DC Output high for control signals (optional)	$V_{OH.CNT}$ (DC)	0.7*VccQ (min)		1, 2	V
DC Output low for control signals	$V_{OL.CNT}$ (DC)	0.3*VccQ (max)			
AC Output high for control signals (optional)	$V_{OH.CNT}$ (AC)	0.8*VccQ (min)			
AC Output low for control signals (optional)	$V_{OL.CNT}$ (AC)	0.2*VccQ (max)			
NOTE 1 Control signals are R/B_n NOTE 2 $V_{OL.CNT(DC)}$ (max) is specified with an IOL(R/B_n) of 3 mA					

4.3 AC Overshoot/Undershoot Requirements

The device may have AC overshoot or undershoot from V_{CCQ} and V_{SSQ} levels. Table 4.3-1 and Table 4.3-2 define the maximum values that the AC overshoot or undershoot may attain. These values apply for 1.2 V V_{CCQ} levels.

Table 4.3-1 — CTT and LTT Interface AC Overshoot/Undershoot Specifications (~200 Mhz - ~600 Mhz)

Parameter	Maximum Value						Unit
	~200 MHz	~266 MHz	~333 MHz	~400 MHz	~533 MHz	~600 MHz	
Max. peak amplitude allowed for overshoot area	0.30						V
Max. peak amplitude allowed for undershoot area	0.30						
Max. overshoot area above VccQ	0.40	0.30	0.24	0.20	0.15	0.13	V*ns
Max. undershoot area below VssQ	0.40	0.30	0.24	0.20	0.15	0.13	
NOTE 1 This standard is intended for devices with no clamp protection and is guaranteed by design.							

Table 4.3-2 — CTT and LTT Interface AC Overshoot/Undershoot Specifications (~800 Mhz - ~1200 Mhz)

Parameter	Maximum Value					Unit
	~800 MHz	~900 MHz	~1000 MHz	~1100 MHz	~1200 MHz	
Max. peak amplitude allowed for overshoot area	0.30					V
Max. peak amplitude allowed for undershoot area	0.30					
Max. overshoot area above VccQ	0.10	0.09	0.08	0.073	0.067	V*ns
Max. undershoot area below VssQ	0.10	0.09	0.08	0.073	0.067	
NOTE 1 This standard is intended for devices with no clamp protection and is guaranteed by design.						

4.3 AC Overshoot/Undershoot Requirements (cont'd)

Table 4.3-3 — CTT and LTT Interface AC Overshoot/Undershoot Specifications (~1400 Mhz - ~1800Mhz)

Parameter	Maximum Value			Unit	
	~1400 MHz	~1600 MHz	~1800 MHz		
Max. peak amplitude allowed for overshoot area	0.30			V	
Max. peak amplitude allowed for undershoot area	0.30				
Max. overshoot area above VccQ	0.057	0.050	0.044	V*ns	
Max. undershoot area below VssQ	0.057	0.050	0.044		
NOTE 1 This standard is intended for devices with no clamp protection and is guaranteed by design.					

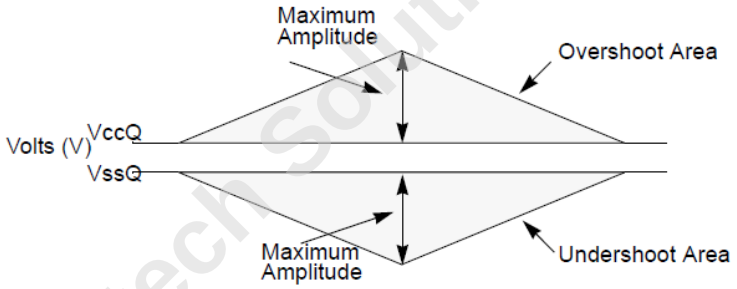


Figure 4.3-1 — Overshoot/Undershoot Diagram

4.4 Recommended DC Operating Conditions

4.4.1 DC Supply Voltage

Lower voltage is generally more preferred for high speed operation in terms of signal integrity and power consumption. 1.2 V V_{CCQ} is recommended to enable speeds up to 800Mbps. A NAND device shall support at least one of 3.3 V V_{CCQ} or 1.8 V V_{CCQ} or 1.2 V V_{CCQ}.

Table 4.4-1 — Supply Voltage Parameter Description

Parameter		Symbol	Min	Typ	Max	Units
Supply voltage for 3.3 V devices[2]		V_{CC}	2.7	3.3	3.6	V
Supply voltage for 2.5 V devices[2]		VCC	2.35	2.5	2.75	V
Supply voltage for 1.8 V devices[2]		V_{CC}	1.7	1.8	1.95	V
Supply voltage for 3.3 V I/O signaling[2]		V_{CCQ}	2.7	3.3	3.6	V
Supply voltage for 1.8 V I/O signaling[2]		V_{CCQ}	1.7	1.8	1.95	V
Supply voltage for 1.2 V I/O signaling[2]		V_{CCQ}	1.14	1.2	1.26	V
Ground voltage supply		V_{SS}	0	0	0	V
Ground voltage supply for I/O signaling		V_{SSQ}	0	0	0	V
External voltage supply[1]		V_{PP}	10.8	12.0	13.2	V

NOTE 1 The maximum external voltage supply (Ipp) is 5 mA per LUN.
NOTE 2 AC noise requirements on Vcc and VccQ are the following:
a) From 10 KHz to 40 MHz, the AC noise shall be less than +/- 3% of the nominal voltage
b) From 40 MHz to 800 MHz, the AC noise shall always be less than +/- 3% of the nominal voltage. If the AC noise is more than +/- 1% of the nominal voltage, a different vendor specific tQSH/tQSL value may be specified.
c) More than 800 MHz, the AC noise shall be less than +/- 3% of the nominal voltage.

4.4.2 DC Output leakage Current Requirements for V_{CCQ} of 1.8 V and V_{CCQ} of 1.2 V

Table 4.4-2 — DC Output Leakage Current Requirements (ILO) for Conditions for V_{CCQ} of 1.8 V and for V_{CCQ} of 1.2 V

Symbol	Parameter	Max
ILO_{pd}	Pull-Down Output leakage current: DQ are disabled: VOUT=VCCQ;	7 uA[1] 15 uA[1,2]
ILO_{pu}	Pull-Up Output leakage current: DQ are disabled: VOUT=0V; ODT disabled	7 uA[1] 15 uA[1,2]

NOTE 1 Absolute leakage value per DQ pin per NAND die. The following signals are required to meet output leakage (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c)
NOTE 2 15 uA Max spec is for devices that support I/O operation >800 MT/s

4.5 Absolute Maximum DC Ratings

Table 4.5-1 — Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Units
VPP Supply Voltage	V_{PP}	-0.6 to +16	V
Vcc = 3.3 V and VccQ = 3.3 V nominal			
Vcc Supply Voltage	Vcc	-0.6 to +4.6	V
Voltage Input	V_{IN}	-0.6 to +4.6	V
VccQ Supply Voltage	VccQ	-0.6 to +4.6	V
Vcc = 3.3 V and Vcc Q = 1.8 V nominal			
Vcc Supply Voltage	Vcc	-0.6 to +4.6	V
Voltage Input	V_{IN}	-0.2 to +2.4	V
VccQ Supply Voltage	VccQ	-0.2 to +2.4	V
Vcc = 3.3 V and VccQ = 1.2 V nominal			
Vcc Supply Voltage	Vcc	-0.6 to +4.6	V
Voltage Input	V_{IN}	-0.2 to +1.5	V
VccQ Supply Voltage	VccQ	-0.2 to +1.5	V
Vcc = 2.5 V and VccQ = 1.8 V nominal			
Vcc Supply Voltage	Vcc	-0.3 to +3.2	V
Voltage Input	V_{IN}	-0.2 to +2.4	V
VccQ Supply Voltage	VccQ	-0.2 to +2.4	V
Vcc = 2.5 V and VccQ = 1.2 V nominal			
Vcc Supply Voltage	Vcc	-0.3 to +3.2	V
Voltage Input	V_{IN}	-0.2 to +1.5	V
VccQ Supply Voltage	VccQ	-0.2 to +1.5	V
Vcc = 1.8 V and VccQ = 1.8 V nominal			
Vcc Supply Voltage	Vcc	-0.2 to +2.4	V
Voltage Input	V_{IN}	-0.2 to +2.4	V
VccQ Supply Voltage	VccQ	-0.2 to +2.4	V

5 Package and Addressing

5.1 BGA-63 (Single x8 / x16 BGA)

Figure 5.1-1 defines the ball assignments for devices using NAND Single x8 / x16 BGA packaging with 8-bit data access for the asynchronous SDR data interface. Figure 5.1-2 defines the ball assignments for devices using NAND Single x8 / x16 BGA packaging with 8-bit data access for the synchronous DDR data interface. Figure 5.1-3 defines the ball assignments for devices using NAND Single x8 / x16 BGA packaging with 16-bit data access for the asynchronous SDR data interface. The NAND Single x8/x16 BGA package with 16-bit data access does not support the Synchronous DDR data interface.

This package uses MO-201.

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP_n	ALE	VSS	CE0_n	WE_n	R/B0_n		
D			VCC	RE_n	CLE	CE1_n	CE2_n	R/B1_n		
E			NC	NC	NC	NC	CE3_n	R/B2_n		
F			NC	NC	NC	NC	VSS	R/B3_n		
G			VSP3	VCC	VSP1	NC	NC	VSP2		
H			NC	IO0	NC	NC	NC	VCCQ		
J			NC	IO1	NC	VCCQ	IO5	IO7		
K			VSSQ	IO2	IO3	IO4	IO6	VSSQ		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

Figure 5.1-1 — Ball Assignments for 8-bit Data Access, Asynchronous SDR only Data Interface

5.1 BGA-63 (Single x8 / x16 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP_n	ALE	VSS	CE0_n	NC	R/B0_n		
D			VCC	W/R_n or RE_0_n	CLE	CE1_n	CE2_n	R/B1_n		
E			NC	NC	NC	NC	CE3_n	R/B2_n		
F			NC	NC	VREFQ	NC	VSS	R/B3_n		
G			VSP3	VCC	VSP1	NC	NC	VSP2		
H			NC	DQ0	DQS_c	CK_c	CK or WE_0_n	VCCQ		
J			NC	DQ1	DQS	VCCQ	DQ5	DQ7		
K			VSSQ	DQ2	DQ3	DQ4	DQ6	VSSQ		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

NOTE 1 WE_n is located at ball H7 when a Synchronous DDR capable part is used in asynchronous SDR mode.

Figure 5.1-2 — Ball Assignments for 8-bit Data Access, Synchronous DDR Data Interface

5.1 BGA-63 (Single x8 / x16 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP_n	ALE	VSS	CE0_n	WE_n	R/B0_n		
D			VCC	RE_n	CLE	CE1_n	CE2_n	R/B1_n		
E			NC	NC	NC	NC	CE3_n	R/B2_n		
F			NC	NC	NC	NC	VSS	R/B3_n		
G			VSP3	VCC	VSP1	IO13	IO15	VSP2		
H			IO8	IO0	IO10	IO12	IO14	VCCQ		
J			IO9	IO1	IO11	VCCQ	IO5	IO7		
K			VSSQ	IO2	IO3	IO4	IO6	VSSQ		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

Figure 5.1-3 — Ball Assignments for 16-bit, Asynchronous SDR Only Data Access

5.2 BGA-100 (Dual x8 BGA)

Figure 5.2-1 defines the ball assignments for devices using NAND Dual x8 BGA packaging with dual 8-bit data access for the asynchronous SDR data interface. Figure 5.2-2 defines the ball assignments for devices using NAND Dual x8 BGA packaging with dual 8-bit data access for the Toggle DDR or Synchronous DDR data interface. The minimum package size is 12 mm x18 mm and the maximum package size is 14 mm x18 mm.

This package uses MO-304.

	1	2	3	4	5	6	7	8	9	10
A	R	R							R	R
B	R									R
C										
D		R	VSP	VSP2_1	WP_1_n	VSP1_1	VSP0_1	VSP	R	
E		R	VSP	VSP2_0	WP_0_n	VSP1_0	VSP0_0	VSP	VDDi	
F		VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	
G		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	
H		VSSQ	VCCQ	R	R	R/B0_1_n	R/B1_1_n or ENo	VCCQ	VSSQ	
J		IO0_1	IO2_1	ALE_1	CE1_1_n	R/B0_0_n	R/B1_0_n	IO5_1	IO7_1	
K		IO0_0	IO2_0	ALE_0	CE1_0_n or ENi	CE0_1_n	CE0_0_n	IO5_0	IO7_0	
L		VCCQ	VSSQ	VCCQ	CLE_1	RE_1_n	VCCQ	VSSQ	VCCQ	
M		IO1_1	IO3_1	VSSQ	CLE_0	RE_0_n	VSSQ	IO4_1	IO6_1	
N		IO1_0	IO3_0	NC	NC	NC	WE_1_n	IO4_0	IO6_0	
P		VSSQ	VCCQ	NC	NC	NC	WE_0_n	VCCQ	VSSQ	
R										
T	R									R
U	R	R							R	R

Figure 5.2-1 — Ball Assignments for Dual 8-bit Data Access, Asynchronous SDR Data Interface

5.2 BGA-100 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10
A	R	R							R	R
B	R									R
C										
D		R	VSP	VSP2_1	WP_1_n	VSP1_1	VSP0_1	VSP	R	
E		R	VSP	VSP2_0	WP_0_n	VSP1_0	VSP0_0	VSP	VDDi	
F		VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	
G		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	
H		VSSQ	VCCQ	VREFQ_1	VREFQ_0	R/B0_1_n	R/B1_0_n or ENo	VCCQ	VSSQ	
J		DQ0_1	DQ2_1	ALE_1	CE1_1_n	R/B0_0_n	R/B1_0_n	DQ5_1	DQ7_1	
K		DQ0_0	DQ2_0	ALE_0	CE1_0_n or ENi	CE0_1_n	CE0_0_n	DQ5_0	DQ7_0	
L		VCCQ	VSSQ	VCCQ	CLE_1	W/R_1_n or RE_1_n	VCCQ	VSSQ	VCCQ	
M		DQ1_1	DQ3_1	VSSQ	CLE_0	W/R_0_n or RE_0_n	VSSQ	DQ4_1	DQ6_1	
N		DQ1_0	DQ3_0	DQS_1_c	DQS_1	RE_1_c	CK_1 or WE_1_n	DQ4_0	DQ6_0	
P		VSSQ	VCCQ	DQS_0_c	DQS_0	RE_0_c	CK_0 or WE_0_n	VCCQ	VSSQ	
R										
T	R									R
U	R	R							R	R

Figure 5.2-2 — Ball Assignments for Dual 8-bit Data Access, Toggle DDR or Synchronous DDR Data Interface

5.3 LGA-52

Figure 5.3-1 defines the pad assignments for devices using NAND LGA packaging with 8-bit data access. An option is specified for two independent 8-bit data buses. Figure 5.3-2 defines the pad assignments for devices using NAND LGA packaging with 16-bit data access. The minimum package size is 12 mm x17 mm and the maximum package size is 14 mm x18 mm. These NAND LGA packages only support the asynchronous SDR data interface. The indicator (the empty circle in these diagrams) in the lower left of the package is a physical package marker that indicates the appropriate orientation of the package.

The NAND LGA package uses MO-303.

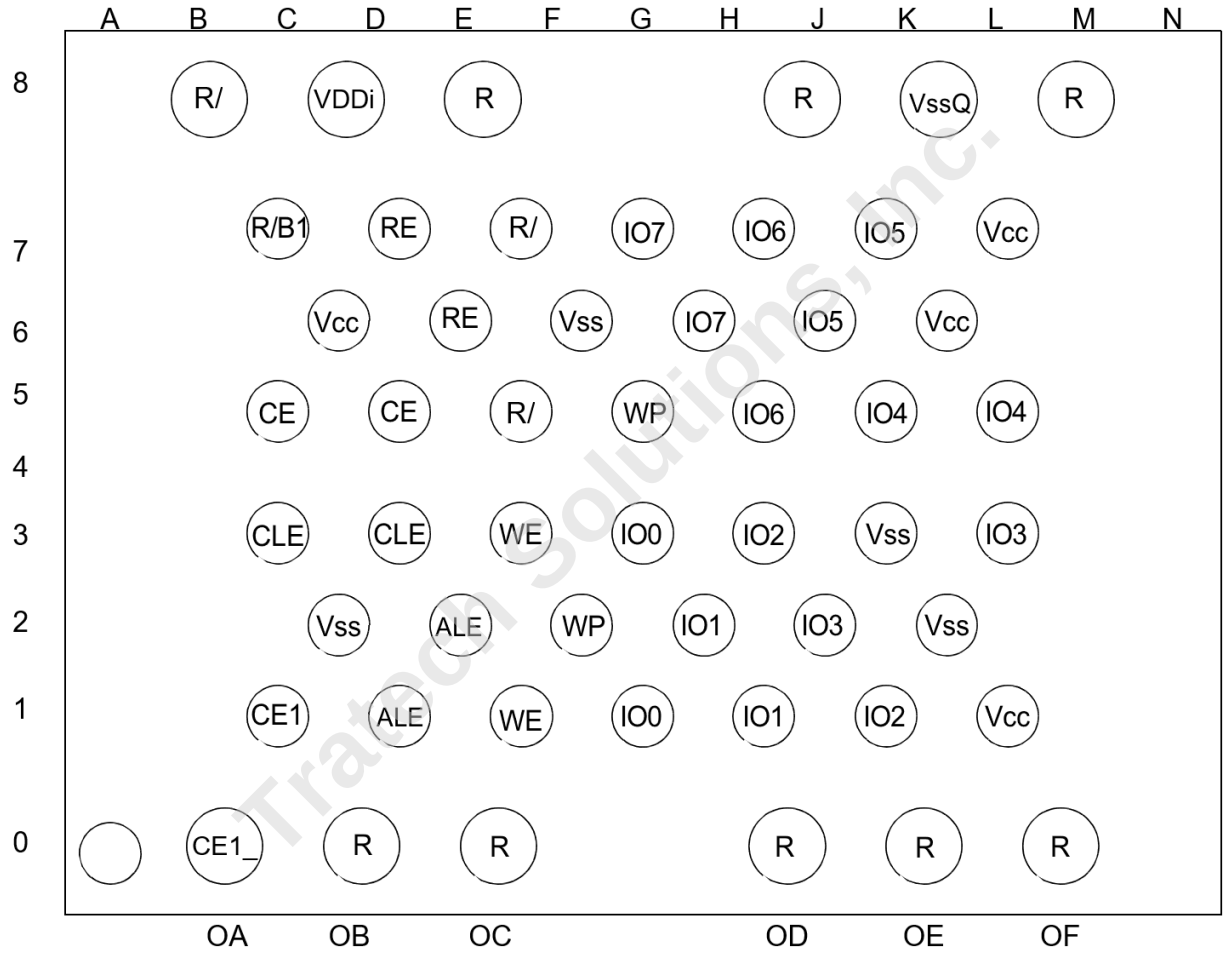


Figure 5.3-1 — LGA Pinout for 8-bit Data Access

5.3 LGA-52 (cont'd)

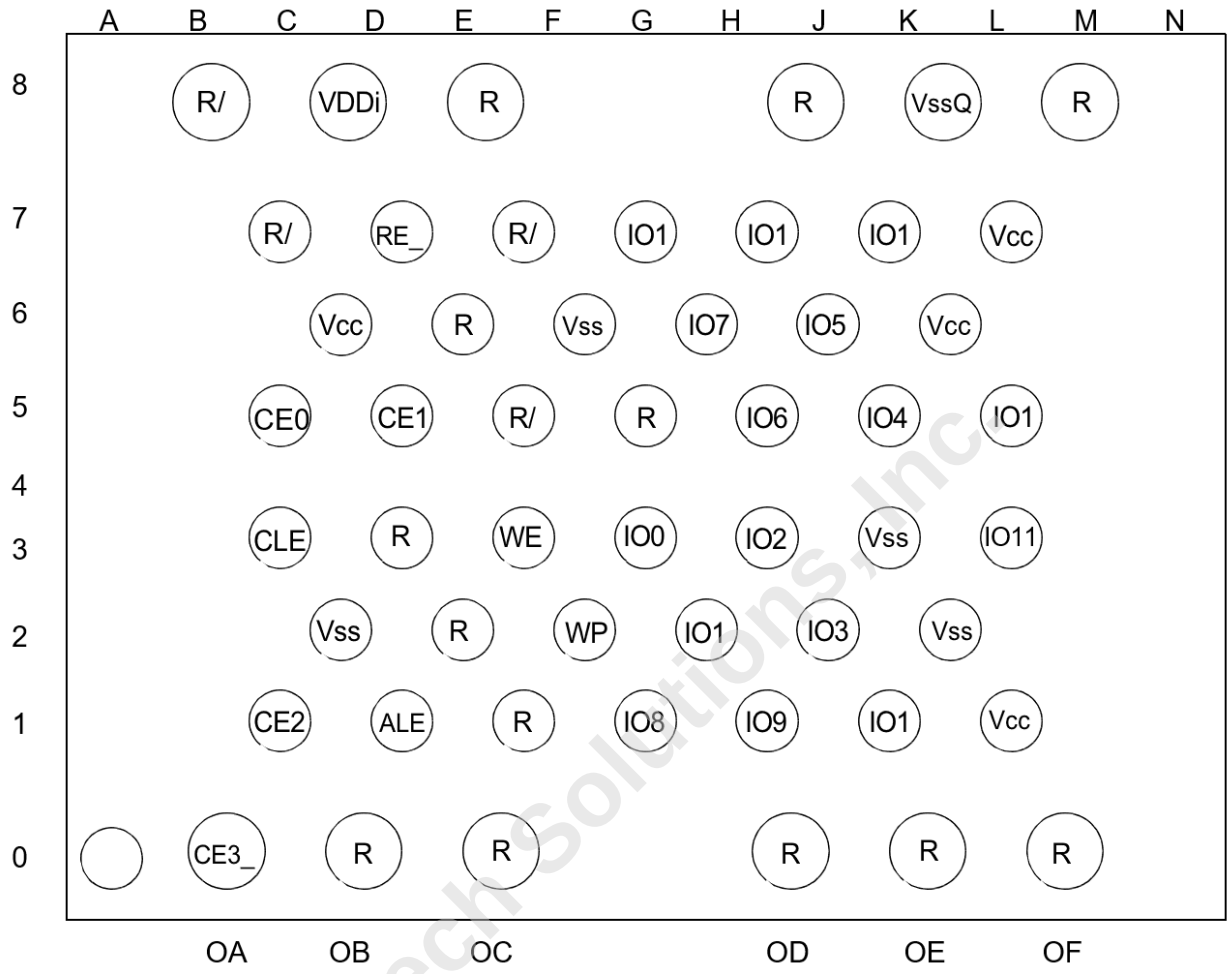


Figure 5.3-2 — LGA Pinout for 16-bit Data Access

5.4 BGA-152/132/136 (Dual x8 BGA)

Figure 5.4-1 to Figure 5.4-3 define the ball assignments for devices using NAND Dual x8 BGA Evolutionary packaging with dual 8-bit data access for the Toggle DDR or Synchronous DDR data interface.
Figure 5.4-4 to Figure 5.4-6 define the ball assignments for devices using NAND Dual x8 BGA Evolutionary packaging with dual 8-bit data access for the asynchronous SDR data interface. 152 BGA is a standard package and 132/136 BGA are the subset packages of 152 BGA for the small size package. NC balls indicate mechanical support balls with no internal connection. NU balls at four corner areas indicate mechanical support balls with possible internal connection. Therefore, NU balls landing pad must be isolated. Any of the support ball locations may or may not be populated with a ball depending upon the NAND Flash Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum package size allowed in the application.

5.4 BGA-152/132/136 (Dual x8 BGA) (cont'd)

The BGA package uses MO-304.

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC	NC						NC	NC	NC	NC
B	NC	NC	NC	NC						NC	NC	NC	NC
C	NU	NU	NU	NU						NU	NU	NU	NU
D	NU	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU	NU
E	NU	NU	VSSQ	DQ2_1	VSSQ	DQS_1 (DQS_1_t)		RE_1_n (RE_1_t) or W/R_1_n	VSSQ	DQ5_1	VSSQ	NU	NU
F			DQ0_1	DQ1_1	DQS_1_c	RE_1_c		WE_1_n or CK_1	VREFQ_1	DQ6_1	DQ7_1		
G			VSSQ	VCCQ	ALE_1	CLE_1		DBI_1 or NU	VSSQ or NU	VCCQ	VSSQ		
H			ENo or NU or CE2_0_n	ENi or NU or CE3_0_n	WP_1_n or ODT_1_n	NU		CE1_1_n	CE0_1_n	RZQ_1	NU		
J			VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS		
K			NU	RZQ_0	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n or ODT_0_n	NU or CE3_1_n	VDDi or NU or CE2_1_n		
L			VSSQ	VCCQ	VSSQ or NU	DBI_0 or NU		CLE_0	ALE_0	VCCQ	VSSQ		
M			DQ7_0	DQ6_0	VREFQ_0	WE_0_n or CK_0		RE_0_c	DQS_0_c	DQ1_0	DQ0_0		
N	NU	NU	VSSQ	DQ5_0	VSSQ	RE_0_n (RE_0_t) or W/R_0_n		DQS_0 or (DQS_0_t)	VSSQ	DQ2_0	VSSQ	NU	NU
P	NU	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU	NU
R	NU	NU	NU	NU						NU	NU	NU	NU
T	NC	NC	NC	NC						NC	NC	NC	NC
U	NC	NC	NC	NC						NC	NC	NC	NC

Figure 5.4-1 — NAND Dual x8 BGA-152 Package Ball Assignments for Dual 8-bit Data Access, Toggle DDR or Synchronous DDR Data Interface

5.4 BGA-152/132/136 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	NC						NC	NC	NC
B	NC	NC	NC						NC	NC	NC
C	NU	NU	NU						NU	NU	NU
D	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU
E	NU	VSSQ	DQ2_1	VSSQ	DQS_1 (DQS_1_t)		RE_1_n (RE_1_t) or W/R_1_n	VSSQ	DQ5_1	VSSQ	NU
F		DQ0_1	DQ1_1	DQS_1_c	RE_1_c		WE_1_n or CK_1	VREFQ_1	DQ6_1	DQ7_1	
G		VSSQ	VCCQ	ALE_1	CLE_1		DBI_1 or NU	VSSQ or NU	VCCQ	VSSQ	
H		ENo or NU or CE2_0_n	ENi or NU or CE3_0_n	WP_1_n or ODT_1_n	NU		CE1_1_n	CE0_1_n	RZQ_1	NU	
J		VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS	
K		NU	RZQ_0	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n or ODT_0_n	NU or CE3_1_n	VDDi or NU or CE2_1_n	
L		VSSQ	VCCQ	VSSQ or NU	DBI_0 or NU		CLE_0	ALE_0	VCCQ	VSSQ	
M		DQ7_0	DQ6_0	VREFQ_0	WE_0_n or CK_0		RE_0_c	DQS_0_c	DQ1_0	DQ0_0	
N	NU	VSSQ	DQ5_0	VSSQ	RE_0_n (RE_0_t) or W/R_0_n		DQS_0 or (DQS_0_t)	VSSQ	DQ2_0	VSSQ	NU
P	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU
R	NU	NU	NU						NU	NU	NU
T	NC	NC	NC						NC	NC	NC
U	NC	NC	NC						NC	NC	NC

Figure 5.4-2 — NAND Dual x8 BGA-132 Package Ball Assignments for Dual 8-bit Data Access, Toggle DDR or Synchronous DDR Data Interface

5.4 BGA-152/132/136 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC	NC						NC	NC	NC	NC
B	NU	NU	NU	NU						NU	NU	NU	NU
C	NU	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU	NU
D	NU	NU	VSSQ	DQ2_1	VSSQ	DQS_1 (DQS_1_t)		RE_1_n (RE_1_t) or W/R_1_n	VSSQ	DQ5_1	VSSQ	NU	NU
E			DQ0_1	DQ1_1	DQS_1_c	RE_1_c		WE_1_n or CK_1	VREFQ_ 1	DQ6_1	DQ7_1		
F			VSSQ	VCCQ	ALE_1	CLE_1		CE3_1_n	CE2_1_n	VCCQ	VSSQ		
G			ENo or NU	ENi or NU	WP_1_n or ODT_1_n	NU		CE1_1_n	CE0_1_n	RZQ_1	NU		
H			VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/ B0_1_n	VCC	VSS		
J			NU	RZQ_0	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n or ODT_0_n	NU	VDDi or NU		
K			VSSQ	VCCQ	CE2_0_n	CE3_0_n		CLE_0	ALE_0	VCCQ	VSSQ		
L			DQ7_0	DQ6_0	VREFQ_ 0	WE_0_n or CK_0		RE_0_c	DQS_0_c	DQ1_0	DQ0_0		
M	NU	NU	VSSQ	DQ5_0	VSSQ	RE_0_n (RE_0_t) or W/R_0_n		DQS_0 (DQS_0_t)	VSSQ	DQ2_0	VSSQ	NU	NU
N	NU	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU	NU
P	NU	NU	NU	NU						NU	NU	NU	NU
R	NC	NC	NC	NC						NC	NC	NC	NC

Figure 5.4-3 — NAND Dual x8 BGA-136 Package Ball Assignments for Dual 8-bit Data Access, Toggle DDR or Synchronous DDR Data Interface

5.4 BGA-152/132/136 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC	NC						NC	NC	NC	NC
B	NC	NC	NC	NC						NC	NC	NC	NC
C	NU	NU	NU	NU						NU	NU	NU	NU
D	NU	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU	NU
E	NU	NU	VSSQ	DQ2_1	VSSQ	NU		RE_1_n	VSSQ	DQ5_1	VSSQ	NU	NU
F			DQ0_1	DQ1_1	NU	NU		WE_1_n	NU	DQ6_1	DQ7_1		
G			VSSQ	VCCQ	ALE_1	CLE_1		CE3_1_n	CE2_1_n	VCCQ	VSSQ		
H			ENo or NU	ENi or NU	WP_1_n or ODT_1_n	NU		CE1_1_n	CE0_1_n	RZQ_1	NU		
J			VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS		
K			NU	RZQ_0	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n or ODT_0_n	NU	VDDi or NU		
L			VSSQ	VCCQ	CE2_0_n	CE3_0_n		CLE_0	ALE_0	VCCQ	VSSQ		
M			DQ7_0	DQ6_0	NU	WE_0_n		NU	NU	DQ1_0	DQ0_0		
N	NU	NU	VSSQ	DQ5_0	VSSQ	RE_0_n		NU	VSSQ	DQ2_0	VSSQ	NU	NU
P	NU	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU	NU
R	NU	NU	NU	NU						NU	NU	NU	NU
T	NC	NC	NC	NC						NC	NC	NC	NC
U	NC	NC	NC	NC						NC	NC	NC	NC

Figure 5.4-4 — NAND Dual x8 BGA-152 Package Ball Assignments for Dual 8-bit Data Access, Asynchronous SDR Data Interface

5.4 BGA-152/132/136 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	NC						NC	NC	NC
B	NC	NC	NC						NC	NC	NC
C	NU	NU	NU						NU	NU	NU
D	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU
E	NU	VSSQ	DQ2_1	VSSQ	NU		RE_1_n	VSSQ	DQ5_1	VSSQ	NU
F		DQ0_1	DQ1_1	NU	NU		WE_1_n	NU	DQ6_1	DQ7_1	
G		VSSQ	VCCQ	ALE_1	CLE_1		CE3_1_n	CE2_1_n	VCCQ	VSSQ	
H		ENo or NU	ENi or NU	WP_1_n or ODT_1_n	NU		CE1_1_n	CE0_1_n	RZQ_1	NU	
J		VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS	
K		NU	RZQ_0	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_n or ODT_0_n	NU	VDDi or NU	
L		VSSQ	VCCQ	CE2_0_n	CE3_0_n		CLE_0	ALE_0	VCCQ	VSSQ	
M		DQ7_0	DQ6_0	NU	WE_0_n		NU	NU	DQ1_0	DQ0_0	
N	NU	VSSQ	DQ5_0	VSSQ	RE_0_n		NU	VSSQ	DQ2_0	VSSQ	NU
P	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU
R	NU	NU	NU						NU	NU	NU
T	NC	NC	NC						NC	NC	NC
U	NC	NC	NC						NC	NC	NC

Figure 5.4-5 — NAND Dual x8 BGA-132 Package Ball Assignments for Dual 8-bit Data Access, Asynchronous SDR Data Interface

5.4 BGA-152/132/136 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC	NC						NC	NC	NC	NC
B	NU	NU	NU	NU						NU	NU	NU	NU
C	NU	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU	NU
D	NU	NU	VSSQ	DQ2_1	VSSQ	NU		RE_1_n	VSSQ	DQ5_1	VSSQ	NU	NU
E			DQ0_1	DQ1_1	NU	NU		WE_1_n	NU	DQ6_1	DQ7_1		
F			VSSQ	VCCQ	ALE_1	CLE_1		CE3_1_n	CE2_1_n	VCCQ	VSSQ		
G			ENo or NU	ENi or NU	WP_1_n or ODT_1_n	NU		CE1_1_n	CE0_1_n	RZQ_1	NU		
H			VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS		
J			NU	RZQ_0	CE0_0_n	CE1_0_n		NU or Vpp	WP_0_ n or ODT_0_n	NU	VDDi or NU		
K			VSSQ	VCCQ	CE2_0_n	CE3_0_n		CLE_0	ALE_0	VCCQ	VSSQ		
L			DQ7_0	DQ6_0	NU	WE_0_n		NU	NU	DQ1_0	DQ0_0		
M	NU	NU	VSSQ	DQ5_0	VSSQ	RE_0_n		NU	VSSQ	DQ2_0	VSSQ	NU	NU
N	NU	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU	NU
P	NU	NU	NU	NU						NU	NU	NU	NU
R	NC	NC	NC	NC						NC	NC	NC	NC

Figure 5.4-6 — NAND Dual x8 BGA-136 Package Ball Assignments for Dual 8-bit Data Access, Asynchronous SDR Data Interface

5.5 BGA-316 (Quad x8 BGA)

Figure 5.5-1 to Figure 5.5-2 define the ball assignments for devices using NAND Quad x8 BGA for the Toggle DDR or Synchronous DDR data interface. BGA-316 supports up to 32 CEs for the future extendibility in terms of the number of die stacks, thus Figure 5.5-1 illustrates the standard package with 16 CEs and Figure 5.5-2 shows the extended type of the package with 32 CEs.NC balls indicate mechanical support balls with no internal connection. NU balls at four corner areas indicate mechanical support balls with possible internal connection. Therefore, NU balls landing pad must be isolated. Any of the support ball locations may or may not be populated with a ball depending upon the NAND Flash Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum package size allowed in the application.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
B	NC	NC	NC	VCCQ	VSS	VCCQ	VSS	VREFQ	VCC	VSS	VCC	VSS	VCC	NC	NC	NC
C	NC	NC	VSS	VCC	VSS	DQ7_2	DQ7_0			VCCQ	VSS	ENi or NU	ENo or NU	VPP	NC	NC
D	NC	VCC	VSS	VSP	VSP	DQ6_2	DQ6_0			VSS	VSS	VSS	VSS	VSS	VCC	NC
E	NC	VCCQ	VSS	VSP	VSP	DQ5_2	DQ5_0			DBI_2 or NU	R/B_2	RZQ_2	VSS	VSS	RFU	NC
F	NC	VSS	VSS	VCCQ	VSS	DQ4_2	DQ4_0			DBI_0 or NU	R/B_0	RZQ_0	VSS	VSS	VSS	NC
G	NC	VCCQ	VSS	VCC	VSS	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			WP_0_n or ODT_0_n	WP_2_n or ODT_2_n	CE1_2_n	CE3_2_n	VSS	VCC	NC
H	NC	VCC	VSS	VCCQ	VSS	DQS_2_c	DQS_0_c			CLE_0	CLE_2	CE1_0_n	CE3_0_n	VSS	RFU	NC
J	NC	VSP	VSP	VSS	DQ3_2	DQ3_0	RE_2_c			RE_0_c	ALE_2	CE0_2_n	CE2_2_n	VSS	VSS	NC
K	NC	VCCQ	VSS	VSS	DQ2_2	DQ2_0	RE_2_n (RE_2_t) or W/R_2_n			RE_0_n (RE_0_t) or W/R_0_n	ALE_0	CE0_0_n	CE2_0_n	VSS	VCC	NC
L	NC	VDDi	VREFQ	VSP	DQ1_2	DQ1_0	WE_2_n or CK_2			WE_0_n or CK_0	DQ0_1	DQ0_3	VSP	VSS	VCCQ	NC
M	NC	VCCQ	VSS	VSP	DQ0_2	DQ0_0	WE_1_n or CK_1			WE_3_n or CK_3	DQ1_1	DQ1_3	VSP	VREFQ	VDDi	NC
N	NC	VCC	VSS	CE2_1_n	CE0_1_n	ALE_1	RE_1_n (RE_1_t) or W/R_1_n			RE_3_n (RE_3_t) or W/R_3_n	DQ2_1	DQ2_3	VSS	VSS	VCCQ	NC
P	NC	VSS	VSS	CE2_3_n	CE0_3_n	ALE_3	RE_1_c			RE_3_c	DQ3_1	DQ3_3	VSS	VSP	VSP	NC
R	NC	RFU	VSS	CE3_1_n	CE1_1_n	CLE_3	CLE_1			DQS_1_c	DQS_3_c	VSS	VCCQ	VSS	VCC	NC
T	NC	VCC	VSS	CE3_3_n	CE1_3_n	WP_3_n or ODT_3_n	WP_1_n or ODT_1_n			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	VSS	VCC	VSS	VCCQ	NC
U	NC	VSS	VSS	VSS	RZQ_1	R/B_1	DBI_1 or NU			DQ4_1	DQ4_3	VSS	VCCQ	VSS	VSS	NC
V	NC	RFU	VSS	VSS	RZQ_3	R/B_3	DBI_3 or NU			DQ5_1	DQ5_3	VSP	VSP	VSS	VCCQ	NC
W	NC	VCC	VSS	VSS	VSS	VSS	VSS			DQ6_1	DQ6_3	VSP	VSP	VSS	VCC	NC
Y	NC	NC	VPP	RFU	RFU	VSS	VCCQ			DQ7_1	DQ7_3	VSS	VCC	VSS	NC	NC
AA	NC	NC	NC	VCC	VSS	VCC	VSS	VCC	VREFQ	VSS	VCCQ	VSS	VCCQ	NC	NC	NC
AB	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

Figure 5.5-1 — NAND Quad x8 BGA- 316 Package Ball Assignments for Quad 8-bit Data Access with up to 16 CE_ns and 4 R/Bs, Toggle DDR or Synchronous DDR Data Interface

5.5 BGA-316 (Quad x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
B	NC	NC	NC	VCCQ	VSS	VCCQ	VSS	VREFQ	VCC	VSS	VCC	VSS	VCC	NC	NC	NC
C	NC	NC	VSS	VCC	VSS	DQ7_2	DQ7_0			VCCQ	VSS	ENi or NU	ENo or NU	VPP	NC	NC
D	NC	VCC	VSS	VSP	VSP	DQ6_2	DQ6_0			VSS	VSS	VSS	VSS	VSS	VCC	NC
E	NC	VCCQ	VSS	VSP	VSP	DQ5_2	DQ5_0			DBI_2 or NU	R/B0_2	RZQ_2	CE6_2_n	CE7_2_n	RFU	NC
F	NC	VSS	VSS	VCCQ	VSS	DQ4_2	DQ4_0			DBI_0 or NU	R/B0_0	RZQ_0	CE6_0_n	CE7_0_n	VSS	NC
G	NC	VCCQ	VSS	VCC	VSS	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			WP_0_n or ODT_0_n	WP_2_n or ODT_2_n	CE1_2_n	CE3_2_n	CE5_2_n	VCC	NC
H	NC	VCC	VSS	VCCQ	VSS	DQS_2_c	DQS_0_c			CLE_0	CLE_2	CE1_0_n	CE3_0_n	CE5_0_n	RFU	NC
J	NC	VSP	VSP	VSS	DQ3_2	DQ3_0	RE_2_c			RE_0_c	ALE_2	CE0_2_n	CE2_2_n	CE4_2_n	VSS	NC
K	NC	VCCQ	VSS	VSS	DQ2_2	DQ2_0	RE_2_n (RE_2_t) or W/R_2_n			RE_0_n (RE_0_t) or W/R_0_n	ALE_0	CE0_0_n	CE2_0_n	CE4_0_n	VCC	NC
L	NC	VDDi	VREFQ	VSP	DQ1_2	DQ1_0	WE_2_n or CK_2			WE_0_n or CK_0	DQ0_1	DQ0_3	VSP	VSS	VCCQ	NC
M	NC	VCCQ	VSS	VSP	DQ0_2	DQ0_0	WE_1_n or CK_1			WE_3_n or CK_3	DQ1_1	DQ1_3	VSP	VREFQ	VDDi	NC
N	NC	VCC	CE4_1_n	CE2_1_n	CE0_1_n	ALE_1	RE_1_n (RE_1_t) or W/R_1_n			RE_3_n (RE_3_t) or W/R_3_n	DQ2_1	DQ2_3	VSS	VSS	VCCQ	NC
P	NC	VSS	CE4_3_n	CE2_3_n	CE0_3_n	ALE_3	RE_1_c			RE_3_c	DQ3_1	DQ3_3	VSS	VSP	VSP	NC
R	NC	RFU	CE5_1_n	CE3_1_n	CE1_1_n	CLE_3	CLE_1			DQS_1_c	DQS_3_c	VSS	VCCQ	VSS	VCC	NC
T	NC	VCC	CE5_3_n	CE3_3_n	CE1_3_n	WP_3_n or ODT_3_n	WP_1_n or ODT_1_n			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	VSS	VCC	VSS	VCCQ	NC
U	NC	VSS	CE7_1_n	CE6_1_n	RZQ_1	R/B0_1	DBI_1 or NU			DQ4_1	DQ4_3	VSS	VCCQ	VSS	VSS	NC
V	NC	RFU	CE7_1_n	CE6_3_n	RZQ_3	R/B0_3	DBI_3 or NU			DQ5_1	DQ5_3	VSP	VSP	VSS	VCCQ	NC
W	NC	VCC	VSS	VSS	VSS	VSS	VSS			DQ6_1	DQ6_3	VSP	VSP	VSS	VCC	NC
Y	NC	NC	VPP	RFU	RFU	VSS	VCCQ			DQ7_1	DQ7_3	VSS	VCC	VSS	NC	NC
AA	NC	NC	NC	VCC	VSS	VCC	VSS	VCC	VREFQ	VSS	VCCQ	VSS	VCCQ	NC	NC	NC
AB	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

Figure 5.5-2 — NAND Quad x8 BGA- 316 Package Ball Assignments for Quad 8-bit Data Access with up to 32 CE_ns and 4 R/Bs, Toggle DDR or Synchronous DDR Data Interface

5.6 BGA-272/252 (Quad x8 BGA)

Figure 5.6-1 and Figure 5.6-2 define the ball assignments for devices using NAND Quad x8 BGA for the Toggle DDR or Synchronous DDR data interface. NC balls indicate mechanical support balls with no internal connection. NU balls at four corner areas indicate mechanical support balls with possible internal connection. Therefore, NU balls landing pad must be isolated. Any of the support ball locations may or may not be populated with a ball depending upon the NAND Flash Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum package size allowed in the application. These BGA packages use MO-210.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NU									NU	NC	NC	NC
B	NC	NC	NU	VCCQ	VSS	VSS	VSS			VCC	VCCQ	VSS	VCCQ	NU	NC	NC
C	NC	NU	VCCQ	VSS	VSS	DQ0_2	DQ0_0			VSS	VSS	VSS	VSS	VCC	NU	NC
D	NU	VCC	VSS	VSS	VSS	DQ1_2	DQ1_0			DQ4_2	DQ4_0	VSS	VSS	VSS	VCC	NU
E	NU	VCC	VSS	VSS	VSS	DQ2_2	DQ2_0			DQ5_2	DQ5_0	VSS	VSS	VSS	VSS	NU
F		VSS	VSS	VSS	DQ3_0	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			DQ6_2	DQ6_0	VSS	VSS	VSS	VCCQ	
G		VCCQ	VSS	VSS	DQ3_2	DQS_2_c	DQS_0_c			VCCQ	DQ7_2	DQ7_0	RZQ_2	RZQ_0	VCCQ	
H		VCCQ	VSS	VSS	VSP0 R	VSP2 R	VSS			WE_0_n or CK_0	CE1_0_n	CE3_0_n	R/B0_0_n	R/B1_0_n	VSS	
J		ENi or NU	ENo or NU	VSS	VSS	DBI_2 or NU	DBI_0 or NU			WE_2_n or CK_2	CE1_2_n	CE3_2_n	R/B0_2_n	R/B1_2_n	VSP6 R	
K		VCC	WP_0_n or ODT_0_n	ALE_0	CLE_0	RE_0_n (RE_0_t) or W/R_0_n	RE_0_c			CE0_2_n	CE0_0_n	CE2_2_n	CE2_0_n	VSP4 or VDDi	VPP	
L		NU	WP_2_n or ODT_2_n	ALE_2	CLE_2	RE_2_n (RE_2_t) or W/R_2_n	RE_2_c			VREFQ	VREFQ	VSS	VSS	VSS	VSS	
M		VSS	VSS	VSS	VSS	VREFQ	VREFQ			RE_3_c	RE_3_n (RE_3_t) or W/R_3_n	CLE_3	ALE_3	WP_3_n or ODT_3_n	NU	
N		VPP	VSP5 or VDDi	CE2_1_n	CE2_3_n	CE0_1_n	CE0_3_n			RE_1_c	RE_1_n (RE_1_t) or W/R_1_n	CLE_1	ALE_1	WP_1_n or ODT_1_n	VCC	
P		VSP7 R	R/B1_3_n	R/B0_3_n	CE3_3_n	CE1_3_n	WE_3_n or CK_3			DBI_1 or NU	DBI_3 or NU	VSS	VSS	NU	NU	
R		VSS	R/B1_1_n	R/B0_1_n	CE3_1_n	CE1_1_n	WE_1_n or CK_1			VSS	VSP3 R	VSP1 R	VSS	VSS	VCCQ	
T		VCCQ	RZQ_1	RZQ_3	DQ7_1	DQ7_3	VCCQ			DQS_1_c	DQS_3_c	DQ3_3	VSS	VSS	VCCQ	
U		VCCQ	VSS	VSS	VSS	DQ6_1	DQ6_3			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	DQ3_1	VSS	VSS	VSS	
V	NU	VSS	VSS	VSS	VSS	DQ5_1	DQ5_3			DQ2_1	DQ2_3	VSS	VSS	VSS	VCC	NU
W	NU	VCC	VSS	VSS	VSS	DQ4_1	DQ4_3			DQ1_1	DQ1_3	VSS	VSS	VSS	VCC	NU
Y	NC	NU	VCC	VSS	VSS	VSS	VSS			DQ0_1	DQ0_3	VSS	VSS	VCCQ	NU	NC
AA	NC	NC	NU	VCCQ	VSS	VCCQ	VCC			VSS	VSS	VSS	VCCQ	NU	NC	NC
AB	NC	NC	NC	NU									NU	NC	NC	NC

Figure 5.6-1 — NAND Quad x8 BGA- 272 Package Ball Assignments for Quad 8-bit Data Access with up to 16 CE_ns and 4 R/Bs, Toggle DDR or Synchronous DDR Data Interface

5.6 BGA-272/252 (Quad x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	NU									NU	NC	NC
B	NC	NU	VCCQ	VSS	VSS	VSS			VCC	VCCQ	VSS	VCCQ	NU	NC
C	NU	VCCQ	VSS	VSS	DQ0_2	DQ0_0			VSS	VSS	VSS	VSS	VCC	NU
D	VCC	VSS	VSS	VSS	DQ1_2	DQ1_0			DQ4_2	DQ4_0	VSS	VSS	VSS	VCC
E	VCC	VSS	VSS	VSS	DQ2_2	DQ2_0			DQ5_2	DQ5_0	VSS	VSS	VSS	VSS
F	VSS	VSS	VSS	DQ3_0	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			DQ6_2	DQ6_0	VSS	VSS	VSS	VCCQ
G	VCCQ	VSS	VSS	DQ3_2	DQS_2_c	DQS_0_c			VCCQ	DQ7_2	DQ7_0	RZQ_2	RZQ_0	VCCQ
H	VCCQ	VSS	VSS	VSP0 R	VSP2 R	VSS			WE_0_n or CK_0	CE1_0_n	CE3_0_n	R/B0_0_n	R/B1_0_n	VSS
J	ENi or NU	ENo or NU	VSS	VSS	DBI_2 or NU	DBI_0 or NU			WE_2_n or CK_2	CE1_2_n	CE3_2_n	R/B0_2_n	R/B1_2_n	VSP6 R
K	VCC	WP_0_n or ODT_0_n	ALE_0	CLE_0	RE_0_n (RE_0_t) or W/R_0_n	RE_0_c			CE0_2_n	CE0_0_n	CE2_2_n	CE2_0_n	VSP4 or VDDi	VPP
L	NU	WP_2_n or ODT_2_n	ALE_2	CLE_2	RE_2_n (RE_2_t) or W/R_2_n	RE_2_c			VREFQ	VREFQ	VSS	VSS	VSS	VSS
M	VSS	VSS	VSS	VSS	VREFQ	VREFQ			RE_3_c	RE_3_n (RE_3_t) or W/R_3_n	CLE_3	ALE_3	WP_3_n or ODT_3_n	NU
N	VPP	VSP5 or VDDi	CE2_1_n	CE2_3_n	CE0_1_n	CE0_3_n			RE_1_c	RE_1_n (RE_1_t) or W/R_1_n	CLE_1	ALE_1	WP_1_n ODT_1_n	VCC
P	VSP7 R	R/B1_3_n	R/B0_3_n	CE3_3_n	CE1_3_n	WE_3_n or CK_3			DBI_1 or NU	DBI_3 or NU	VSS	VSS	NU	NU
R	VSS	R/B1_1_n	R/B0_1_n	CE3_1_n	CE1_1_n	WE_1_n or CK_1			VSS	VSP3 R	VSP1 R	VSS	VSS	VCCQ
T	VCCQ	RZQ_1	RZQ_3	DQ7_1	DQ7_3	VCCQ			DQS_1_c	DQS_3_c	DQ3_3	VSS	VSS	VCCQ
U	VCCQ	VSS	VSS	VSS	DQ6_1	DQ6_3			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	DQ3_1	VSS	VSS	VSS
V	VSS	VSS	VSS	VSS	DQ5_1	DQ5_3			DQ2_1	DQ2_3	VSS	VSS	VSS	VCC
W	VCC	VSS	VSS	VSS	DQ4_1	DQ4_3			DQ1_1	DQ1_3	VSS	VSS	VSS	VCC
Y	NU	VCC	VSS	VSS	VSS	VSS			DQ0_1	DQ0_3	VSS	VSS	VCCQ	NU
AA	NC	NU	VCCQ	VSS	VCCQ	VCC			VSS	VSS	VSS	VCCQ	NU	NC
AB	NC	NC	NU									NU	NC	NC

Figure 5.6-2 — NAND Quad x8 BGA- 252 Package Ball Assignments for Quad 8-bit Data Access with up to 16 CE_ns and 4 R/Bs, Toggle DDR or Synchronous DDR Data Interface

5.7 BGA-178/154/146 (Dual x8 BGA)

Figure 5.7-1, Figure 5.7-2, and Figure 5.7-3 define the ball assignments for devices using NAND Dual x8 BGA for the Toggle DDR or Synchronous DDR data interface. NC balls indicate mechanical support balls with no internal connection. NU balls indicate mechanical support balls with possible internal connection. Therefore, NU balls landing pad must be isolated. Any of the support ball locations may or may not be populated with a ball depending upon the NAND Flash Vendor's actual package size. Therefore, it is recommended to consider landing pad location for all possible support balls based upon maximum package size allowed in the application.

The package size of BGA-178 is 13.5 mm x13.5 mm with 0.8 mm ball pitch and uses MO-216. The package size of BGA-154 is either 11.5 mm x13.5 mm or 12.8 mm x13.5 mm with 0.8 mm ball pitch and uses MO-210. The package size of BGA-146 is either 10 mm x18 mm or 10 mm x14 mm with 0.8 mm ball pitch and uses MO-210.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	NC	NC	NC	NC								NC	NC	NC	NC
B	NC	NU	NU	NU								NU	NU	NU	NC
C	NC	NU	NU	VCCQ	VSS	VPP	VSS	VCC	VSS	VCCQ	VSS	VCCQ	NU	NU	NC
D	NC	NU	VCCQ	VCC	RFU	VPP	PSL_0 ZQ_0	VREF_0	RFU	VSP	VSP	VCC	VCCQ	NU	NC
E	NC	NU	VSS	DQ5_0	VCCQ	DQ7_0	CE1_0_n	CE0_0_n	WP_1_n ODT_1_n	DQ0_1	VCCQ	DQ2_1	VSS	NU	NC
F	NC	NU	VCCQ	DQ4_0	VSS	DQ6_0	CE2_0_n	R/B0_0_n	ALE_1	DQ1_1	VSS	DQ3_1	VCCQ	NU	NC
G		NU	VCC	RE_0_n W/R_0_n	RE_0_c	WE_0_n CLK_0	CE3_0_n	R/B1_0_n	CLE_1	DBI_1 or NU	DQS_1_c	DQS_1_t	VSS	NU	
H															
J		NU	VSS	DQS_0_t	DQS_0_c	DBI_0 or NU	CLE_0	R/B1_1_n	CE3_1_n	WE_1_n CLK_1	RE_1_c	RE_1_n W/R_1_n	VCC	NU	
K	NC	NU	VCCQ	DQ3_0	VSS	DQ1_0	ALE_0	R/B0_1_n	CE2_1_n	DQ6_1	VSS	DQ4_1	VCCQ	NU	NC
L	NC	NU	VSS	DQ2_0	VCCQ	DQ0_0	WP_0_n ODT_0_n	CE0_1_n	CE1_1_n	DQ7_1	VCCQ	DQ5_1	VSS	NU	NC
M	NC	NU	VCCQ	VCC	VSP	VSP	RFU	VREF_1	PSL_1 ZQ_1	VPP	RFU	VCC	VCCQ	NU	NC
N	NC	NU	NU	VCCQ	VSS	VCCQ	VSS	VCC	VSS	VPP	VSS	VCCQ	NU	NU	NC
P	NC	NU	NU	NU								NU	NU	NU	NC
R	NC	NC	NC	NC								NC	NC	NC	NC

Figure 5.7-1 — NAND Dual x8 BGA-178 Package Ball Assignments for Dual 8-bit Data Access, Toggle DDR or Synchronous DDR Data Interface

5.7 BGA-178/154/146 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC								NC	NC	NC
B	NU	NU	NU								NU	NU	NU
C	NU	NU	VCCQ	VSS	VPP	VSS	VCC	VSS	VCCQ	VSS	VCCQ	NU	NU
D	NU	VCCQ	VCC	RFU	VPP	PSL_0 ZQ_0	VREF_0	RFU	VSP	VSP	VCC	VCCQ	NU
E	NU	VSS	DQ5_0	VCCQ	DQ7_0	CE1_0_n	CE0_0_n	WP_1_n ODT_1_n	DQ0_1	VCCQ	DQ2_1	VSS	NU
F	NU	VCCQ	DQ4_0	VSS	DQ6_0	CE2_0_n	R/B0_0_n	ALE_1	DQ1_1	VSS	DQ3_1	VCCQ	NU
G	NU	VCC	RE_0_n W/R_0_n	RE_0_c	WE_0_n CLK_0	CE3_0_n	R/B1_0_n	CLE_1	DBI_1 or NU	DQS_1_c	DQS_1_t	VSS	NU
H													
J	NU	VSS	DQS_0_t	DQS_0_c	DBI_0 or NU	CLE_0	R/B1_1_n	CE3_1_n	WE_1_n CLK_1	RE_1_c	RE_1_n W/R_1_n	VCC	NU
K	NU	VCCQ	DQ3_0	VSS	DQ1_0	ALE_0	R/B0_1_n	CE2_1_n	DQ6_1	VSS	DQ4_1	VCCQ	NU
L	NU	VSS	DQ2_0	VCCQ	DQ0_0	WP_0_n ODT_0_n	CE0_1_n	CE1_1_n	DQ7_1	VCCQ	DQ5_1	VSS	NU
M	NU	VCCQ	VCC	VSP	VSP	RFU	VREF_1	PSL_1 ZQ_1	VPP	RFU	VCC	VCCQ	NU
N	NU	NU	VCCQ	VSS	VCCQ	VSS	VCC	VSS	VPP	VSS	VCCQ	NU	NU
P	NU	NU	NU								NU	NU	NU
R	NC	NC	NC								NC	NC	NC

Figure 5.7-2 — NAND Dual x8 BGA-154 Package Ball Assignments for Dual 8-bit Data Access, Toggle DDR or Synchronous DDR Data Interface

5.7 BGA-178/154/146 (Dual x8 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	NC	NC				NC	NC	NC	NC
B	NU	NU	NU	NU	NU		NU	NU	NU	NU	NU
C	NU	VCCQ	VSS	VCCQ	VSS		VCC	VCCQ	VSS	VCCQ	NU
D	VCCQ	VCC	DQ2_0	DQ3_0	DQS_0_t		RE_0_n W/R_0_n	DQ4_0	DQ5_0	VCC	VCCQ
E	VSS	VSP	VCCQ	VSS	DQS_0_c		RE_0_c	VSS	VCCQ	RFU	VSS
F	VCCQ	VSP	DQ0_0	DQ1_0	DBI_0 or NU		WE_0_n CLK_0	DQ6_0	DQ7_0	VPP	VPP
G	VSS	RFU	WP_0_n ODT_0_n	ALE_0	CLE_0		CE3_0_n	CE2_0_n	CE1_0_n	PSL_0 ZQ_0	VSS
H	VCC	VREF_1	CE0_1_n	R/B0_1_n	R/B1_1_n		R/B1_0_n	R/B0_0_n	CE0_0_n	VREF_0	VCC
J	VSS	PSL_1 ZQ_1	CE1_1_n	CE2_1_n	CE3_1_n		CLE_1	ALE_1	WP_1_n ODT_1_n	RFU	VSS
K	VPP	VPP	DQ7_1	DQ6_1	WE_1_n CLK_1		DBI_1 or NU	DQ1_1	DQ0_1	VSP	VCCQ
L	VSS	RFU	VCCQ	VSS	RE_1_c		DQS_1_c	VSS	VCCQ	VSP	VSS
M	VCCQ	VCC	DQ5_1	DQ4_1	RE_1_n W/R_1_n		DQS_1_t	DQ3_1	DQ2_1	VCC	VCCQ
N	NU	VCCQ	VSS	VCCQ	VCC		VSS	VCCQ	VSS	VCCQ	NU
P	NU	NU	NU	NU	NU		NU	NU	NU	NU	NU
R	NC	NC	NC	NC				NC	NC	NC	NC

Figure 5.7-3 — NAND Dual x8 BGA-146 Package Ball Assignments for Dual 8-bit Data Access, Toggle DDR or Synchronous DDR Data Interface

5.8 CE_n to R/B_n Mapping

There may be two independent 8-bit data buses in some JEDEC packages (i.e., the BGA-152 package). There may be four independent 8-bit data buses in some JEDEC packages (i.e., the BGA-316 and BGA-272 packages).

Any signal with a channel (i.e., 8-bit data bus) designator (for example, "x" for CE0_x_n) could not be used by another channel. For example, CE0_0 cannot be used on any channel other than channel 0 or R/B0_1 cannot be used for any channel other than channel 1.

In some package configurations, there are multiple CE_n signals per R/B_n signal. Table 5.8-1 describes the R/B_n signal that each CE_n uses in the case when there are two R/B_n signals and more than one CE_n per 8-bit data bus. Table 5.8-2 describes the R/B_n signal that each CE_n uses in the case when there is a single R/B_n signal per 8-bit data bus. Table 5.8-3 provides the case when there is a single CE_n and two R/B_n signals per 8-bit data bus. For packages that only support two 8-bit data buses, R/B0_2_n, R/B1_2_n, R/B0_3_n and R/B1_3_n shall be ignored.

Table 5.8-1 — R/B_n Signal Use per CE_n with Two R/B_n Signals per Channel

Signal Name	CE_n
R/B0_0_n	CE0_0_n, CE2_0_n, CE4_0_n, CE6_0_n
R/B0_1_n	CE0_1_n, CE2_1_n, CE4_1_n, CE6_1_n
R/B0_2_n	CE0_2_n, CE2_2_n, CE4_2_n, CE6_2_n
R/B0_3_n	CE0_3_n, CE2_3_n, CE4_3_n, CE6_3_n
R/B1_0_n	CE1_0_n, CE3_0_n, CE5_0_n, CE7_0_n
R/B1_1_n	CE1_1_n, CE3_1_n, CE5_1_n, CE7_1_n
R/B1_2_n	CE1_2_n, CE3_2_n, CE5_2_n, CE7_2_n
R/B1_3_n	CE1_3_n, CE3_3_n, CE5_3_n, CE7_3_n

Table 5.8-2 — R/B_n Signal Use per CE_n with a Single R/B_n Signal per Channel

Signal Name	CE_n
R/B0_0_n	CE0_0_n, CE1_0_n, CE2_0_n, CE3_0_n, CE4_0_n, CE5_0_n, CE6_0_n, CE7_0_n
R/B0_1_n	CE0_1_n, CE1_1_n, CE2_1_n, CE3_1_n, CE4_1_n, CE5_1_n, CE6_1_n, CE7_1_n
R/B0_2_n	CE0_2_n, CE1_2_n, CE2_2_n, CE3_2_n, CE4_2_n, CE5_2_n, CE6_2_n, CE7_2_n
R/B0_3_n	CE0_3_n, CE1_3_n, CE2_3_n, CE3_3_n, CE4_3_n, CE5_3_n, CE6_3_n, CE7_3_n

5.8 CE_n to R/B_n Mapping (cont'd)

Table 5.8-3 — R/B_n Signal Use per CE_n with Two R/B_n Signals per Channel and One CE_n per Channel

Signal Name	CE_n
R/B0_0_n	CE0_0_n
R/B0_1_n	CE0_1_n
R/B0_2_n	CE0_2_n
R/B0_3_n	CE0_3_n
R/B1_0_n	CE0_0_n
R/B1_1_n	CE0_1_n
R/B1_2_n	CE0_2_n
R/B1_3_n	CE0_3_n

R/B_n shall reflect the logical AND of the SR[6] (Status Register bit 6) values for all LUNs on the corresponding NAND Target or Volume. In the case that more than one NAND target or Volume share an R/B_n signal, R/B_n shall reflect the logical AND of the SR[6] (Status Register bit 6) values for all LUNs connected to the shared R/B_n signal. For example, R/B0_0 is logical AND of the SR[6] values for all LUNs that share R/B0_0. Thus, R/B_n reflects whether any LUN is busy on a particular NAND Target or if there are multiple NAND Targets that share R/B_n, R/B_n reflects whether any LUN is busy on any of the shared NAND Targets.

6 Command Sets for NAND Flash memory

6.1 Basic Command Definition

Table 6.1-1 outlines the commands defined for NAND Flash memory.

The value specified in the first command cycle identifies the command to be performed. Some commands have a second command cycle as specified in Table 6.1-1. Typically, commands that have a second command cycle include an address.

Table 6.1-1 — Command Set

Command	O/M	1st Cycle	2nd Cycle	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy	Target Level Commands
Page Read	M	00h	30h		Y	
Copyback Read	O	00h	35h		Y	
Change Read Column	M	05h	E0h		Y	
Read Cache Random	O	00h	31h		Y	
Read Cache Sequential	O	31h	na		Y	
Read Cache End	O	3Fh	na		Y	
Block Erase	M	60h	D0h		Y	
Page Program	M	80h	10h		Y	
Copyback Program	O	85h	10h		Y	
Change Write Column	M	85h	na		Y	
Get Features	O	EEh	na			Y
Set Features	O	EFh	na			Y
Page Cache Program	O	80h	15h		Y	
Read Status	M	70h	na	Y		
Read Unique ID	O	EDh	na			Y
Reset	M	FFh	na	Y	Y	Y
Synchronous Reset	O	FCh	na	Y	Y	Y
Reset LUN	O	FAh		Y	Y	

6.2 Primary and Secondary Command Definition for the Advanced Operation

Table 6.2-1 defines the Primary and Secondary Commands. Primary commands are the recommended implementation for a particular command. Secondary commands are an alternate implementation approach that is allowed for backwards compatibility. Commands may be used with any data interface (asynchronous SDR, Toggle DDR, or Synchronous DDR).

Table 6.2-1 — Primary and Secondary Commands

Command	O/M	Primary or Secondary	1st Cycle	2nd Cycle	ONFI or Toggle-mode Heritage (remove in future)
Multi-plane Read	Refer to Note1	Primary	00h	32h	ONFI
	O	Secondary	60h	30h	Toggle-mode
Multi-plane Read Cache Random	Refer to Note1	Primary	00h	31h	ONFI
	O	Secondary	60h	3Ch	Toggle-mode
Multi-plane Copyback Read	Refer to Note1	Primary	00h	35h	ONFI
	O	Secondary	60h	35h	Toggle-mode
Random Data Out	Refer to Note1	Primary	00h 05h	n/a E0h	Toggle-mode
	O	Secondary	06h	E0h	ONFI
Multi-plane Program	Refer to Note1	Primary	80h or 81h	11h	Toggle-mode
	O	Secondary	80h	11h	ONFI
Multi-plane Copyback Program	Refer to Note1	Primary	85h or 81h	11h	Toggle-mode
	O	Secondary	85h	11h	ONFI
Multi-plane Block Erase	Refer to Note1	Primary	60h	n/a or D1h	Toggle-mode (for n/a 2nd cycle) and ONFI (for D1h 2nd cycle)
Read Status Enhanced	Refer to Note1	Primary	78h	n/a	ONFI
	O	Secondary	F1h/F2h	n/a	Toggle-mode

NOTE1 If the corresponding feature tied to the command is applicable to the device (see vendor datasheet), the primary command shall be supported

6.3 Get Feature for Each LUN

Figure 6.3-1 shows Get Feature for each LUN operation timing diagram. This operation requires two address cycles. The LUN address comes first followed by the Feature address. The two address cycles cannot be interchanged. Writing two addresses is what distinguishes this command from the standard Get Feature operation which requires a single Feature address.

When the LUN address is issued, 00h is used for LUN0 and 01h is for LUN1.

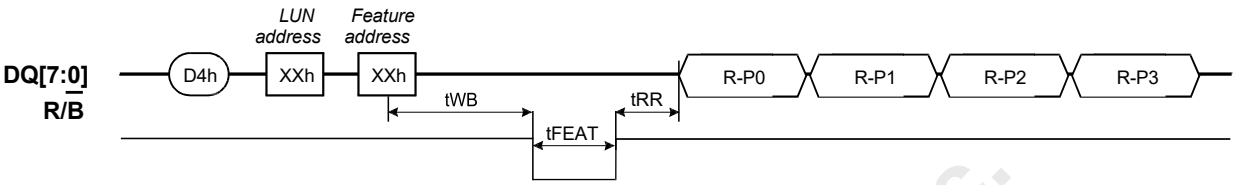


Figure 6.3-1 — Get Feature for Each LUN Sequence

6.4 Set Feature for Each LUN

Figure 6.4-1 depicts Set Feature for each LUN operation timing diagram. This operation requires two address cycles. The LUN address comes first followed by the Feature address. The two address cycles cannot be interchanged. Writing two addresses is what distinguishes this command from the standard Set Feature operation which requires a single Feature address.

When the LUN address is issued, 00h is used for LUN0 and 01h is for LUN1.

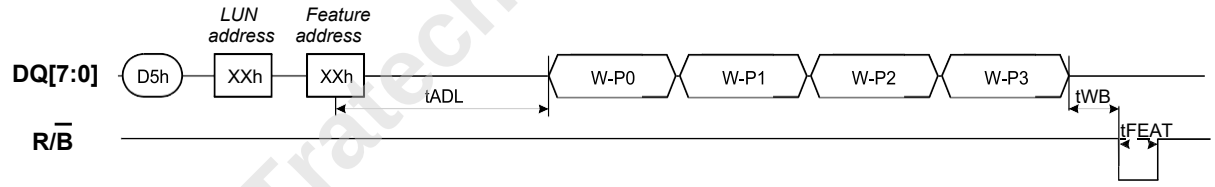


Figure 6.4-1 — Set Feature for Each LUN Sequence

7 Feature Address Registers

7.1 Feature Address 02h (Interface Configuration Register)

Table 7.1-1 — Feature Table for Interface Configuration Register [02h]

Sub Feature Parameter	7	6	5	4	3	2	1	0
B0	ODT Self-Termination (with Rtt Value)				Reserved	RE (CMPR)	DQS (CMPD)	VrefQ (VEN)
B1	# of Latency DQS cycle for WRITE				# of Latency DQS cycle for READ			
B2	Reserved	VOH for LTT (optional)	DBI for WRITE	DBI for READ	Internal VrefQ Value Setting (Read Only)		Interface Type	
B3	Reserved							

B0[0] for internal or external VrefQ
0 (default) = internal VrefQ
1 = external VrefQ

B0[1] for complementary/differential DQS
0 (default) = disable DQS_c
1 = enable DQS_c

B0[2] for complementary/differential RE
0 (default) = disable RE_c
1 = enable RE_c

B2[1:0] for Interface Type.
00b (default) = CTT Interface
01b = LTT Interface
10b-11b = Reserved

B2[3:2] for Internal VrefQ Value Setting (Read Only)
00b = NAND Uses Value1 Range/Step Size
01b = NAND Uses Value2 Range/Step Size
10b = NAND Uses Value3 Range/Step Size
11b = Reserved

B2[4] for DBI for Read
0 (default) = DBI for Read is disabled
1 = DBI for Read is enabled

B2[5] for DBI for Write
0 (default) = DBI for Write is disabled
1 = DBI for Write is enabled

B2[6] for VOH for LTT (Optional)
0 (default) = VccQ/3
1 = VccQ/2.5

7.2 Feature Address 05h

User can switch between WP and ODT functions via set-feature.

Table 7.2-1 — Feature Table for WP/ODT Mode Selection [05h]

Sub Feature Parameter	7	6	5	4	3	2	1	0
B0-2	Reserved (0)							
B3	Reserved (0)	WP/ODT Mode Selection	Reserved (0)					

B3[6] for WP and ODT selection mode [1: ODT Operation, 0: WP Operation(Default)]

7.3 Feature Address 10h

Table 7.3-1 — Feature Table for CTT Output Drive Strength and LTT Pull-down Drive Strength (Optional Location2) [10h]

Sub Feature Parameter	7	6	5	4	3	2	1	0
B0	Reserved				CTT Output Driver Pull-up/Pull-down and LTT Pull-Down Driver Strength Settings (Optional Location2 for LTT PDDS: See Vendor Datasheet)			
B1 – B3	Reserved							

7.4 Feature Address 20h

To be used for DCC training, Read Training, and Write training (Tx side).

Table 7.4-1 — Feature Table for DCC, Read Training, and Write Training (Tx side) [20h]

Sub Feature Parameter	7	6	5	4	3	2	1	0
B0	Reserved (0)					DCC Factory Setting	DCCI_EN	DCCE_EN
B1	Reserved (0)							
B2	Reserved (0)			Read Training Defined Pattern Length	Write Training Data Size [3:0] 0000 : 08 Bytes 0001 : 16 Bytes 0010 : 24 Bytes 0011 : 32 Bytes 0100 : 40 Bytes 0101 : 48 Bytes 0110 : 56 Bytes 0111 : 64 Bytes 1000 : 72 Bytes 1001 : 80 Bytes 1010 : 88 Bytes 1011 : 96 Bytes 1100 : 104 Bytes 1101 : 112 Bytes 1110 : 120 Bytes 1111 : 128 Bytes			
B3	Reserved (0)							

7.4 Feature Address 20h (cont'd)

- B0[0] for the enabler of explicit DCC Training using Set Feature [1: Turn on training, 0: turn off training] default=0.
- B0[1] for the enabler of implicit DCC Training during warm up cycles [1: Enable, 0: Disable] default=0. Host can set DCC En/Disable=Disable if host doesn't need DCC with low frequency operation.
- B0[2] is for DCC factory setting. This is an optional function for the NAND device, please refer to the vendor datasheet if DCC factory setting is supported or not. If set to a 1, then the factory DCC settings would be used by the LUN. If cleared to 0, then the DCC calibrated settings would be used by the LUN.
- B2[3:0] are read only bits for data size for write training (up to 128bytes)
- B2[4] read only bit for data pattern length for read training [1: 32 Bytes, 0: 16 Bytes]

7.5 Feature Address 21h

To be used for Write Training (Rx side)

Table 7.5-1 — Feature Table for Write Training (Rx side) [21h]

Sub Feature Parameter	7	6	5	4	3	2	1	0
B0	Reserved (0)					Write Training Rx with Internal VrefQ Training (Optional)	All LUN	Factory setting
B1	St_ dq3[1]	St_ dq3[0]	St_ dq2[1]	St_ dq2[0]	St_ dq1[1]	St_ dq1[0]	St_ dq0[1]	St_ dq0[0]
B2	St_ dq7[1]	St_ dq7[0]	St_ dq6[1]	St_ dq6[0]	St_ dq5[1]	St_ dq5[0]	St_ dq4[1]	St_ dq4[0]
B3	Reserved (0)							

- B0[0] keep input path settings as determined by training/reset to factory settings [1 = factory setting; 0 = trained value]
- B0[1] Enables All LUN option. This is an optional function for the NAND device, please refer to the vendor datasheet if All LUN Write Training (Rx side) is supported or not. If this bit is set to a 1 prior to Write Training (Rx side) then the LUN address cycle is ignored and the write training is performed by all enabled LUNs which have this bit set.
- B0[2] for Write Training (Rx side) With Internal VrefQ Training (Optional)
  - 0 (default) = Normal Write Training (Rx side) for CTT and LTT Interfaces.
  - 1 = Write Training (Rx side) with Internal VrefQ Training (for LTT Interface only).
- B1[7:0] Status bits for dq[3:0]
- B2[7:0] Status bits for dq[7:4]
- B1[1:0]:
  - 00: Centering of dqs to dq0 data eye is successful.
  - 01: Centering of dqs/dqsn to dq0 data eye failed with dq0 being too slow with respect to dqs/dqsn
  - 10: Centering of dqs/dqsn to dq0 data eye failed with dq0 being too fast with respect to dqs/dqsn
  - 11: Centering of dqs/dqsn to dq0 data eye failed for unknown reasons
- B1[3:2], B1[5:4], B1[7:6], B2[1:0], B2[3:2], B2[5:4], B2[7:6] represent the status of dq[7:1] similar to B1[1:0] for dq0.

7.6 Feature Address 22h

Table 7.6-1 — Feature Table for LTT CH_ODT, Pull-down Drive Strength (Optional Location1), and ODT Control Type1 Configuration [22h]

Sub Feature Parameter	7	6	5	4	3	2	1	0
B0	LTT Pull-Down Driver Strength (PDDS) (Optional Location1 for LTT PDDS: See Vendor Datasheet)				Channel ODT (CH_ODT) Value for VOH Calibration (For LTT Pull-up Driver Strength)			
B1	LTT Target ODT Value for DQ/DQS Input[1]				LTT Non-Target ODT Value for DQ/DQS Input[1]			
B2	LTT Target ODT Value for RE Input[1]				LTT Non-Target ODT Value for RE Input[1]			
B3	Reserved				LTT Non-Target ODT Value for DQ/DQS Output[1]			
NOTE 1 These fields are applicable to ODT Control Type1 NAND Devices only (ie. ODT control is done via ODT_n pin).								

7.7 Feature Address 23h

7.7.1 FA23h for NAND Devices that Support Value1 or Value2 Settings

Table 7.7-1 — Feature Table for Internal VrefQ for NAND Devices that Support Value1 or Value2 Settings [23h] [1,2]

Sub-feature Parameter	7	6	5	4	3	2	1	0
B0	Internal VrefQ Value1/Value2 Settings							Reserved
B1	Reserved							
B2	Reserved							
B3	Reserved							
NOTE 1 The NAND internal VrefQ shall not be set to a setting beyond the allowable range even during Write Training. NOTE 2 NAND is not required to implement VrefQ beyond the NAND Minimum Internal VrefQ Allowable Range.								

7.7.1 FA23h for NAND Devices that Support Value1 or Value2 Settings (cont'd)

Table 7.7-2 — Internal VrefQ Value1 Range, Step Size, and Tolerance

Internal VrefQ Value1 Range/Step Size				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Default	TBD			VccQ
Vref_min	0%	-	-	VccQ
Vref_max	-	-	63.50%	VccQ
Vref_step	0.35%	0.50%	0.65%	VccQ
Vref_Set_Tol	-1.75%	0%	1.75%	VccQ

Table 7.7-3 — Internal VrefQ Value2 Range, Step Size, and Tolerance

Internal VrefQ Value2 Range/Step Size				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Default	TBD			VccQ
Vref_min	0%	-	-	VccQ
Vref_max	-	-	99.22%	VccQ
Vref_step	0.58%	0.78%	0.98%	VccQ
Vref_Set_Tol	-1.95%	0%	1.95%	VccQ

7.7.1 FA23h for NAND Devices that Support Value1 or Value2 Settings (cont'd)

Table 7.7-4 — Internal VrefQ Value1 Setting Versus Value as % of VccQ

Code	VrefQ (% of VccQ)	Code	VrefQ (% of VccQ)	Code	VrefQ (% of VccQ)	Code	VrefQ (% of VccQ)
0000000b	0.00	0100000b	16.00	1000000b	32.00	1100000b	48.00
0000001b	0.50	0100001b	16.50	1000001b	32.50	1100001b	48.50
0000010b	1.00	0100010b	17.00	1000010b	33.00	1100010b	49.00
0000011b	1.50	0100011b	17.50	1000011b	33.50	1100011b	49.50
0000100b	2.00	0100100b	18.00	1000100b	34.00	1100100b	50.00
0000101b	2.50	0100101b	18.50	1000101b	34.50	1100101b	50.50
0000110b	3.00	0100110b	19.00	1000110b	35.00	1100110b	51.00
0000111b	3.50	0100111b	19.50	1000111b	35.50	1100111b	51.50
0001000b	4.00	0101000b	20.00	1001000b	36.00	1101000b	52.00
0001001b	4.50	0101001b	20.50	1001001b	36.50	1101001b	52.50
0001010b	5.00	0101010b	21.00	1001010b	37.00	1101010b	53.00
0001011b	5.50	0101011b	21.50	1001011b	37.50	1101011b	53.50
0001100b	6.00	0101100b	22.00	1001100b	38.00	1101100b	54.00
0001101b	6.50	0101101b	22.50	1001101b	38.50	1101101b	54.50
0001110b	7.00	0101110b	23.00	1001110b	39.00	1101110b	55.00
0001111b	7.50	0101111b	23.50	1001111b	39.50	1101111b	55.50
0010000b	8.00	0110000b	24.00	1010000b	40.00	1110000b	56.00
0010001b	8.50	0110001b	24.50	1010001b	40.50	1110001b	56.50
0010010b	9.00	0110010b	25.00	1010010b	41.00	1110010b	57.00
0010011b	9.50	0110011b	25.50	1010011b	41.50	1110011b	57.50
0010100b	10.00	0110100b	26.00	1010100b	42.00	1110100b	58.00
0010101b	10.50	0110101b	26.50	1010101b	42.50	1110101b	58.50
0010110b	11.00	0110110b	27.00	1010110b	43.00	1110110b	59.00
0010111b	11.50	0110111b	27.50	1010111b	43.50	1110111b	59.50
0011000b	12.00	0111000b	28.00	1011000b	44.00	1111000b	60.00
0011001b	12.50	0111001b	28.50	1011001b	44.50	1111001b	60.50
0011010b	13.00	0111010b	29.00	1011010b	45.00	1111010b	61.00
0011011b	13.50	0111011b	29.50	1011011b	45.50	1111011b	61.50
0011100b	14.00	0111100b	30.00	1011100b	46.00	1111100b	62.00
0011101b	14.50	0111101b	30.50	1011101b	46.50	1111101b	62.50
0011110b	15.00	0111110b	31.00	1011110b	47.00	1111110b	63.00
0011111b	15.50	0111111b	31.50	1011111b	47.50	1111111b	63.50

7.7.1 FA23h for NAND Devices that Support Value1 or Value2 Settings (cont'd)

Table 7.7-5 — Internal VrefQ Value2 Setting Versus Value as % of VccQ

Code	VrefQ (% of VccQ)	Code	VrefQ (% of VccQ)	Code	VrefQ (% of VccQ)	Code	VrefQ (% of VccQ)
0000000b	0.00	0100000b	25.00	1000000b	50.00	1100000b	75.00
0000001b	0.78	0100001b	25.78	1000001b	50.78	1100001b	75.78
0000010b	1.56	0100010b	26.56	1000010b	51.56	1100010b	76.56
0000011b	2.34	0100011b	27.34	1000011b	52.34	1100011b	77.34
0000100b	3.13	0100100b	28.13	1000100b	53.13	1100100b	78.13
0000101b	3.91	0100101b	28.91	1000101b	53.91	1100101b	78.91
0000110b	4.69	0100110b	29.69	1000110b	54.69	1100110b	79.69
0000111b	5.47	0100111b	30.47	1000111b	55.47	1100111b	80.47
0001000b	6.25	0101000b	31.25	1001000b	56.25	1101000b	81.25
0001001b	7.03	0101001b	32.03	1001001b	57.03	1101001b	82.03
0001010b	7.81	0101010b	32.81	1001010b	57.81	1101010b	82.81
0001011b	8.59	0101011b	33.59	1001011b	58.59	1101011b	83.59
0001100b	9.38	0101100b	34.38	1001100b	59.38	1101100b	84.38
0001101b	10.16	0101101b	35.16	1001101b	60.16	1101101b	85.16
0001110b	10.94	0101110b	35.94	1001110b	60.94	1101110b	85.94
0001111b	11.72	0101111b	36.72	1001111b	61.72	1101111b	86.72
0010000b	12.50	0110000b	37.50	1010000b	62.50	1110000b	87.50
0010001b	13.28	0110001b	38.28	1010001b	63.28	1110001b	88.28
0010010b	14.06	0110010b	39.06	1010010b	64.06	1110010b	89.06
0010011b	14.84	0110011b	39.84	1010011b	64.84	1110011b	89.84
0010100b	15.63	0110100b	40.63	1010100b	65.63	1110100b	90.63
0010101b	16.41	0110101b	41.41	1010101b	66.41	1110101b	91.41
0010110b	17.19	0110110b	42.19	1010110b	67.19	1110110b	92.19
0010111b	17.97	0110111b	42.97	1010111b	67.97	1110111b	92.97
0011000b	18.75	0111000b	43.75	1011000b	68.75	1111000b	93.75
0011001b	19.53	0111001b	44.53	1011001b	69.53	1111001b	94.53
0011010b	20.31	0111010b	45.31	1011010b	70.31	1111010b	95.31
0011011b	21.09	0111011b	46.09	1011011b	71.09	1111011b	96.09
0011100b	21.88	0111100b	46.88	1011100b	71.88	1111100b	96.88
0011101b	22.66	0111101b	47.66	1011101b	72.66	1111101b	97.66
0011110b	23.44	0111110b	48.44	1011110b	73.44	1111110b	98.44
0011111b	24.22	0111111b	49.22	1011111b	74.22	1111111b	99.22

7.7.2 FA23h for NAND Devices that Support Value3 Settings

Table 7.7-6 — Feature Table for Internal VrefQ for NAND Devices that Support Value3 Settings [23h]

Sub feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	Internal VrefQ Value3 Settings							
B1	Reserved							
B2	Reserved							
B3	Reserved							

Table 7.7-7 — NAND Minimum Internal VrefQ Allowable Range for NAND Devices that Support Value3 Settings (1.2 V VccQ)

Internal VrefQ Value3 Range/Step Size				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Default	Vendor Specific			VccQ
Vref_min	Vendor Specific			VccQ
Vref_max	Vendor Specific but has to be greater than NAND Minimum Internal VrefQ Allowable max values			VccQ
Vref_step	Vendor specific. Vendor can specify Vref_step Typ to be within 0.25% - 0.75% of VccQ			VccQ
Vref_Set_Tol	-1.75%	0%	1.75%	VccQ

For NAND devices that support Value3 Settings:

- VREFI is the VrefQ voltage inside the NAND. VREFI is calculated in the following manner: VREFI = (VrefQ Setting)*Vref_step + Vref_min.
- VrefQ Setting can range from 0 ~ 255 (8b)
- If the calculated VREFI ≥ Vref_max, then actual VREFI = Vref_max
- A table showing feature address register setting versus the expected actual VREFI value can be derived using the formula above and represented in the vendor datasheet

7.8 Feature Address 24h (WDCA)

Table 7.8-1 — Feature Table for Write Duty Cycle Adjustment [24h]

Sub feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	Reserved			WDCA Step Control				
B1	Reserved							
B2	Reserved							
B3	Reserved							

B0[4:0] for WDCA Step Control
00000b: 0step (default)
00001b: +1step
00010b: +2steps
00011b: +3steps
00100b ~ 01111b: +4steps ~ +15steps (Optional)
10000b: 0step
10001b: -1step
10001b: -2steps
10011b: -3steps
10100b ~ 11111b: -4steps ~ -15steps (Optional)

7.9 Feature Address 40h, 41h, and 42h (Per-Pin VrefQ Adjustment)

7.9.1 Per-Pin VrefQ Adjustment via Offset

For NAND vendors that implement per-pin VrefQ adjustment via the offset method, the following is the FA40h, FA41h and FA42h definition:

Table 7.9-1 — Feature Table for Per-Pin VrefQ Adjustment DQ0-DQ7 [40h]

Sub feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	VREF Offset for DQ1				VREF Offset for DQ0			
B1	VREF Offset for DQ3				VREF Offset for DQ2			
B2	VREF Offset for DQ5				VREF Offset for DQ4			
B3	VREF Offset for DQ7				VREF Offset for DQ6			

Table 7.9-2 — Feature Table for Per-Pin VrefQ Adjustment DBI [41h]

Sub feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	Reserved				VREF Offset for DBI			
B1	Reserved							
B2	Reserved							
B3	Reserved							

Table 7.9-3 — Reserved [42h]

Sub feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	Reserved							
B1	Reserved							
B2	Reserved							
B3	Reserved							

For each VREF Offset setting in FA40h and FA41h the decoding is as follows:

0000b: 0 step offset (default)
0001b: +1 step offset
0010b: +2 steps offset
0011b: +3 steps offset
0100b – 0111b: +4 ~ +7 steps offset
1000b: 0 step offset
1001b: -1 step offset
1010b: -2 steps offset
1011b: -3 steps offset
1100b – 1111b: -4 ~ -7 steps offset

7.9.2 Per-Pin VrefQ Adjustment via Absolute Setting

For NAND vendors that implement per-pin VrefQ adjustment via the absolute setting method, Table 7.9-4, Table 7.9-5, and Table 7.9-6 define FA40h, FA41h, and FA42h.

Table 7.9-4 — Feature Table for Per-Pin VrefQ Adjustment DQ0-DQ3 [40h]

Sub feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	VREF Setting for DQ0							
B1	VREF Setting for DQ1							
B2	VREF Setting for DQ2							
B3	VREF Setting for DQ3							

Table 7.9-5 — Feature Table for Per-Pin VrefQ Adjustment DQ4-DQ7 [41h]

Sub feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	VREF Setting for DQ4							
B1	VREF Setting for DQ5							
B2	VREF Setting for DQ6							
B3	VREF Setting for DQ7							

Table 7.9-6 — Feature Table for Per-Pin VrefQ Adjustment DBI [42h]

Sub feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	VREF Setting for DBI							
B1	Reserved							
B2	Reserved							
B3	Reserved							

8 Data Interface and Timing

8.1 Test Conditions

8.1.1 Combo Interface Devices

TBD

8.1.2 Legacy CTT-Only Interface Devices

The testing conditions that shall be used to verify compliance with a particular timing mode are below. The test conditions are the same regardless of the number of LUNs per Target.

Table 8.1-1 — Testing Conditions

Parameter	Single-ended	Differential
Positive input transition	VIL (DC) to VIH (AC)	VILdiff (DC) max to VIHdiff (AC) min
Negative input transition	VIH (DC) to VIL (AC)	VIHdiff (DC) min to VILdiff (AC) max
Minimum input slew rate	tIS = 1.0 V/ns	tIS = 2.0 V/ns
Input timing levels	VccQ / 2 if internal VREFQ or external VREFQ	crosspoint
Output timing levels	Vtt	crosspoint
Driver strength	Default[1]	Default[1]
Output reference load	50 Ohms to Vtt	50 Ohms to Vtt
NOTE 1 Default value is 35 Ohms or 37.5 Ohms.		

Table 8.1-2 — Differential AC and DC Input Levels

Parameter	Symbol	Min	Max	Units
Differential input high	VIHdiff (DC)	2 x [VIH (DC) – VREFQ]	Refer to Note 1.	V
Differential input low	VILdiff (DC)	Refer to Note 1.	2 x [VIL(DC) – VREFQ]	V
Differential input high AC	VIHdiff (AC)	2 x [VIH (AC) – VREFQ]	Refer to Note 1.	V
Differential input low AC	VILdiff (AC)	Refer to Note 1.	2 x [VIL(AC) – VREFQ]	V
NOTE 1 These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t and DQS_c) need to be within the respective limits [VIH(DC) max, VIL(DC) min] for single-ended signals as well as the limitations for overshoot and undershoot.				

The testing conditions used for output slew rate testing are specified below. Output slew rate is verified by design and characterization; it may not be subject to production test. The minimum slew rate is the minimum of the rising edge and the falling edge slew rate. The maximum slew rate is the maximum of the rising edge and the falling edge slew rate. Slew rates are measured under normal SSO conditions, with half of the DQ signals per data byte driving high and half of the DQ signals per data byte driving low. The output slew rate is measured per individual DQ signal. The differential parameters are used when the DQS signal is configured to operate as a differential signal.

8.1.2 Legacy CTT-Only Interface Devices (cont'd)

Table 8.1-3 — Testing Conditions for Output Slew Rate

Parameter	Single-ended	Differential
VOL(AC)	Vtt – (VccQ * 0.10)	—
VOH(AC)	Vtt + (VccQ * 0.10)	—
VOLdiff(AC)		-0.2 * VccQ
VOHdiff(AC)		0.2 * VccQ
Positive output transition	VOL (AC) to VOH (AC)	VOLdiff(AC) to VOHdiff(AC)
Negative output transition	VOH (AC) to VOL (AC)	VOHdiff(AC) to VOLdiff(AC)
tRISE[1]	Time during rising edge from VOL(AC) to VOH(AC)	—
tFALL[1]	Time during falling edge from VOH(AC) to VOL(AC)	—
tRISEdiff[2]	—	Time during rising edge from VOLdiff(AC) to VOHdiff(AC)
tFALLdiff[2]	—	Time during falling edge from VOHdiff(AC) to VOLdiff(AC)
Output slew rate rising edge	[VOH(AC) – VOL(AC)] / tRISE	[VOHdiff(AC) – VOLdiff(AC)] / tRISEdiff
Output slew rate falling edge	[VOH(AC) – VOL(AC)] / tFALL	[VOHdiff(AC) – VOLdiff(AC)] / tFALLdiff
Output reference load		5pf to Vss

NOTE 1 Refer to Figure 8.1-1.
NOTE 2 Refer to Figure 8.1-2.

8.1.2 Legacy CTT-Only Interface Devices (cont'd)

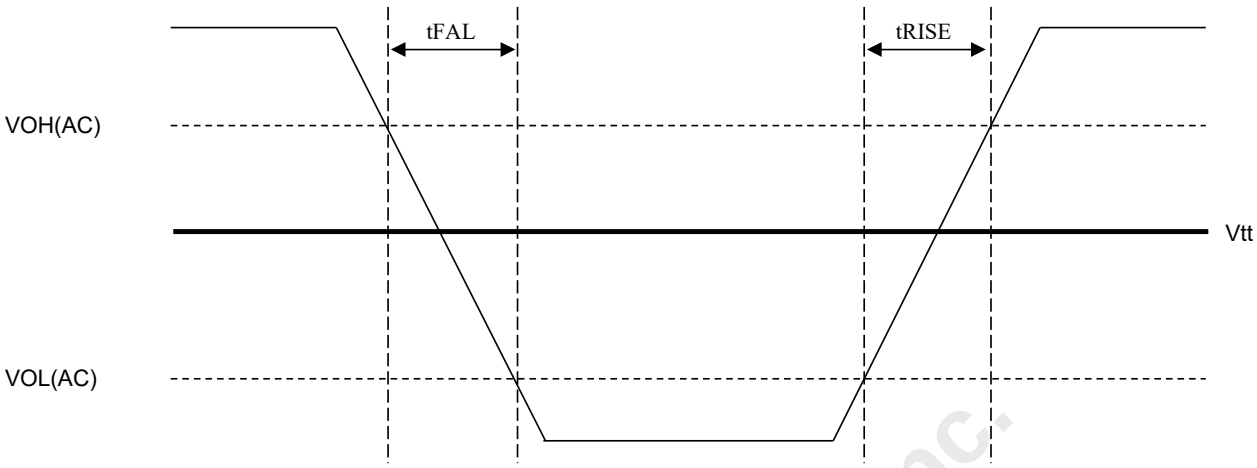


Figure 8.1-1 — tRISE and tFALL Definition for Output Slew Rate, (Single-ended)

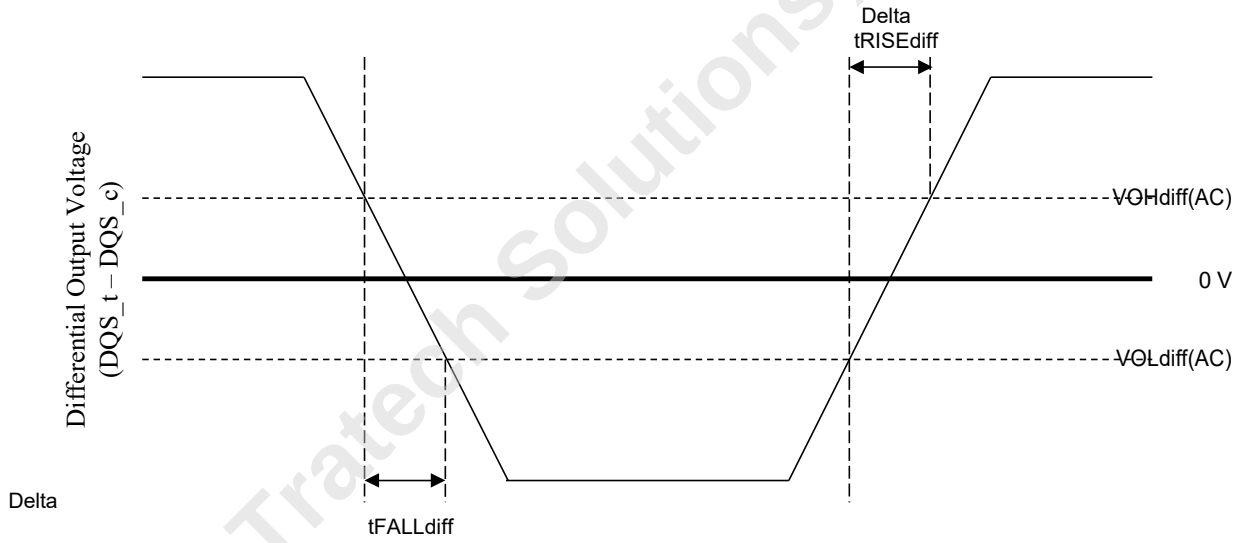


Figure 8.1-2 — tRISEdiff and tFALLdiff Definition for Output Slew Rate, (Differential)

The output slew rate matching ratio is specified below. The output slew rate mismatch is determined by the ratio of fast slew rate and slow slew rate. If the rising edge is faster than the falling edge, then divide the rising slew rate by the falling slew rate. If the falling is faster than the rising edge, then divide the falling slew rate by the rising slew rate. The output slew rate mismatch is verified by design and characterization; it may not be subject to production test

Table 8.1-4 — Output Slew Rate Matching Ratio

Parameter	Max
Output Slew Rate Matching Ratio (Pull-up to Pull-down), without ZQ calibration	1.4
Output Slew Rate Matching Ratio (Pull-up to Pull-down), with ZQ calibration	1.3

8.2 ZQ Calibration

ZQ calibration is required to make the driver strength of LUNs attached to a same channel consistent and it helps improve the signal integrity. ZQ calibration is highly recommended to be used for higher speed over 400 Mbps

8.2.1 ZQ Calibration Command sets

If a device supports ZQ calibration, Long ZQ calibration, and Short ZQ calibration shall be supported.

Table 8.2-1 — Long ZQ Calibration and Short Calibration Commands

Command	O/M	1st Cycle	2nd Cycle	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy	Target Level Commands
Long ZQ calibration	M	F9h	-			
Short ZQ calibration	M	D9h	-			

8.2.2 ZQ Calibration Process

ZQ calibration shall be performed after the driver strength setting and it shall be re-calibrated when the driver strengths are changed. ZQ calibration shall be done when the target device does not perform any other operation. If VREFQ is used, VREFQ shall be also enabled before ZQ calibration performs.
F9h is used for an initial ZQ calibration and D9h is for a run-time ZQ calibration. The initial ZQ calibration takes 1us as maximum and the run-time ZQ calibration does 0.3 µs as maximum. RZQ ball of the BGA package shall be connected to Vss through 300 ohm resistor (300 ohm +/- 1% tolerance external resistor).

During busy period for ZQ calibration, any command including Read Status shall not be issued. The host shall check Busy/Ready status via R/Bn pin or shall wait the specified period of time (i.e., tZQCL or tZQCS) to ensure the ZQ calibration done. After the device turns into Ready state, the host shall issue Read Status to check the pass/fail of the calibration. If Reset command is issued during ZQ calibration, the state of the devices are not guaranteed and host needs to re-run the ZQ calibration. Before executing short ZQ calibration operation, long ZQ calibration shall be completed successfully, without any abortion by Reset, at least once after power-up. When ZQ calibration is aborted by a Reset command, it will take maximum 10 µs (i.e., tRST) to complete the reset operation. If Reset operation is done during long ZQ calibration, the ZQ calibrated value will return to the factory default one. If Reset is done during short ZQ calibration, the ZQ calibrated value will return to the vendor specific value. If ZQ calibration operation fails, the ZQ calibrated value will return to the vendor specific value.

During the ZQ calibration, all devices are connected to the DQ bus should be in high impedance, therefore the on-die-termination is off.

Commands for ZQ calibration is followed by one cycle of LUN selection. 00h for LUN select points LUN0 and 01h does LUN1. Figure 8.2-1 illustrates the sequence of ZQ calibration.

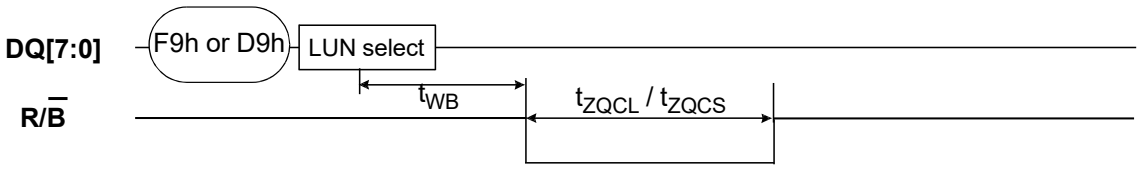


Figure 8.2-1 — ZQ Calibration Sequence

8.3 Package Electrical Specifications and Pad Capacitance

The requirements in this section apply to devices that support the VccQ=1.2 V. The requirements in this section are optional for devices that support VccQ = 1.8 V when the device supports I/O speeds 533 MT/s or less and required for devices that support VccQ = 1.8 V when the device supports I/O speeds greater than 533 MT/s.

ZIO applies to DQ[7:0], DQS_t, DQS_c, RE_t and RE_c. TdIO RE applies to RE_t and RE_c. TdIO and TdIOMismatch apply to DQ[7:0], DQS_t and DQS_c. Mismatch and Delta values are required to be met across same data bus on given package (i.e., package channel), but not required across all channels on a given package.

Table 8.3-1 — Package Electrical Specification

Symbol	Parameter	<=400 MT/s		533 MT/s		667 MT/s		800 MT/s to 1200 MT/s		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Z_{IO}	Input/Output Zpkg	35	90	35	90	35	90	35	90	Ohms
Td_{IO}	Input/Output Pkg Delay	-	160	-	160	-	145	-	130	ps
$Td_{IO\ RE}$	Input/Output Pkg Delay	-	160	-	160	-	145	-	130	ps
Td_{IO}Mismatch	Input/Output Pkg Delay Mismatch	-	50	-	40	-	40	-	40	ps
$D\ Z_{IO\ DQS}$	Delta Zpkg for DQS_t and DQS_c	-	10	-	10	-	10	-	10	Ohms
$D\ Td_{IO\ DQS}$	Delta Pkg Delay for DQS_t and DQS_c	-	10	-	10	-	10	-	10	ps
$D\ Z_{IO\ RE}$	Delta Zpkg for RE_t and RE_c	-	10	-	10	-	10	-	10	Ohms
$D\ Td_{IO\ RE}$	Delta Pkg Delay for RE_t and RE_c	-	10	-	10	-	10	-	10	ps

NOTE 1 The package parasitic(L and C) are validated using package only samples. The capacitance is measured with Vcc, VccQ, Vss, and VssQ shorted with all other signal pins floating. The inductance is measured with Vcc, VccQ, Vss, and VssQ shorted and all other signal pins shorted at the die side(not pin).

NOTE 2 Package only impedance (ZIO) is calculated based on the Lpkg and Cpkg total for a given pin where:
ZIO(total per pin) = SQRT(Lpkg/Cpkg)

NOTE 3 Package only delay(TdIO) is calculated based on Lpkg and Cpkg total for a given pin where:
TdIO(total per pin) = SQRT(Lpkg*Cpkg)

NOTE 4 Mismatch for TdIO (TdIOMismatch) is value of Pkg Delay of fastest I/O minus the value of Pkg Delay for slowest I/O.

NOTE 5 Delta for DQS is Absolute value of ZIO(DQS_t-ZIO(DQS_c) for impedance(Z) or absolute value of TdIO(DQS_t)-TdIO(DQS_c) for delay(Td)

NOTE 6 Delta for RE is Absolute value of ZIO(RE_t-ZIO(RE_c) for impedance(Z) or absolute value of TdIO(RE_t)-TdIO(RE_c) for delay(Td)

8.3 Package Electrical Specifications and Pad Capacitance (cont'd)

Table 8.3-2 — Pad Capacitances Apply to DQ[7:0]. DQS_t, DQS_c, RE_t, and RE_c.

Symbol	Parameter	<=400 MT/s		533 MT/s		667 MT/s		800 MT/s to 1200 MT/s		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
C_{IO}	Input/Output Capacitance	-	2.5	-	2.5	-	2.5	-	2.5	pF
C_{ZQ}	ZQ capacitance	-	2.875	-	2.875	-	2.875	-	2.875	pF
$D C_{IO DQS}$	Delta Input/Output Capacitance DQS_t and DQS_c	0	0.2	0	0.2	0	0.2	0	0.2	pF
$D C_{IO RE}$	Delta Input/Output Capacitance for RE_t and RE_c	0	0.2	0	0.2	0	0.2	0	0.2	pF

NOTE 1 These parameters are not subject to a production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with Vcc, VccQ, Vss, and VssQ applied and all other pins floating (accept the pin under test). VccQ = 1.2 V, VBIAS = VccQ/2 and on-die termination off.
NOTE 2 These parameters apply to monolithic die, obtained by de-embedding the package L and C parasitics.
NOTE 3 Delta for DQS is the absolute value of CIO(DQS_t) - CIO(DQS_c).
NOTE 4 Delta for RE is the absolute value of CIO(RE_t) - CIO(RE_c).

8.4 tCD Parameter

Table 8.4-1 — Timing Parameter Description

Parameter	Description
tCD	$\overline{CE}$ setup time to DQS(DQS_t) low after $\overline{CE}$ has been high for greater than 1us

Table 8.4-2 — tCD Timing Parameter

Parameter	200 MHz		266 MHz		333 MHz		400 MHz		533 MHz		600 MHz		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tCD[1]	100	-	100	-	100	-	100	-	100	-	100	-	ns

NOTE 1 If host is unable to track CE high time, then host shall use tCD timing.

8.5 Additional Timing Parameter for I/O Speed Greater than 400 MT/s

Table 8.5-1 — Timing Parameter Description

Parameter	Description
tWHR2	$\overline{WE}$ High to RE Low for Random data out
tADL	Address to Data Loading Time
tCR	CE Low to RE Low
tCR2	$\overline{CE}$ Low to $\overline{RE}$ Low when $\overline{CE}$ has been high for a period greater than or equal to 1 us. If host is unable to track $\overline{CE}$ high time, then host shall use tCR2 timing for tCR parameter.

Table 8.5-2 — Timing Parameters Shall be Used for NAND Device that are Capable of I/O Speed Greater than 400MT/S

Parameter	Min	Max	Unit
tWHR2	400	-	ns
tADL	400	-	ns
tCR	10	-	ns
tCR2	100	-	ns

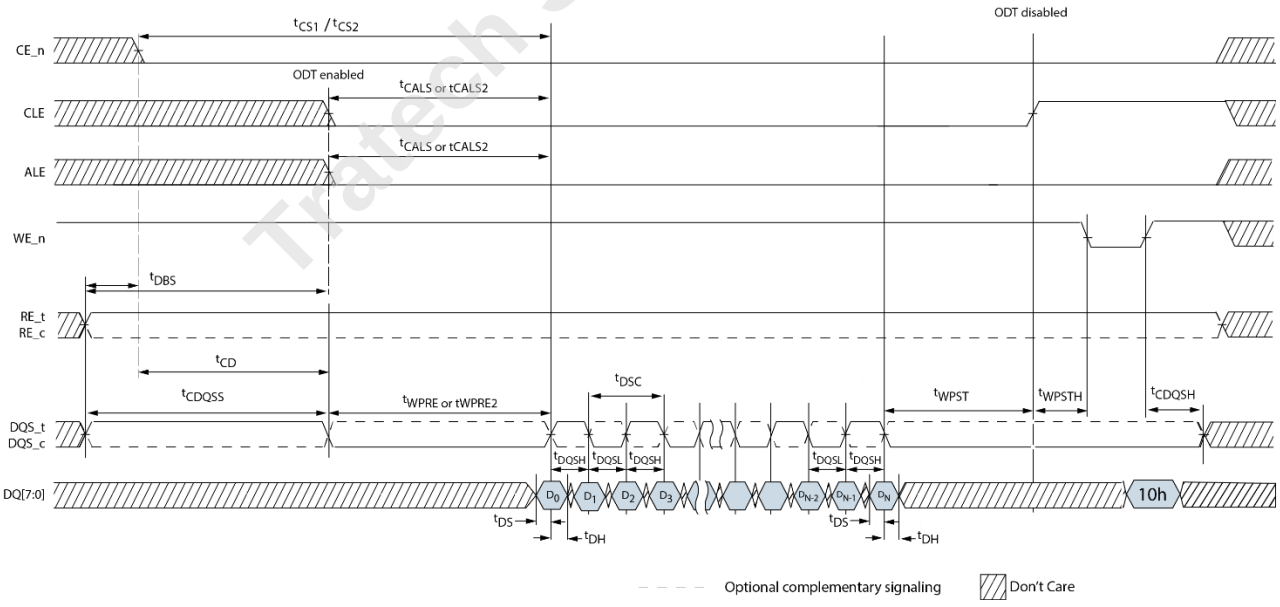


Figure 8.5-1 — Timing Parameter Description

8.6 Data Training

8.6.1 ODT Disable and Re-Enable

8.6.1.1 Need for ODT Control During LTT Interface Training

ODT termination causes signal swing on the channel to be smaller than that of an unterminated channel.

ODT termination is typically enabled during data input and data output bus cycles. Set Feature commands have data input cycles and for some NAND devices, ODT will turn on during these data input cycles. Read Status has data output cycles and for some NAND devices, ODT will turn on during these data output cycles.

Once the LTT interface has been enabled, the NAND and controller internal VrefQ will still be at an untrained state and the smaller signal swing with ODT can cause failure of Set Feature or Read Status and Get Feature sequences.

Efficient ODT disable/re-enable control methods are needed to control ODT termination while the LTT interface is still being configured and trained.

8.6.1.2 ODT Control NAND Device Types

NAND devices fall under the following types:

- Type1 NAND Device: Employ Pin/Hardware based ODT Control
- Type2 NAND Device: Employ Command based ODT Control

On Type1 devices, ODT control is done via pin or the ODT control is already built into the NAND hardware itself and no additional command for ODT control is needed. Type1 devices shall ignore 1Bh and 1Ch commands.

On Type2 devices, ODT control is done via commands (i.e. Matrix Termination). Type2 devices shall support one of the following options for ODT disable and re-enable:

- 1Bh/1Ch Commands:
    - 1Bh turns OFF target and non-target ODT operations
    - 1Ch re-enables target and non-target ODT operations
- Vendor Specific Command/Address sequence

8.6.1.3 ODT Disable (1Bh) and ODT Re-Enable (1Ch) Commands

ODT Disable (1Bh) and ODT Re-Enable (1Ch) commands are used on Type2 NAND devices for ODT termination control.

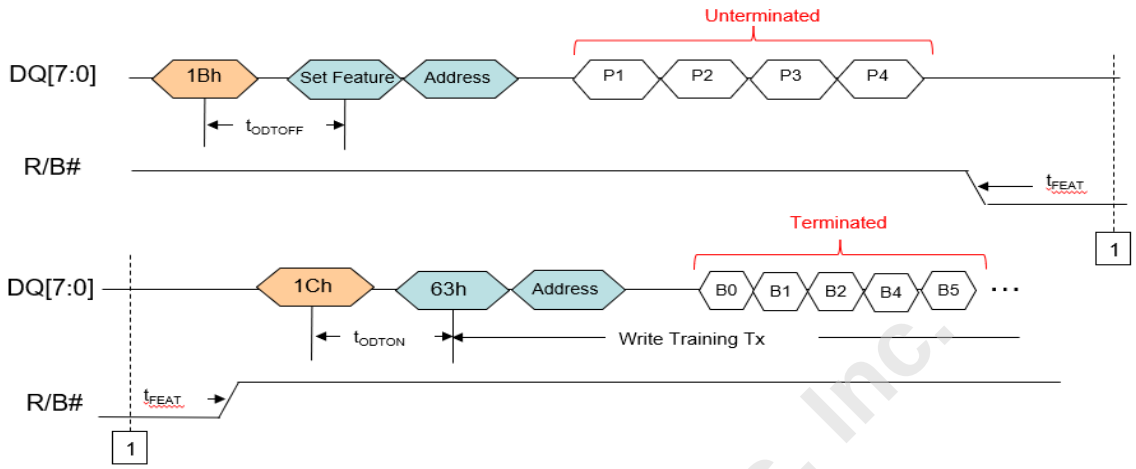


Figure 8.6-1 — ODT Disable (1Bh) and ODT Re-Enable (1Ch) Commands Timing Diagram

Table 8.6-1 — tODTOFF and tODTON Specifications

Parameter	Symbol	Min	Max	Notes	Unit
ODT Disable (1Bh) command to next command	tODTOFF	100	-		ns
ODT Re-Enable (1Ch) command to next command	tODTON	100	-		ns

8.6.2 Interface Training Flows

Training features shown in this section shall be supported by NAND devices operating over 800 MT/s in heavily loaded systems.

DCC Training is the feature for the NAND to compensate duty cycle mismatch of RE_t/c signal. Read/Write DQ Training is the feature for the host to align DQS and DQ signals caused by un-matched DQS path. For combo interface (CTT+LTT) devices, Read/Write DQ Training may also be used to train the controller/ NAND internal VrefQ voltages.

8.6.2.1 Combo Interface (CTT+LTT) Devices Training Flow

8.6.2.1.1 Initial Configurations

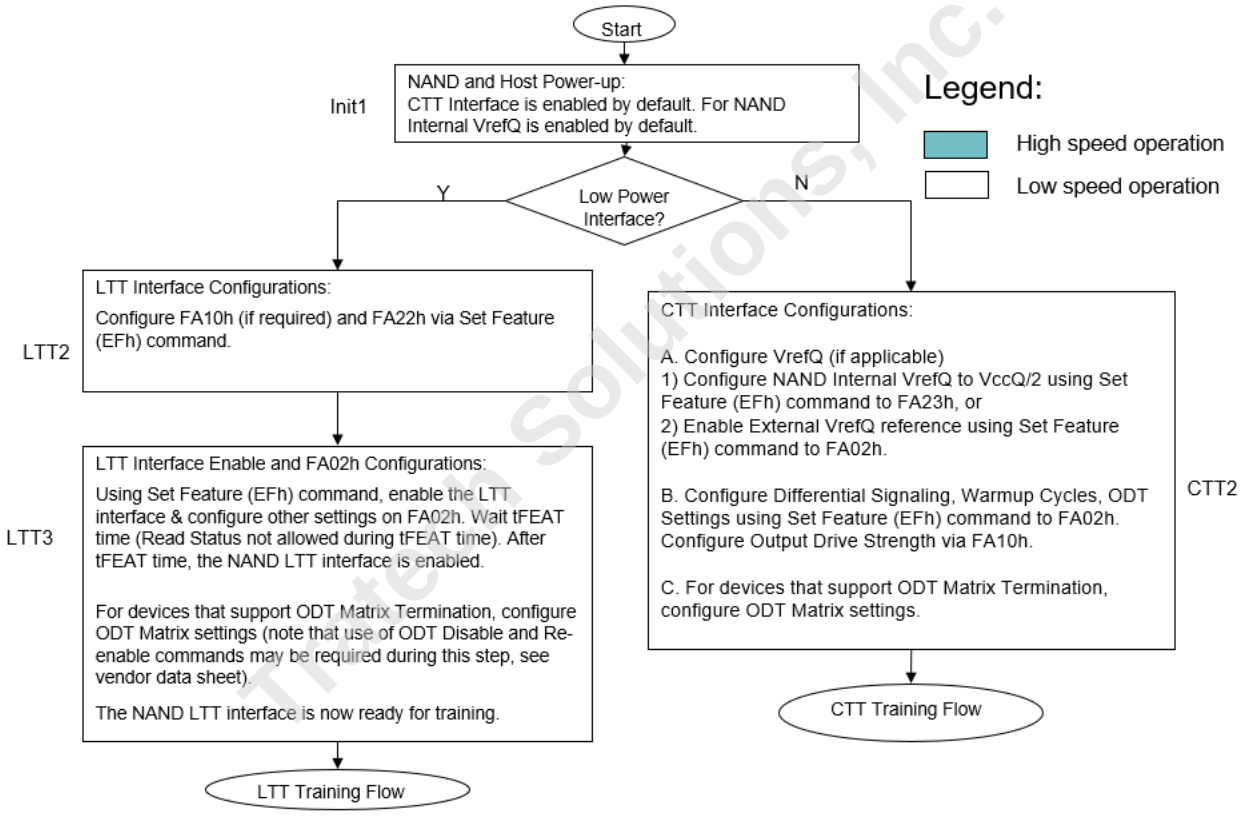


Figure 8.6-2 — Initial Configurations

8.6.2.1.2 LTT Interface Training Flow

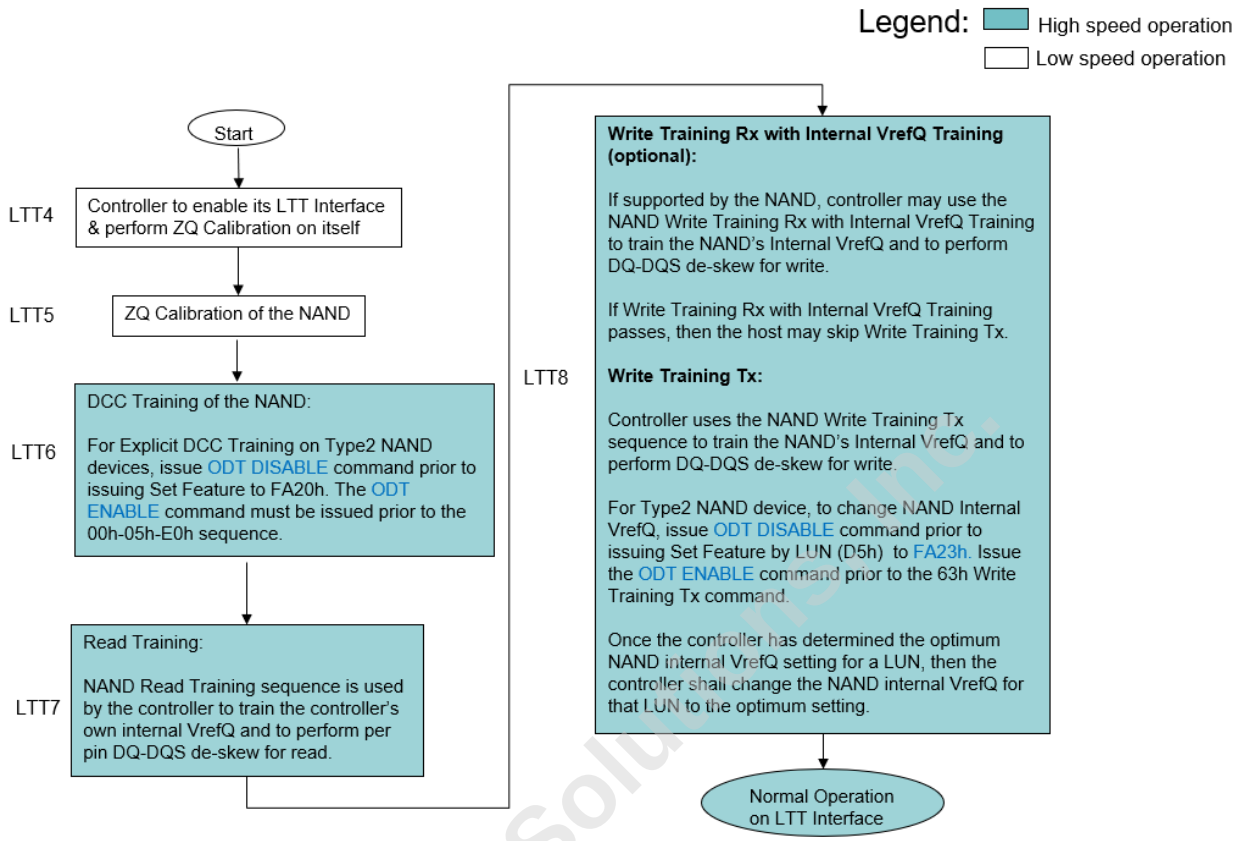


Figure 8.6-3 — LTT Training Flow

The following are Read Status and Get Feature command restrictions during the LTT Interface Training flow:

1. Read Status and Get Feature commands are not allowed during and in between LTT3 (NAND-side LTT interface enable) and LTT4 (Controller-side LTT interface enable)
2. Read Status and Get Feature commands are allowed during LTT5 (NAND-side ZQ calibration), LTT6 (NAND-side DCC training) and prior to LTT7 (Read Training) completion, subject to the following conditions:
   - ODT on the NAND-side must be turned off prior to data output cycles (ie. through ODT Disable command or ODT pin)
   - ODT on the controller-side must also be turned-off prior to Read Status/Get Features sequence)
   - Read Status/Get Features must be done at a tRC(avg) ≥ 30ns. The output signals shall meet Single-Ended AC and DC Output Levels for Unterminated DQ-Related Signals specifications when evaluated using Output Timing Reference Load for Unterminated Channel, and with default PDDS and default CH_ODT settings
3. Read Status and Get Feature commands are allowed after LTT7 (Read Training) completion without having to disable ODT on NAND-side or Controller-side prior to Read Status/Get Features sequence.

8.6.2.1.3 CTT Interface Training Flow

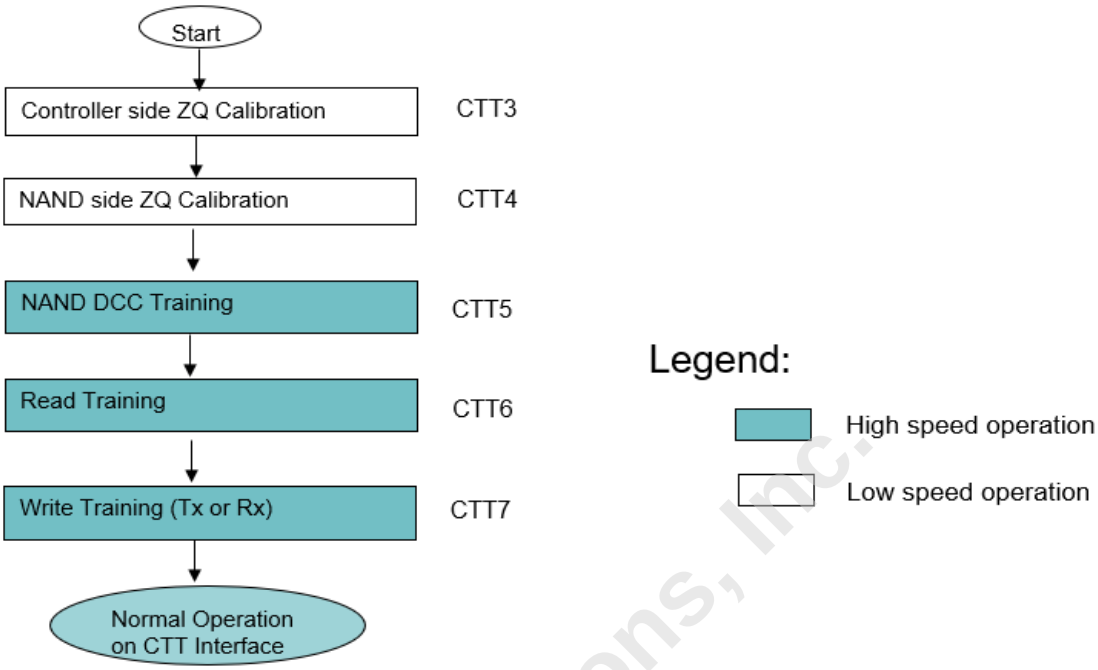


Figure 8.6-4 — CTT Training Flow

8.6.2.2 Legacy CTT-Only Devices Training Flow

Figure 8.6-5 shows when each training shall be done after power-on for devices that only support the CTT interface. I/F Initialization shall be done before training at slower interface speeds such as High-Speed Interface setting, Driver Strength setting, and ZQ calibration. The host shall operate DCC training before Read/Write DQ training. If the host uses the NAND device over 800 MT/s, the host shall complete all the trainings defined in this section when training is required.

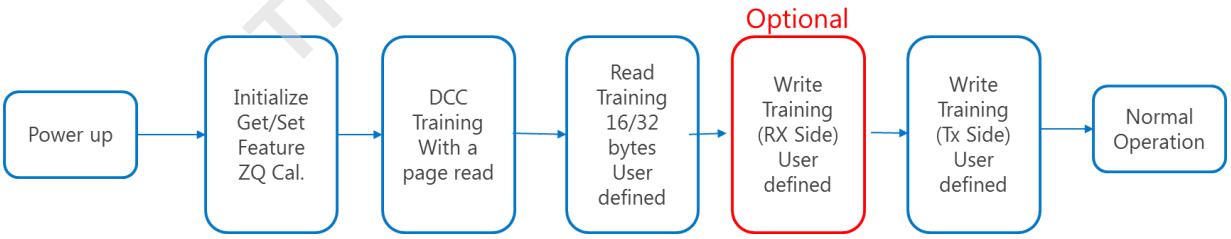


Figure 8.6-5 — Training Flow After Power-On

8.6.3 DCC Training

DCC Training shall be performed after the ZQ calibration is completed. This section defines two types of DCC. One is explicit DCC and the other is implicit DCC.

Explicit DCC is initiated by the host to issue specific command sequence defined in clause 8.6.1.1 or clause 8.6.1.2. Either or both of Explicit DCC shall be supported by the NAND devices operating over 800 MT/s.

Implicit DCC is optional feature for the NAND devices and is initiated by the host to set DCCI_EN enable which is assigned in B0[1] of Feature Address 20h. If DCCI_EN is enabled, the NAND device carries out DCC training to update the training result during warm up cycles where “warm up cycles” is sometimes referred to “DQS latency”. Implicit DCC may require specific number of warm up cycles to be set and it shall be given by vendor datasheet.

8.6.3.1 DCC (RE_t/c) Training Using Set Feature

DCC training using Set Feature is initiated by the host to set DCCE_EN enable which is assigned in B0[0] of Feature Address 20h. When this is enabled, DCCI_EN which is assigned in B0[1] is “don’t care”. On power-up, DCCE_EN shall be disabled. The host shall enable it to perform DCC Training. Refer to Feature Address description for more information.

After Set Feature, the host shall issue the Random Data Out command with address information based on the Set Feature command used to enable the DCC training feature. If the Set Feature command used was an EFh command, then the addresses for the Random Data Out command sequence shall be filled with 00h. If the Set Feature command used was the D5h (Set Feature for Each LUN) command, then the addresses for the Random Data Out command sequence must have the same LUN address that was used during the D5h command. If LUN address is not used in the Random Data Out sequence, then fix all column address to “00h”. The host shall then calibrate RE_t and RE_c by sending those signals for a page size. (Page size shall be given by vendor datasheet.)

During the data output cycles produced by these RE_t and RE_c toggles, the DQ and DQS of the LUNs under training may be driven or Hi-Z depending on the NAND vendor DCC Training implementation. Refer to the NAND vendor datasheet to see if DQ and DQS are driven or Hi-Z during this time. The data for these data output cycles shall be invalid and ignored by the host. When doing multi-LUN DCC training for LUN’s which share the same channel, the DQ and DQS signals of the LUNs involved in the training shall be Hi-Z during the data output cycles of the Random Data Out sequence to avoid bus contention.

After sending RE_t and RE_c for page size length, Status Check shall be performed to confirm whether DCC is Pass or Fail via SR[0]. If fail, the host shall issue Random Data Out command and resend RE_t and RE_c signals to calibrate again. If EFh is used, all the LUNs under the Target perform DCC (All LUN DCC). If D5h command is used, selected LUN under the Target performs DCC (Single LUN DCC). The device may support either or both of All LUN DCC and Single LUN DCC. See vendor’s datasheet. After completing Explicit DCC using Set Feature, DCCE_EN shall be set to 0.

8.6.3.1 DCC (RE_t/c) Training Using Set Feature (cont'd)

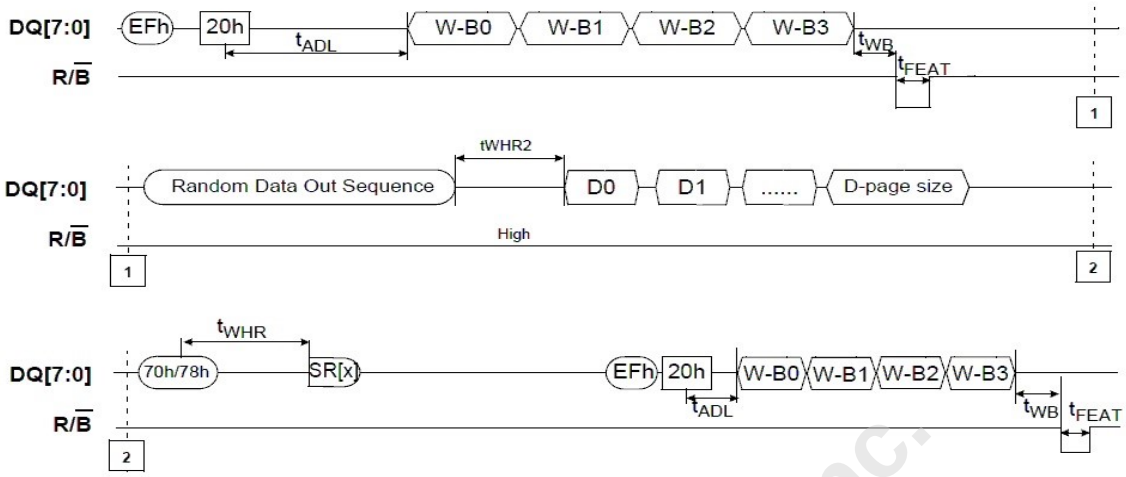


Figure 8.6-6 — DCC (RE_t/c) Training using Set Feature

8.6.3.2 DCC (RE_t/c) Training using Command (Optional)

DCC training using a command can be initiated using CMD18h followed by LUN Address. After issuing LUN address, the host shall calibrate RE_t and RE_c by toggling these signals for a page size. (Page size shall be given by vendor data sheet). The data returned by the device is vendor specific data pattern so that there is no impact of data pattern on DCC training. After sending the required number of RE_t and RE_c signals, Status Check shall be performed to confirm whether DCC is Pass or Fail. If status is a Fail, user has to issue RESET command (FFh) wait for the RESET command to execute and then re-issue the Command based DCC sequence.

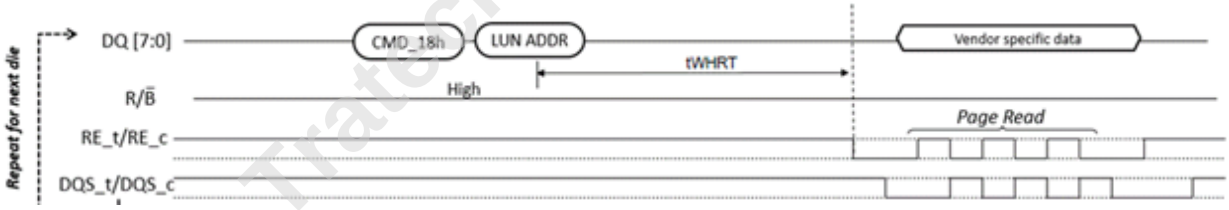


Figure 8.6-7 — DCC (RE_t/c) Training using Command (Optional)

Timing specs of RE_t/RE_c during DCC page read will follow normal Read timing as per vendor data sheet.

8.6.4 Read DQ Training

Read DQ Training is the function that outputs a 16 bit user-defined pattern on each of the DQ pins. It means a total of 16 bytes is output by the NAND device (note some vendors may provide a 32 byte pattern).

Read DQ Training is initiated by issuing a [Read DQ Training] command 62h followed by LUN Address then three address cycles. Three address cycles are 1st address (8bit invert mask), 2nd address (first eight bit pattern) and 3rd address (second eight bit pattern). Figure 8.6-8 shows example data pattern (i.e., 1st 35h, 2nd 5Ah, 3rd 82h address).

8.6.4 Read DQ Training (cont'd)

Pin	Inverse Setting (Mask)		0~15																16~31 (Optional)													
			1st Input DATA : 5Ah								2nd Input DATA : 82h								Swap 1st,2nd data of DQ4~7 ↔ DQ0~3 (Optional)															
DQ0	1 (Inverse)	35h	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ1	0		0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ2	1 (Inverse)		1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1
DQ3	0		0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1
DQ4	1 (Inverse)		1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ5	1 (Inverse)		1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1
DQ6	0		0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ7	0		0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1

Figure 8.6-8 — Example of User Defined Pattern for Read Training

If '1' is indicated by a bit in 1st address, DQx corresponding to a bit shall be inverted and the NAND device outputs data pattern designated by 2nd and 3rd addresses masked I/O following in invert mask indicated by 1st address by RE, /RE toggling, the data will inversed by masked I/O. For DBI pin behavior during Read DQ Training refer to section 8.8.3 DBI Behavior During Read DQ Training.

If host issues RE, /RE toggling for more than the vendor defined pattern length, data will be wrapped.

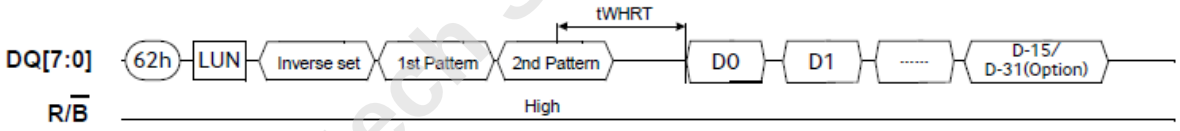


Figure 8.6-9 — Read DQ Training

During Read DQ Training, the controller shall optimize its own internal VrefQ voltage (required on LTT interface, optional on CTT interface) and also optimize the strobe point of DQ signals by DQS. tDVWp is the output valid window for a single DQ pin while tDVWd is the output valid window of all DQ pins taken as a group. The NAND may require DCC training to meet tDVWp or tDVWd specifications. In order for a system to take advantage of the wider per-pin data-eye opening (tDVWp) though, the system must be able to adjust each DQ pin relative to DQS during Read DQ Training.

8.6.4 Read DQ Training (cont'd)

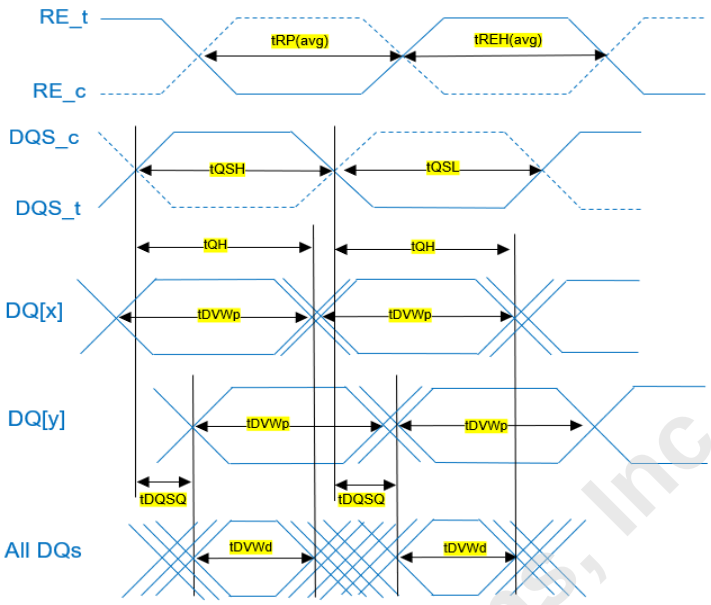


Figure 8.6-10 — Read Data Output Valid Window Timings

8.6.5 Write DQ Training (Tx Side)

To perform Write training at Tx side, the controller shall issue 63h command followed LUN address. After issuing LUN address, the host shall input data pattern and confirm whether the input is successfully done by checking the output by NAND in following sequence.

Data sizes for Write DQ is pre-defined by NAND. The host shall recognize the data sizes by Get Feature (Feature Address = 20h, B2) and shall input and output the data based on the size. After writing data to the NAND with 63h command, the data can be read back with 64h command followed by LUN address and the results shall be compared with "expected" data to see if further training (DQ delay) is needed. For DBI pin behavior during Write DQ Training (Tx Side) refer to section 8.8.2 DBI Behavior During Write DQ Training (Tx Side).

If fewer data than pre-defined data bytes are written, then unwritten registers will have un-defined data when read back. If over pre-defined data bytes read were executed, the data are also un-defined and invalid.

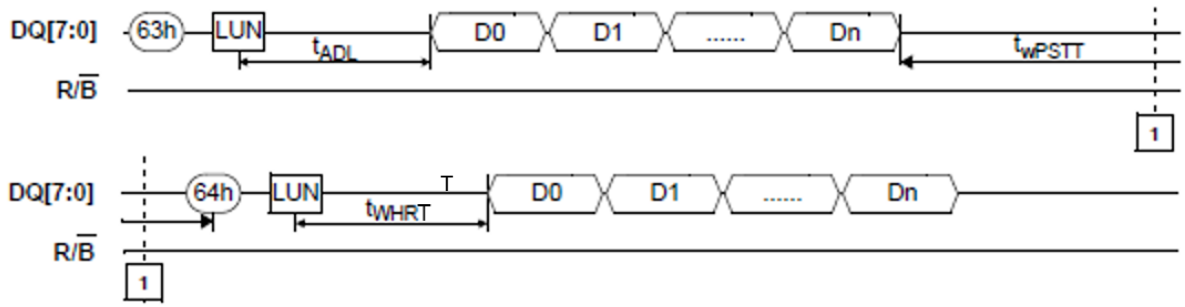


Figure 8.6-11 — Write DQ Training (Tx side)

8.6.5.1 NAND Internal VrefQ Training (Required for LTT, Optional for CTT)

The controller shall find the optimum internal VrefQ level for each NAND die by performing internal VrefQ scan and using the Write Training Tx sequence to produce a pass/fail result each scanned internal VrefQ level. Once the optimum level has been found, the host shall configure the NAND to use that level.

The host shall not set the NAND internal VrefQ to a setting beyond the allowable internal VrefQ range during Write Training Internal VrefQ training.

See Feature Address 23h for NAND internal VrefQ, step size, range, and accuracy requirements.

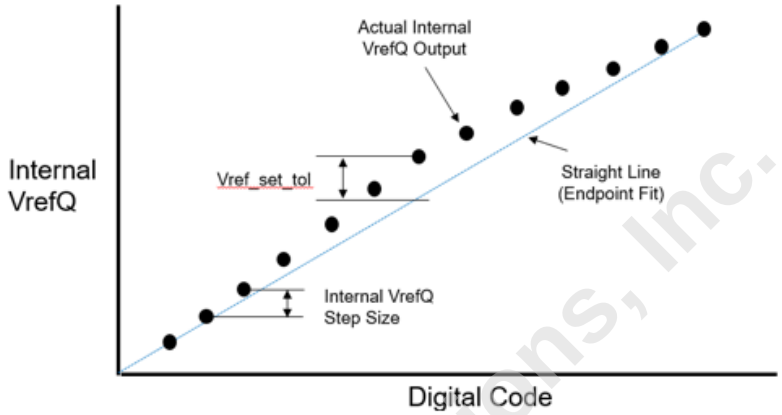


Figure 8.6-12 — NAND Internal VrefQ Characteristics

8.6.5.2 Timing De-skew of Each DQ Versus DQS

The controller shall also find the optimum input timing by timing scan between each DQ to DQS_c/DQS_t and shall compensate input timing of each DQ and DQS to be the optimum per pin per chip.

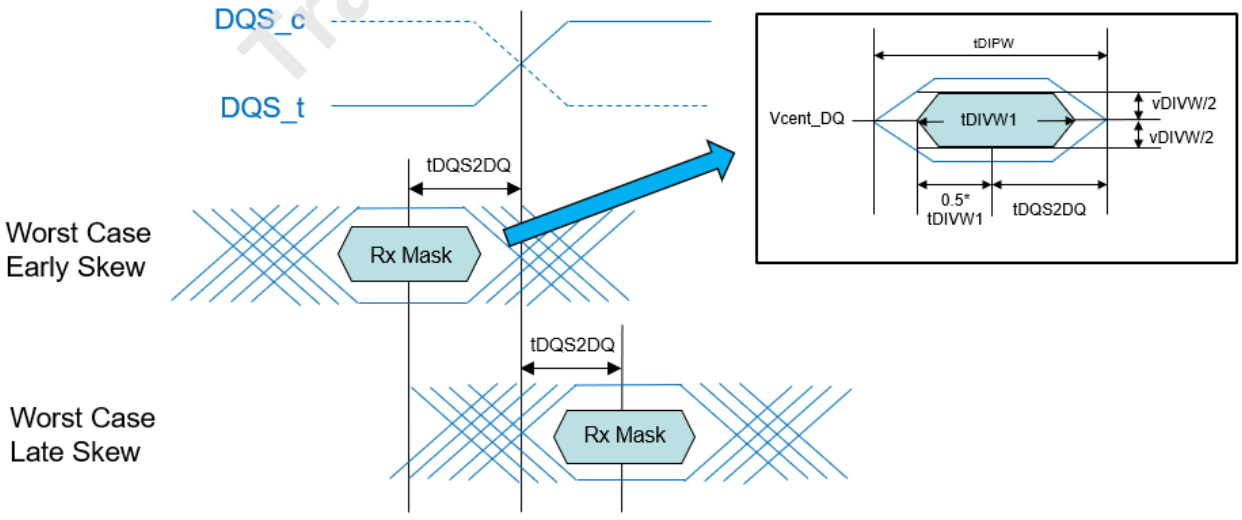


Figure 8.6-13 — Write DQ Training (Tx Side) Range for Data Input

8.6.5.2 Timing De-skew of Each DQ Versus DQS (cont'd)

Write DQ Training of NAND shall be used to find optimum input timing at "NAND internal latch", not at "NAND pin".

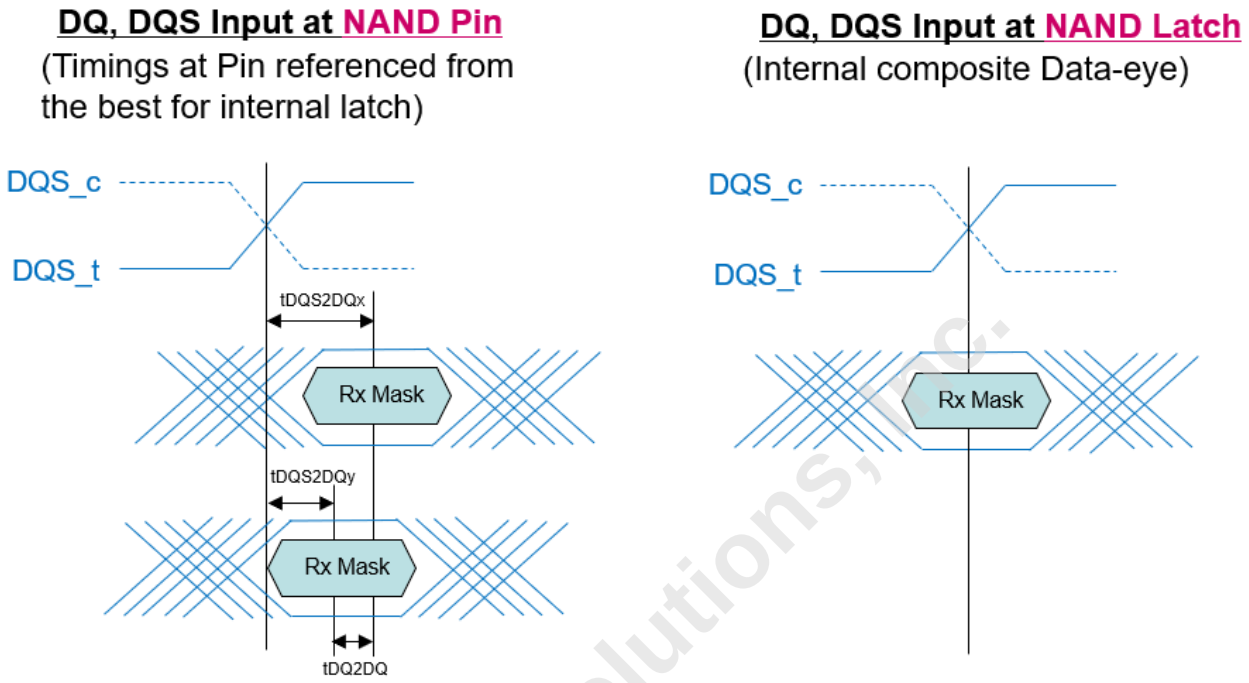
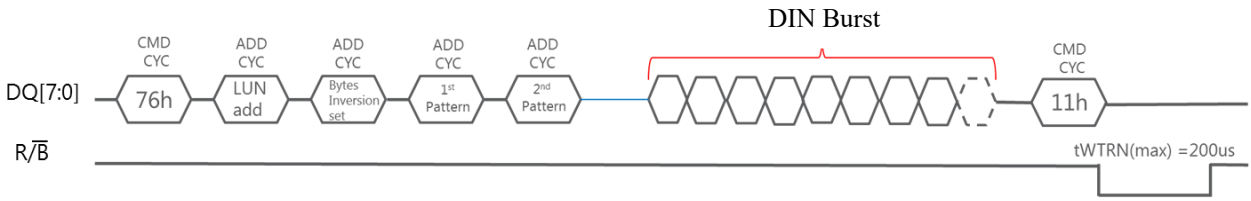


Figure 8.6-14 — Write DQ Training (Tx Side) Timing De-skew at NAND Latch Versus NAND Pin

8.6.6 Write DQ Training (Rx Side, Optional)

To perform Write training at Rx side, the controller shall issue 76h command followed by LUN address. After issuing LUN address, the host shall issue 3 address cycles for data pattern format. The definition of these 3 address cycles are the same as the ones mentioned in read training. After the 3 address cycles, the host shall issue data input with the same pattern determined by the 3 address cycles for 1 full page. The input data shall be wrapped around the data pattern length (16 or 32) until a full-page data is issued. The training sequence shall be ended by 11h command and the NAND will perform write training during the R/B_ time (tWRTN). The host may poll the R/B_ status by status command to check the completion of the training operation. The status of the training for each DQ can be checked by issuing Get Feature by LUN with address 21h (B1 and B2). The complete byte definition is given in the Feature Address 21h table.



DIN Burst: Data Input with the same pattern specified in 3 address cycle wrapping around the data pattern length (16 or 32) for 1 full page

Figure 8.6-15 — Write DQ Training (Rx Side) Optional

8.6.6 Write DQ Training (Rx Side, Optional) (cont'd)

If Write Training (Rx Side) passes, then the host may skip Write Training (Tx Side). Figure 8.6-16 is an example of the process for doing Write Training on the Rx side.

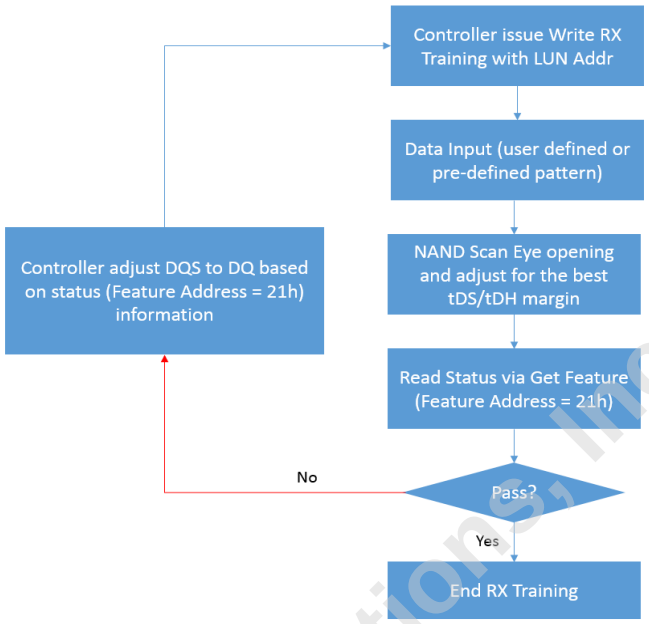


Figure 8.6-16 — Flow Chart for Write DQ Training (Rx Side)

8.6.6.1 Write DQ Training (Rx Side) With Internal VrefQ Training (Optional and LTT Interface Only)

Write DQ Training (Rx Side) with Internal VrefQ Training is an optional feature used only on the LTT interface. It is enabled by setting Feature Address 21h B0[2] =1. On the CTT Interface, Feature Address 21h B0[2] is ignored by the NAND.

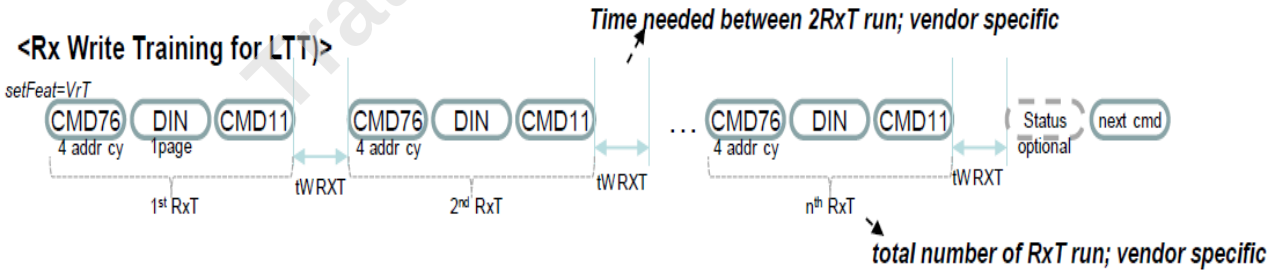


Figure 8.6-17 — Write DQ Training (Rx Side) with Internal VrefQ Training Mode Sequence

An RxT sequence is defined as a CMD76h (4 address cycles) – DIN (1 page) – CMD11h sequence. At the end of each RxT sequence, a wait time of tWRXT(min) of 200ns is required. The host repeats the RxT sequence an n number of times, where n is vendor specific. Status Reads (Read Status and Get Features commands) are available after the whole sequence has completed (after the tWRXT time of the nth RxT iteration has completed).

If Write Training (Rx Side) passes, then the host may skip Write Training (Tx Side). After the training has completed, the host shall clear Feature Address 21h B0[2] = 0.

8.6.7 Write Duty Cycle Adjustment (WDCA, Optional)

Write Duty Cycle Adjustment (WDCA) is an optional feature that provides a way to compensate for input DQS duty cycle loss at the NAND device. The WDCA feature is controlled via FA24h.

The diagram below shows the NAND interface training flow with WDCA. The controller repeats between configuring WDCA settings and performing Write Training sequence to find the optimum WDCA setting.

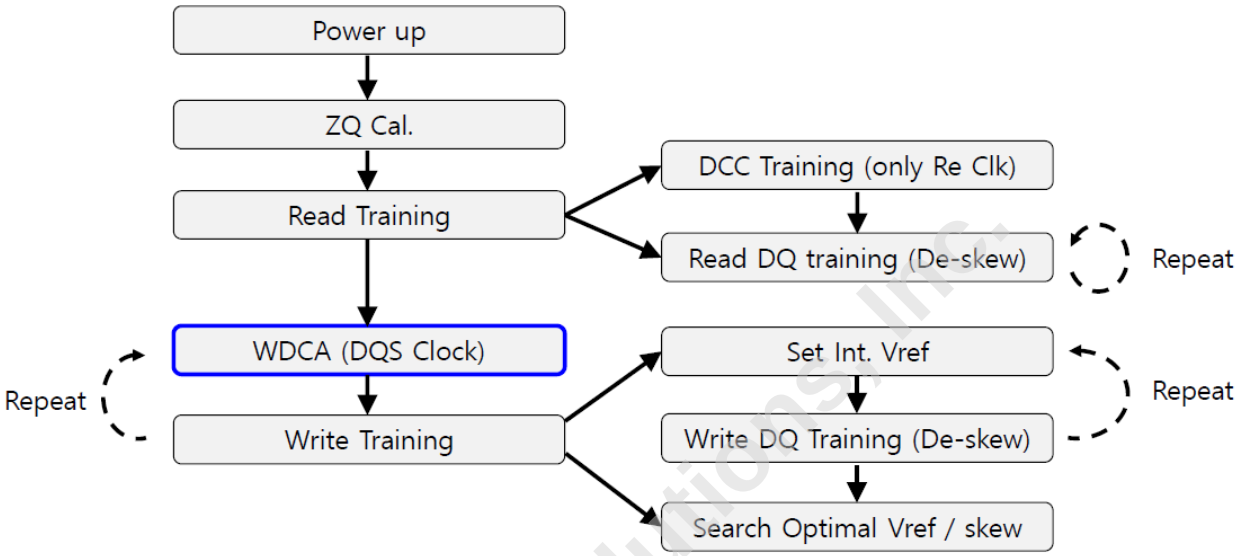


Figure 8.6-18 — Data Training Flow with WDCA

8.6.8 Write Training Monitor

With voltage and temperature changes on the system, there is a need for a method to monitor whether the last obtained optimum training settings are still sufficient to produce low error rates on the interface. A method to monitor sufficiency of the last obtained optimum settings is described in Figure 8.6-19 and Figure 8.6-20

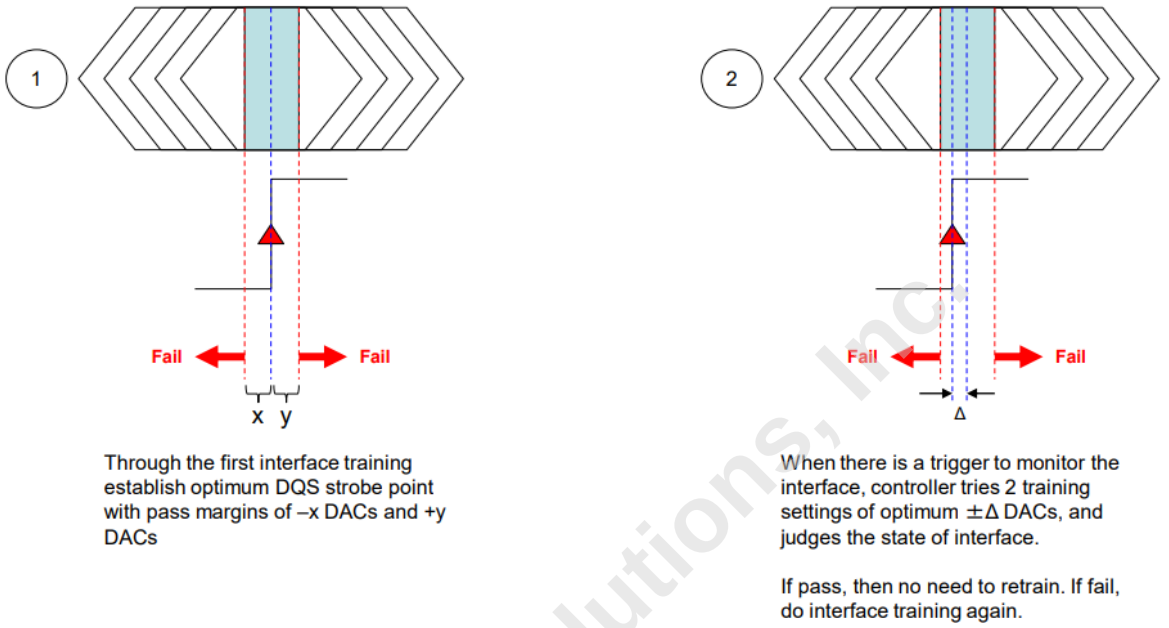


Figure 8.6-19 — Write Training Monitoring Method

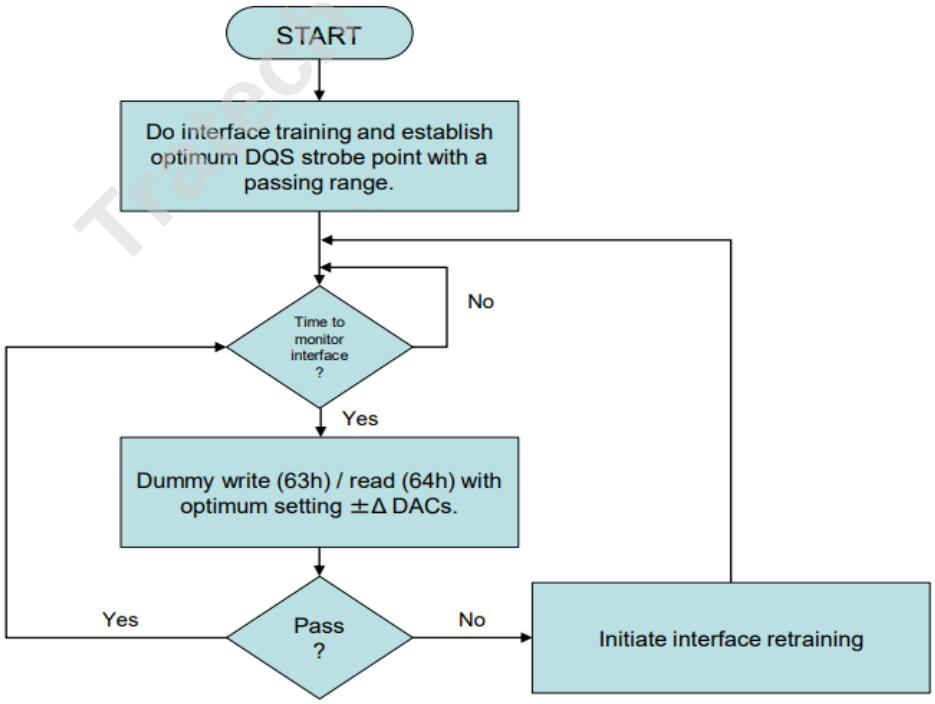


Figure 8.6-20 – Write Training Monitor Flowchart

8.6.9 Per-Pin VrefQ Adjustment

Per-pin VrefQ adjustment is an optional feature that allows NAND devices to compensate for pin-pin timing variation. Per-pin VrefQ adjustment may be implemented by NAND vendors in one of two ways: either Per-Pin VrefQ Adjustment via Offset or Per-Pin VrefQ Adjustment via Absolute Setting. NAND vendors shall select one of the defined implementations.

8.6.9.1 Per-Pin VrefQ Adjustment via Offset

With this implementation, the base NAND VrefQ setting is provided by FA23h while FA40h and FA41h provide the pin specific offset information. The final VrefQ setting for a pin is determined by the base setting from FA23h and the offset information from FA40h/41h.

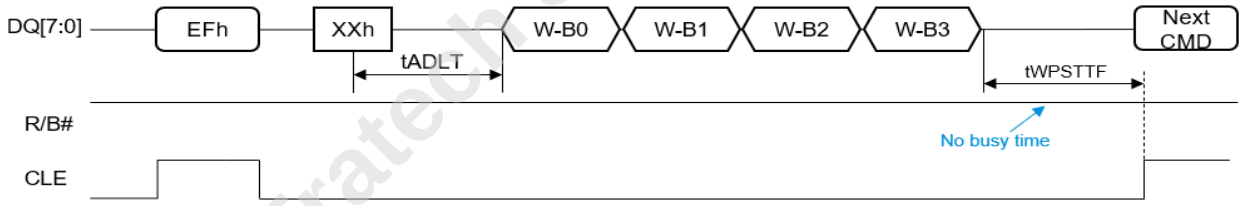
8.6.9.2 Per-Pin VrefQ Adjustment via Absolute Setting

With this implementation, the NAND VrefQ setting is initially provided by FA23h (common VrefQ setting). If user configures any of the per-pin VrefQ setting registers: FA40h/41h/42h, the settings in FA40h/41h/42h are used by the NAND instead and the setting in FA23h is ignored. In order to make the NAND revert to using the common VrefQ setting from FA23h again, a vendor specific interface reset command needs to be issued by the host to the NAND.

8.6.10 Fast Set/Get Feature

Fast Set/Get Feature is an optional feature that reduces training time overhead related to configuring FA23h/FA24h during Internal VrefQ/WDCA training. The feature does not require a different command opcode but is automatically invoked when the controller issues a Set Features (EFh), Set Features for Each LUN (D5h), Get Features (EEh) or Get Features for Each LUN (D4h) command to specific feature address registers (FA23h and FA24h) on a NAND device which supports Fast Set/Get Feature.

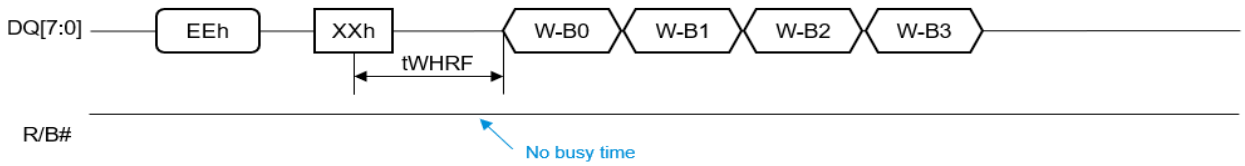
Figure 8.6-21 shows the Fast Set Feature command sequence using a Set Features (EFh) command:



Note1 Fast Set Feature behavior may also be invoked by a Set Feature for Each LUN (D5h) command.

Figure 8.6-21 — Fast Set Feature Sequence with Set Features (EFh) Command

Figure 8.6-22 shows the Fast Get Feature command sequence using a Get Features (EEh) command:



Note1: Fast Get Feature behavior may also be invoked by a Get Feature for Each LUN (D4h) command.

Figure 8.6-22 — Fast Set Feature Sequence with Get Features (EEh) Command

8.7 Pausing Data Input/Output

The pausing of data output may be done in the middle of a data output burst by pausing RE_n (RE_t/RE_c) and holding the signal(s) static high or low until the data burst is resumed. The pausing of data input may also be done in the middle of a data input burst by pausing DQS (DQS_t/DQS_c) and holding the signal(s) static high or low until the data burst is resumed. The data burst can be considered paused if DQS (DQS_t/DQS_c) or RE_n (RE_t/RE_c) is paused such that the current I/O frequency is not maintained for the data burst. WE_n shall be held high during data input and output burst pause time. ODT (if enabled) stays ON the entire pause time and warmup cycles (if enabled) are not re-issued when re-starting a data burst from pause.

Pausing in the middle of a data input or data output burst is only allowed up to the 800MT/s data rate. Above 800MT/s, for signal integrity reasons, pausing in the middle of a data input or data output burst is not allowed, and if the data burst is interrupted, the host is required to exit first the data burst prior to resuming it.

A data burst is exited when any of ALE, CLE or CE_n is driven to 1. After a data burst has been exited, if warmup cycles are enabled, then warmup cycles are required when re-starting the data burst.
Refer to vendor datasheet for details on re-issuing warmup cycles when exiting and re-starting data bursts. After a data burst has been exited, ODT also may be disabled, however if needed to meet the signal integrity needs of the system, ODT must be re-enabled prior to re-starting the data burst. If the host desires to end the data burst, after exiting the data burst, a new command is issued.

The figure below is an example of exiting a data input burst with a CLE=1 and resuming the data input burst with a CLE=0. Warmup cycles if enabled are required to be issued when the data input burst is resumed.

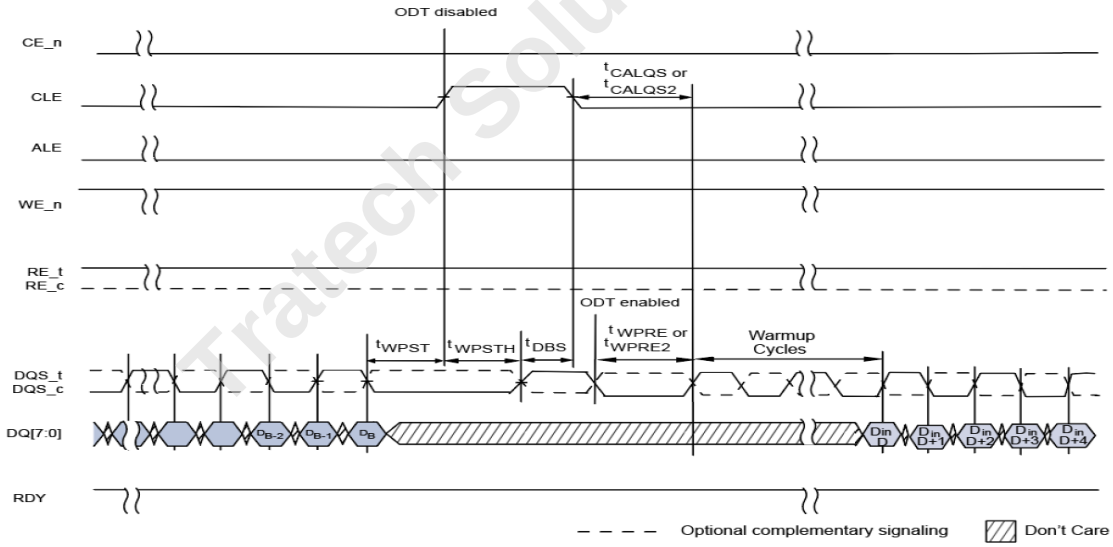


Figure 8.7-1 — Example of Data Input Burst Exit with CLE=1 and Resume with CLE=0

8.7 Pausing Data Input/Output (cont'd)

Figure 8.7-2 is an example of exiting a data output burst with a CLE=1 and resuming the data output burst with a CLE=0. Warmup cycles if enabled are required to be issued when the data output burst is resumed.

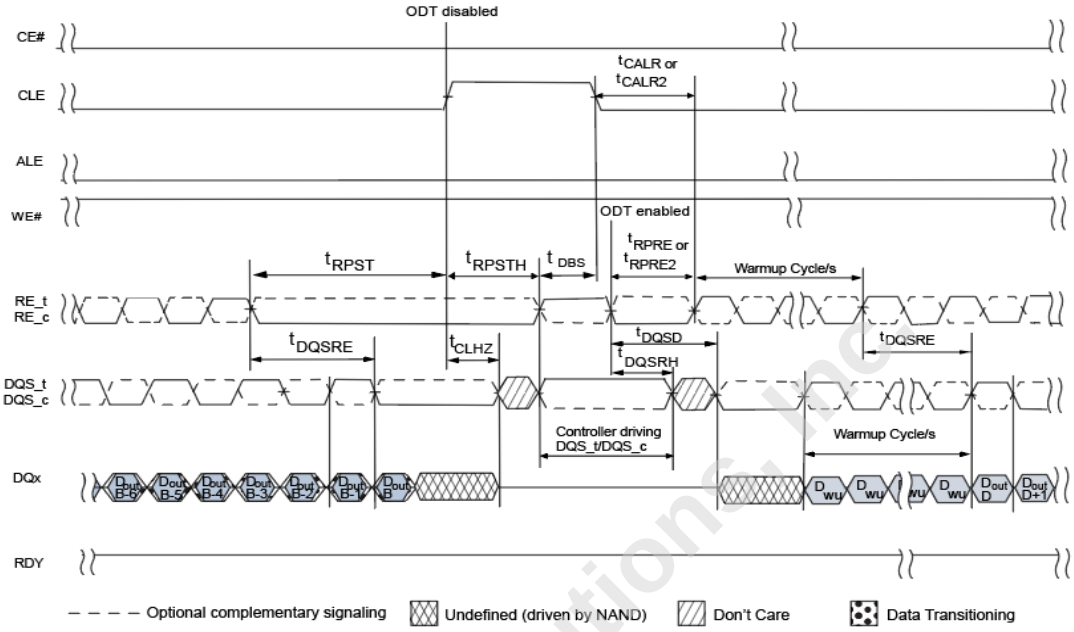
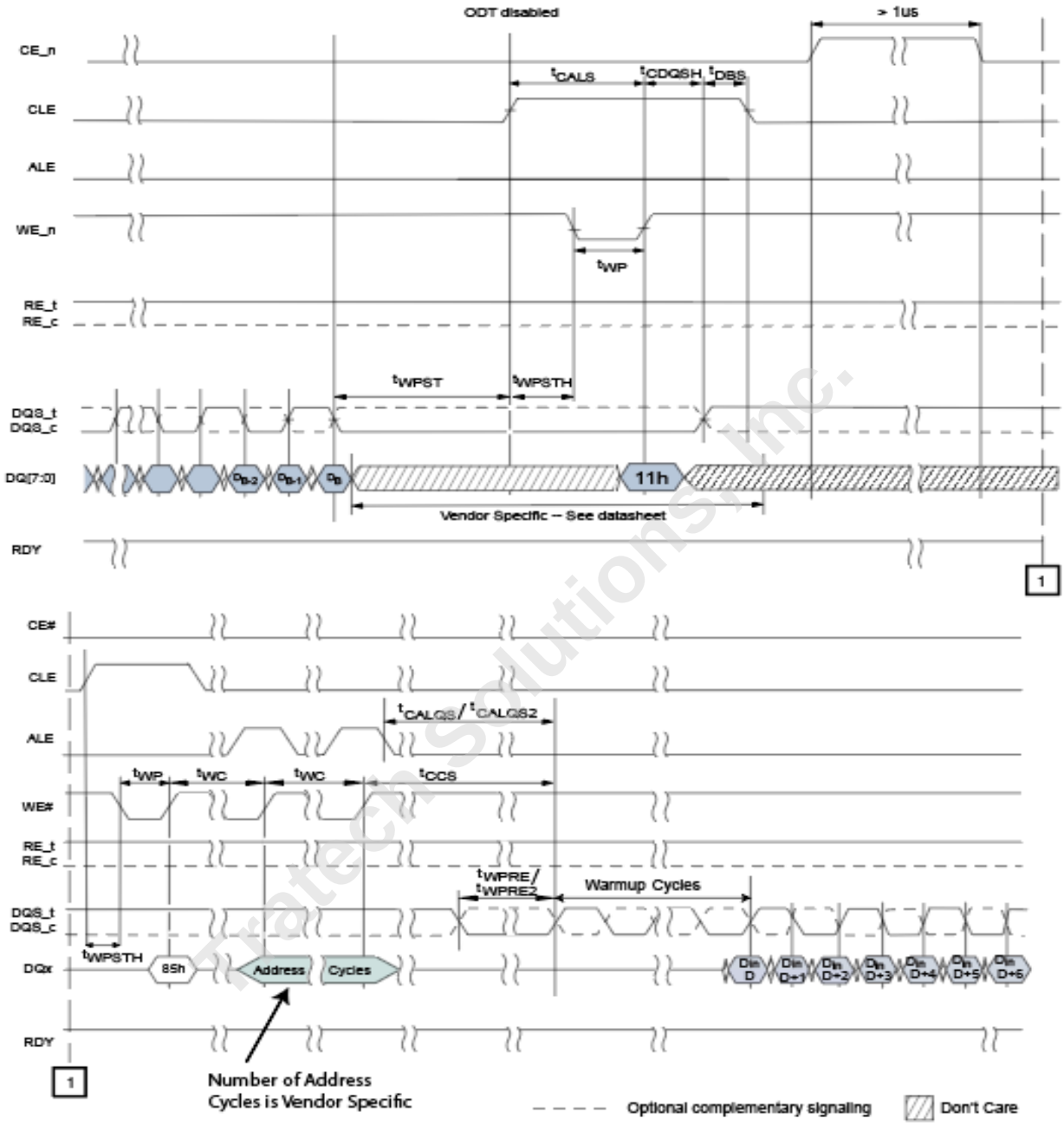


Figure 8.7-2 — Example of Data Output Burst Exit with CLE=1 and Resume with CLE=0

For devices that support >800 MT/s, if the input burst is exited and CE_n is brought high for >1 µs, the host may be required to issue vendor specific command (e.g., 11h) to exit and end the data burst (see vendor datasheet). To restart the exited data input burst a Change Write Column command shall be issued. For devices that support >800 MT/s, to restart an exited data output burst when CE_n has been high for >1 µs a Change Read Column command shall be issued.

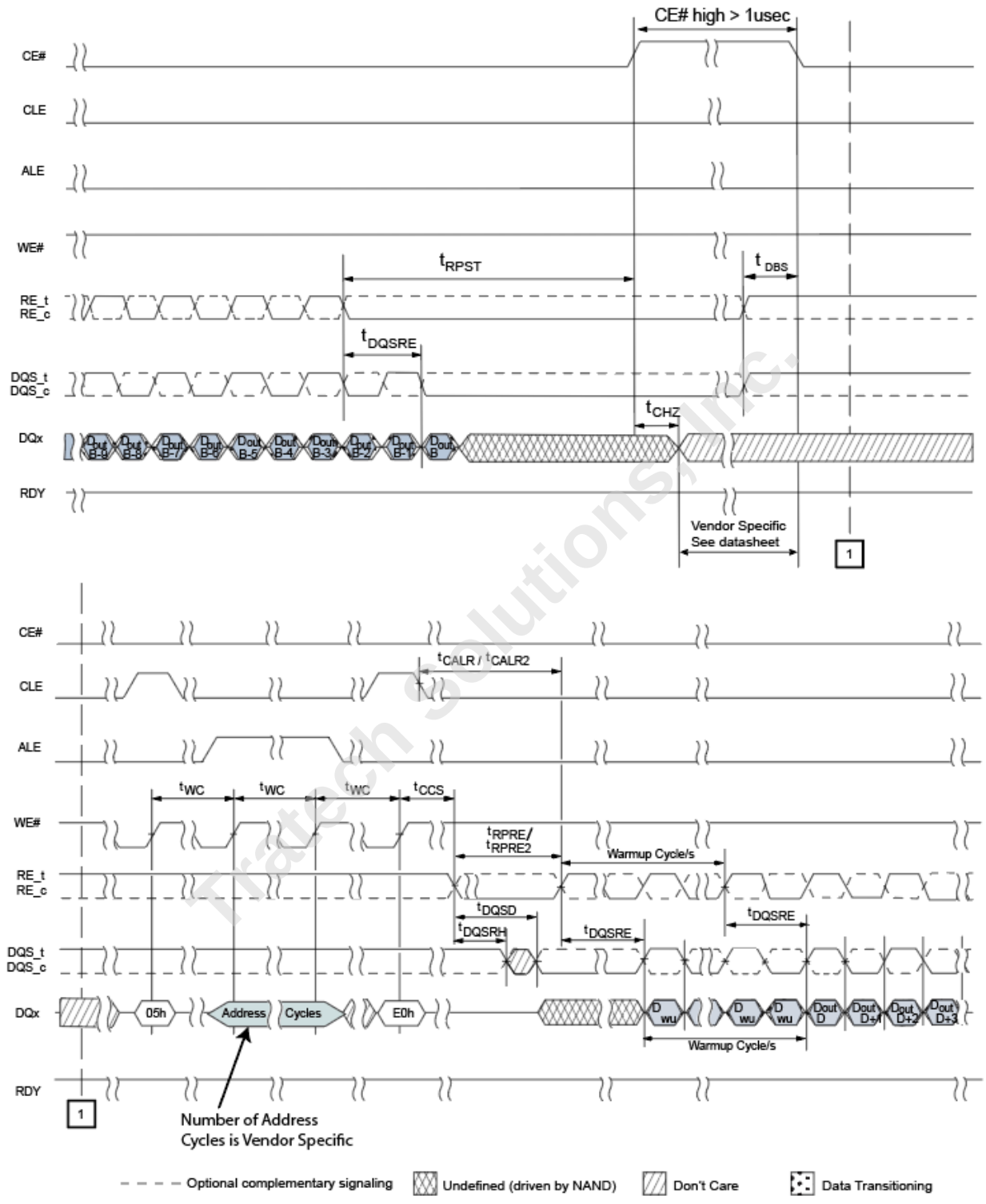
8.7 Pausing Data Input/Output (cont'd)



NOTE 1 Over 1 µs CE_n High case, DQS_t, and DQS_c states after data burst are optional. See vendor datasheet.

Figure 8.7-3 — Example of Data Input Exit with CE_n High >1 µs for Devices Supporting >800 MT/s

8.7 Pausing Data Input/Output (cont'd)



NOTE 1 Over 1 µs CE_n High case, RE_t, and RE_c states after data burst are optional. See vendor datasheet.

Figure 8.7-4 — Example of Data Output Exit With CE_n High >1µs for Devices Supporting >800 MT/s

8.8 Data Bus Inversion (DBI) Purpose and Function

Data Bus Inversion (DBI) is an optional function for NAND device to reduce power consumption and power/bus noise during data input/output. The device supporting DBI shall have DBI pin to designate if the DQ signals are inverted by transmitter side or not.

DBI signal through DBI pin shall be synchronized with DQ signals. DBI is regarded as DQ, such that specifications such as AC parameters and Interface training shall be applied to DBI.

DBI signal shall be either 0 or 1 during data input/output, where 0 indicates the DQ signals in the same cycle are not inverted and 1 indicates the DQ signals in the same cycle are inverted. In the case where NAND device output DQ with DBI, the device shall invert DQ signal with setting DBI to 1 if the number of 1's of DQ signals is more than 4. Otherwise, if the number of 1's is equal to or less than 4, the device shall not invert DQ signal with setting DBI to 0.

DBI function shall be activated/deactivated by Set Feature.

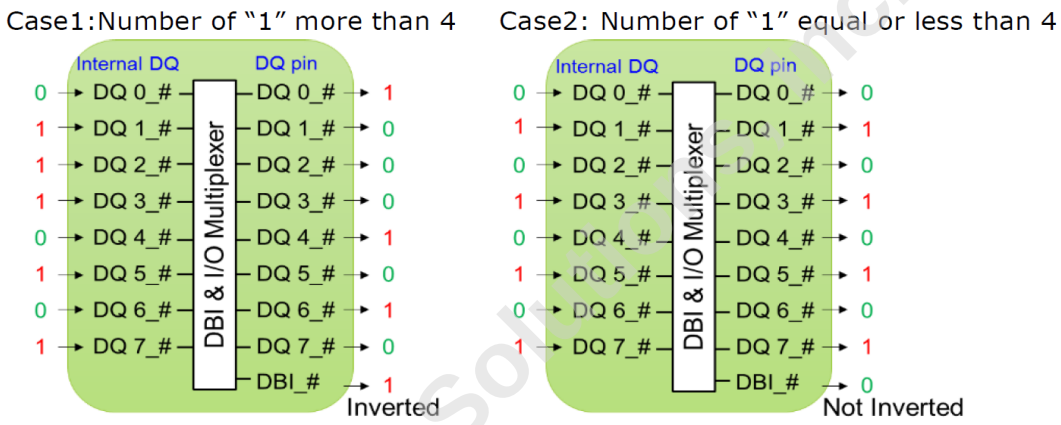


Figure 8.8-1 — DBI Function Illustration

8.8.1 DBI Behavior During Different Modes of Operation

Table 8.8-1 shows the NAND DBI encoding behavior on the DQ[7:0] pins and the DBI pin behavior in different modes of operation when DBI is enabled:

Table 8.8-1 — DBI Encoding of DQ[7:0] and DBI Pin Behavior During Different Modes of Operation

Mode of Operation	DQ[7:0] Behavior (With or Without DBI Encoding)	DBI Pin Behavior (Encoding flag/9th DQ pin/ "0")
Command/address	Without DBI encoding	"0"
Data Input	With DBI encoding	Encoding flag
Data Output	With DBI encoding	Encoding flag
SET Feature/ GET Feature/ Read ID/ Read Status	Without DBI encoding	"0"
Write DQ Training (Tx side)	Without DBI encoding	9th DQ pin
Read DQ Training	Without DBI encoding	9th DQ pin

8.8.2 DBI Behavior During Write DQ Training (Tx Side)

The host shall recognize the Write DQ Training (Tx Side) data size of the NAND by GET Feature to Feature Address 20h B2[3:0] and shall input and output data during Write DQ Training (Tx Side) based on that information.

With DBI enabled during Write DQ Training (Tx Side), the DBI pin acts like a 9th DQ pin and the data on DQ[7:0] are not affected by the values on the DBI pin and vice-versa. If the data that was input to the LUN during a 63h command sequence for example was the one shown in the table below, then if the LUN successfully captured the data, the same data pattern will be output by the LUN on the DQ[7:0] and DBI pins during the 64h command sequence.

Table 8.8-2 — Write DQ Training (Tx side) Example with DBI

Pin	Byte0	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7
DQ7	1	1	1	0	0	0	1	1
DQ6	0	1	1	1	1	0	1	0
DQ5	1	0	0	1	1	0	0	1
DQ4	1	1	0	1	0	1	0	1
DQ3	1	0	1	0	1	0	1	0
DQ2	1	0	0	0	0	1	1	1
DQ1	0	0	1	1	0	0	1	0
DQ0	0	0	0	0	0	1	0	0
DBI	0	1	0	1	1	0	1	1

8.8.3 DBI Behavior During Read DQ Training

With DBI enabled during Read DQ Training, the DBI pin outputs data in a similar fashion as a DQ pin with an Inverse Mask value of “0”. Table 8.8-3 illustrates this behavior:

Table 8.8-3 — Read DQ Training Example with DBI

Pin	Order	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Inverse Mask	1st Pattern = 1Fh								2nd Pattern = 7Fh							
		1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0
DQ7	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1
DQ6	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0
DQ5	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1
DQ4	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0
DQ3	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1
DQ2	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1
DQ1	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0
DQ0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0
DBI	NOTE 1	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	0

NOTE 1 The inverse mask does not apply to the DBI pin. The DBI pin outputs data in a similar fashion as a DQ pin with an Inverse Mask value of “0”.

9 Parameter Page

9.1 Parameter Page Data Structure Definition

Parameter page definitions defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.

Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the target will return how many data bytes are in a page. For a device that supports 16-bit data access, the host is required to convert byte values to word values for its use.

All optional parameters that are not implemented shall be cleared to 0h by the target.

Table 9.1-1 — JEDEC Parameter Page Data Structure Definition

Byte	O/M	Description
	Revision information and features block	
0-3	M	Parameter page signature Byte 0: “J” (= 4Ah) Byte 1: “E” (= 45h) Byte 2: “S” (= 53h) Byte 3: “D” (= 44h)
4-5	M	Revision number 3-15: Reserved (0) 2: 1 = supports parameter page revision 1.0 and standard revision 1.0 1: 1 = supports vendor specific parameter page 0: Reserved (0)
6-7	M	Features supported 10-15 Reserved (0) 9: 1 = supports changing pin function between WP_n and ODT_n 8: 1 = supports program page register clear enhancement 7: 1 = supports external Vpp 6: 1 = supports Toggle Mode DDR 5: 1 = supports Synchronous DDR 4: 1 = supports multi-plane read operations 3: 1 = supports multi-plane program and erase operations 2: 1 = supports non-sequential page programming 1: 1 = supports multiple LUN operations 0: 1 = supports 16-bit data bus width
8-10	M	Optional commands supported 11-23: Reserved (0) 10: 1 = supports Synchronous Reset 9: 1 = supports Reset LUN (Primary) 8: 1 = supports Small Data Move 7: 1 = supports Multi-plane Copyback Program (Primary) 6: 1 = supports Random Data Out (Primary) 5: 1 = supports Read Unique ID 4: 1 = supports Copyback 3: 1 = supports Read Status Enhanced (Primary) 2: 1 = supports Get Features and Set Features 1: 1 = supports Read Cache commands 0: 1 = supports Page Cache Program command

Table 9.1-1 — JEDEC Parameter Page Data Structure Definition (cont'd)

11-12	O	Secondary commands supported 8-15: Reserved (0) 7: 1 = supports secondary Read Status Enhanced 6: 1 = supports secondary Multi-plane Block Erase 5: 1 = supports secondary Multi-plane Copyback Program 4: 1 = supports secondary Multi-plane Program 3: 1 = supports secondary Random Data Out 2: 1 = supports secondary Multi-plane Copyback Read 1: 1 = supports secondary Multi-plane Read Cache Random 0: 1 = supports secondary Multi-plane Read
13	O	Number of Parameter Pages
14-31		Reserved (0)
	Manufacturer information block	
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64-69	M	JEDEC manufacturer ID (6 bytes)
70-79		Reserved (0)
	Memory organization block	
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-91		Reserved (0)
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	M	Number of logical units (LUNs)
101	M	Number of address cycles 4-7: Column address cycles 0-3: Row address cycles
102	M	Number of bits per cell
103	M	Number of programs per page
104	M	Multi-plane addressing 4-7: Reserved (0) 0-3: Number of plane address bits
105	M	Multi-plane operation attributes 3-7: Reserved (0) 2: 1= read cache supported 1: 1 = program cache supported 0: 1= No multi-plane block address restrictions
106-143		Reserved (0)

Table 9.1-1 — JEDEC Parameter Page Data Structure Definition (cont'd)

		Electrical parameters block
144-145	O	Asynchronous SDR speed grade 6-15: Reserved (0) 5: 1 = supports 20 ns speed grade (50 MHz) 4: 1 = supports 25 ns speed grade (40 MHz) 3: 1 = supports 30 ns speed grade (~33 MHz) 2: 1 = supports 35 ns speed grade (~28 MHz) 1: 1 = supports 50 ns speed grade (20 MHz) 0: 1 = supports 100 ns speed grade (10 MHz)
146-147	O	Toggle Mode DDR2 and NV-DDR2 speed grade 11-15: Reserved (0) 10: 1 = supports 2.5 ns speed grade (400 MHz) 9: 1 = supports 3 ns speed grade (~333 MHz) 8: 1 = supports 3.75 ns speed grade (~266 MHz) 7: 1 = supports 5 ns speed grade (200 MHz) 6: 1 = supports 6 ns speed grade (~166 MHz) 5: 1 = supports 7.5 ns speed grade (~133 MHz) 4: 1 = supports 10 ns speed grade (100 MHz) 3: 1 = supports 12 ns speed grade (~83 MHz) 2: 1 = supports 15 ns speed grade (~66 MHz) 1: 1 = supports 25 ns speed grade (40 MHz) 0: 1 = supports 30 ns speed grade (~33 MHz)
148-149	O	Synchronous DDR speed grade 6-15: Reserved (0) 5: 1 = supports 10 ns speed grade (100 MHz) 4: 1 = supports 12 ns speed grade (~83 MHz) 3: 1 = supports 15 ns speed grade (~66 MHz) 2: 1 = supports 20 ns speed grade (50 MHz) 1: 1 = supports 30 ns speed grade (~33 MHz) 0: 1 = supports 50 ns speed grade (20 MHz)
150	O	Asynchronous SDR features 0-7: Reserved (0)
151	O	Toggle-mode DDR features 0-7: Reserved (0)
152	O	Synchronous DDR features 2-7: Reserved (0) 1: Device supports CK stopped for data input 0: tCAD value to use
153-154	M	tPROG Maximum page program time (µs)
155-156	M	tBERS Maximum block erase time (µs)
157-158	M	tR Maximum page read time (µs)
159-160	O	tR Maximum multi-plane page read time (µs)
161-162	O	tCCS Minimum change column setup time (ns)
163-164	M	I/O pin capacitance, typical
165-166	M	Input pin capacitance, typical
167-168	O	CK pin capacitance, typical
169	M	Driver strength support 5-7: Reserved (0) 4: 1 = supports 35 Ohm, 37.5 Ohm and 50 Ohm drive strength. Default is 35 Ohm. 3: 1 = supports 37.5 Ohm and 50 Ohm drive strength. Default is 37.5 Ohm. 2: 1 = supports 18 Ohm drive strength 1: 1 = supports 25 Ohm drive strength 0: 1 = supports 35 Ohm and 50 Ohm drive strength . Default is 35 Ohm.
170-171	O	t_{ADL} Program page register clear enhancement tADL value (ns)

Table 9.1-1 — JEDEC Parameter Page Data Structure Definition (cont'd)

172-175	O	Toggle Mode with CTT and ONFI NV-DDR3 speed grade 21-31: Reserved (0) 20: 1=supports 0.556 ns speed grade (~1800 Mhz) 19: 1=supports 0.625 ns speed grade (1600 Mhz) 18: 1=supports 0.714 ns speed grade (~1400 Mhz) 17: 1=supports 0.833 ns speed grade (~1200 MHz) 16: 1=supports 0.909 ns speed grade (~1100 MHz) 15: 1=supports 1.0 ns speed grade (1000 MHz) 14: 1=supports 1.111 ns speed grade (~900 MHz) 13: 1=supports 1.25 ns speed grade (800 MHz) 12: 1=supports 1.667 ns speed grade (~600 MHz) 11: 1=supports 1.875 ns speed grade (~533 MHz) 10: 1=supports 2.5 ns speed grade (400 MHz) 9: 1 = supports 3 ns speed grade (~333 MHz) 8: 1 = supports 3.75 ns speed grade (~266 MHz) 7: 1 = supports 5 ns speed grade (200 MHz) 6: 1 = supports 6 ns speed grade (~166 MHz) 5: 1 = supports 7.5 ns speed grade (~133 MHz) 4: 1 = supports 10 ns speed grade (100 MHz) 3: 1 = supports 12 ns speed grade (~83 MHz) 2: 1 = supports 15 ns speed grade (~66 MHz) 1: 1 = supports 25 ns speed grade (40 MHz) 0: 1 = supports 30 ns speed grade (~33 MHz)
176-179	O	Toggle Mode with LTT and ONFI NV-LPDDR4 speed grade 21-31: Reserved (0) 20: 1=supports 0.556 ns speed grade (~1800 Mhz) 19: 1=supports 0.625 ns speed grade (1600 Mhz) 18: 1=supports 0.714 ns speed grade (~1400 Mhz) 17: 1=supports 0.833 ns speed grade (~1200 MHz) 16: 1=supports 0.909 ns speed grade (~1100 MHz) 15: 1=supports 1.0 ns speed grade (1000 MHz) 14: 1=supports 1.111 ns speed grade (~900 MHz) 13: 1=supports 1.25 ns speed grade (800 MHz) 12: 1=supports 1.667 ns speed grade (~600 MHz) 11: 1=supports 1.875 ns speed grade (~533 MHz) 10: 1=supports 2.5 ns speed grade (400 MHz) 9: 1 = supports 3 ns speed grade (~333 MHz) 8: 1 = supports 3.75 ns speed grade (~266 MHz) 7: 1 = supports 5 ns speed grade (200 MHz) 6: 1 = supports 6 ns speed grade (~166 MHz) 5: 1 = supports 7.5 ns speed grade (~133 MHz) 4: 1 = supports 10 ns speed grade (100 MHz) 3: 1 = supports 12 ns speed grade (~83 MHz) 2: 1 = supports 15 ns speed grade (~66 MHz) 1: 1 = supports 25 ns speed grade (40 MHz) 0: 1 = supports 30 ns speed grade (~33 MHz)
180-207		Reserved (0)
	ECC and endurance block	
208	M	Guaranteed valid blocks at beginning of target
209-210	M	Block endurance for guaranteed valid blocks

Table 9.1-1 — JEDEC Parameter Page Data Structure Definition (cont'd)

211-218	M	ECC and endurance information block 0 Byte 211: Number of bits ECC correctability Byte 212: Codeword size Byte 213-214: Bad blocks maximum per LUN Byte 215-216: Block endurance Byte 217-218: Reserved (0)
219-226	O	ECC and endurance information block 1 Byte 219: Number of bits ECC correctability Byte 220: Codeword size Byte 221-222: Bad blocks maximum per LUN Byte 223-224: Block endurance Byte 225-226: Reserved (0)
227-234	O	ECC and endurance information block 2 Byte 227: Number of bits ECC correctability Byte 228: Codeword size Byte 229-230: Bad blocks maximum per LUN Byte 231-232: Block endurance Byte 233-234: Reserved (0)
235-242	O	ECC and endurance information block 3 Byte 235: Number of bits ECC correctability Byte 236: Codeword size Byte 237-238: Bad blocks maximum per LUN Byte 239-240: Block endurance Byte 241-242: Reserved (0)
243-271		Reserved (0)
	Reserved	
272-419		Reserved (0)
	Vendor specific block	
420-421	M	Vendor specific Revision number
422-509		Vendor specific
	CRC for Parameter Page	
510-511	M	Integrity CRC
	Redundant Parameter Pages	
512-1023	M	Value of bytes 0-511
1024-1535	M	Value of bytes 0-511
1536+		Additional redundant parameter pages

9.2 Byte 0-3: Parameter Page Signature

This field contains the parameter page signature. When two or more bytes of the signature are valid, then it denotes that a valid copy of the parameter page is present.

Byte 0 shall be set to 4Ah. Byte 1 shall be set to 45h. Byte 2 shall be set to 53h. Byte 3 shall be set to 44h.

9.3 Byte 4-5: Revision number

This field indicates the revisions of the parameter page and standard that the target complies to. The target may support multiple revisions of the standard. This is a bit field where each defined bit corresponds to a particular specification revision that the target may support.

Bit 0 shall be cleared to zero.

Bit 1 when set to one indicates that the target supports vendor specific parameter page.

Bit 2 when set to one indicates that the target supports parameter page rev. 1.0 and standard rev. 1.0. Bits 3-15 are reserved and shall be cleared to zero.

9.4 Byte 6-7: Features Supported

This field indicates the optional features that the target supports.

Bit 0 when set to one indicates that the target's data bus width is 16-bits. Bit 0 when cleared to zero indicates that the target's data bus width is 8-bits. The host shall use the indicated data bus width for all commands that are defined to be transferred at the bus width (x8 or x16). Note that some commands, like Read ID, always transfer data as 8-bit only.

Bit 1 when set to one indicates that the target supports multiple LUN operations. If bit 1 is cleared to zero, then the host shall not issue commands to a LUN unless all other LUNs on the target are idle (i.e., R/B_n is set to one).

Bit 2 when set to one indicates that the target supports non-sequential page programming operations, such that the host may program pages within a block in arbitrary order. Bit 2 when cleared to zero indicates that the target does not support non-sequential page programming operations. If bit 2 is cleared to zero, the host shall program all pages within a block in order starting with page 0.

Bit 3 when set to one indicates that the target supports multi-plane program and erase operations. Bit 4 when set to one indicates that the target supports multi-plane read operations.

Bit 5 when set to one indicates that the Synchronous DDR data interface is supported by the target. If bit 5 is set to one, then the target shall indicate the Synchronous DDR timing modes supported in the Synchronous DDR timing mode support field. Bit 5 when cleared to zero indicates that the Synchronous DDR data interface is not supported by the target.

Bit 6 when set to one indicates that the Toggle Mode DDR data interface is supported by the target. If bit 6 is set to one, then the target shall indicate the Toggle Mode DDR timing modes supported in the Toggle Mode DDR timing mode support field. Bit 6 when cleared to zero indicates that the Toggle Mode DDR data interface is not supported by the target.

Bit 7 when set to one indicates that the target supports external Vpp. If bit 7 is cleared to zero, then the target does not support external Vpp.

Bit 8 when set to one indicates that the target supports clearing only the page register for the LUN addressed with the Program (80h) command. If bit 8 is cleared to zero, then a Program (80h) command clears the page register for each LUN that is part of the target. At power-on, the device clears the page register for each LUN that is part of the target.

Bit 9 when set to one indicates that the NAND device can switch between WP function and ODT function via set-feature. If bit 9 is cleared to zero, the WP pin of NAND device will operate only for Write Protect (Conventional operation).

Bits 10-15 are reserved and shall be cleared to zero.

9.5 Byte 8-10: Optional Commands Supported

This field indicates the optional commands that the target supports.

Bit 0 when set to one indicates that the target supports the Page Cache Program command. If bit 0 is cleared to zero, the host shall not issue the Page Cache Program command to the target.

Bit 1 when set to one indicates that the target supports the Read Cache Random, Read Cache Sequential, and Read Cache End commands. If bit 1 is cleared to zero, the host shall not issue the Read Cache Sequential, Read Cache Random, or Read Cache End commands to the target.

Bit 2 when set to one indicates that the target supports the Get Features and Set Features commands. If bit 2 is cleared to zero, the host shall not issue the Get Features or Set Features commands to the target.

Bit 3 when set to one indicates that the target supports the Read Status Enhanced command. If bit 3 is cleared to zero, the host shall not issue the Read Status Enhanced command to the target. Read Status Enhanced shall be supported if the target has multiple LUNs or supports multi-plane operations.

Bit 4 when set to one indicates that the target supports the Copyback Program and Copyback Read commands. If bit 4 is cleared to zero, the host shall not issue the Copyback Program or Copyback Read commands to the target. If multi-plane operations are supported and this bit is set to one, then multi-plane copyback operations shall be supported.

Bit 5 when set to one indicates that the target supports the Read Unique ID command. If bit 5 is cleared to zero, the host shall not issue the Read Unique ID command to the target.

Bit 6 when set to one indicates that the target supports the Random Data Out command. If bit 6 is cleared to zero, the host shall not issue the Random Data Out command to the target.

Bit 7 when set to one indicates that the target supports the Multi-plane Copyback Program command. If bit 7 is cleared to zero, the host shall not issue the Multi-plane Copyback Program command to the target.

Bit 8 when set to one indicates that the target supports the Small Data Move command for both Program and Copyback operations. If bit 8 is cleared to zero, the target does not support the Small Data Move command for Program or Copyback operations. The Small Data Move command is mutually exclusive with overlapped multi-plane support. When bit 8 is set to one, the device shall support the 11h command to flush any internal data pipeline regardless of whether multi-plane operations are supported.

Bit 9 when set to one indicates that the target supports the Reset LUN command. If bit 9 is cleared to zero, the host shall not issue the Reset LUN command.

Bit 10 when set to one indicates that the target supports the Synchronous Reset command. If bit 10 is cleared to zero, the host shall not issue the Synchronous Reset command.

Bits 11-23 are reserved and shall be cleared to zero.

9.6 Byte 11-12: Secondary Commands Supported

This field indicates the secondary commands that the target supports.

Bit 0 when set to one indicates that the target supports the secondary Multi-plane Read command. If bit 0 is cleared to zero, the host shall not issue the secondary Multi-plane Read command to the target.

Bit 1 when set to one indicates that the target supports the secondary Multi-plane Read Cache Random command. If bit 1 is cleared to zero, the host shall not issue the secondary Multi-plane Read Cache Random command to the target.

9.6 Byte 11-12: Secondary Commands Supported (cont'd)

Bit 2 when set to one indicates that the target supports the secondary Multi-plane Copyback Read command. If bit 2 is cleared to zero, the host shall not issue the secondary Multi-plane Copyback Read command to the target.

Bit 3 when set to one indicates that the target supports the secondary Random Data Out command. If bit 3 is cleared to zero, the host shall not issue the secondary Random Data Out command to the target.

Bit 4 when set to one indicates that the target supports the secondary Multi-plane Program command. If bit 4 is cleared to zero, the host shall not issue the secondary Multi-plane Program command to the target.

Bit 5 when set to one indicates that the target supports the secondary Multi-plane Copyback Program command. If bit 5 is cleared to zero, the host shall not issue the secondary Multi-plane Copyback Program command to the target.

Bit 6 when set to one indicates that the target supports the secondary Multi-plane Block Erase command. If bit 6 is cleared to zero, the host shall not issue the secondary Multi-plane Block Erase command to the target.

Bit 7 when set to one indicates that the target supports the secondary Read Status Enhanced command. If bit 7 is cleared to zero, the host shall not issue the secondary Read Status Enhanced command to the target.

Bits 8-15 are reserved and shall be cleared to zero.

9.7 Byte 13: Number of Parameter Pages

This field specifies the number of parameter pages present, including the original and the subsequent redundant versions.

9.8 Byte 14-31 : Reserved (0)

9.9 Byte 32-43: Device Manufacturer

This field contains the manufacturer of the device. The content of this field is an ASCII character string of twelve bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

There is no standard for how the manufacturer represents their name in the ASCII string. If the host requires use of a standard manufacturer ID, it should use the JEDEC manufacturer ID.

9.10 Byte 44-63: Device Model

This field contains the model number of the device. The content of this field is an ASCII character string of twenty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

9.11 Byte 64-69: JEDEC Manufacturer ID

This field contains the JEDEC manufacturer ID for the manufacturer of the device.

9.12 Byte 70-79 : Reserved (0)

9.13 Byte 80-83: Number of Data Bytes per Page

This field contains the number of data bytes per page. The value reported in this field shall be a power of two. The minimum value that shall be reported is 512 bytes.

9.14 Byte 84-85: Number of Spare Bytes per Page

This field contains the number of spare bytes per page. There are no restrictions on the value.

9.15 Byte 86-91 : Reserved (0)

9.16 Byte 92-95: Number of Pages per Block

This field contains the number of pages per block.

9.17 Byte 96-99: Number of Blocks per Logical Unit

This field contains the number of blocks per logical unit. There are no restrictions on this value.

9.18 Byte 100: Number of Logical Units (LUNs)

This field indicates the number of logical units the target supports. Logical unit numbers are sequential, beginning with a LUN address of 0. This field shall be greater than zero.

9.19 Byte 101: Number of Address Cycles

This field indicates the number of address cycles used for row and column addresses. The reported number of address cycles shall be used by the host in operations that require row and/or column addresses (e.g., Page Program).

Bits 0-3 indicate the number of address cycles used for the row address. This field shall be greater than zero.

Bits 4-7 indicate the number of address cycles used for the column address. This field shall be greater than zero.

NOTE Throughout this standard examples are shown with 2-byte column addresses and 3-byte row addresses. However, the host is responsible for providing the number of column and row address cycles in each of these sequences based on the values in this field.

9.20 Byte 102: Number of Bits per Cell

This field indicates the number of bits per cell in the Flash array. This field shall be greater than zero. A value of FFh indicates that the number of bits per cell is not specified.

9.21 Byte 103: Number of Programs per Page

This field indicates the maximum number of times a portion of a page may be programmed without an erase operation. After the number of programming operations specified have been performed, the host shall issue an erase operation to that block before further program operations to the affected page. This field shall be greater than zero.

9.22 Byte 104: Multi-plane Addressing

This field describes parameters for multi-plane addressing.

Bits 0-3 indicate the number of bits that are used for plane addresses. This value shall be greater than 0h when multi-plane operations are supported.

Bits 4-7 are reserved.

9.23 Byte 105: Multi-plane Operation Attributes

This field describes attributes for multi-plane operations. This byte is mandatory when multi-plane operations are supported as indicated in the Features supported field.

9.23 Byte 105: Multi-plane Operation Attributes (cont'd)

Bit 0 indicates that there are no block address restrictions for the multi-plane operation. If set to one all block address bits may be different between multi-plane operations. If cleared to zero, there are block address restrictions

Bit 1 indicates whether program cache is supported with multi-plane programs. If set to one then program cache is supported for multi-plane program operations. If cleared to zero then program cache is not supported for multi-plane program operations. Note that program cache shall not be used with multi-plane copyback program operations.

Bit 2 indicates whether read cache is supported with multi-plane reads. If set to one then read cache is supported for multi-plane read operations. If cleared to zero then read cache is not supported for multi-plane read operations. Note that read cache shall not be used with multi-plane copyback read operations.

Bits 3-7 are reserved.

9.24 Byte 106-143 : Reserved (0)

9.25 Byte 144-145: Asynchronous SDR Speed Grade

This field indicates the asynchronous SDR speed grades supported.

Bit 0 when set to one indicates that the target supports the 100 ns speed grade (10 MHz). Bit 1 when set to one indicates that the target supports the 50 ns speed grade (20 MHz). Bit 2 when set to one indicates that the target supports the 35 ns speed grade (~28 MHz). Bit 3 when set to one indicates that the target supports the 30 ns speed grade (~33 MHz). Bit 4 when set to one indicates that the target supports the 25 ns speed grade (40 MHz). Bit 5 when set to one indicates that the target supports the 20 ns speed grade (50 MHz). Bits 6-15 are reserved and shall be cleared to zero.

9.26 Byte 146-147: Toggle-mode DDR2 and NV-DDR2 Speed Grade

This field indicates the Toggle-mode DDR2 and NV-DDR2 speed grades supported. The target shall support an inclusive range of speed grades. The speed grades indicated by this field shall be based on the VccQ voltage level defined as Toggle-mode DDR2 and NV-DDR2 mode whose VccQ voltage level is 1.8V.

Bit 0 when set to one indicates that the target supports the 30 ns speed grade (~33 MHz). Bit 1 when set to one indicates that the target supports the 25 ns speed grade (40 MHz). Bit 2 when set to one indicates that the target supports the 15 ns speed grade (~66 MHz). Bit 3 when set to one indicates that the target supports the 12 ns speed grade (~83 MHz). Bit 4 when set to one indicates that the target supports the 10 ns speed grade (100 MHz). Bit 5 when set to one indicates that the target supports the 7.5 ns speed grade (~133 MHz). Bit 6 when set to one indicates that the target supports the 6 ns speed grade (~166 MHz). Bit 7 when set to one indicates that the target supports the 5 ns speed grade (200 MHz). Bit 8 when set to one indicates that the target supports the 3.75 ns speed grade (~266 MHz). Bit 9 when set to one indicates that the target supports the 3 ns speed grade (~333 MHz). Bit 10 when set to one indicates that the target supports the 2.5 ns speed grade (400 MHz). Bits 11-15 are reserved and shall be cleared to zero.

9.27 Byte 148-149: Synchronous DDR Speed Grade

This field indicates the synchronous DDR speed grades supported. The target shall support an inclusive range of speed grades.

Bit 0 when set to one indicates that the target supports the 50 ns speed grade (20 MHz). Bit 1 when set to one indicates that the target supports the 30 ns speed grade (~33 MHz). Bit 2 when set to one indicates that the target supports the 20 ns speed grade (50 MHz). Bit 3 when set to one indicates that the target supports the 15 ns speed grade (~66 MHz). Bit 4 when set to one indicates that the target supports the 12 ns speed grade (~83 MHz). Bit 5 when set to one indicates that the target supports the 10 ns speed grade (100 MHz). Bits 6-15 are reserved and shall be cleared to zero.

9.28 Byte 150: Asynchronous SDR Features

This field describes features and attributes for asynchronous SDR operation. This byte is mandatory when the asynchronous SDR data interface is supported.

Bits 0-7 are reserved.

9.29 Byte 151: Toggle-mode DDR Features

This field describes features and attributes for Toggle-mode DDR operation. This byte is mandatory when the Toggle-mode DDR data interface is supported.

Bits 0-7 are reserved.

9.30 Byte 152: Synchronous DDR Features

This field describes features and attributes for synchronous DDR operation. This byte is mandatory when the synchronous DDR data interface is supported.

Bit 0 indicates the tCAD value that shall be used by the host. If bit 0 is set to one, then the host shall use the tCADs (slow) value in synchronous DDR command, address and data transfers. If bit 0 is cleared to zero, then the host shall use the tCADf (fast) value in synchronous DDR command, address and data transfers.

Bit 1 indicates that the device supports the CK being stopped during data input. If bit 1 is set to one, then the host may optionally stop the CK during data input for power savings. If bit 1 is set to one, the host may pause data while the CK is stopped. If bit 1 is cleared to zero, then the host shall leave CK running during data input.

Bits 2-7 are reserved.

9.31 Byte 153-154: Maximum Page Program Time

This field indicates the maximum page program time (tPROG) in microseconds.

9.32 Byte 155-156: Maximum Block Erase Time

This field indicates the maximum block erase time (tBERS) in microseconds.

9.33 Byte 157-158: Maximum Page Read Time

This field indicates the maximum page read time (tR) in microseconds.

9.34 Byte 159-160: Maximum multi-plane Page Read Time

This field indicates the maximum page read time (tR) for multi-plane page reads in microseconds. Multi-plane page read times may be longer than single page read times. This field shall be supported if the target supports multi-plane reads as indicated in the Features supported field.

9.35 Byte 161-162: Minimum Change Column Setup Time

This field indicates the minimum change column setup time (tCCS) in nanoseconds. This parameter is used for the asynchronous SDR and synchronous DDR data interfaces.

After issuing a Change Read Column command, the host shall not read data until a minimum of tCCS time has elapsed. After issuing a Change Write Column command including all column address cycles, the host shall not write data until a minimum of tCCS time has elapsed. The value of tCCS shall always be longer than or equal to tWHR and tADL when the Toggle-mode DDR or Synchronous DDR data interface is supported.

9.36 Byte 163-164: I/O Pin Capacitance, Typical

This field indicates the typical I/O pin capacitance for the target. This field is specified in 0.1 pF units. For example, a value of 31 corresponds to 3.1 pF. The variance from this value is less than +/- 0.5 pF per LUN. As an example, if two LUNs are present than the total variance is less than +/- 1 pF.

9.37 Byte 165-166: Input Pin Capacitance, Typical

This field indicates the typical input pin capacitance for the target. This value applies to all inputs except the following: CK, CK_n, CE_n and WP_n signals. This field is specified in 0.1 pF units. For example, a value of 31 corresponds to 3.1 pF. The variance from this value is less than +/- 0.5 pF per LUN. As an example, if two LUNs are present than the total variance is less than +/- 1 pF.

9.38 Byte 167-168: CK Input Pin Capacitance, Typical

This field indicates the typical CK input pin capacitance for the target. This value applies to the CK and CK_n signals. This field is specified in 0.1 pF units. For example, a value of 31 corresponds to 3.1 pF. The variance from this value is less than +/- 0.25 pF per LUN. As an example, if two LUNs are present than the total variance is less than +/- 0.5 pF. This field shall be supported if the Synchronous DDR data interface is supported.

9.39 Byte 169: Driver Strength Support

This field describes if the target supports configurable driver strengths and its associated features.

Bit 0 when set to one indicates that the target supports configurable driver strength settings as defined in Table 4.2-2. If this bit is set to one, then the device shall support both the 35 Ohm and 50 Ohm settings. If this bit is set to one, then the device shall power-on with a driver strength at the 35 Ohm value defined in Table 4.2-2. If bit 0, bit 3, and bit 4 are cleared to zero, then the driver strength at power-on is undefined.

Bit 1 when set to one indicates that the target supports the 25 Ohm setting in Table 4.2-2 for use in the I/O Drive Strength setting.

Bit 2 when set to one indicates that the target supports the 18 Ohm setting in Table 4.2-2 for use in the I/O Drive Strength setting.

Bit 3 when set to one indicates that the target supports configurable driver strength settings as defined in Table 4.2-2. If this bit is set to one, then the device shall support both the 37.5 Ohm and 50 Ohm settings. If this bit is set to one, then the device shall power-on with a driver strength at the 37.5 Ohm value defined in Table 4.2-2. If bit 0, bit 3, and bit 4 are cleared to zero, then the driver strength at power-on is undefined.

Bit 4 when set to one indicates that the target supports configurable driver strength settings as defined in Table 4.2-2. If this bit is set to one, then the device shall support the 35 Ohm, 37.5 Ohm, and 50 Ohm settings. If this bit is set to one, then the device shall power-on with a driver strength at the 35 Ohm value defined in Table 4.2-2. If bit 0, bit 3, and bit 4 are cleared to zero, then the driver strength at power-on is undefined.

Bits 5-7 are reserved.

9.40 Byte 170-171: Program Page Register Clear Enhancement tADL Value

This field indicates the ALE to data loading time (tADL) in nanoseconds when the program page register clear enhancement is enabled. If the program page register clear enhancement is disabled, then the tADL value is as defined for the selected timing mode. This increased tADL value only applies to Program (80h) command sequences; it does not apply for Set Features, Copyback, or other commands.

9.41 Byte 172-175: Toggle-mode with CTT and ONFI NV-DDR3 Speed Grade

This field indicates the Toggle-mode with CTT and ONFI NV-DDR3 speed grades supported. The target shall support an inclusive range of speed grades. The speed grades indicated by this field shall be based on the VccQ voltage level defined as Toggle-mode with CTT and ONFI NV-DDR3 mode whose VccQ voltage level is 1.2 V if the value of interface type setting B2[1:0] of features 02h is 00b.

Bit 0 when set to one indicates that the target supports the 30 ns speed grade (~33 MHz). Bit 1 when set to one indicates that the target supports the 25 ns speed grade (40 MHz). Bit 2 when set to one indicates that the target supports the 15 ns speed grade (~66 MHz). Bit 3 when set to one indicates that the target supports the 12 ns speed grade (~83 MHz). Bit 4 when set to one indicates that the target supports the 10 ns speed grade (100 MHz). Bit 5 when set to one indicates that the target supports the 7.5 ns speed grade (~133 MHz). Bit 6 when set to one indicates that the target supports the 6 ns speed grade (~166 MHz). Bit 7 when set to one indicates that the target supports the 5 ns speed grade (200 MHz). Bit 8 when set to one indicates that the target supports the 3.75 ns speed grade (~266 MHz). Bit 9 when set to one indicates that the target supports the 3 ns speed grade (~333 MHz). Bit 10 when set to one indicates that the target supports the 2.5 ns speed grade (400 MHz). Bit 11 when set to one indicates that the target supports the 1.875 ns speed grade (~533 MHz). Bit 12 when set to one indicates that the target supports the 1.667 ns speed grade (~600 MHz). Bit 13 when set to one indicates that the target supports the 1.250 ns speed grade (~800 MHz). Bit 14 when set to one indicates that the target supports the 1.111 ns speed grade (~900 MHz). Bit 15 when set to one indicates that the target supports the 1.000 ns speed grade (~1000 MHz). Bit 16 when set to one indicates that the target supports the 0.909 ns speed grade (~1100 MHz). Bit 17 when set to one indicates that the target supports the 0.833 ns speed grade (~1200 MHz). Bit 18 when set to one indicates that the target supports the 0.714 ns speed grade (~1400 MHz). Bit 19 when set to one indicates that the target supports the 0.625 ns speed grade (1600 MHz). Bit 20 when set to one indicates that the target supports the 0.556 ns speed grade (~1800 MHz). Bits 21-31 are reserved and shall be cleared to zero.

9.42 Byte 176-179: Toggle Mode with LTT and ONFI NV-LPDDR4 Speed Grade

This field indicates the Toggle Mode with LTT and ONFI NV-LPDDR4 speed grade supported. The target shall support an inclusive range of speed grades. The speed grades indicated by this field shall be applied if the value of interface type setting B2[1:0] of features 02h is 01b.

Bit 0 when set to one indicates that the target supports the 30 ns speed grade (~33 MHz). Bit 1 when set to one indicates that the target supports the 25 ns speed grade (40 MHz). Bit 2 when set to one indicates that the target supports the 15 ns speed grade (~66 MHz). Bit 3 when set to one indicates that the target supports the 12 ns speed grade (~83 MHz). Bit 4 when set to one indicates that the target supports the 10 ns speed grade (100 MHz). Bit 5 when set to one indicates that the target supports the 7.5 ns speed grade (~133 MHz). Bit 6 when set to one indicates that the target supports the 6 ns speed grade (~166 MHz). Bit 7 when set to one indicates that the target supports the 5 ns speed grade (200 MHz). Bit 8 when set to one indicates that the target supports the 3.75 ns speed grade (~266 MHz). Bit 9 when set to one indicates that the target supports the 3 ns speed grade (~333 MHz). Bit 10 when set to one indicates that the target supports the 2.5 ns speed grade (400 MHz). Bit 11 when set to one indicates that the target supports the 1.875 ns speed grade (~533 MHz). Bit 12 when set to one indicates that the target supports the 1.667 ns speed grade (~600 MHz). Bit 13 when set to one indicates that the target supports the 1.250 ns speed grade (~800 MHz). Bit 14 when set to one indicates that the target supports the 1.111 ns speed grade (~900 MHz). Bit 15 when set to one indicates that the target supports the 1.000 ns speed grade (~1000 MHz). Bit 16 when set to one indicates that the target supports the 0.909 ns speed grade (~1100 MHz). Bit 17 when set to one indicates that the target supports the 0.833 ns speed grade (~1200 MHz). Bit 18 when set to one indicates that the target supports the 0.714 ns speed grade (~1400 MHz). Bit 19 when set to one indicates that the target supports the 0.625 ns speed grade (1600 MHz). Bit 20 when set to one indicates that the target supports the 0.556 ns speed grade (~1800 MHz). Bits 21-31 are reserved and shall be cleared to zero.

9.43 Byte 180-207: Reserved (0)

9.44 Byte 208: Guaranteed Valid Blocks at Beginning of Target

This field indicates the number of guaranteed valid blocks starting at block address 0 of the target. The minimum value for this field is 1h. The blocks are guaranteed to be valid for the endurance specified for this area when the host follows the specified number of bits to correct in ECC information block 0.

9.45 Byte 209-210: Block Endurance for Guaranteed Valid Blocks

This field indicates the minimum number of program/erase cycles per addressable page/block in the guaranteed valid block area. This value requires that the host is using at least the minimum ECC correctability reported in ECC information block 0. This value is not encoded. If the value is 0000h, then no minimum number of cycles is specified, though the block(s) are guaranteed valid from the factory.

9.46 Byte 211-218: ECC Information Block 0

This block of parameters describes a set of ECC and endurance information. The parameters are related, and thus the parameters are specified as a set.

Byte 211: Number of bits ECC correctability. This field indicates the number of bits that the host should be able to correct per codeword. The codeword size is reported in byte 212. With this specified amount of error correction by the host, the target shall achieve the block endurance specified in bytes 215-216. When the specified amount of error correction is applied by the host and the block endurance is followed, then the maximum number of bad blocks specified in bytes 213-214 shall not be exceeded by the device. All used bytes in the page shall be protected by ECC including the spare bytes if the ECC requirement reported in byte 211 has a value greater than zero. When this value is cleared to zero, the target shall return valid data.

Byte 212: Codeword size. The number of bits of ECC correctability specified in byte 211 is based on a particular ECC codeword size. The ECC codeword size is specified in this field as a power of two. The minimum value that shall be reported is 512 bytes (a value of 9).

Byte 213-214: Bad blocks maximum per LUN. This field contains the maximum number of blocks that may be defective at manufacture and over the life of the device per LUN. The maximum rating assumes that the host is following the block endurance requirements and the ECC requirements reported in this ECC and endurance information block.

Byte 215-216: Block endurance. This field indicates the maximum number of program/erase cycles per addressable page/block. This value assumes that the host is using the ECC correctability reported in byte 211. The block endurance is reported in terms of a value and a multiplier according to the following equation: value x 10multiplier. Byte 215 comprises the value. Byte 216 comprises the multiplier. For example, a block endurance of 75,000 cycles would be reported as a value of 75 and a multiplier of 3 (75 x 103). The value field shall be the smallest possible; for example 100,000 shall be reported as a value of 1 and a multiplier of 5 (1 x 105). If the value is 0000h, then no maximum number of cycles is specified.

9.47 Byte 219-226: ECC Information Block 1

This block of parameters describes an additional set of ECC and endurance information. The parameters are related, and thus the parameters are specified as a set. The layout is and definition for this block is equivalent to ECC information block 0. If this set of parameter is not specified, the block shall be cleared to 0h.

9.48 Byte 227-234: ECC Information Block 2

This block of parameters describes an additional set of ECC and endurance information. The parameters are related, and thus the parameters are specified as a set. The layout is and definition for this block is equivalent to ECC information block 0. If this set of parameter is not specified, the block shall be cleared to 0h.

9.49 Byte 235-242: ECC Information Block 3

This block of parameters describes an additional set of ECC and endurance information. The parameters are related, and thus the parameters are specified as a set. The layout is and definition for this block is equivalent to ECC information block 0. If this set of parameter is not specified, the block shall be cleared to 0h.

9.50 Byte 243 - 419 : Reserved (0)

9.51 Byte 420-421: Vendor Specific Revision Number

This field indicates a vendor specific revision number. This field should be used by vendors to indicate the supported layout for the vendor specific parameter page area and the vendor specific feature addresses. The format of this field is vendor specific.

9.52 Byte 422-509: Vendor Specific

This field is reserved for vendor specific use.

9.53 Byte 510-511: Integrity CRC

The Integrity CRC (Cyclic Redundancy Check) field is used to verify that the contents of the parameter page were transferred correctly to the host. The CRC of the parameter page is a word (16-bit) field. The CRC calculation covers all of data between byte 0 and byte 509 of the parameter page inclusive.

The CRC shall be calculated on byte (8-bit) quantities starting with byte 0 in the parameter page. The bits in the 8-bit quantity are processed from the most significant bit (bit 7) to the least significant bit (bit 0).

The CRC shall be calculated using the following 16-bit generator polynomial: $G(X) = X16 + X15 + X2 + 1$ This polynomial in hex may be represented as 8005h.

The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

9.54 Byte 512-1023: Redundant Parameter Page 1

This field shall contain the values of bytes 0-511 of the parameter page. Byte 512 is the value of byte 0.

The redundant parameter page is used when the integrity CRC indicates that there was an error in bytes 0-511. The redundant parameter page shall be stored in nonvolatile media; the target shall not create these bytes by retransmitting the first 512 bytes.

9.55 Byte 1024-1535: Redundant Parameter Page 2

This field shall contain the values of bytes 0-511 of the parameter page. Byte 1024 is the value of byte 0.

The redundant parameter page is used when the integrity CRC indicates that there was an error in bytes 0-511 and in the first redundant parameter page. The redundant parameter page shall be stored in nonvolatile media; the target shall not create these bytes by retransmitting the first 512 bytes.

9.56 Byte 1536+: Additional Redundant Parameter Pages

Bytes at offset 1536 and above may contain additional redundant copies of the parameter page. There is no limit to the number of redundant parameter pages that the target may provide. The target may provide additional copies to guard against the case where all three mandatory copies have invalid CRC checks.

The host should determine whether an additional parameter page is present by checking the first Dword. If at least two out of four bytes match the parameter page signature, then an additional parameter page is present.

10 Low Latency NAND

10.1 Low Latency NAND Overview

Low Latency NAND is NAND flash memory with faster random access time (tR). Low Latency NAND has three classes defined by random access time.

10.2 Low Latency NAND Parameter Table

Table 10.2-1 — Low Latency NAND Parameter Table[1,2]

Category	Item	Unit	Low Latency NAND		
			Class A	Class B	Class C
Power	Vcc	V	3.3 V or 2.5 V		
	VccQ	V	1.2 V		
	Vpp	V	12 V (Optional)		
Organization	# of Plane	EA	32P or 16P or 8P		
	Page Size	KB	4 KB or 2 KB		
Performance	Page Read Time	µs (Avg.)	3 µs	5 µs	7 µs
	Page Program Time	µs (Avg.)	100 µs	100 µs	300 µs
	Block Erase Time	ms (Avg.)	5 ms	5 ms	5 ms
Interface	JEDEC Link	-	JESD230 (Low Latency NAND supports IO speed defined in JESD230)		
	Wide IO	-	X8		
Package	Low Latency NAND supports all packages which are defined in JESD230 specification (132 BGA / 152 BGA / 168 BGA / 316 BGA and so on)				

NOTE 1 There are three grades for Low Latency NAND according to read time: 3us page read time for Class A, 5 µs page read time for Class B and 7us page read time for Class C
NOTE 2 Low Latency NAND supports IO speed defined in JESD230

Annex A — (Informative) Differences between Revisions

This table briefly describes most of the changes made to entries that appear in this standard, JESD230F, compared to its predecessor, JESD230E. If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

A.1 Differences between JESD230F.01 and JESD230F (October 2022)

Clause	Term and Description of Change
7.8	Corrected typographical error in Table 7.8-1 — Feature Table for Write Duty Cycle Adjustment [24h]" as follows: (1) The note below Table 7.8-1 changed from B0[3:0] for WDCA Step Control to B0[4:0] for WDCA Step Control (2) I/O 4 is now part of WDCA Step Control

A.2 Differences between JESD230F and JESD230E (February 2022)

Clause	Term and Description of Change
3.1	Added JESD230F information to the NAND Interface Spec Overview
3.2	Added 2800Mbps, 3200Mpbs, and 3600Mbps details to Supporting Features and Operating Conditions Versus Data Transfer Rate
4.1.1	Added 2800Mbps, 3200Mpbs, and 3600Mbps details to CTT and LTT Interface AC/DC Levels
4.1.2	Added 2800Mbps, 3200Mpbs, and 3600Mbps details to CTT and LTT Interface DQ Rx Mask Specification
4.1.3	Included Controller CTT and LTT Interface DQ Rx Mask Specification details
4.1.5	Added 2800Mbps, 3200Mpbs, and 3600Mbps details to CTT and LTT Interface (1.2V VccQ) VIHL_AC Definition
4.1.6	Separated out a second table for the different VrefQ Value 3 setting in the Minimum Internal VrefQ Allowable Range
4.3	Updated the table for Max. overshoot and undershoot values for 1400Mhz, 1600Mhz and 1800Mhz to the CTT and LTT Interface AC Overshoot and Undershoot Specification
7.1	Updated the Feature Address 02h Register to include the option to support the Value 3 Range/Step Size
7.7.2	Updated the Feature Address 23h to include options for supporting the Value 3 Settings
7.7.2	Added an additional table to NAND Minimum Internal VrefQ Allowable Range for NAND Devices that Support Value 3 Settings (1.2V VccQ)
7.8	Added a Feature Address 24h (WDCA) section and table for Write Duty Cycle Adjustment
7.9	Added a Feature Address 40h, 41h and 42h section with details on Per-Pin VrefQ Adjustment via Offset/Absolute Settings and accompanying tables
8.6.2	Updated the Initial Configurations Interface Training Flow diagram: Specifically details for LTT2 and LTT3 in the Low Power Interface boxes.
8.6.3	New section and information for DCC (RE_t/c) Training Using Set Feature
8.6.7	New section and information for Write Duty Cycle Adjustment (WDCA)
8.6.8	New section and information for Write Training Monitor
8.6.9	New section and information for Per-Pin VrefQ Adjustment that includes options via Offset and via Absolute Setting
8.6.10	New section and information for Fast Set/Get Feature
9.1	Updated the Parameter Page Data Structure Definition for bytes 172-175 and 176-179 to include details for all speed grade options for both NV-DDR3 and NV-LPDDR4 speed grades
9.1	Removed bytes 178 and 179 from Reserved (updated Reserved bytes are 180-207)

A.3 Differences between JESD230E and JESD230D (June 2019)

Clause	Term and Description of Change
2.6	Added VPP and DBI pin descriptions
3	Added new NAND Interface General Information section
4	Added new Input, Output, AC Overshoot/Undershoot specifications for Como CTT+LTT Interface and for higher data rates up to 2.4Gbps
5	Added 178b/154b/146b Dual Channel packages. Updated 152b/132b, 252b/272b and 316b package ball maps with locations of DBI balls. Updated CE_n changes to Synchronous 132b/152b package ball maps.
7	Added Feature Address Registers 02h, 22h, 23h. Updated information for Feature Address Registers 10h and 21h.
8.6	Under Data Training section: added ODT Disable and Re-enable sub-section, added Interface Training Flows sub-section, added VrefQ Training verbiage in Read DQ Training and Write DQ Training (Tx Side) sub-sections, added Write DQ Training (Rx Side) with Internal VrefQ Training sub-section
8.7	Under Pausing Data Input/Output: added data pause requirements for >800MT/s, updated language for data burst pause versus data burst exit, updated figures
8.8	Added DBI section
9	Parameter Page Changes for CTT (Bytes 172-175) and LTT (Bytes 176-179)
10	Added Section 10 Low Latency NAND

A.4 Differences between JESD230D and JESD230C (October 2016)

Clause	Term and Description of Change
2.6	Added ODT_x_n pin and related notes to pin description table
3.2	Added 533Mhz and 600Mhz AC Overshoot/Undershoot Specs
3.3.1	Added 2.5 V Vcc DC Supply Voltage
3.3.2	Added 15uA ILOpd and ILOpu max spec for devices which support >800 MT/s
3.4	Added Absolute Maximum DC Ratings Section
4.4	Added ODT_x_n to BGA-152/132/136 ball maps
4.5	Added ODT_x_n to BGA-316 ball maps
4.6	Added ODT_x_n to BGA-272 ball maps
4.6	Added BGA-252 ball package and MO-210 reference
4.7	Corrected CE_n to RB_n mapping pin labelling error
6	Section 6 Get/Set Feature for each LUN changed to Feature Address Registers section
6.1	Moved Section 6.1 Get Feature for each LUN to Section 5.3
6.1	Added Feature Address 05h
6.2	Moved Section 6.2 Set Feature for each LUN section to Section 5.4
6.2	Added Feature Address 20h
6.3	Added Feature Address 21h
7.1	Added 37.5 Ohms as Default Value
7.3	Added 37.5 Ohms to Nominal Driver Strength Setting
7.5	Added 533Mhz and 600Mhz tCD specs
7.7	Added Data Training Section
7.8	Added Data Input/Output Pause Section
8.1	Changes to Parameter Page Data Structure Bytes 6-7, 146-147, 169, 172-173 for 37.5 Ohm output driver strength and higher speed grades
8.4	Changes to Parameter Page Byte 6-7 description for WP/ODT switch functionality
8.26	Changes to Parameter Page Byte 146-147 descriptions for Toggle-mode DDR2 and NV-DDR2 higher speed grades
8.39	Changes to Parameter Page Byte 169 description for 37.5 Ohms
8.41	Changes to Parameter Page Byte 172-173 description for Toggle-mode DDR3/4 and NV-DDR3 higher speed grades

A.5 Differences between JESD230C and JESD230B (July 2014)

Clause	Term and Description of Change
2.6	Pin Description
3	Physical Interface
3.3	Recommended DC Operating Conditions
4.7	CE_n to R/B_n Mapping
7	Data Interface and Timing (New Chapter)
7.1	Test Condition
7.4	Package Electrical Specifications and Pad Capacitance
7.5	tCD Parameter
7.6	Additional Timing Parameter for I/O Speed Greater than 400 MT/s

A.6 Differences between JESD230B and JESD230A (August 2013)

Clause	Description of change
2	VccQ added
6	ZQ calibration added
7	Driver strength added
8.1.38	Driver strength support description changes in Byte 169 of the parameter page

A.7 Differences between JESD230A and JESD230 (October 2012)

Clause	Description of change
2.5	New BGA-316 (Quad x8) package added
2.6	New BGA-272 (Quad x8) package added
5	Parameter page, revision 1 added

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Standard Improvement Form **JEDEC Standard No. JESD230F.01**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

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_____

3. Other suggestions for document improvement:

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