SUKANTA DEY

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CURRENT POSITION

Ph.D. Research Scholar in the department of Computer Science and Engineering at Indian Institute of Technology Guwahati. Currently pursuing research in VLSI CAD. Expertise knowledge of coding in C/C++, Python and Matlab. Have 3 years experience in Research & Development of software tools for VLSI Power Integrity, Reliability issues in On-chip Power Grid Network, IR/EM Analysis. Looking for an internship position in your esteemed firm so that I can use my technical knowledge for development of some projects. Research interests:

- VLSI Design/VLSI CAD/Electronics Design Automation.
- Artificial Intelligence/Machine Learning/Deep Learning.
- Evolutionary Algorithms/Single objective/Multi-objective Optimizations.

ACADEMIC QUALIFICATION

Indian Institute of Technology Guwahati, Guwahati, India

Ph.D. in Computer Science & Engineering *December 2015 - July 2019 (Expected)*

PhD Advisors : Dr. Sukumar Nandi, Professor, Dept. of CSE, IIT Guwahati &
Dr. Gaurav Trivedi, Asst. Professor, Dept. of EEE, IIT Guwahati

PhD Thesis: Handling Reliability Issues of Power Grid Networks of VLSI System-on-Chips (SoC)
Abstract: Designing a power grid network for a complex VLSI SoC is becoming critical for the success of the product, as most chips are still designed using old techniques that are ill-suited to the latest fabrication technologies, resulting in an expensive, over-designed product. Furthermore, the power network as designed is too large, which has several knock-on effects that impact area, timing, and power. Therefore, in this thesis, a proposal for developing efficient and reliable power grid network design for SoCs have been considered.

M.Tech. in Computer Science & Engineering *July 2014 - December 2015*
CPI: 7.08/10
Project: Analog Layout Design Automation
In the project, difficulties in analog circuit layout design have been identified and an algorithm has been devised to identify the symmetrical current mirrors of any analog amplifier IC.

Assam Engineering College, Guwahati, India *August 2010 - July 2014*
Bachelor of Engineering *in Electronics & Telecommunication*
Overall Grade: 73.82 %
Project: Spread Spectrum based secure communication system
In the project, a prototype of Direct Sequence Spread Spectrum Technique has been developed,which is widely used in Code Division Multiple Access (CDMA) communication and further transmitter and receiver for this communication technique was developed. Later a demonstration was shown on how this technology is used for secure communication by comparing the message in the receiver and in a third party interceptor.

Maharishi Vidya Mandir Sr. Secondary School, Guwahati, India *May 2010*
Class 12^{th}, *Science*
Central Board of Secondary Education (CBSE), New Delhi
Overall Grade: 78.50 %

Kamakhya Vidyalaya High School, Guwahati, India *May 2008*
Class 10^{th}
Board of Secondary Education Assam
Overall Grade: 78.66 %

EXPERIENCE

Indian Institute of Technology Guwahati *July 2014 - Present*
Teaching Assistant

Working as a Teaching Assistant for the various Under Graduate and Post Graduate courses in the Dept. of Computer Science and Engineering at IIT Guwahati.

Texas Instruments India, Bengaluru *December 2015*
Project Trainee

Undergone training for a project "Analog Layout Design Automation". Interacted with the analog circuit design engineers and layout design engineers to find out the difficulties in making analog layout so as to make an automated tool.

Brigosha Technologies Pvt. Ltd., Guwahati *July 2013*
Summer Intern

Undergone training on embedded system and worked on projects with PIC18 micro-controller and its application.

PUBLICATIONS

Sukanta Dey, Satyabrata Dash, Sukumar Nandi, Gaurav Trivedi, **"Markov Chain Model using Lévy Flight for VLSI Power Grid Analysis "** in *30th IEEE/ACM International Conference on VLSI Design 2017, Hyderabad, India, 7-11 January 2017.*

Satyabrata Dash, **Sukanta Dey**, Deepak Joshi, Gaurav Trivedi, **"Minimizing Area of VLSI Power Distribution Networks Using River Formation Dynamics "** in *Journal of Systems and Information Technology, Emerald* (communicated)

TECHNICAL STRENGTHS

Operating Systems	Ubuntu, CentOS, Fedora.
Computer Languages	C, C++, Python, Verilog, VHDL, ngSpice, Matlab.
Tools	Vim, gedit, Xilinx ISE Design Suite, Cadence Virtuoso Design Environment.
ML/DL libraries	TensorFlow, numpy, matplotlib, scikit-learn, scipy, pandas, jupyter.

PERSONAL DETAILS

Date of Birth	12-November-1991
Mother's Name	Mrs. Anita Dey.
Father's Name	Mr. Subhas Ch. Dey.
Hobbies	Coding, Writing, Internet surfing, Swimming, Bicycling .
Permanent Address	Sagar Housing Complex, 102/A, Guwahati - 781012, Assam, India.