SUKANTA DEY

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CURRENT POSITION

I am a final year Ph.D. candidate at IIT Guwahati, specializing in Machine Learning techniques for Electronics Design Automation (EDA). My Ph.D. thesis title is *Design Methodology for On-Chip Power Grid Interconnect: AI/ML Perspective*. I will submit my Ph.D. thesis by September 2020 and will be available for joining in your esteemed institution from October 2020 onwards. My domain of expertise is Machine Learning, Deep Learning, Electronics Design Automation, VLSI Physical Design, Hardware Security, and Combinatorial Optimization. I have 6 years experience of CAD tools development. I have excellent command in C, C++, Python programming languages with excellent debugging and troubleshooting skills. My works related to Ph.D. thesis have been published in reputed EDA journals/conferences, e.g., ACM TODAES journal, DATE, ISVLSI, VLSID conferences. Before joining IIT Guwahati, I have completed my Bachelor's in Electronics and Telecommunication Engineering from Assam Engineering College in 2014. Research interests:

- VLSI Design/VLSI CAD/Electronics Design Automation.
- Artificial Intelligence/Machine Learning/Deep Learning.
- Hardware Security and Machine Learning Security.

ACADEMIC QUALIFICATION

IIT Guwahati, Guwahati, India *July 2014 - January 2021 (Expected)*
M.Tech-Ph.D. ***in Computer Science & Engineering***
Specialization: ***Machine Learning for EDA***
MTech Grade: 7.08
PhD Thesis: Design Methodology for On-Chip Power Grid Interconnect: AI/ML Perspective
Abstract: Designing a power grid network for a microprocessor chip is crucial in order to ensure adequate power delivery to all the underlying functional blocks. Power grids suffer from two major issues, that is, IR drop, and electromigration. The reliability of the chip reduces due to these two issues of the power grids. It is necessary to mitigate these two reliability issues during the chip design phase, which is a time-consuming iterative process. For larger power grid designs, the conventional method takes a considerable amount of time for power grid design sign-off. It also involves significant human labor. Therefore, in this thesis, we use AI/ML techniques to automate the power grid design flow, which shows a significant speedup than the conventional approaches with acceptable accuracy limit.

Assam Engineering College, Guwahati, India *August 2010 - July 2014*
Bachelor of Engineering *in Electronics & Telecommunication*
Grade: 73.82 %

Maharishi Vidya Mandir Sr. Secondary School, Guwahati, India *May 2010*
Class 12^{th}, *Science*, Central Board of Secondary Education (CBSE), New Delhi, India
Grade: 78.50 %

Kamakhya Vidyalaya High School, Guwahati, India *May 2008*
Class 10^{th}, Board of Secondary Education Assam, India
Grade: 78.66 %

WORK/INTERN EXPERIENCE

Indian Institute of Technology Guwahati, India *July 2014 - Present*
Graduate Research Student

I am working on different projects related to EDA with the emphasis on handling different backend design challenges of a System-on-Chip (SoC) using Machine Learning techniques. My work is to provide efficient solutions of SoC design using different optimization techniques, machine learning methods, and numerical methods. With the help of various programming languages such as C, C++, Python, Matlab to implement the SoC design solutions and test it on standard netlists/benchmark circuits. I am also working as a Teaching Assistant for the Under Graduate & PostGraduate courses in the Dept. of CSE, IIT Guwahati. I also mentor BTech students, Summer Trainees, and Interns in completing various projects related to EDA.

Texas Instruments, Bengaluru, India *December 2015*
Project Trainee

Undergone training for a project "Analog Layout Design Automation". We interacted with the analog circuit design engineers and layout design engineers to discover the difficulties in making analog layout so as to make an automated tool. The manual layout generation for the analog circuits is a tedious task that increases the design cycle and production time. To automate part of the layout generation process where we proposed an algorithm to identify the matched current mirrors of any analog circuit automatically. Finally, we develop a tool to solve the problem.

PROJECTS UNDERTAKEN

Machine Learning for Electronics Design Automation *January 2016 - Present*

Electronics Design Automation (EDA) deals with the design and automation of the integrated circuits (IC) from its circuit specifications to its corresponding circuit layout generation. EDA's fundamental objective is to improve the design cycle in terms of sign-off time and automate the design process in order to reduce human involvement in the design flow, while optimizing different design objectives. With the advancement of technology, the semiconductor industry faces strict product schedule and other competitive pressures. In this context, EDA must deliver "design-based equivalent scaling" to help continue essential industry trajectories. Recently, machine learning has been successful in predicting different complicated tasks. Therefore, a powerful tool for scaling the design flow will be the use of machine learning techniques, both inside and "around" design tools and flows. Therefore, in this project, machine learning tools for various problems of the backend design of ICs are developed.

Security Issues of Deep Learning Models and EDA Flow *January 2018 - Present*

Recently, it has been demonstrated that the deep learning models suffer from security issues by the contamination of adversarial samples in the training dataset. In this project, different security and vulnerabilities of the deep learning models are studied. In order to accomplish that, various attacks are performed on the deep learning systems, and efforts are made to obtain its countermeasures. The primary objective of this project is to create robust and trustworthy deep learning models. Further, due to the global nature of semiconductor manufacturing supply chain, threats are arising in the various portions of the design cycle. Studying threats in the EDA flow and IC design flow is also important in order to produce trustworthy IC. Therefore, various threats in EDA flows are studied in this project.

PUBLICATIONS

Summary: ACM TODAES 2020, IEEE/ACM DATE 2020, IEEE/ACM VLSI Design 2019, IEEE ISVLSI 2018, IEEE/ACM VLSI Design 2017.

Journal papers:

Sukanta Dey, Sukumar Nandi, Gaurav Trivedi, **"Machine Learning Approach for Fast Electromigration Aware Aging Prediction in Incremental Design of Large Scale On-Chip Power Grid Network"** in *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol 25, Issue 5, Article 42, August, 2020.

Sukanta Dey, Sukumar Nandi, Gaurav Trivedi, **"PGOpt: Multi-objective Design Space Exploration Framework for Large-Scale On-Chip Power Grid Design in VLSI SoC using Evolutionary Computing Technique"** in *Microprocessors and Microsystems Journal (MICPRO), Elsevier.* (Under Minor Revision)

Sukanta Dey, Sukumar Nandi, Gaurav Trivedi, **"Thermal-Aware Runtime Power/Ground TSV Repair for Reliability Enhancement in 3-D ICs"** (To be Communicated)

Satyabrata Dash, **Sukanta Dey**, Deepak Joshi, Gaurav Trivedi, **"Minimizing Area of VLSI Power Distribution Networks Using River Formation Dynamics "** in *Journal of Systems and Information Technology (JSIT), Emerald, Vol 20, Issue 4, pp 417-429, 2018. [Scopus indexed, Q2, SJR=0.4]*

Conference papers:

Sukanta Dey, Sukumar Nandi, Gaurav Trivedi, **"PowerPlanningDL: Reliability-Aware Framework for On-Chip Power Grid Design using Deep Learning "** in *IEEE/ACM Design, Automation and Test in Europe (DATE 2020), Grenoble, France, 9-13th March 2020. (long presentation paper)*

Sukanta Dey, Satyabrata Dash, Sukumar Nandi, Gaurav Trivedi, **"PGIREM: Reliability Constrained IR Drop Minimization and Electromigration Assessment of VLSI Power Grid Networks using Cooperative Coevolution "** in *IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2018), Hong Kong SAR, China, 9-11th July 2018.*

Sukanta Dey, Satyabrata Dash, Sukumar Nandi, Gaurav Trivedi, **"Markov Chain Model using Lévy Flight for VLSI Power Grid Analysis "** in *30th IEEE/ACM International Conference on VLSI Design (VLSID 2017), Hyderabad, India, 7-11 January 2017.*

Satyabrata Dash, **Sukanta Dey**, Anish J. Augustine, Rudra Sankar Dhar, Jan Pidani, Zdenk Nmec, Gaurav Trivedi , **"RiverOpt: A Multiobjective Optimization Framework based on Modified River Formation Dynamics Heuristic "** in *30th IEEE/ACM International Conference on VLSI Design (VLSID 2019), New Delhi, India, 5-9 January 2019.*

Sukanta Dey, Pradeepkumar Bhale, Sukumar Nandi, **"ReFIT: Reliability Challenges and Failure Rate Mitigation Techniques for IoT Systems "** in *20th International Conference on Innovations for Community Services (I4CS 2020), Bhubaneswar, India, 12-14th January 2020, Springer CCIS.*

Pradeepkumar Bhale, **Sukanta Dey**, Sukumar Nandi, **"Energy Efficient Approach to Detect Sinkhole Attack using Roving IDS in 6LoWPAN Network "** in *20th International Conference on Innovations for Community Services (I4CS 2020), Bhubaneswar, India, 12-14th January 2020, Springer CCIS.*

Sukanta Dey, Abhishek Kumar, Mehul Sawarkar, Pranav Kumar Singh, Sukumar Nandi, **"Evade-PDF: Towards Evading Machine Learning based PDF Malware Classifiers "** in *2nd ISEA International Conference on Security and Privacy (ISEA-ISAP 2018), Jaipur, India, 9-13th January 2019, Springer CCIS.*

Pranav Kumar Singh, Anish V Monsy, Rajan Garg, **Sukanta Dey**, Sukumar Nandi, **"JSpongeGen: A Pseudo Random Generator for Low Resource Devices "** in *15th International Conference on Distributed Computing and Internet Technology (ICDCIT 2019), Bhubaneswar, India, 10-13th January 2019, Springer LNCS.*

Book Chapters:

Sukanta Dey, Sukumar Nandi, Gaurav Trivedi, **"PGRDP: Reliability, Delay, and Power-Aware Area Minimization of Large-Scale VLSI Power Grid Network using Cooperative Coevolution "** in *in the Book: Intelligent Computing Paradigam - Recent Trends, Springer (Chapter 6)*, 2019.

Satyabrata Dash, Deepak Joshi, **Sukanta Dey**, Meenali Janveja, Gaurav Trivedi, **"StormOptimus: A single objective constrained optimizer based on brainstorming process for VLSI circuits "** in *in the Book: Brain Storm Optimization Algorithms: Concepts, Principles and Applications, Springer Verlag (Chapter 9)*, 2019.

TECHNICAL STRENGTHS

Operating Systems	Ubuntu, CentOS, Fedora.
Computer Languages	C, C++, Python 2 & 3, Matlab.
ML/DL libraries	TensorFlow 1.0/2.0, numpy, matplotlib, scikit-learn, scipy, pandas, jupyter.
CAD language/tools	Verilog, VHDL, HSPICE, ngSPICE, Cadence Virtuoso, Xilinx ISE.
Other Tools	Vim, gedit, sublime, git, github, LaTeX for drafting.

PERSONAL DETAILS

Date of Birth	12-November-1991
Mother's Name	Mrs. Anita Dey.
Father's Name	Mr. Subhas Ch. Dey.
Hobbies	Coding, Writing, Internet surfing, Swimming, Bicycling .
Permanent Address	Sagar Housing Complex, 102/A, Guwahati - 781012, Assam, India.