SUKANTA DEY

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CURRENT POSITION

I am a Ph.D. candidate at the Indian Institute of Technology Guwahati (IIT Guwahati), with VLSI CAD specialization. My Ph.D. thesis title is "Machine Learning and Optimization Techniques for Reliable On-chip Power Grid Design." I am going to submit my Ph.D. thesis by May 2020 and will be available for joining in your esteemed company from July 2020. My domain of expertise is VLSI CAD, VLSI Physical Design, On-Chip Power Grid Planning, Machine Learning, Deep Learning, Design for Reliability, Optimization techniques. My works related to Ph.D. thesis have been published in reputed VLSI conferences, for e.g., DATE, ISVLSI, VLSID conferences. I have good command in C, C++, Python programming languages. I also have hands-on experience in different CAD tools such as Synopsys HSPICE, Cadence Virtuoso. Before joining IIT Guwahati, I have completed my Bachelor's in Electronics and Telecommunication Engineering from Assam Engineering College in 2014. Research interests:

- VLSI Design/VLSI CAD/Electronics Design Automation.
- Artificial Intelligence/Machine Learning/Deep Learning.
- Evolutionary Algorithms/Single objective/Multi-objective Optimizations.

ACADEMIC QUALIFICATION

Indian Institute of Technology Guwahati, Guwahati, India

Ph.D. in Computer Science & Engineering *December 2016 - July 2020 (Expected)*

PhD Advisors : Prof. Sukumar Nandi, Professor, Dept. of CSE, IIT Guwahati &
Dr. Gaurav Trivedi, Asst. Professor, Dept. of EEE, IIT Guwahati

PhD Thesis: Machine Learning and Optimization Techniques for Reliable On-chip Power Grid Design
Abstract: Designing a power grid network for a complex VLSI SoC is becoming critical for the success of the product, as most chips are still designed using old techniques that are ill-suited to the latest fabrication technologies, resulting in an expensive, over-designed product. Furthermore, the power network as designed is too large, which has several knock-on effects that impact area, timing, and power. Therefore, in this thesis, a proposal for developing efficient and reliable power grid network design for SoCs have been considered.

M.Tech. in Computer Science & Engineering *July 2014 - December 2016*
CPI: 7.08/10
Project: Analog Layout Design Automation
In the project, difficulties in analog circuit layout design have been identified and an algorithm has been devised to identify the symmetrical current mirrors of any analog amplifier IC.

Assam Engineering College, Guwahati, India *August 2010 - July 2014*
Bachelor of Engineering *in Electronics & Telecommunication*
Overall Grade: 73.82 %
Project: Spread Spectrum based secure communication system
In the project, a prototype of Direct Sequence Spread Spectrum Technique has been developed,which is widely

used in Code Division Multiple Access (CDMA) communication and further transmitter and receiver for this communication technique was developed. Later a demonstration was shown on how this technology is used for secure communication by comparing the message in the receiver and in a third party interceptor.

Maharishi Vidya Mandir Sr. Secondary School, Guwahati, India *May 2010*
Class 12^{th}, *Science*
Central Board of Secondary Education (CBSE), New Delhi
Overall Grade: 78.50 %

Kamakhya Vidyalaya High School, Guwahati, India *May 2008*
Class 10^{th}
Board of Secondary Education Assam
Overall Grade: 78.66 %

EXPERIENCE

Indian Institute of Technology Guwahati *July 2014 - Present*
Graduate Research Student

Working on different projects related to VLSI CAD with the emphasis on handling different backend design challenges of a System-on-Chip (SoC). Providing efficient solutions of SoC design using different optimization techniques, machine learning methods, and numerical methods. Using different programming languages such as C, C++, Python, Matlab to implement the SoC design solutions and test it on standard netlists/benchmark circuits. Working as a Teaching Assistant for the Under Graduate & Post Graduate courses in the Dept. of CSE, IIT Guwahati. Mentoring BTech students, Summer Trainees, and Interns in completing various projects related to VLSI CAD.

Texas Instruments India, Bengaluru *December 2015*
Project Trainee

Undergone training for a project "Analog Layout Design Automation". Interacted with the analog circuit design engineers and layout design engineers to find out the difficulties in making analog layout so as to make an automated tool. The manual layout generation for the analog circuits is a tedious task which increases the design cycle and production time. To automate part of the layout generation process where we proposed an algorithm to automatically identify the matched current mirrors of any analog circuit.

Brigosha Technologies Pvt. Ltd., Guwahati *July 2013*
Summer Intern

Undergone training on embedded system and worked on projects with PIC18 micro-controller and its application.

PUBLICATIONS

Sukanta Dey, Sukumar Nandi, Gaurav Trivedi, **"PowerPlanningDL: Reliability-Aware Framework for On-Chip Power Grid Design using Deep Learning "** in *IEEE/ACM Design, Automation and Test in Europe Conference (DATE 2020), Grenoble, France, 9-13th March 2020. (To appear)*

Sukanta Dey, Satyabrata Dash, Sukumar Nandi, Gaurav Trivedi, **"PGIREM:Reliability-Constrained IR Drop Minimization and Electromigration Assessment of VLSI Power Grid Networks using Cooperative Coevolution "** in *17th IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2018, Hong Kong SAR, China, 9-11th July 2018.*

Sukanta Dey, Satyabrata Dash, Sukumar Nandi, Gaurav Trivedi, **"Markov Chain Model using Lévy Flight for VLSI Power Grid Analysis "** in *30th International Conference on VLSI Design (VLSID) 2017, Hyderabad, India, 7-11 January 2017.*

Sukanta Dey, Sukumar Nandi, Gaurav Trivedi, **"PGRDP: Reliability, Delay, and Power - Aware Area Minimization of VLSI Power Grid Networks using Cooperative Coevolution"** in *the Book: Intelligent Computing System, Studies in Computational Intelligence, Springer.*

Satyabrata Dash, **Sukanta Dey**, Anish J. Augustine, Rudra Sankar Dhar, Jan Pidani, Zdenk Nmec, Gaurav Trivedi, **"RiverOpt: A Multiobjective Optimization Framework based on Modified River Formation Dynamics Heuristic "** in *32nd International Conference on VLSI Design (VLSID) 2019, New Delhi, India, 5-9 January 2019.*

Satyabrata Dash, **Sukanta Dey**, Deepak Joshi, Gaurav Trivedi, **"Minimizing Area of VLSI Power Distribution Networks Using River Formation Dynamics "** in *Journal of Systems and Information Technology (JSIT), 2018, Vol 20, Issue 4, Emerald.*

Satyabrata Dash, Deepak Joshi, **Sukanta Dey**, Meenali Janveja, Gaurav Trivedi, **"StormOptimus: A single objective constrained optimizer based on brainstorming process for VLSI circuits "** in *the Book: Brain Storm Optimization Algorithms: Concepts, Principles and Applications, Springer Verlag.*

Sukanta Dey, Pradeepkumar Bhale and Sukumar Nandi, **"ReFIT: Reliability Challenges and Failure Rate Mitigation Techniques for IoT Systems "** in *20th International Conference on Innovations for Community Services (I4CS 2020), Bhubaneswar, India, 12-14th January 2020.* (To appear)

Pradeepkumar Bhale, **Sukanta Dey** and Sukumar Nandi, **"Energy Efficient Approach to Detect Sinkhole Attack using Roving IDS in 6LoWPAN Network "** in *20th International Conference on Innovations for Community Services (I4CS 2020), Bhubaneswar, India, 12-14th January 2020.* (To appear)

Sukanta Dey, Abhishek Kumar, Mehul Sawarkar, Pranav Kumar Singh and Sukumar Nandi, **"Evade-PDF: Towards Evading Machine Learning based PDF Malware Classifiers "** in *2nd ISEA International Conference on Secuirty and Privacy (ISEA-ISAP) 2018, Jaipur, India, 9-13th January 2019.* (To appear)

Pranav Kumar Singh, Anish V Monsy, Rajan Garg, **Sukanta Dey**, Sukumar Nandi,, **"JSpongeGen: A Pseudo Random Generator for Low Resource Devices "** in *15th International Conference on Distributed Computing and Internet Technology (ICDCIT) 2019, Bhubaneswar, India, 10-13th January 2019.*

TECHNICAL STRENGTHS

Operating Systems	Ubuntu, CentOS, Fedora.
Computer Languages	C, C++, Python, Verilog, VHDL, ngSpice, Matlab.
Tools	Vim, gedit, Xilinx ISE Design Suite, Cadence Virtuoso Design Environment.
ML/DL libraries	TensorFlow, numpy, matplotlib, scikit-learn, scipy, pandas, jupyter.

PERSONAL DETAILS

Date of Birth	12-November-1991
Mother's Name	Mrs. Anita Dey.
Father's Name	Mr. Subhas Ch. Dey.
Hobbies	Coding, Writing, Internet surfing, Swimming, Bicycling .
Permanent Address	Sagar Housing Complex, 102/A, Guwahati - 781012, Assam, India.