nPM1300 Hardware Design Guidelines

White Paper

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NORDIC® SEMICONDUCTOR

Contents

Revision history

Date	Description
2023-10-19	First release

1 Introduction

This document provides guidelines for the hardware design and integration of nPM1300. It is intended for system integrators and hardware engineers.

nPM1300 is a *Power Management Integrated Circuit (PMIC)* with a linear-mode battery charger suitable for Lithium-ion (*Li-ion*), *Lithium-polymer (Li-Poly)*, and Lithium iron phosphate ($LiFePO_4$) batteries. It comes in a compact 5 mm x 5 mm *Quad Flat No-lead Package (QFN)* or a 3.1 mm x 2.4 mm *Wafer Level Chip Scale Package (WLCSP)* supplemented with regulated supplies, load switches, and a variety of system management features. nPM1300 has two highly efficient dual mode DC/DC buck regulators with configurable output. The buck regulators have automatic mode switching from hysteretic to *Pulse Width Modulation (PWM)* depending on load condition.

2 Block diagram

The block diagram shows an overview of nPM1300.

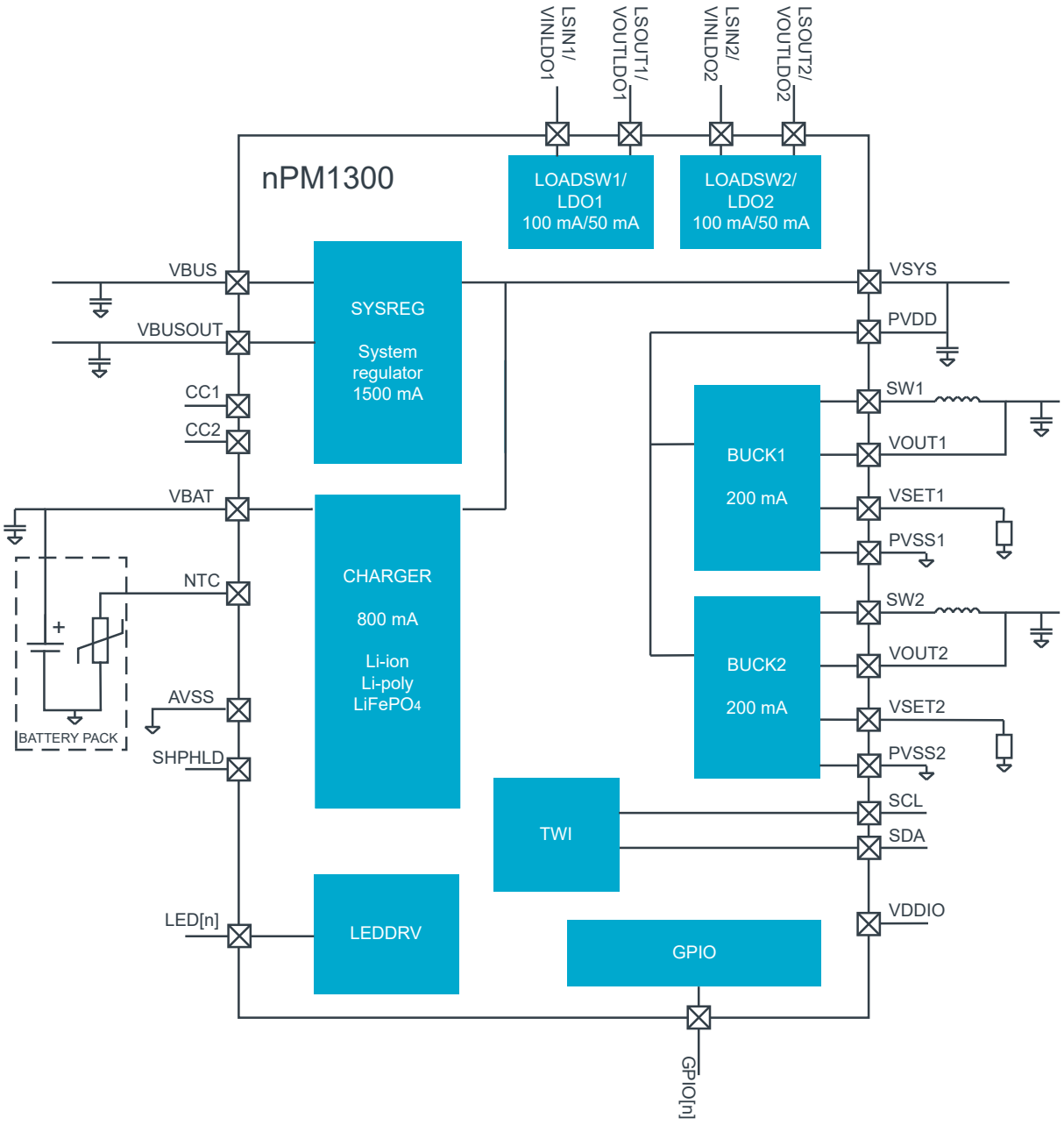

Figure 1: nPM1300 block diagram

3 Hardware integration

This section provides hardware design instructions and tips for successful nPM1300 integration, especially related to buck component selection for good performance. For pinout, reference schematic, and layout, refer to the nPM1300 Product Specification, as well as the nPM1300 PMIC reference design.

3.1 Selecting inductors for BUCK DC/DC regulators

The buck regulators of nPM1300 are designed to operate with inductors that have a nominal inductance of 2.2 µH with ± 20% tolerance. To ensure loop stability, do not use inductors with other nominal inductances.

The saturation current of the inductor should be greater than 400 mA. This saturation current requirement should be respected even if the load current range required in the application during design is lower than the maximum load current of the buck regulator. This is because the inductor peak current level is higher than the load current, especially when the buck regulator operates in hysteretic mode.

The choice of inductor has a significant effect on the performance of the buck regulator, especially the efficiency. The choice is typically a compromise between size, performance, and cost. The Direct Current Resistance (DCR) given by the manufacturer is one key indicator of the performance. However, the DCR is not a definitive performance metric as the losses in the inductor also include various frequency-dependent effects like magnetic hysteresis losses, eddy currents, and skin effects.

The following table shows examples of inductor models selected for area, performance, and cost optimized applications.

Manufacturer	Part number	Package (metric)	Height (mm)	DCR max (mΩ)	Comment
Taiyo Yuden	LSCNB1608HKT2R2MD	1608	0.8	292	Small footprint, thin
Taiyo Yuden	MDKK1616T2R2MM	1616	1	250	Small footprint
TDK	VLS201610HBX-2R2M-1	2016	1	142	Good performance
TDK	MLP2016H2R2MT0S1	2016	1	170	Good performance
Samsung Electro-Mechanics	CIGT201610EH2R2MNE	2016	1	87	Good performance
Samsung Electro-Mechanics	CIGT252008LM2R2MNE	2520	0.8	97	Good performance, inexpensive, thin

Table 1: nPM1300 inductor examples

The following table shows a comparison of buck efficiencies for different inductor manufacturer and models at 3.0 V output voltage. Efficiency numbers were measured by using the nPM1300 *Evaluation Kit (EK)* with default components and different buck inductors. The input current used in the efficiency calculations includes the whole device battery current.

Manufacturer	Part number	Package (metric)	*PWM* efficiency (%) at 150 mA
Samsung Electro-Mechanics	CIGT252008LM2R2MNE	2520	92.8
TDK	MLP2016H2R2MT0S1	2016	92.7
TDK	VLS201610HBX-2R2M-1	2016	92.6
TDK	MLZ2012M2R2HT000	2012	92.6
TDK	TFM201610ALMA2R2MTAA	2016	92.5
Wurth	74479275222	2012	92.5
Murata	LQM21PN2R2MEHD	2012	92.5
Murata	LQM21PN2R2MCAD	2012	92.4
Taiyo Yuden	MDKK1616T2R2MM	1616	92.4
TDK	MLZ2012A2R2WTD25	2012	92.3
TDK	MLP2012V2R2MT0S1	2012	92.3
Murata	LQM18PN2R2MGHD	1608	92.3
Taiyo Yuden	LSCN1608HKT2R2MD	1608	92.2
Samsung Electro-Mechanics	CIGT201610EH2R2MNE	2016	92.2
TDK	MLP2012S2RR2MT0S1	2012	92.2
Wurth	74479763222	1608	92.0
Taiyo Yuden	LSBHB1608KK2R2M	1608	91.8
Taiyo Yuden	MBKK1608T2R2M	1608	91.8
Murata	LQM21PN2R2MC0D	2012	91.7
Murata	LQM18PN2R2MDHD	1608	91.7
NJ	MIPSDZ1608G2R2PA	1608	91.6
TDK	MLZ1608A2R2WT000	1608	91.3

Table 2: nPM1300 BUCK1 efficiency comparison with VIN = 3.8 V, VOUT1 = 3.0 V

The following graph shows the typical efficiencies for BUCK1 in PWM mode.

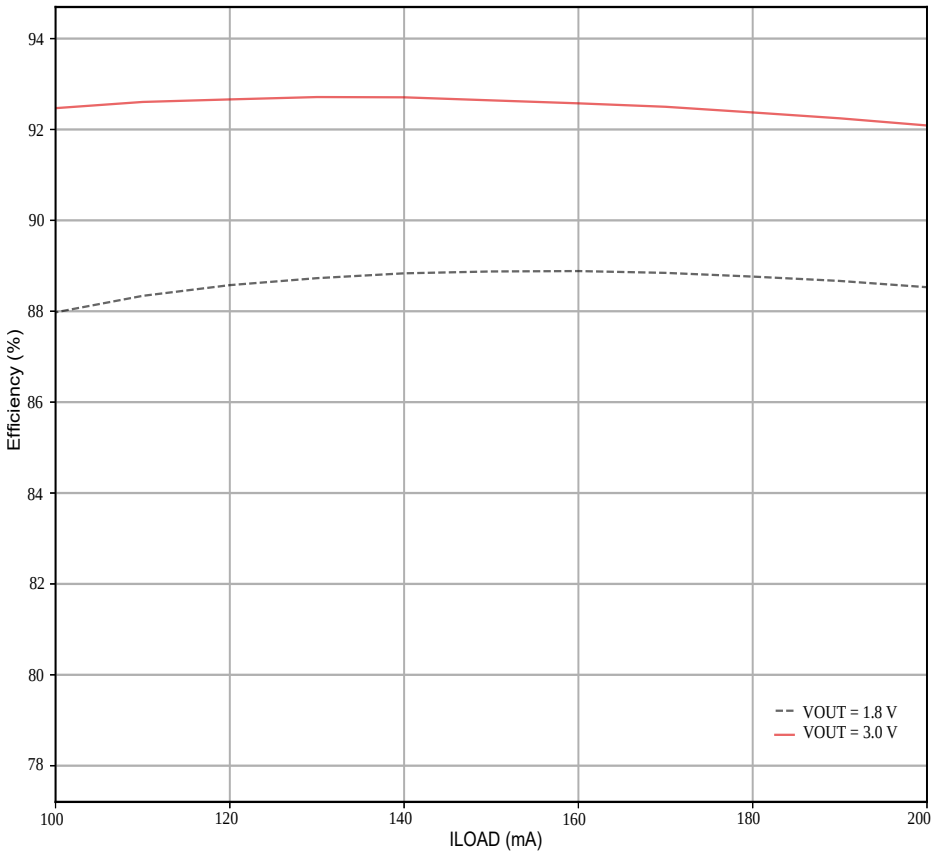

Figure 2: Typical efficiency for BUCK1 using inductor VLS201610HBX-2R2M in PWM mode and VBAT = 3.8 V

4 End product hardware design

Selecting external components for nPM1300 and having a well designed *Printed Circuit Board (PCB)* layout are both crucial for optimum performance.

The design of a product often aims to achieve a small form factor together with an attractive appearance. However, to achieve a product with solid performance, other design factors must also be considered. Some of those design factors conflict with the small form-factor target. Typically, this means a compromise in the design that can affect the performance or appearance of the product.

4.1 PCB stack-up

The nPM1300 PMIC reference design layouts use four-layer and six-layer *PCB*s. The use of at least four layers is recommended.

The key benefit of using a PCB design with four layers or higher is to properly incorporate ground planes very close to the power and signal routings. Ground planes improve both power and signal integrity for the circuit by improving return current paths, reducing crosstalk between signals, and reducing unwanted *Electromagnetic Interference (EMI)*.

It is beneficial to have a large ground plane without discontinuities, since lower frequency return currents spread across the plane. For higher harmonic return currents, for instance in switching regulators, a ground plane ensures the lowest impedance for the current.

Other benefits of ground planes are controlled impedance in transmission lines (such as RF signals) and heat sinking for self-heating components, which improves the overall longevity of components.

It is possible to route nPM1300 *QFN* on a two-layer board, but in that case, care must be taken to ensure a solid ground plane under the high current paths (DC/DC input, output, and switch traces).

If nPM1300 *WLCSP* is used on a board with via in small pads, it is recommended to use via capping to ensure good solderability.

Other components on the board might have requirements for the stack-up, like 50 Ω impedance on RF lines and *Universal Serial Bus (USB)* routing differential impedance. Using microvias and a four-layer PCB might also set restrictions on the stack-up, as an aspect ratio of 1:1 is common for laser cut vias.

4.2 PCB layout guidelines

A well designed *PCB* is necessary to achieve good performance. A poor layout can lead to loss in performance or functionality.

To ensure functionality, it is essential to follow the schematics and layout references closely. This is especially true for the buck regulators used in nPM1300.

PCB parasitic extraction tools can be used to analyze and iterate to achieve a good PCB layout, but usually good results are achieved by following guidelines for PCB layout design.

4.2.1 Routing and component placement

The following guidelines can help you design you *PCB* layout.

- For the buck regulators, place the input capacitors as close as possible to the voltage input and power ground of nPM1300.
- Use wide traces for the voltage input to reduce voltage drop and parasitic resistance and inductance.

- In buck regulators, the input has the highest rate of current change (di/dt). Therefore input routing loop area and impedance are critical. See figure Figure 3: Buck regulator switching cycles on page 10.
- Keep the trace between the positive node of the input capacitor and the voltage input of nPM1300 as short as possible.
- Keep the trace between the negative node of the input capacitor and power ground as short as possible.
- The input capacitance provides a low-impedance voltage source for the buck regulators. The inductance of the connection is the most important parameter of a local decoupling capacitor. Keep the parasitic inductance on these traces as small as possible.
- The parasitic inductance can be decreased by using a ground plane as close as possible to the top layer by using a thin dielectric layer between the top layer and the ground plane.
- Keep power and ground traces for sensitive analog blocks (**VBUS**, **VBAT**, and **AVSS**) away from noisy signals.
- Avoid direct connection to the switch power input and ground (**PVDD**, **PVSS1**, **PVSS2**) trace.
- Use separate bypass capacitors just for the analog supply close to nPM1300 taking into account the noise free ground connection.
- Avoid high switch currents flowing in the ground plane on the point where a sensitive analog supply decoupling capacitor is connected to the ground plane.
- Splitting ground to power, analog, and digital grounds (star grounding) is generally not recommended or feasible and can cause more problems than it solves.
- Place the components so that the digital, analog, and switch powers do not interfere with each other. This allows the system to find the lowest impedance return path in the ground plane.

4.2.2 Improving current loop design

When designing the *PCB* layout, follow the design guidelines for an improved current loop design.

- To minimize *EMI* from the loop antenna, minimize the current loop area for the buck regulator loops.
- Place components as close as possible to the **PVDD**, **PVSS1/2**, and **SW1/2** pins.
- Visualize both switching cycles and how the current flows in both cycles on the PCB, including the ground plane.
- The current should ideally rotate in the same direction in both switching cycles as shown in the following figure. This minimizes the change in magnetic field and therefore EMI.
- Some inductors have a dot showing the rotation direction around the core. If possible, place the inductor so that the current direction follows the main current loop rotation. In some cases, a current direction change cannot be avoided.
- When placing components and minimizing current loops, pay attention to input and output capacitor grounds and their position. The grounds should be close to each other and, if possible, on the same copper area on the top layer and strongly connected to the ground plane. This automatically minimizes the loops.

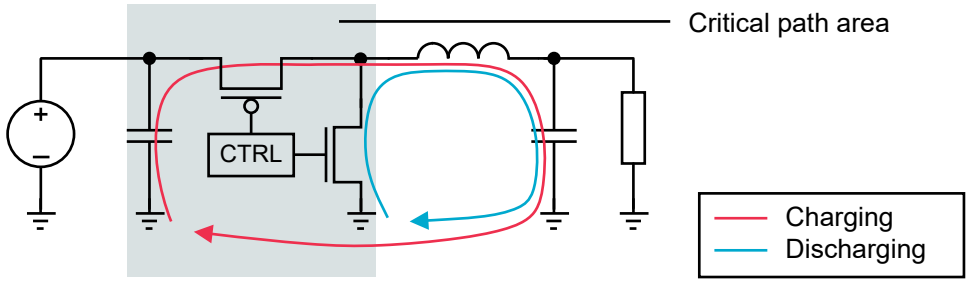

Figure 3: Buck regulator switching cycles

At low frequencies, the current flows in the path of least resistance, which is typically the shortest path, but at high frequencies the current follows the path of least inductance. In practice, this means that at high frequency the return current in the ground plane goes through the path that creates the smallest loop area. In the ground plane this path is right under the positive current on the top layer. Keep the ground plane intact in this area. The following figure illustrates the current path at low and high frequencies and the area (in grey) where the ground layer should be kept intact.

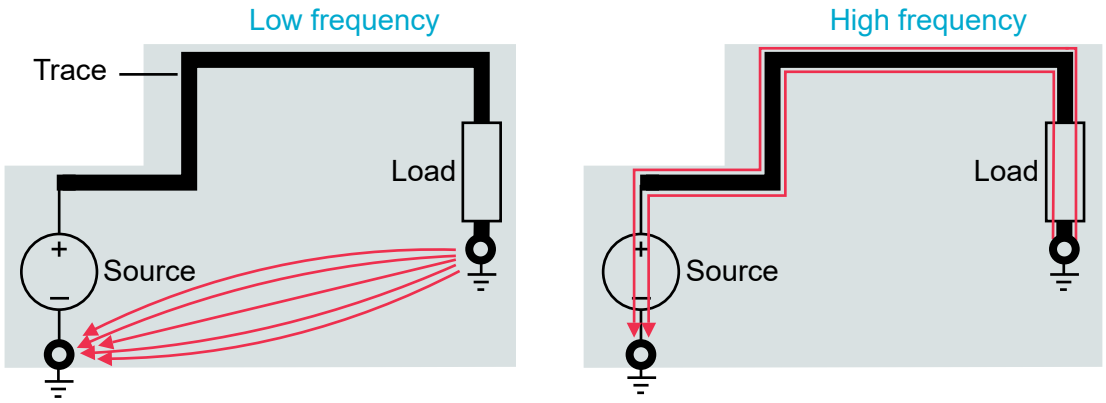

Figure 4: Current paths at low and high frequencies

Use the following guidelines for the ground layer:

- Keep the ground plane intact.
- A solid ground plane as the second layer is critical. Any traces or routes here is likely to increase the high current loop area and cause issues with EMI, EMC, or radio sensitivity.
- If routing on the ground plane is unavoidable, limit routing directly under nPM1300 to short escape routing and change layer as soon as possible. Do not route under the high current paths on top.
- Distance to the ground plane affects current loop area. Therefore it is recommended to use the second layer for ground. Also, using thinner prepreg reduces the loop area.

4.2.3 Trace width and via current capability

Follow the design recommendations for trace width and vias.

- For high current paths, trace widths must be considered based on the maximum load condition to minimize the voltage drop and inductance.
- Via current capabilities must be considered and calculated. The use of more and bigger vias is always better for both voltage drop and reduced inductance.
- Place ground vias close to the signal via for signal integrity and reduced return path impedance.
- Use via stitching to couple the ground plane and ground pours strongly together.

Glossary

DC

Direct Current

Electromagnetic Interference (EMI)

Electromagnetic noise or energy that causes disturbance and unwanted effects that interfere with the operation of an electrical circuit.

Evaluation Kit (EK)

A platform used to evaluate different development platforms.

Li-ion

Lithium-ion

Lithium-polymer (Li-Poly)

A rechargeable battery of lithium-ion technology using a polymer electrolyte instead of a liquid electrolyte.

Low-Dropout Regulator (LDO)

A linear voltage regulator that can operate even when the supply voltage is very close to the desired output voltage.

Power Management Integrated Circuit (PMIC)

A chip used for various functions related to power management.

Printed Circuit Board (PCB)

A board that connects electronic components.

Pulse Width Modulation (PWM)

A form of modulation used to represent an analog signal with a binary signal where the switching frequency is fixed, and all the pulses corresponding to one sample are contiguous in the digital signal.

Quad Flat No-lead Package (QFN)

A near chip scale package with pads on four sides encapsulated in plastic.

System on Chip (SoC)

A microchip that integrates all the necessary electronic circuits and components of a computer or other electronic systems on a single integrated circuit.

Two-wire Interface (TWI)

An I^2C compatible serial communication protocol that enables devices to exchange data by using a two-wire bus system, allowing multiple devices to be connected and controlled by a master device.

Universal Serial Bus (USB)

An industry standard that establishes specifications for cables and connectors and protocols for connection, communication, and power supply between computers, peripheral devices, and other computers.

Wafer Level Chip Scale Package (WLCSP)

Die size package with an array pattern of solder balls at a pitch that is compatible with circuit board assembly process.

Recommended reading

In addition to the information in this document, you may need to consult other documents.

Nordic documentation

- nPM1300 Product Specification
- nPM1300 EK product page
- nPM1300 EK Hardware
- nPM1300 PMIC reference design

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