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**TCAN28443-Q1, TCAN28453-Q1, TCAN28463-Q1, TCAN28473-Q1
TCAN28445-Q1, TCAN28455-Q1, TCAN28465-Q1, TCAN28475-Q1**
SLLSFE8 – DECEMBER 2020 – REVISED AUGUST 2022

TCAN284xx-Q1 Automotive CAN FD and LIN System Basis Chip (SBC) with Integrated Watchdog, Selective Wake and Advanced CAN Bus Fault Diagnostics

1 Features

- AEC-Q100 (Grade 1): Qualified for automotive applications
- Meets the requirements for CAN FD ISO 11898-2:2016
- Local interconnect network (LIN) physical layer specification ISO/DIS 17987-4 compliant and conforms to SAEJ2602 recommended practice for LIN
- CAN FD and LIN transceiver higher data rates
 - CAN FD supports 5 Mbps
 - LIN transceiver supports fast mode of 200 kbps
- Classic CAN backwards compatible
- Multiple methods to wake from sleep mode
 - CAN and LIN bus wake up pattern (WUP)
 - Local wake up (LWU) via WAKE pins
 - Using a high side switch, cyclic sensing wake up is supported
 - CAN selective wake up frame (WUF)
 - Digital wake up utilizing SW pin
- Low drop out (LDO) regulator supporting 250 mA externally at 3.3 V or 5 V, VCC1
- 5 V LDO regulator supports up to 200 mA externally, VCC2
- Control of an external PNP transistor supporting 350 mA at 1.8 V, 2.5 V, 3.3 V or 5 V
- 3.3 V and 5 V MCU support
- CAN and LIN support ±58 V Bus fault protection
- Timeout, window and Q&A watchdog support
- EEPROM to save device configuration
- Advanced CAN bus fault diagnostics
- QFN (32) package with improved automated optical inspection (AOI) capability

2 Applications

- Body electronics and lighting
- Infotainment and cluster
- Hybrid, electric and power train systems
- Industrial transportation

3 Description

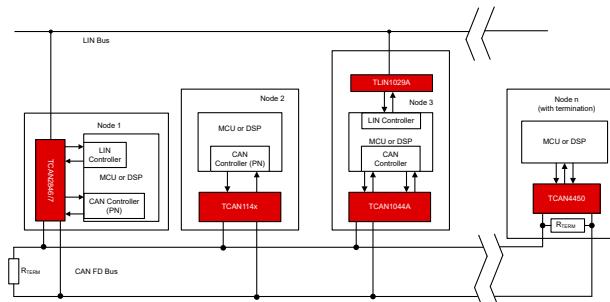
The TCAN284xx-Q1 is a family of system basis chips (SBC) that provide a control area network flexible data rate capable (CAN FD) transceiver. The TCAN2846-Q1 and TCAN2847-Q1 includes a local interconnect network (LIN) transceiver. The CAN FD transceiver supports data rates up to 5 Mbps while the LIN transceiver supports fast mode data rates up to 200 kbps. The VCC1 LDO provides 3.3 V or 5 V $\pm 2\%$ with up to 250 mA of current and determines the digital IO logic values. If more current is needed and external PNP transistor can be used to support up to 350 mA and voltages of 1.8 V, 2.5 V, 3.3 V or 5 V. VCC2 LDO provides 5 V up to 200 mA.

The TCAN284xx-Q1 includes features such as LIMP, three local wake inputs and four high side switches. The high side switch can be on/off, 10-bit PWM or timer controlled. Using the GFO pin it is possible to control an external CAN FD, LIN transceiver, CAN SBC or LIN SBC. The WAKE pins can be configured for static sensing, cyclic sensing (with HSS4 pin) and pulse based for waking up. These devices provide EEPROM to store specific device configuration information thus avoiding extensive reprogramming after power fluctuations.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
TCAN284xx-Q1	QFN (RHB) (32)	5.0mm x 5.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematics

ADVANCE INFORMATION



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2020	*	Initial release.
March 3rd, 2022	0.9986	<ul style="list-style-type: none"> • Updated Bus Fault Detection and Communication Section • Updated Registers 8'h54[6] and 8'h59[6]
April 1st, 2022	0.9987	<ul style="list-style-type: none"> • Updated how part number shows up in registers 0x00h - 0x07h • Cleaned up information in registers
April 21st, 2022	0.9988	<ul style="list-style-type: none"> • Updated device state diagram and SWE timer specifically • Updated Restart Mode figure • Updated Sleep Mode figure • Clarification rewrite for Sleep Mode via Sleep Wake Error section • Updated SWE Timer by Mode flow chart
July 15th, 2022	0.9989	<ul style="list-style-type: none"> • Updated Watchdog Window and Time-out Timer Configuration Table WD_TIMER column • Updated WD_TIMER default value from 000b to 011b in 8'h14[7:5] • Register clean up
August 26th, 2022	1.00	<ul style="list-style-type: none"> • Updated State diagram • Updated all four brownout timing diagrams • Changed register Access Type from U to H

Device Comparison Table

Device Number	CAN FD Transceiver	LIN Transceiver	Selective Wake	3.3 V LDO	5 V LDO
TCAN28443RHBQ1	X			X	
TCAN28445RHBQ1	X				X
TCAN28453RHBQ1	X		X	X	
TCAN28455RHBQ1	X		X		X
TCAN28463RHBQ1	X	X		X	
TCAN28465RHBQ1	X	X			X
TCAN28473RHBQ1	X	X	X	X	
TCAN28475RHBQ1	X	X	X		X

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5 Pin Configuration and Functions

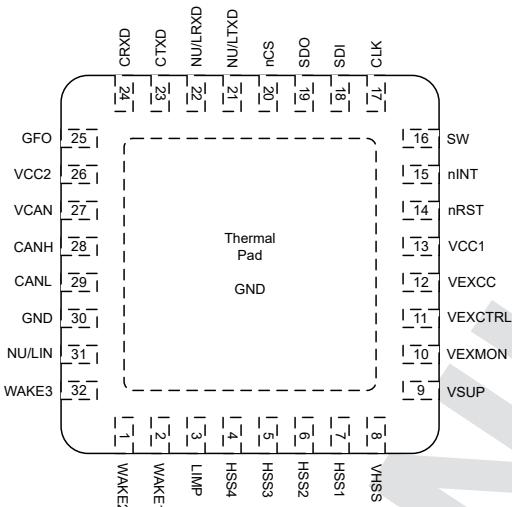


Figure 5-1. TCAN284x-Q1 RHB Package, 32 Pin (QFN), Top View

Table 5-1. Pin Functions RHB Package

NO.	NAME ⁽¹⁾		TYPE	DESCRIPTION
	TCAN2844 TCAN2845	TCAN2846 TCAN2847		
1	WAKE2	WAKE2	high voltage	Local wake input terminal, high voltage capable
2	WAKE1	WAKE1	high voltage	Local wake input terminal, high voltage capable
3	LIMP	LIMP	high voltage	Limp home output (Active low; open-drain output)
4	HSS4	HSS4	high voltage	High side switch
5	HSS3	HSS3	high voltage	High side switch
6	HSS2	HSS2	high voltage	High side switch
7	HSS1	HSS1	high voltage	High side switch
8	VHSS	VHSS	power	High side switch power
9	VSUP	VSUP	high voltage power	High voltage supply from the battery
10	VEXMON	VEXMON	power	External PNP emitter connection, shunt connection
11	VEXCTRL	VEXCTRL	power	External PNP base control
12	VEXCC	VEXCC	power	External PNP collector connection feedback
13	VCC1	VCC1	power	LDO supply output: 3.3 V or 5 V
14	nRST	nRST	digital	VCC output monitor pin (active low) and device reset input
15	nINT	nINT	digital	Interrupt output (active low)
16	SW	SW	digital	Programming mode input pin (SPI configurable active high or active low)
17	CLK	CLK	digital	SPI clock input
18	SDI	SDI	digital	SPI data input
19	SDO	SDO	digital	SPI data output
20	nCS	nCS	digital	Chip select input (active low)
21	NU	LTXD	digital	LIN transmit data input (low for dominant and high for recessive bus states) NU is not used and should not be connected to anything
22	NU	LRXD	digital	LIN receive data output (low for dominant and high for recessive bus states), tri-state NU is not used and should not be connected to anything
23	CTXD	CTXD	digital	CAN transmit data input (low for dominant and high for recessive bus states)
24	CRXD	CRXD	digital	CAN receive data output (low for dominant and high for recessive bus states), tri-state
25	GFO	GFO	digital	Function output pin (SPI configurable)
26	VCC2	VCC2	power	5 V LDO output
27	VCAN	VCAN	power	CAN FD transceiver 5 V power supply input
28	CANH	CANH	bus I/O	High level CAN bus I/O line
29	CANL	CANL	bus I/O	Low level CAN bus I/O line
30	GND	GND	power	Ground connection: Must be soldered to ground

Table 5-1. Pin Functions RHB Package (continued)

NO.	NAME ⁽¹⁾		TYPE	DESCRIPTION
	TCAN2844 TCAN2845	TCAN2846 TCAN2847		
31	NU	LIN	high voltage I/O	LIN bus input/output pin: NU is not used and should not be connected to anything
32	WAKE3	WAKE3	high voltage	Local wake input terminal, high voltage capable
PAD	GND	GND	power	Ground connection: Must be soldered to ground

- (1) The thermal pad, PAD, is a device ground pin must be soldered to GND

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
VSUP	Supply voltage ⁽²⁾	-0.3	40	V
VHSS	High-side switches supply voltage ⁽²⁾	-0.3	40	V
VEXMON	External PNP emitter monitor voltage	-0.3	40	V
VEXCC	External PNP collector feedback voltage ⁽²⁾	-0.3	28	V
VEXCTRL	External PNP base control voltage	-0.3	40	V
VCC1	Regulated 3.3 V and 5 V output supply	-0.3	6	V
V _{nRST}	Reset output voltage	-0.3	V _{CC} + 0.3	V
VCAN	CAN transceiver supply voltage	-0.3	6	V
VCC2	5 V output supply ⁽²⁾	-0.3	28	V
V _{BUSCAN}	CAN bus I/O voltage (CANH, CANL)	-58	58	V
V _{BUSLIN}	LIN bus I/O voltage	-58	58	V
V _{WAKE}	WAKE input voltage	-0.3	40	V
V _{HSSx}	High-side switch pin output voltage range	-0.3	40 and V _O ≤ V _{SUP} +0.3	V
V _{LIMP}	LIMP pin output voltage range	-0.3	40 and V _O ≤ V _{SUP} +0.3	V
V _{LOGIC_IN}	Logic pin input voltage range	-0.3	6	V
V _{LOGIC_OUT}	Logic pin output voltage range	-0.5	6	V
I _{O(LOGIC)}	Logic pin output current		8	mA
I _(WAKE)	WAKE pin input current		3	mA
I _(LIMP)	LIMP pin input current		20	mA
I _{O(nRST)}	Reset output current	-5	5	mA
T _J	Junction temperature	-55	165	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Able to support load dumps of up to 40 V for 300ms

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM) Classification Level H2, V _{SUP} , CANL/H, LIN, VSUP, VHSS and WAKE, per AEC Q100-002 ⁽¹⁾	±8000	V
		Human body model (HBM) Classification Level 3A, all other pins, per AEC Q100-002 ⁽¹⁾	±4000	
		Charged device model (CDM) Classification Level C5, per AEC Q100-011	±750	
		Corner pins	±750	
		Other pins	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 IEC ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge according to IEC 62228-2 for LIN and IEC 62228-3 for CAN ⁽¹⁾	contact discharge, LIN, CANH, CANL, VSUP, VHSS, WAKE	±8000	V

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge according to IEC 62228-2 for LIN and IEC 62228-3 for CAN ⁽¹⁾	Indirect ESD, LIN, CANH, CANL, VSUP, VHSS, WAKE	±15000	V	
V _(ESD)	Electrostatic discharge according to SAE J2962-1 for LIN and J2962-2 for CAN ⁽²⁾	contact discharge (LIN, CANH, CANL)	±8000	V	
		air-gap discharge (CANH, CANL)	±15000		
		air-gap discharge (LIN)	±25000		
ISO7637-2 and IEC 62215-3 Transients, LIN, CANH/L, VSUP, VHSS and WAKE ⁽³⁾		Pulse 1	-100	V	
		Pulse 2	75		
		Pulse 3a	-150		
		Pulse 3b	100		
IS07637-3 Slow Transient Pulse CAN and LIN bus terminals to GND ⁽⁴⁾	Direct coupling capacitor "slow transient pulse" with 100 nF coupling capacitor - powered	±30	V		

(1) IEC 62228-2 and IEC 62228-3 ESD performed by a third party. Different system-level configurations may lead to results.

(2) SAE J2962-1 and SAE J2962-2 testing performed at 3rd party US3 approved EMC test facility.

(3) ISO 7637-2 according to IEC 62228-2 and IEC 62228-3 are system-level transient tests. Different system-level configurations may lead to different results.

(4) ISO 7637-3 is a system-level transient test. Different system-level configurations may lead to different results.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VSUP	Supply voltage ^{(1) (2)}	4.5	28	28	V
VHSS	High-side switches supply voltage	5	28	28	V
VCAN	CAN Transceiver supply voltage	4.5	5	5.5	V
V _{LIN}	LIN bus input voltage	0	28	28	V
I _{O(HDO)}	Digital output high level current	–2			mA
I _{O(LDO)}	Digital output low level current		2	2	mA
I _{O(LIMP)}	LIMP pin current when configured as LIMP		6	6	mA
I _{O(HSSX)}	High side switch pin current	60	100	100	mA
C _(VSUP)	V _{SUP} supply capacitance	100			nF
C _(VEXCC)	VEXCC supply capacitance;	4.7			µF
ESR _C	VEXCC ESR capacitance requirements	1	150	150	mΩ
C _(VCC1/2)	VCC1 and VCC2 supply capacitance; 50 µA to full load	1			µF
C _(VCC1/2)	VCC1 and VCC2 supply capacitance; no load to full load	4.7			µF
ESR _{CO}	VCC1 and VCC2 output ESR capacitance requirements	0.001	1	1	Ω
TSDWR	Thermal shut down warning	145	165	165	°C
TSDWF	Thermal shut down warning release	130	155	155	°C
TSDWHYS	Thermal shut down warning hysteresis		10.0	10.0	°C
TSDR	Thermal shut down	165	200	200	°C
TSDF	Thermal shut down release	155	190	190	°C
TSDHYS	Thermal shut down hysteresis		10.0	10.0	°C
T _J	Operating junction temperature range	–40	150	150	°C

- (1) When VCC1 is 3.3 V output, VCC1 will work with a VSUP of 4.5 V but other LDOs will be in pass thru mode and output voltage will not be at regulated value. For all LDOs to be in regulation VSUP needs to be at or above 5.5 V.
- (2) When VCC1 is 3.3 V output and VSUP is above 4.5V, the LIN transceiver will function but may not meet the electrical or timing parameters.

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		RHB (QFN)	UNIT
		32-PINS	
R _{θJA}	Junction-to-ambient thermal resistance	31.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	11.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	21.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	2.8	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	11.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.6 Supply Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply from Battery					
VSUP	Operational supply voltage ⁽¹⁾	5.5	28		V
ISUP _{normdom}	Battery supply current device in normal mode with CAN FD and LIN bus dominant	40	60		mA
ISUP _{normrex}	Battery supply current device in normal mode with CAN FD and LIN bus recessive	5	7.5		mA
ISUP _{stbyswo}	Battery supply current, standby mode with selective wake off	240	300		µA
ISUP _{slpswo}	Battery supply current, sleep mode with selective wake off	25	60		µA
ISUP _{slpswotrx}	Battery supply current, sleep mode with selective wake, LDO's and transceivers off	18	42		µA
ISUP _{slpswoact}	Battery supply current, sleep mode with selective wake on and WUP has taken place on CAN bus - bus active	480	550		µA
VSUP _{(PU)R}	Supply on detection	VSUP rising; see Figure 7-17	1.8	3.9	V
VSUP _{(PU)F}	Supply off detection	VSUP falling; see Figure 9-10 and Figure 9-11	1.7	3.5	V
VSUP _{(PU)HYS}	Supply off detection hysteresis		50	550	mV
UVSUP _{5R}	Supply undervoltage recovery	VSUP rising; see Figure 7-17 , Figure 9-10 and Figure 9-11	4.9	5.5	V
UVSUP _{5F}	Supply undervoltage detection	VSUP falling; see Figure 9-10 and Figure 9-11	4.5	5.1	V
UVSUP _{5HYS}	Supply undervoltage detection hysteresis		200	600	mV

6.6 Supply Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
UVSUP _{33R}	Supply undervoltage recovery	VSUP rising; see Figure 7-17 , Figure 9-10 and Figure 9-11	3.7		4.4	V
UVSUP _{33F}	Supply undervoltage detection	VSUP falling; see Figure 9-10 and Figure 9-11	3.55		4.25	V
UVSUP _{33HYS}	Supply undervoltage detection hysteresis		50		300	mV
VHSS	High-side switches operational supply voltage	All Modes of operation	5		28	V
IHSS	High-side switch current	VHSS = 14 V, - All four HSS On and full load		400	600	mA
IHSS	High-side switch current - no load	Additional current from each HSS pin			110	µA
UVHSS _R	High-side switches supply undervoltage recovery	VHSS rising	4.2		4.9	V
UVHSS _F	High-side switches supply undervoltage detection	VHSS falling	3.9		4.75	V
OVHSS	VHSS over-voltage threshold for the high-side switches	When VHSS exceeds limit, the HSSx turns off	20		22	V
OVHSS _{HYS}	VHSS over-voltage threshold hysteresis		875		1100	mV

Supply from VCC1 and VCC2

VCC1 ₅	Regulated output	VSUP = 5.5 V to 28 V, ICC1 = 1 to 250 mA	4.9	5	5.1	V
VCC1 ₃₃	Regulated output	VSUP = 5.5 V to 28 V, ICC1 = 1 to 250 mA	3.234	3.3	3.366	V
ICC1 _{slp}	VCC1 sleep mode supply current	Sleep mode; VCC1 enabled and no load		22	30	µA
		Sleep mode; VCC1 disabled	-1		10	µA
ICC1	Output current	VCC1 in regulation with 14 V VSUP	0		250	mA
ICC1 _{SINK}	VCC1 current sink capability	VSUP = 14 V and register 8'h0D[3] = 0b	-17	-11	-7	µA
		VSUP = 14 V and register 8'h0D[3] = 1b	-155	-112	-75	µA
ICC1 _{LIM}	VCC1 output current limit	VCC1 short to ground	300		750	mA
UVCC1 _{5RPR}	VCC1 undervoltage recovery threshold pre-warning	VCC1 rising	4.65	4.8	4.9	V
UVCC1 _{5FPR}	VCC1 undervoltage detection threshold pre-warning	VCC1 falling	4.6	4.7	4.85	V
UVCC1 _{5R1}	VCC1 undervoltage recovery threshold 1	VCC1 rising, Register 8'h0E[4:3] = 00b	4.60	4.70	4.85	V
UVCC1 _{5F1}	VCC1 undervoltage detection threshold 1	VCC1 falling, Register 8'h0E[4:3] = 00b	4.50	4.60	4.75	V
UVCC1 _{5R2}	VCC1 undervoltage recovery threshold 2	VCC1 rising, Register 8'h0E[4:3] = 01b	3.85	4.00	4.15	V
UVCC1 _{5F2}	VCC1 undervoltage detection threshold 2	VCC1 falling, Register 8'h0E[4:3] = 01b	3.75	3.90	4.05	V
UVCC1 _{5R3}	VCC1 undervoltage recovery threshold 3	VCC1 rising, Register 8'h0E[4:3] = 10b	3.25	3.40	3.55	V
UVCC1 _{5F3}	VCC1 undervoltage detection threshold 3	VCC1 falling, Register 8'h0E[4:3] = 10b	3.15	3.30	3.45	V
UVCC1 _{5R4}	VCC1 undervoltage recovery threshold 4	VCC1 rising, Register 8'h0E[4:3] = 11b	2.50	2.75	2.90	V
UVCC1 _{5F4}	VCC1 undervoltage detection threshold 4	VCC1 falling, Register 8'h0E[4:3] = 11b	2.40	2.65	2.80	V
UVCC1 _{5HYS}	Undervoltage detection 5 V LDO hysteresis		70		175	mV

6.6 Supply Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
UVCC1 _{33RPR}	VCC1 undervoltage recovery threshold pre-warning	VCC1 rising	3.1	3.2	3.28	V
UVCC1 _{33FPR}	VCC1 undervoltage detection threshold pre-warning	VCC1 falling	3	3.1	3.2	V
UVCC1 _{33R1}	VCC1 undervoltage recovery threshold 1	VCC1 rising, Register 8'h0E[4:3] = 00b	3	3.1	3.2	V
UVCC1 _{33F1}	VCC1 undervoltage detection threshold 1	VCC1 falling, Register 8'h0E[4:3] = 00b	2.95	3.05	3.15	V
UVCC1 _{33R2}	VCC1 undervoltage recovery threshold 2	VCC1 rising, Register 8'h0E[4:3] = 01b	2.55	2.651	2.75	V
UVCC1 _{33F2}	VCC1 undervoltage detection threshold 2	VCC1 falling, Register 8'h0E[4:3] = 01b	2.5	2.6	2.7	V
UVCC1 _{33R3}	VCC1 undervoltage recovery threshold 3	VCC1 rising, Register 8'h0E[4:3] = 10b	2.25	2.35	2.45	V
UVCC1 _{33F3}	VCC1 undervoltage detection threshold 3	VCC1 falling, Register 8'h0E[4:3] = 10b	2.2	2.3	2.4	V
UVCC1 _{33R4}	VCC1 undervoltage recovery threshold 4	VCC1 rising, Register 8'h0E[4:3] = 11b	2.05	2.15	2.25	V
UVCC1 _{33F4}	VCC1 undervoltage detection threshold 4	VCC1 falling, Register 8'h0E[4:3] = 11b	2	2.1	2.2	V
UVCC1 _{33HYS}	Undervoltage detection 3.3 V LDO hysteresis		45	100	mV	
OVCC1 _{5R}	Over voltage 5 V VCC threshold to enter sleep mode or fail-safe mode	Ramp Up	5.3	5.6	V	
OVCC1 _{5F}	Over voltage 5 V VCC threshold	Ramp Down	5.2	5.5	V	
OVCC1 _{5HYS}	Over voltage 5 V VCC threshold hysteresis		90	175	mV	
OVCC1 _{33R}	Over voltage 3.3 V VCC threshold to enter sleep mode or fail-safe mode	Ramp Up	3.5	3.8	V	
OVCC1 _{33F}	Over voltage 3.3 V VCC threshold	Ramp Down	3.4	3.6	V	
OVCC1 _{33HYS}	Over voltage 3.3 V VCC threshold hysteresis		140	185	mV	
VCC1 _{5SC}	VCC1 short circuit threshold to enter sleep mode or fail-safe mode for 5 V LDO	VSUP ≥ V _{POR}		1.7	2.3	V
VCC1 _{33SC}	VCC1 short circuit threshold to enter sleep mode or fail-safe mode for 3.3 V LDO	VSUP ≥ V _{POR}		1.1	1.2	V
VCC2nom	Normal operation regulated output	VSUP = 14 V, ICC2 = 5 to 200 mA	4.9	5	5.1	V
VCC2red	Reduced operation regulated output	VSUP = 8V - 18V; ICC2 = 10µA - 5mA; T _j = 25°C - 125°C	4.95	5	5.05	V
ICC2	Supply current	VCC2 in regulation with 14 V VSUP			200	mA
ICC2	Supply current	Standby mode; V _{TXD} = VCC1, R _L = 50 Ω, C _L = open, VCC2 = no load		3.5	8	µA
ICC2 _{slp}	VCC2 sleep mode supply current	Sleep mode; VCC2 enabled and no load		16	30	µA
		Sleep mode; VCC2 disabled	-1		1	µA
ICC2 _{LIM}	VCC2 output current limit	VCC2 short to ground	250		650	mA
UVCC2 _R	Undervoltage recovery VCC2	VCC2 rising	4.6		4.9	V
UVCC2 _F	Undervoltage detection VCC2	VCC2 falling	4.5		4.75	V

6.6 Supply Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
UVCC2 _{HYS}	Undervoltage detection VCC2 hysteresis		120	250	mV	
OVCC2 _R	Over voltage CAN LDO threshold	Ramp Up	5.3	5.6	V	
OVCC2 _F	Over voltage CAN LDO threshold	Ramp Down	5.2	5.5	V	
OVCC2 _{HYS}	Over voltage CAN LDO threshold hysteresis		80	170	mV	
VCC2 _{SC}	CAN LDO short circuit threshold	VSUP ≥ UVSUP	1.7	2.3	V	
V _{5DROP1}	Dropout voltage (5 V LDO output, VCC1 & VCC2)	VSUP = 3.5 V, ICC1/2 = 50 mA		500	mV	
V _{5DROP2}	Dropout voltage (5 V LDO output VCC1)	VSUP = 5 V, ICC1 = 150 mA		500	mV	
V _{5DROP2}	Dropout voltage (5 V LDO output VCC2)	VSUP = 5 V, ICC2 = 30 mA		500	mV	
V _{33DROP1}	Dropout voltage (3.3 V LDO output)	VSUP = 3.5 V, ICC1 = 50 mA		500	mV	
VCCEXT						
VEXCC ₁₈	1.8 V PNP output voltage supported	5.5 V ≤ VSUP ≤ 28 V 10 mA ≤ I _{VCCEXT} ≤ 350 mA	1.764	1.8	1.836	V
VEXCC ₂₅	2.5 V PNP output voltage supported	5.5 V ≤ VSUP ≤ 28 V 10 mA ≤ I _{VCCEXT} ≤ 350 mA	2.45	2.5	2.55	V
VEXCC ₃₃	3.3 V PNP output voltage supported	5.5 V ≤ VSUP ≤ 28 V 10 mA ≤ I _{VCCEXT} ≤ 350 mA	3.234	3.3	3.366	V
VEXCC ₅	5 V PNP output voltages supported	5.5 V ≤ VSUP ≤ 28 V 10 mA ≤ I _{VCCEXT} ≤ 350 mA	4.9	5	5.1	V
VEXCC _{ACC}	PNP output voltages accuracy	5.5 V ≤ VSUP ≤ 28 V 10 mA ≤ I _{VCCEXT} ≤ 350 mA	-2		2	%
UVEXCC _R	VEXCC exiting undervoltage event	5.5 V ≤ VSUP ≤ 28 V	0.86	0.9	0.92	V _{EXCC}
UVEXCC _F	VEXCC entering undervoltage event	5.5 V ≤ VSUP ≤ 28 V	0.80	0.85	0.89	V _{EXCC}
UVEXCC _{HSY}	VEXCC entering undervoltage hysteresis	5.5 V ≤ VSUP ≤ 28 V VEXCC = 1.8V	50		350	mV
OVEXCC _R	VEXCC entering overvoltage event	5.5 V ≤ VSUP ≤ 28 V	1.1	1.15	1.2	V _{EXCC}
OVEXCC _F	VEXCC exiting overvoltage event	5.5 V ≤ VSUP ≤ 28 V	1.07	1.1	1.12	V _{EXCC}
OVEXCC _{HYS}	VEXCC exiting overvoltage hysteresis	5.5 V ≤ VSUP ≤ 28 V VEXCC = 1.8V	45		300	mV
VEXCC _{SC18}	VEXCC short circuit detect for 1.8 V and 2.5 V	5.5 V ≤ VSUP ≤ 28 V		1.1	1.2	V
VEXCC _{SC}	VEXCC short circuit detect for 3.3 V and 5 V	5.5 V ≤ VSUP ≤ 28 V		1.7	2.3	V
IEXCC _{SLP}	VEXCC sleep mode supply current	Sleep mode; VEXCC enabled and no load			25	µA
		Sleep mode; VEXCC disabled	-1		1	µA
IEXCC _{LIM}	Current limit for external PNP	5.5 V ≤ VSUP ≤ 28 V	450			mA
IVEXCC	Input current on VEXCC	VEXCC = 5 V, 3.3 V, 2.5 V and 1.8 V	0	3	10	µA
VVEXCTRL	Voltage output on base pin of external PNP	5.5 V ≤ VSUP ≤ 28 V			28	V
IVEXCTRL	Current on base pin of external PNP	VVEXCTRL = 13.5 V			50	mA
IVEXCTRL _{LKG}	Current on base pin VEXCTRL leakage	VVEXCTRL = 13.5; T _j = 25°C			5	µA
IVEXMON	VEXMON pin input current	VEXMON = VSUP	0	3	10	µA
IVEXMON _{LKG}	VEXMON pin input leakage current ext PNP disabled	VEXMON = VSUP; T _j = 25°C			5	µA
VSHUNTT _H	Output current shunt voltage threshold (2)		0.15		0.44	V

6.6 Supply Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RLINC}	Current increase regulation reaction time	VEXCC = 5 V to 0 V; I _{VECTRL} = 20 mA, See Figure 8-10			20	μs
t_{RLDEC}	Current decrease regulation reaction time	VEXCC = 0 V to 5 V; I _{VECTRL} = 20 mA, See Figure 8-10			5	μs
Supply from VCAN						
IVCAN	Supply current	Normal mode: Recessive, V _{TXD} = VCC1, VEXCC, VCC1 and VCC2 = no load		3	5	mA
		Normal mode: Dominant, V _{TXD} = 0 V, R _L = 60 Ω and C _L = open, typical bus load, VEXCC, VCC1 and VCC2 = no load		60		mA
		Normal mode: Dominant, V _{TXD} = 0 V, R _L = 50 Ω and C _L = open, high bus load, VEXCC, VCC1 and VCC2 = no load		65		mA
		Normal mode: Dominant with bus fault, V _{TXD} = 0 V, CANH = -25 V, R _L and C _L = open, VEXCC, VCC1 and VCC2 = no load		100		mA
UVCAN _R	Supply undervoltage recovery	VCAN rising		4.2	4.5	V
UVCAN _F	Supply undervoltage detection	VCAN falling	3.5	4		V
UVCAN _{HYS}	VCAN Supply undervoltage detections hysteresis		200	275		mV

- (1) When VCC1 is 3.3 V output, VCC1 will work with a VSUP of 4.5 V but other LDOs will be in pass thru mode and output voltage will not be at regulated value. For all LDOs to be in regulation VSUP needs to be at or above 5.5 V.
- (2) Threshold at which the current limit starts to operate and is only active when VEXCC is configured for stand-alone configuration

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN Driver						
V _{O(D)}	Bus output voltage (dominant) CANH	See Figure 7-4 , V _{CTXD} = 0 V, R _L = 50 Ω to 65 Ω, C _L = open, R _{CM} = open	2.75		4.5	V
	Bus output voltage (dominant) CANL		0.5		2.25	V
V _{O(R)}	Bus output voltage (recessive)	See Figure 7-1 and Figure 7-4 V _{CTXD} = VCC1, R _L = open (no load), R _{CM} = open	2	2.5	3	V
V _(DIFF)	Maximum differential voltage rating	V _(DIFF) = V _{CANH} - V _{CANL}	-42		42	V
V _{OD(D)}	Differential output voltage(dominant)	See Figure 7-1 and Figure 7-4 , V _{CTXD} = 0 V, 50 Ω ≤ R _L ≤ 65 Ω, C _L = open, R _{CM} = open	1.5		3	V
		See Figure 7-1 and Figure 7-4 V _{CTXD} = 0 V, 45 Ω ≤ R _L ≤ 70 Ω, C _L = open, R _{CM} = open	1.4		3	V
		See Figure 7-1 and Figure 7-4 V _{CTXD} = 0 V, R _L = 2.24 kΩ, C _L = open, R _{CM} = open	1.5		5	V
V _{OD(R)}	Differential output voltage(recessive)	See Figure 7-1 and Figure 7-4 , V _{CTXD} = VCC1, R _L = 60 Ω, C _L = open, R _{CM} = open	-120		12	mV
		See Figure 7-1 and Figure 7-4 V _{CTXD} = VCC1, R _L = open (no load), C _L = open, R _{CM} = open	-50		50	mV

6.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(\text{INACT})}$	Bus output voltage on CANH with bus biasing inactive (STBY)	See Figure 7-1 and Figure 7-4 , $V_{\text{CTXD}} = V_{\text{CC1}}$, $R_L = \text{open}$, $C_L = \text{open}$, $R_{\text{CM}} = \text{open}$	-0.1	0.1	V
	Bus output voltage on CANL with bus biasing inactive (STBY)		-0.1	0.1	V
	Bus output voltage on CANH - CANL (recessive) with bus biasing inactive (STBY)		-0.2	0.2	V
V_{SYM}	Output symmetry (dominant or recessive) $(V_{O(\text{CANH})} + V_{O(\text{CANL})})/V_{\text{CC}}$	See Figure 7-1 and Figure 7-4 , $R_L = 60 \Omega$, $C_L = \text{open}$, $R_{\text{CM}} = \text{open}$, $C_1 = 4.7 \text{ nF}$, $\text{CTXD} = 250 \text{ kHz}$, 1 MHz, 2.5 MHz	0.9	1.1	V/V
$V_{\text{SYM_DC}}$	Output symmetry (dominant or recessive) $(V_{\text{CC}} - V_{O(\text{CANH})} - V_{O(\text{CANL})})$ with a frequency that corresponds to the highest bit rate for which the HS-PMA implementation is intended, however, at most 1 MHz (2 Mbit/s)	See Figure 7-1 and Figure 7-4 , $R_L = 60 \Omega$, $C_L = \text{open}$, $R_{\text{CM}} = \text{open}$, $C_1 = 4.7 \text{ nF}$	-400	400	mV
$I_{\text{OS_DOM}}$	Short-circuit steady-state output current, dominant See Figure 7-1 and Figure 7-8	$-3.0 \text{ V} \leq V_{\text{CANH}} \leq +18.0 \text{ V}$, CANL = open, $V_{\text{CTXD}} = 0 \text{ V}$	-100		mA
		$-3.0 \text{ V} \leq V_{\text{CANL}} \leq +18.0 \text{ V}$, CANH = open, $V_{\text{CTXD}} = 0 \text{ V}$		100	mA
$I_{\text{OS_REC}}$	Short-circuit steady-state output current, recessive See Figure 7-1 and Figure 7-8	$-42 \text{ V} \leq V_{\text{BUS}} \leq +42 \text{ V}$, $V_{\text{BUS}} = \text{CANH} = \text{CANL}$	-5	5	mA
CAN Receiver					
V_{ITDOM}	Receiver dominant state differential input voltage range, bus biasing active	$-12.0 \text{ V} \leq V_{\text{CANL}} \leq +12.0 \text{ V}$ $-12.0 \text{ V} \leq V_{\text{CANH}} \leq +12.0 \text{ V}$ See Figure 7-5 and Table 8-8	0.9	8	V
V_{ITREC}	Receiver recessive state differential input voltage range, bus biasing active		-3	0.5	V
V_{HYS}	Hysteresis voltage for input-threshold, normal and selective wake modes			135	mV
$V_{\text{DIFF_DOM}}$	Receiver dominant state differential input voltage range, bus biasing inactive	$-12.0 \text{ V} \leq V_{\text{CANL}} \leq +12.0 \text{ V}$ $-12.0 \text{ V} \leq V_{\text{CANH}} \leq +12.0 \text{ V}$ See Figure 7-5 and Table 8-8	1.15	8	V
$V_{\text{DIFF_REC}}$	Receiver recessive state differential input voltage range, bus biasing inactive		-3	0.4	V
$V_{\text{CM_NORM}}$	Common mode range: normal		-12	12	V
$V_{\text{CM_STBY}}$	Common mode range: standby mode		-12	12	V
$I_{\text{IOFF(LKG)}}$	Power-off (unpowered) bus input leakage current	$\text{CANH} = \text{CANL} = 5 \text{ V}$, $\text{VCAN} = \text{VSUP}$ pulled to GND via 0 ohm and $47 \text{ k}\Omega$ resistor		5	μA
C_I	Input capacitance to ground (CANH or CANL)			30	pF
C_{ID}	Differential input capacitance			15	pF
R_{ID}	Differential input resistance	$V_{\text{CTXD}} = V_{\text{CC1}}$, normal mode: $-2.0 \text{ V} \leq V_{\text{CANH}} \leq +7.0 \text{ V}$; $-2.0 \text{ V} \leq V_{\text{CANL}} \leq +7.0 \text{ V}$	12	100	k Ω
R_{IN}	Single ended Input resistance (CANH or CANL)	$-2.0 \text{ V} \leq V_{\text{CANH}} \leq +7.0 \text{ V}$ $-2.0 \text{ V} \leq V_{\text{CANL}} \leq +7.0 \text{ V}$	6	50	k Ω
$R_{\text{IN(M)}}$	Input resistance matching: $[1 - (R_{\text{IN(CANH)}} / R_{\text{IN(CANL)}})] \times 100\%$	$V_{\text{CANH}} = V_{\text{CANL}} = 5.0 \text{ V}$	-1	1	%
LIN					
V_{OH}	HIGH level output voltage ⁽¹⁾	LIN recessive, $\text{LTXD} = \text{high}$, $I_O = 0 \text{ mA}$, $\text{VSUP} = 5.5 \text{ V}$ to 28 V	0.85		VSUP

6.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OL}	LOW level output voltage ⁽¹⁾	LIN dominant, LTXD = low, VSUP = 5.5 V to 28 V			0.2	VSUP
V _{IH}	HIGH level input voltage ⁽¹⁾	LIN recessive, LTXD = high, I _O = 0 mA, VSUP = 5.5 V to 28 V	0.47		0.6	VSUP
V _{IL}	LOW level input voltage ⁽¹⁾	LIN dominant, LTXD = low, VSUP = 5.5 V to 28 V	0.4		0.53	VSUP
V _{SUP_NON_OP}	V _{SUP} where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11)	LTXD & LRXD open, V _{LIN} = 5.5 V to 45 V, VCC = no load	-0.3		45	V
I _{BUS_LIM}	Limiting current (ISO/DIS 17987 Param 12)	LTXD = 0 V, V _{LIN} = 28 V, VSUP = 28 V, V _{BUSdom} ≤ 0.251 * VSUP, VCCx = no load;	40	90	200	mA
I _{BUS_PAS_dom}	Receiver leakage current, dominant (ISO/DIS 17987 Param 13)	V _{LIN} = 0 V, VSUP = 12 V Driver off/recessive;	-1			mA
I _{BUS_PAS_rec1}	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V _{LIN} ≥ VSUP, 5.5 V ≤ VSUP ≤ 28 V Driver off;			20	µA
I _{BUS_PAS_rec2}	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V _{LIN} = VSUP, Driver off;	-5		5	µA
I _{BUS_NO_GND}	Leakage current, loss of ground (ISO/DIS 17987 Param 15)	GND = VSUP, VSUP = 12 V, 0 V ≤ V _{LIN} ≤ 28 V;	-1		1	mA
I _{BUSrec_NO_GND}	Leakage current, loss of ground LIN bus is in recessive state	GND = VSUP, VSUP = 12 V = V _{LIN} V;	-100		100	µA
I _{BUS_NO_BAT}	Leakage current, loss of supply (ISO/DIS 17987 Param 16)	0 V ≤ V _{LIN} ≤ 28 V, VSUP = GND;			10	µA
V _{BUSdom}	Low level input voltage (ISO/DIS 17987 Param 17)	LIN dominant (including LIN dominant for wake up);			0.4	VSUP
V _{BUSrec}	High level input voltage (ISO/DIS 17987 Param 18)	LIN recessive;	0.6			VSUP
V _{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 19)	V _{BUS_CNT} = (V _{IL} + V _{IH})/2;	0.475	0.5	0.525	VSUP
V _{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 20) ⁽²⁾	V _{HYS} = (V _{IH} - V _{IL}); V _{HYS} = (V _{th_rec} - V _{th_dom}) ⁽³⁾	0.07		0.175	VSUP
V _{SERIAL_DIODE}	Serial diode LIN term pull-up path (ISO/DIS 17987 Param 21)	By design and characterization	0.4	0.7	1.0	V
R _{LIN}	Internal pull-up resistor to V _{SUP} on LIN (ISO/DIS 17987 Param 26)	Normal and Standby modes	20	45	60	kΩ
I _{RSLEEP}	Pull-up current source to V _{SUP}	Sleep mode, VSUP = 12 V, LIN = GND	-20		-2	µA
C _{LIN,PIN}	Capacitance of the LIN pin	By design and characterization			25	pF
LIMP Output (Open-drain)						
V _{OL}	Open-drain output voltage (active low)	External Pull-up; 4.5V < V < 28V, I _{LIMP} = - 6 mA		0.5	1	V
I _{LKG(LIMP)}	Output current (inactive)	V _{LIMP} = 0V to 28 V	-2		2	µA
HSS1, HSS2, HSS3, HSS4 (High voltage output)						
ΔV _{HHSS}	Hi-level voltage drop for HSS with respect to V _{HSS}	I _{HSS} = - 60 mA		0.42	1.2	V
R _{dson}	HSS output drain-to-source on resistance	I _O = - 60 mA		7	16	Ω
I _{O(HSS)}	Output current support	V _{HSS} = 14 V,		60	100	mA
I _{OC(HSS)}	HSS overcurrent limit	V _{HSS} = 14 V	150		300	mA
I _{OL(HSS)}	HSS open load current	V _{HSS} = 14 V			3.0	mA
I _{OLHYS(HSS)}	HSS open load current hysteresis	V _{HSS} = 14 V	0.05	0.45	1	mA
I _{Ikg}	Leakage current	HSS = 0 V, Sleep Mode	-1		1	µA

6.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{R/F}$	Output rise and fall times (HSS) $V_{HSS} \leq 28 \text{ V}, I_{LOAD} = 60 \text{ mA}, R_L = 220 \Omega, 80\%/20\%$	0.45		2.5	$\text{V}/\mu\text{s}$
t_{HSS_on}	Switching on delay (HSS) from SPI command to on $V_{HSS} = 14 \text{ V}, I_{LOAD} = 60 \text{ mA}, V_{OUT} = 80\% \text{ of } V_{HSS}$			60	μs
t_{HSS_off}	Switching off delay (HSS) from SPI command to off $V_{HSS} = 14 \text{ V}, I_{LOAD} = 60 \text{ mA}, V_{OUT} = 20\% \text{ of } V_{HSS}$			140	μs
t_{OCFLTR}	HSS overcurrent filter time $V_{HSS} = 14 \text{ V}$		16		μs
t_{OLFLTR}	HSS open load filter time $V_{HSS} = 14 \text{ V}$		64		μs
t_{OCOFF}	HSS overcurrent shut off time $I_{O(HSS)} > I_{OC(HSS)}$	200		300	μs

WAKE1, WAKE2, WAKE3 Input Terminal (High voltage input)

V_{IH}	High-level input voltage: Sleep, selective wake-up or standby mode, WAKE pin enabled (7)	Register setting 00b VCC1 based	0.7		VCC1
		Register setting 01b	2.5	2.6	3.5
		Register setting 10b	3.8	4.1	5
		Register setting 11b	5.6	6.1	7
V_{IL}	Low-level input voltage: Sleep, selective wake-up or standby mode, WAKE pin enabled (7)	Register setting 00b VCC1 based			0.3
		Register setting 01b	1.5	2.4	2.8
		Register setting 10b	3.0	3.9	4.2
		Register setting 11b	5	5.9	6.3
I_{IL}	Low-level input current	WAKE = 1 V		15	μA
t_{WAKE}	Wake up hold time from a wake edge on WAKE in standby or sleep mode for static sensing.	See Figure 8-26 and Figure 8-27		140	μs
$t_{WAKE_INVALID}$	WAKE pin pulses shorter than this will be filtered out in standby or sleep mode for static sensing.	See Figure 8-26 and Figure 8-27	10		μs

SDI, CLK, nCS, SW, CTXD, LTXD Input Terminals

V_{IH}	High-level input voltage		0.7		VCC1
V_{IL}	Low-level input voltage			0.3	VCC1
$V_{IHSWINT}$	SW pin high-level input voltage when VCC1 is missing for sleep or fail-safe mode	Register 8'h0E[1] = 1 and/or 8'h0E[2] = 1 and VCC1 missing in sleep or fail-safe mode		1.1	V
$V_{ILSWINT}$	SW low-level input voltage when VCC1 is missing for sleep or fail-safe mode	Register 8'h0E[1] = 1 and/or 8'h0E[2] = 1 and VCC1 missing in sleep or fail-safe mode		0.4	V
$I_{IHSWINT}$	High-level input leakage current for SW pin when VCC1 is off	VCC1 off, internal pull-down enabled, Vin = 1.5 V	-2.5	7	μA
$I_{IHSWINT}$	High-level input leakage current for SW pin when VCC1 is off	VCC1 off, internal pull-down enabled, Vin = 0 V	-1	1	μA
$I_{ILSWINT}$	Low-level input leakage current for SW pin when VCC1 is off	VCC1 off, internal pull-up enabled, Vin = 1.5 V	-1	1	μA
$I_{ILSWINT}$	Low-level input leakage current for SW pin when VCC1 is off	VCC1 off, internal pull-up enabled Vin = 0 V	-30	-2	μA
I_{IHSW}	High-level input leakage current for SW pin when VCC1 is on	VCC1 on, internal pull-down enabled	-1	1	μA
I_{ILSW}	Low-level input leakage current for SW pin when VCC1 is on	VCC1 on, internal pull-up enabled	-30	-2	μA
I_{IH}	High-level input leakage current	VCC1 $\pm 5\%$	-1	1	μA
I_{IL}	Low-level input leakage current	Inputs = 0 V, VCC1 $\pm 5\%$	-30	-2	μA
I_{ILnCS}	Low-level input leakage current for nCS	Inputs = 0 V, VCC1 $\pm 5\%$	-30	-2	μA
C_{IN}	Input Capacitance	at 20 MHz	4	10	pF

6.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{LKG(OFF)}	Unpowered leakage current	Inputs = 5.5 V, VCC1 = VSUP = 0 V	-1	0	1	µA
R _{pd}	SW pin pull-down resistor		230	350	455	kΩ
R _{pu}	Pull-up resistor (SDI, CLK, nCS, SW, CTXD and LTXD pins)		250	350	450	kΩ
CRXD, LRXD, SDO, GFO, nINT Output Terminals						
V _{OH}	HIGH level output voltage	I _{OH} = -2 mA	0.8			VCC1
V _{OL}	LOW level output voltage	I _{OL} = 2 mA		0.2		VCC1
I _{LKG(OFF)}	Unpowered leakage current	V _{nCS} = VCC1; V _O = 0 V to VCC1	-5		5	µA
nRST Terminal (input/output)						
V _{IH}	High level input switching threshold voltage	Based off of internal voltage	2.1			V
V _{IL}	Low level input switching threshold voltage	Based off of internal voltage		0.8		V
V _{OL}	Low-level output voltage	Based upon external pull up to VCC1		0.2		VCC1
I _{OL}	Low-level output current, open drain	nRST = 0.4 V	1.5			mA
I _{LKG}	Leakage current, high-level	nRST = VCC1	-5		5	µA
R _{PU}	Pull-up resistance (Output pulled up to VCC1)		10	30	50	kΩ
LIN Duty Cycle						
D1	Duty Cycle 1 (ISO/DIS 17987 Param 27 and J2602 Normal battery) ^{(4) (5)}	TH _{REC(MAX)} = 0.744 x VSUP, TH _{DOM(MAX)} = 0.581 x VSUP, VSUP = 7 V to 18 V, t _{BIT} = 50/52 µs, D1 = t _{BUS_rec(min)} /(2 x t _{BIT}), (See Figure 7-13, Figure 7-14)	0.396			
D2	Duty Cycle 2 (ISO/DIS 17987 Param 28 and J2602 Normal battery) ^{(4) (5)}	TH _{REC(MIN)} = 0.422 x VSUP, TH _{DOM(MIN)} = 0.284 x VSUP, VSUP = 7.6 V to 18 V, t _{BIT} = 50/52 µs, D2 = t _{BUS_rec(MAX)} /(2 x t _{BIT}) (See Figure 7-13, Figure 7-14)		0.581		
D3	Duty Cycle 3 (ISO/DIS 17987 Param 29 and J2602 Normal battery) ^{(4) (5)}	TH _{REC(MAX)} = 0.778 x VSUP, TH _{DOM(MAX)} = 0.616 x VSUP, VSUP= 7 V to 18 V, t _{BIT} = 96 µs (10.4 kbps), D3 = t _{BUS_rec(min)} /(2 x t _{BIT}), (See Figure 7-13, Figure 7-14)	0.417			
D4	Duty Cycle 4 (ISO/DIS 17987 Param 30 and J2602 Normal battery) ^{(4) (5)}	TH _{REC(MIN)} = 0.389 x VSUP, TH _{DOM(MIN)} = 0.251 x VSUP, VSUP= 7.6 V to 18 V, t _{BIT} = 96 µs (10.4 kbps), D4 = t _{BUS_rec(MAX)} /(2 x t _{BIT}) (See Figure 7-13, Figure 7-14)		0.59		
D1 _{LB}	Duty Cycle 1 J2602 Low battery ^{(5) (6)}	TH _{REC(MAX)} = 0.665 x VSUP, TH _{DOM(MAX)} = 0.499 x VSUP, VSUP = 5.5 V to 7 V, t _{BIT} = 50/52 µs, D1 _{LB} = t _{BUS_rec(min)} /(2 x t _{BIT}) (See Figure 7-13, Figure 7-14)	0.396			
D2 _{LB}	Duty Cycle 2 J2602 Lowl battery ^{(5) (6)}	TH _{REC(MIN)} = 0.496 x VSUP, TH _{DOM(MIN)} = 0.361 x VSUP, VSUP = 6.1 V to 7 V, t _{BIT} = 50/52 µs, D2 _{LB} = t _{BUS_rec(MAX)} /(2 x t _{BIT}) (See Figure 7-13, Figure 7-14)		0.581		
D3 _{LB}	Duty Cycle 3 J2602 Low battery ^{(5) (6)}	TH _{REC(MAX)} = 0.665 x VSUP, TH _{DOM(MAX)} = 0.499 x VSUP, VSUP = 5.5 V to 7 V, t _{BIT} = 96 µs, D3 _{LB} = t _{BUS_rec(min)} /(2 x t _{BIT}) (See Figure 7-13, Figure 7-14)	0.417			

6.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D4 _{LB}	Duty Cycle 4 J2602 Low battery ^{(5) (6)}	$TH_{REC(MIN)} = 0.496 \times VSUP$, $TH_{DOM(MIN)} = 0.361 \times VSUP$, $VSUP = 6.1 \text{ V}$ to 7 V , $t_{BIT} = 96 \mu\text{s}$, $D4_{LB} = t_{BUS_rec(MAX)} / (2 \times t_{BIT})$ (See Figure 7-13, Figure 7-14)			0.59	
T _{r-d max}	$t_{REC(MAX)} - t_{DOM(MIN)}$ ⁽⁵⁾	$TH_{REC(MAX)} = 0.744 \times VSUP$, $TH_{DOM(MAX)} = 0.581 \times VSUP$, $VSUP = 7 \text{ V}$ to 18 V , $t_{BIT} = 52 \mu\text{s}$ (19.231 kbps), (See Figure 7-13, Figure 7-14)			10.8	μs
T _{d-r max}	$t_{DOM(MAX)} - t_{REC(MIN)}$ ⁽⁵⁾	$TH_{REC(MIN)} = 0.422 \times VSUP$, $TH_{DOM(MIN)} = 0.284 \times VSUP$, $VSUP = 7.6 \text{ V}$ to 18 V , $t_{BIT} = 52 \mu\text{s}$ (19.231 kbps), (See Figure 7-13, Figure 7-14)			8.4	μs
T _{r-d max}	$t_{REC(MAX)} - t_{DOM(MIN)}$ ⁽⁵⁾	$TH_{REC(MAX)} = 0.778 \times VSUP$, $TH_{DOM(MAX)} = 0.616 \times VSUP$, $VSUP = 7 \text{ V}$ to 18 V , $t_{BIT} = 96 \mu\text{s}$ (10.4 kbps), (See Figure 7-13, Figure 7-14)			15.9	μs
T _{d-r max}	$t_{DOM(MAX)} - t_{REC(MIN)}$ ⁽⁵⁾	$TH_{REC(MIN)} = 0.389 \times VSUP$, $TH_{DOM(MIN)} = 0.251 \times VSUP$, $VSUP = 7.6 \text{ V}$ to 18 V , $t_{BIT} = 96 \mu\text{s}$ (10.4 kbps), (See Figure 7-13, Figure 7-14)			17.28	μs

- (1) SAE J2602 loads include: commander: 5.5 nF; 4 kΩ and for a responder: 5.5 nF; 875 Ω
- (2) V_{HYS} is defined for both ISO 17987 and SAE J2602-1.
- (3) $V_{HYS} = (V_{th_rec} - V_{th_dom})$ where V_{th_rec} and V_{th_dom} are the actual voltage values from V_{BUSrec} and V_{BUSDom}
- (4) ISO 17987 loads include 1 nF; 1 kΩ/ 6.8nF; 660 Ω/ 10 nF; 500 Ω; with t_{BIT} values of 50 μs and 96 μs
- (5) SAE J2602 loads include: commander: 5.5 nF; 4 kΩ/ 899 pF; 20 kΩ and for a responder: 5.5 nF; 875 Ω/ 899 pF; 900 Ω; with t_{BIT} values of 52 μs and 96 μs
- (6) ISO 17987 does not have a low battery specification. Using the ISO 17987 loads, these low battery duty cycle parameters are covered for t_{BIT} values of 50 μs and 96 μs
- (7) Selected using Register 8'h12[1:0] default value 10b for WAKE1; Register 8'h2B[5:4] default value 10b for WAKE2; Register 8'h2B[1:0] default value 10b for WAKE3

6.8 Timing Requirements

		MIN	NOM	MAX	UNIT
Supply					
t _{PWRUP}	Time after VSUP exceeds UVSUP and VCC1> UVCC1			2	ms
t _{UVFLTR}	Under-voltage detection delay time for VCC1, VCC2 and VEXCC	5	50		μs
t _{UVCC1PR}	Under-voltage filter time for VCC1 pre-warning	0.5	7		μs
t _{UVCANFLTR}	Under-voltage filter time for VCAN	5	10		μs
t _{OVFLTR}	Over-voltage detect filter time on VCC1, VCC2 and VEXCC	20	45		μs
t _{OVFLTRVHSS}	Over-voltage detect filter time on VHSS	4	35		μs
t _{VSC}	Short to ground on VCC1, VCC2 and VEXCC detection delay time	75	100	125	μs
t _{VSCLS}	Short to ground for VCC1 and VEXCC detection delay time when load sharing	0.5	1	1.5	ms
t _{LDOON}	Time LDO is on to determine if a fault event is present after a previous uncleared detection, see Figure 7-18			3.5	ms
t _{LDOOFF}	Time VCC1 LDO is off in fail-safe mode before accepting wake events and checking for fault conditions	250	300	350	ms
Mode Change					

6.8 Timing Requirements (continued)

		MIN	NOM	MAX	UNIT
$t_{MODE_STBY_NOM_CTRX}$	CAN transceiver state change time based upon SPI write from off or wake capable to on or listen state where CRXD mirror CAN bus			70	μs
$t_{MODE_STBY_NOM_LTRX}$	LIN transceiver state change time based upon SPI write from off or wake capable to on or fast state where LRXD mirror LIN bus			70	μs
$t_{MODE_NOM_SLP}$	Time from SPI sleep command where CAN and/or LIN transceiver is off and RXD doesn't reflect the bus, see Figure 7-19			200	μs
$t_{MODE_NOM_STBY}$	SPI write to go to standby from normal mode, see Figure 7-20			70	μs
Device Timing					
t_{RSTN_act}	Time required for $VCC1 \geq UVCC1$ to leave Restart mode, see Figure 7-17 , Figure 7-18 , Figure 8-23 and Figure 9-10 as examples	1.5	2	2.5	ms
t_{NRSTIN}	Input pulse required on the nRST pin to recognize a device reset, see Figure 8-19	75	100	125	μs
t_{RSTTO}	Time required for $VCC1 > UVCC1R$ before the device enters fail-safe mode if enabled or to sleep mode if fail-safe mode is disabled	120	150	180	ms
t_{NRST_TOG}	nRST pin output toggle high to low to high time. reg 8'h29[5] = 0, see Figure 8-19	1.5	2	2.5	ms
	nRST pin output toggle high to low to high time. reg 8'h29[5] = 1, see Figure 8-19	10	15	20	ms
$t_{WK_TIMEOUT}$	Bus wake-up timeout value; See Figure 8-23	0.5		2	ms
t_{WK_FILTER}	Bus time to meet filtered bus requirements for wake up request; See Figure 8-23	0.5		1.8	μs
$t_{WK_WIDTH_MIN}$	Minimum WAKE Pin pulse width (2) (3) (4) Register 8'h11[3:2] = 00b; See Figure 8-28	10			ms
	Minimum WAKE Pin pulse width (2) (3) (4) Register 8'h11[3:2] = 01b; See Figure 8-28	20			ms
	Minimum WAKE Pin pulse width (2) (3) (4) Register 8'h11[3:2] = 10b; See Figure 8-28	40			ms
	Minimum WAKE Pin pulse width (2) (3) (4) Register 8'h11[3:2] = 11b; See Figure 8-28	80			ms
$t_{WK_WIDTH_INVALID}$	Maximum WAKE Pin pulse width that is considered invalid (2) (3) (4) Register 8'h11[3:2] = 00b; See Figure 8-28			5	ms
	Maximum WAKE Pin pulse width that is considered invalid (2) (3) (4) Register 8'h11[3:2] = 01b; See Figure 8-28			10	ms
	Maximum WAKE Pin pulse width that is considered invalid (2) (3) (4) Register 8'h11[3:2] = 10b; See Figure 8-28			20	ms
	Maximum WAKE Pin pulse width that is considered invalid (2) (3) (4) Register 8'h11[3:2] = 11b; See Figure 8-28			40	ms
$t_{WK_WIDTH_MAX}$	Maximum WAKE Pin pulse window (2) Register 8'h11[1:0] = 00b; See Figure 8-28	750		950	ms
	Maximum WAKE Pin pulse window (2) Register 8'h11[1:0] = 01b; See Figure 8-28	1000		1250	ms
	Maximum WAKE Pin pulse window (2) Register 8'h11[1:0] = 10b; See Figure 8-28	1500		1875	ms
	Maximum WAKE Pin pulse window (2) Register 8'h11[1:0] = 11b; See Figure 8-28	2000		2500	ms

6.8 Timing Requirements (continued)

		MIN	NOM	MAX	UNIT
t_{WK_CYC}	Sampling window for cyclic sensing; Standby or Sleep mode, Register 8'h12[5] = 0b; see Figure 8-31	10	25	35	μs
	Sampling window for cyclic sensing; Standby or Sleep mode, Register 8'h12[5] = 1b; see Figure 8-31	55	70	85	μs
$t_{SILENCE_CAN}$	Timeout for bus inactivity Timer is reset and restarted, when bus changes from dominant to recessive or vice versa.	0.6		1.2	s
$t_{INACTIVE}$	SWE timer used for fail-safe and mode inactivity. Can be programmed to different values using register 8'h1C[6:3]	4	5	6	min
t_{Bias}	Time from the start of a dominant-recessive-dominant sequence. Each phase 6 μs until $V_{sym} \geq 0.1$. See Figure 7-10			250	μs
t_{SW}	SW pin filter time for a state change to be recognized	130			μs
t_{INITWD}	Initial long window for watchdog, see Figure 8-52			150	ms
t_{CTXD_DTO}	Dominant time out ⁽¹⁾ See , $R_L = 60 \Omega$, $C_L = \text{open}$; See Figure 7-7	1		5	ms
t_{LTXD_DTO}	LIN dominant state time out	20	45	80	ms
t_{TOGGLE}	RXD pin toggle timing when programmed after a WUP; See Figure 8-23	5	10	15	μs

- (1) The CTXD dominant time out (t_{CTXD_DTO}) disables the driver of the transceiver once the CTXD has been dominant longer than t_{CTXD_DTO} , which releases the CAN bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after CTXD has been returned HIGH (recessive). While this protects the CAN bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on CTXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{CTXD_DTO} minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = $11/t_{CTXD_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps}$.
- (2) This parameter is valid only when register 11h[7:6] = 11b
- (3) This is the minimum pulse width for a WAKE pin input that device will detect as a good pulse. Value between the min $t_{WK_WIDTH_MIN}$ and max $t_{WK_WIDTH_INVALID}$ is indeterminant and may or may not be considered valid.
- (4) This parameter is set based upon the programmed value for $t_{WK_WIDTH_INVALID}$ register 11h[3:2]

6.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switching Characteristics (CAN Transceiver)					
t_{pHR}	Propagation delay time, high CTXD to driver recessive	35	55	90	ns
t_{pLD}	Propagation delay time, low CTXD to driver dominant	25	46	90	ns
$t_{sk(p)}$	Pulse skew ($ t_{pHR} - t_{pLD} $)	6	25		ns
$t_{R/F}$	Differential output signal rise time:	10	48	85	ns
t_{pHR}	Propagation delay time, high CTXD to driver recessive	50	118	140	ns
t_{pLD}	Propagation delay time, low CTXD to driver dominant	35	90	140	ns
$t_{sk(p)}$	Pulse skew ($ t_{pHR} - t_{pLD} $)	23	40		ns
$t_{R/F}$	Differential output signal rise time:	10	55	75	ns
t_{pRH}	Propagation delay time, bus recessive input to high CRXD output	50	84	115	ns
t_{pDL}	Propagation delay time, bus dominant input to RXD low output	40	55	110	ns

6.9 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pRH}	Propagation delay time, bus recessive input to high CRXD output	Typical conditions: CANL = 1.5 V, CANH = 3.5 V, CAN_SLOPE_CTRL_EN 8'h0E[7] = 1b;	50	80	140	ns
	Propagation delay time, bus dominant input to RXD low output	See Figure 7-5	40	58	140	ns
t_{LOOP}	Loop Delay ⁽¹⁾	Typical conditions: $R_L = 60 \Omega$, $C_L = 100 \text{ pF}$, $C_{CRXD} = 15 \text{ pF}$, 4.5V \leq VCAN \leq 5.5 V, VCC1 $\pm 2\%$, CAN_SLOPE_CTRL_EN 8'h0E[7] = 0b		215		ns
t_{LOOP}	Loop Delay ⁽¹⁾	Typical conditions: $R_L = 60 \Omega$, $C_L = 100 \text{ pF}$, $C_{CRXD} = 15 \text{ pF}$, 4.5V \leq VCAN \leq 5.5 V, VCC1 $\pm 2\%$, CAN_SLOPE_CTRL_EN 8'h0E[7] = 1b		255		ns

Transmitter and Receiver Switching Characteristics (CAN)

$t_{Bit(Bus)2M}$	Transmitted recessive bit width @ 2 Mbps, intended for use with bit rates above 1 Mbps up to 2 Mbps	Typical conditions: $R_L = 60 \Omega$, $C_L = 100 \text{ pF}$, $C_{CRXD} = 15 \text{ pF}$; See Figure 7-6	440	525	ns	
$t_{Bit(Bus)5M}$	Transmitted recessive bit width @ 5 Mbps, intended for use with bit rates above 2 Mbps up to 5 Mbps		160	210	ns	
$t_{Bit(Bus)8M}$	Transmitted recessive bit width @ 8 Mbps, intended for use with bit rates above 5 Mbps up to 8 Mbps	Typical conditions: $R_L = 60 \Omega$, $C_L = 100 \text{ pF}$, $C_{CRXD} = 15 \text{ pF}$	80	135	ns	
$t_{Bit(RXD)2M}$	Received recessive bit width @ 2 Mbps,	Typical conditions: $R_L = 60 \Omega$, $C_L = 100 \text{ pF}$, $C_{CRXD} = 15 \text{ pF}$; See Figure 7-6	410	540	ns	
$t_{Bit(RXD)5M}$	Received recessive bit width @ 5 Mbps,		130	210	ns	
$t_{Bit(RXD)8M}$	Received recessive bit width @ 8 Mbps,	Typical conditions: $R_L = 60 \Omega$, $C_L = 100 \text{ pF}$, $C_{CRXD} = 15 \text{ pF}$	65	120	ns	
Δt_{Rec}	Receiver Timing symmetry @ 2 Mbps, intended for use with bit rates above 1 Mbps up to 2 Mbps	Typical conditions: $R_L = 60 \Omega$, $C_L = 100 \text{ pF}$, $C_{CRXD} = 15 \text{ pF}$	-60	-11	35	ns
	Receiver Timing symmetry @ 5 Mbps, intended for use with bit rates above 2 Mbps up to 5 Mbps		-30		10	ns

Switching Characteristics (LIN)

t_{rx_pdf}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	$R_{LRXD} = 2.4 \text{ k}\Omega$, $C_{RXD} = 20 \text{ pF}$ (See Figure 7-14)		6	μs	
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time (ISO/DIS 17987 Param 32)	Rising edge with respect to falling edge, ($t_{rx_sym} = t_{rx_pdf} - t_{rx_pdr}$), $R_{RXD} = 2.4 \text{ k}\Omega$, $C_{LRXD} = 20 \text{ pF}$ (Figure 7-14 ,)	-2	2	μs	
t_{LINBUS}	LIN wakeup time (minimum dominant time on LIN bus for wakeup)	See Figure 8-25	25	100	150	μs
t_{CLEAR}	Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See Figure 8-25	10	60	μs	

Fast Mode (LIN)

DR	Data Rate	$5.5 \text{ V} \leq \text{VSUP} \leq 18 \text{ V}$, $R_{LIN} = 500 \Omega$ and $C_{LIN(bus)} = 600 \text{ pF}$		200	kbps
t_{rx_pdr}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	$R_{LRXD} = 2.4 \text{ k}\Omega$, $C_{LRXD} = 20 \text{ pF}$ (See Figure 7-14)		5	μs
$t_{tx/f}$	LIN transmitter rise and fall time	$5.5 \text{ V} \leq \text{VSUP} \leq 18 \text{ V}$, $R_{LIN} = 500 \Omega$ and $C_{LIN(bus)} = 600 \text{ pF}$		1.5	μs

SPI Switching Characteristics

f_{CLK}	CLK, SPI clock frequency ⁽²⁾	Normal and standby modes, Sleep mode - if VCC1 is present		4	MHz
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6.9 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CLK}	CLK, SPI clock period ⁽²⁾		250		ns
t_{CLKR}	CLK rise time ⁽²⁾			40	ns
t_{CLKF}	CLK fall time ⁽²⁾			40	ns
t_{CLKH}	CLK, SPI clock high ⁽²⁾		125		ns
t_{CLKL}	CLK, SPI clock low ⁽²⁾		125		ns
t_{nCSS}	nCS chip select setup time ⁽²⁾		100		ns
t_{nCSH}	nCS chip select hold time ⁽²⁾		100		ns
t_{nCSD}	nCS chip select disable time ⁽²⁾		50		ns
t_{SISU}	Data in setup time ⁽²⁾		50		ns
t_{SIH}	Data in hold time ⁽²⁾		50		ns
t_{SOV}	Data out valid ⁽²⁾			80	ns
t_{RSO}	SO rise time ⁽²⁾			40	ns
t_{FSO}	SO fall time ⁽²⁾			40	ns

(1) Time span from signal edge on TXD input to next signal edge with same polarity on RXD output, the maximum of delay of both signal edges is to be considered.

(2) Specified by design

7 Parameter Measurement Information

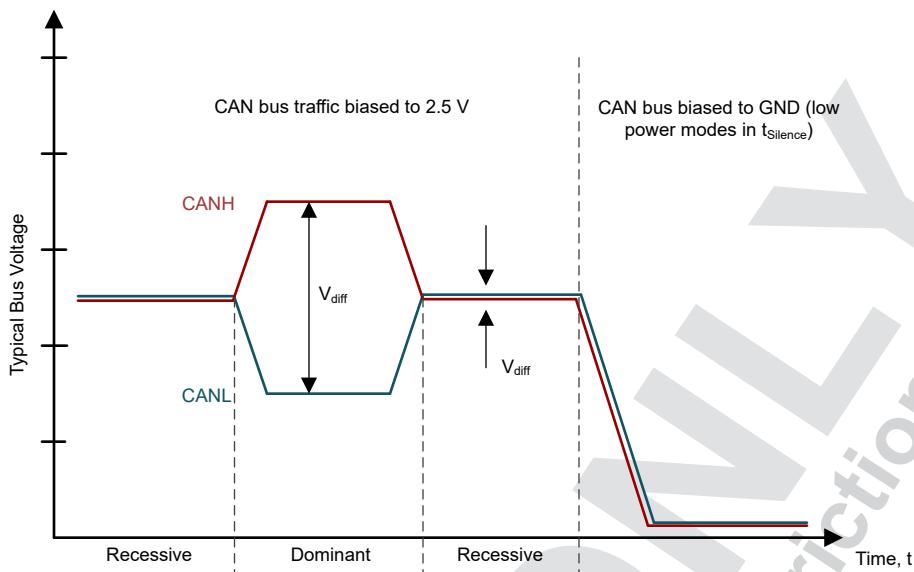
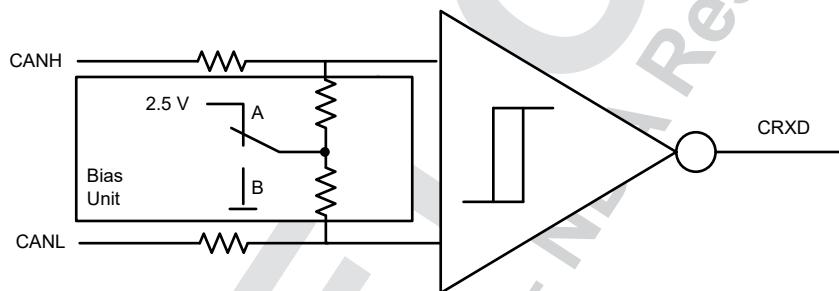


Figure 7-1. Bus States (Physical Bit Representation)



Note

A: Selective Wake, Normal, Listen Modes

B: Standby and Sleep Modes (Low Power)

Figure 7-2. Simplified Recessive Common Mode Bias Unit and Receiver

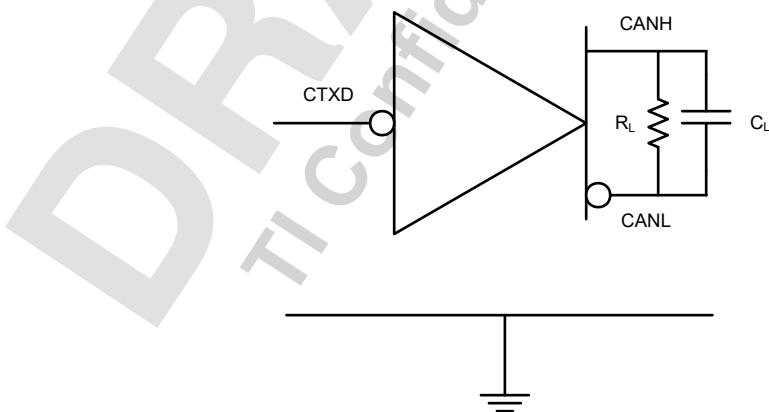


Figure 7-3. Supply Test Circuit

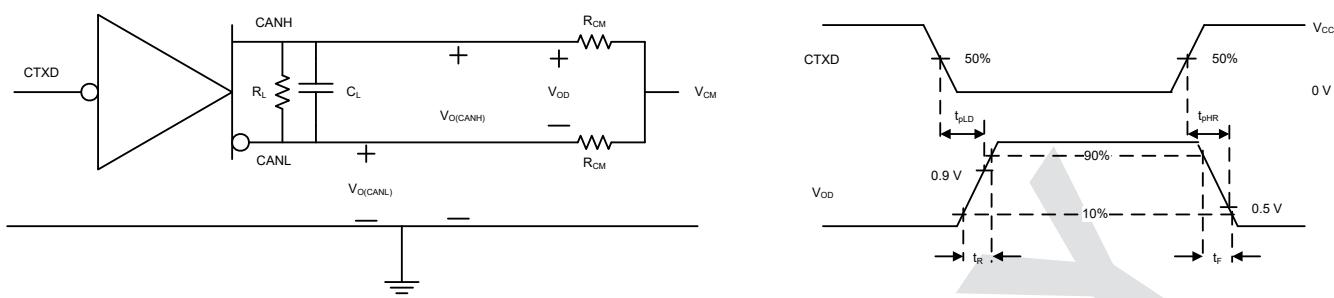


Figure 7-4. Driver Test Circuit and Measurement

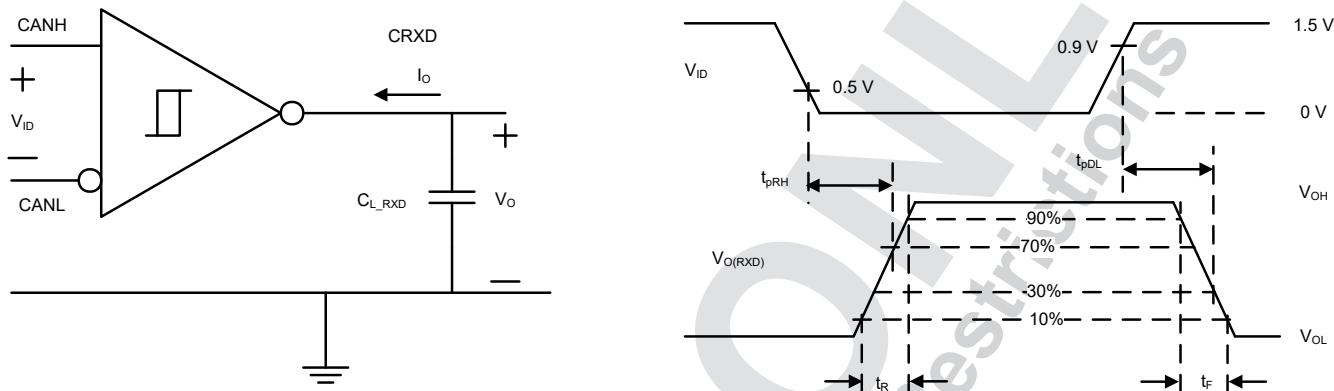


Figure 7-5. Receiver Test Circuit and Measurement

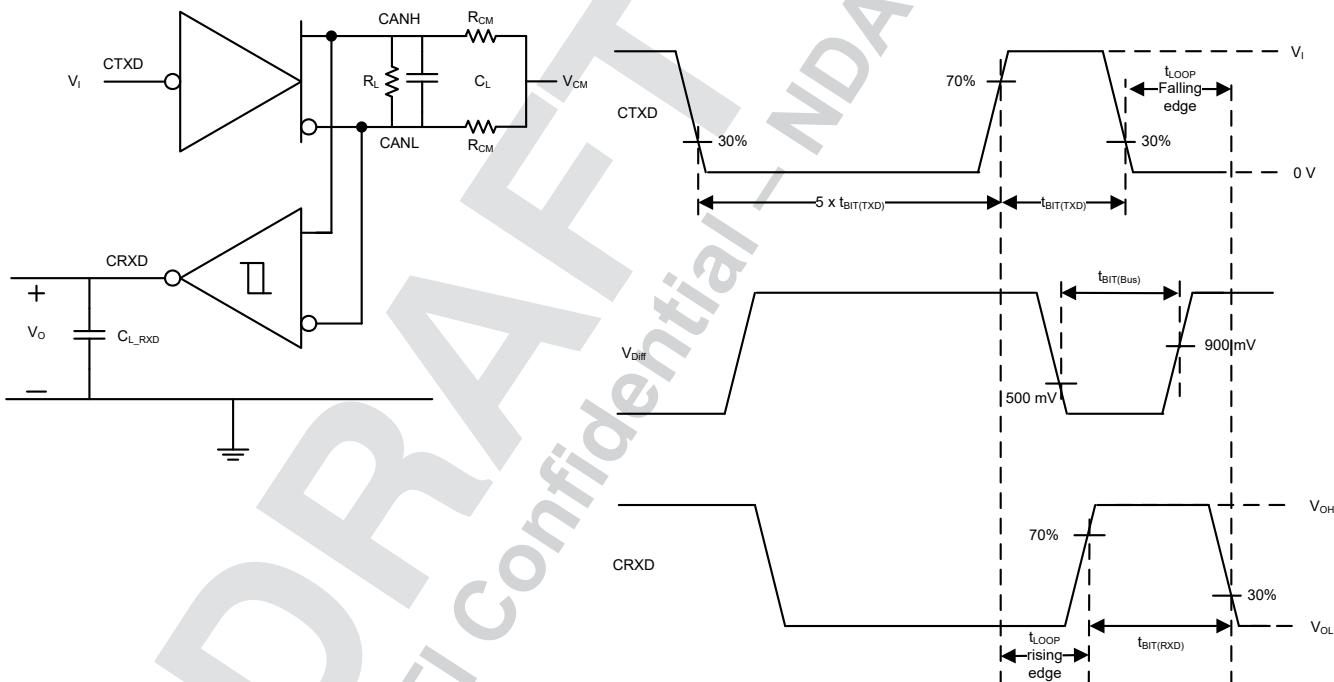


Figure 7-6. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

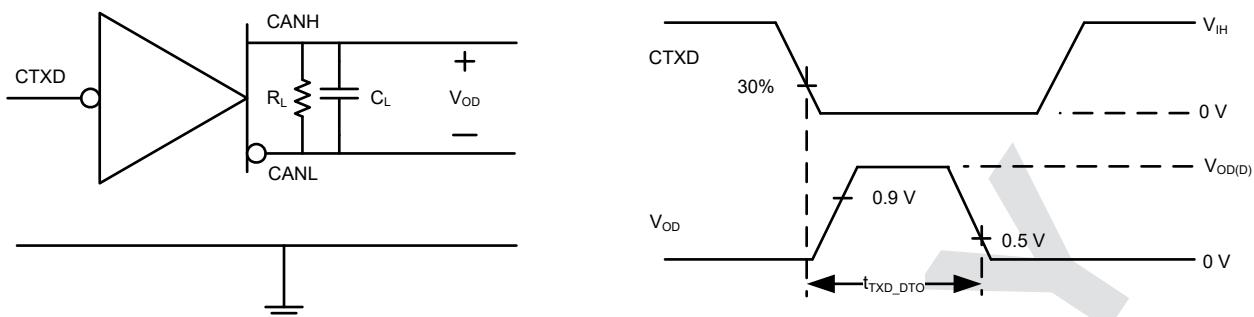


Figure 7-7. TXD Dominant Time Out Test Circuit and Measurement

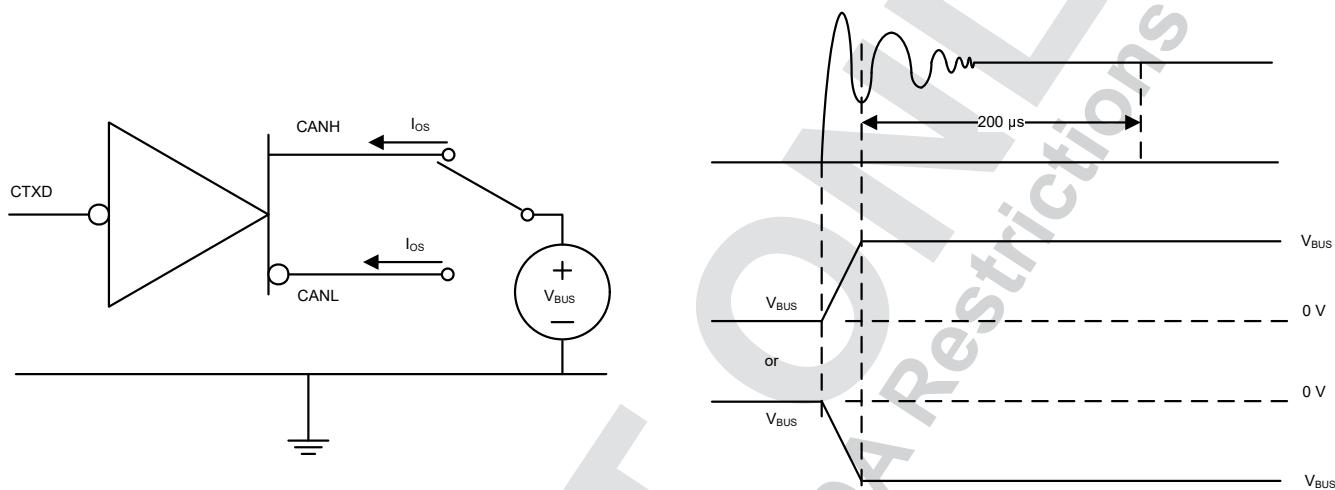


Figure 7-8. Driver Short-Circuit Current Test and Measurement

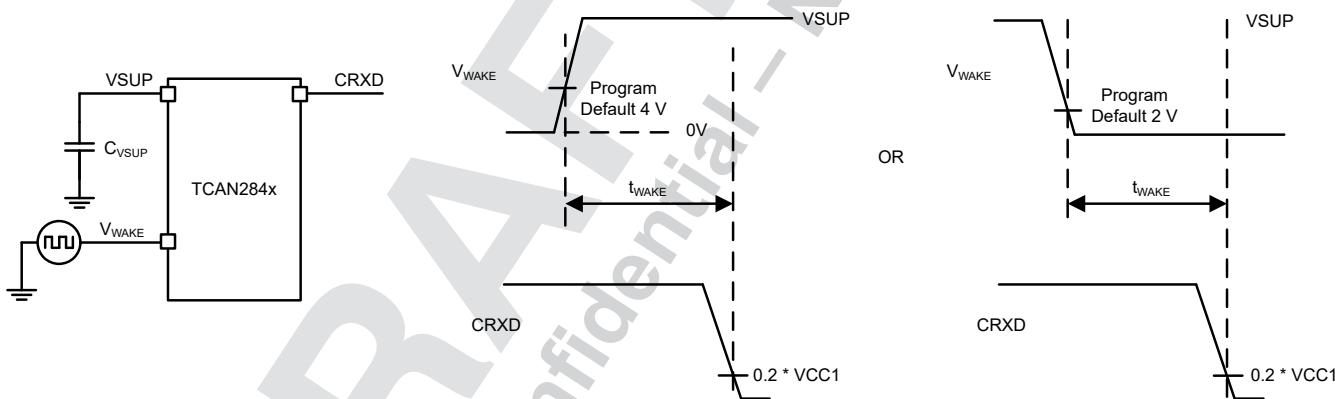


Figure 7-9. t_{WAKE} While Monitoring RXD Output

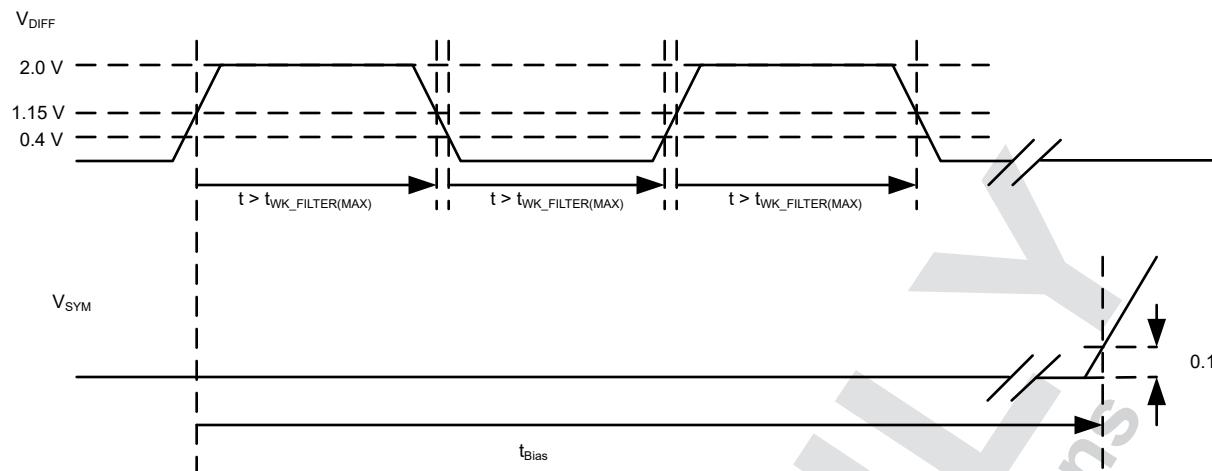


Figure 7-10. Test Signal Definition for Bias Reaction Time Measurement

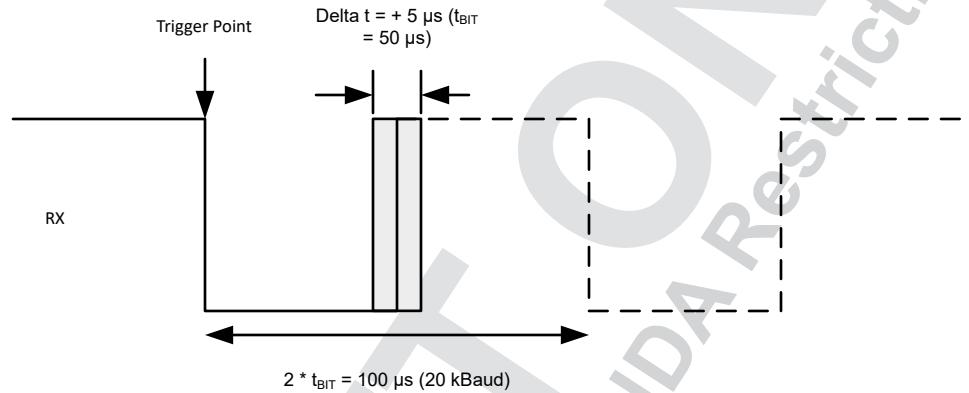


Figure 7-11. LIN RX Response: Operating Voltage Range

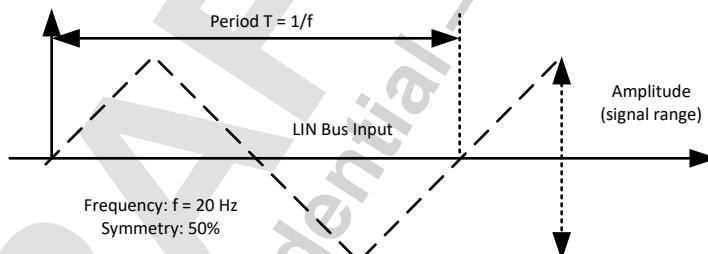


Figure 7-12. LIN Bus Input Signal

ADVANCE INFORMATION

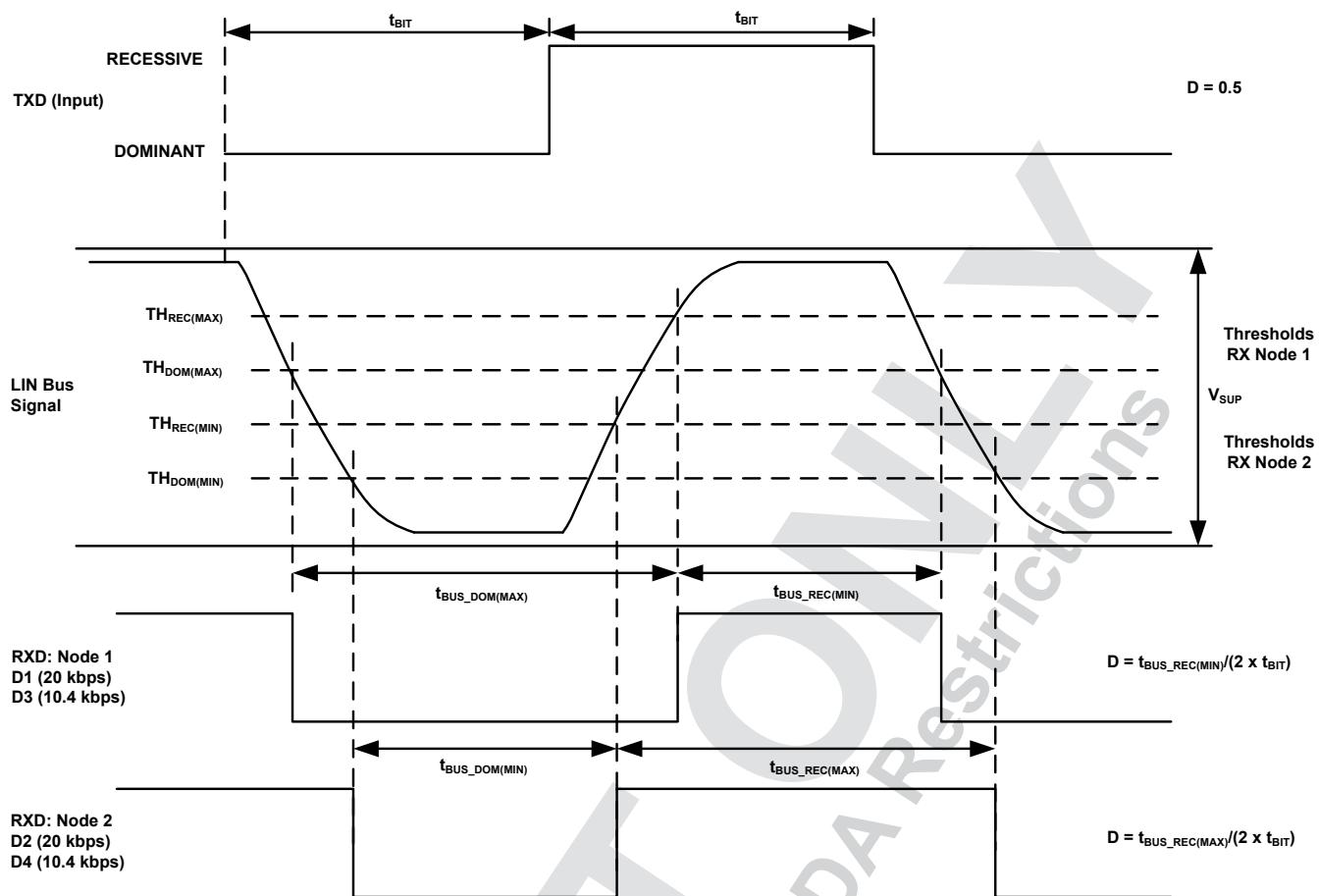


Figure 7-13. Definition of LIN Bus Timing

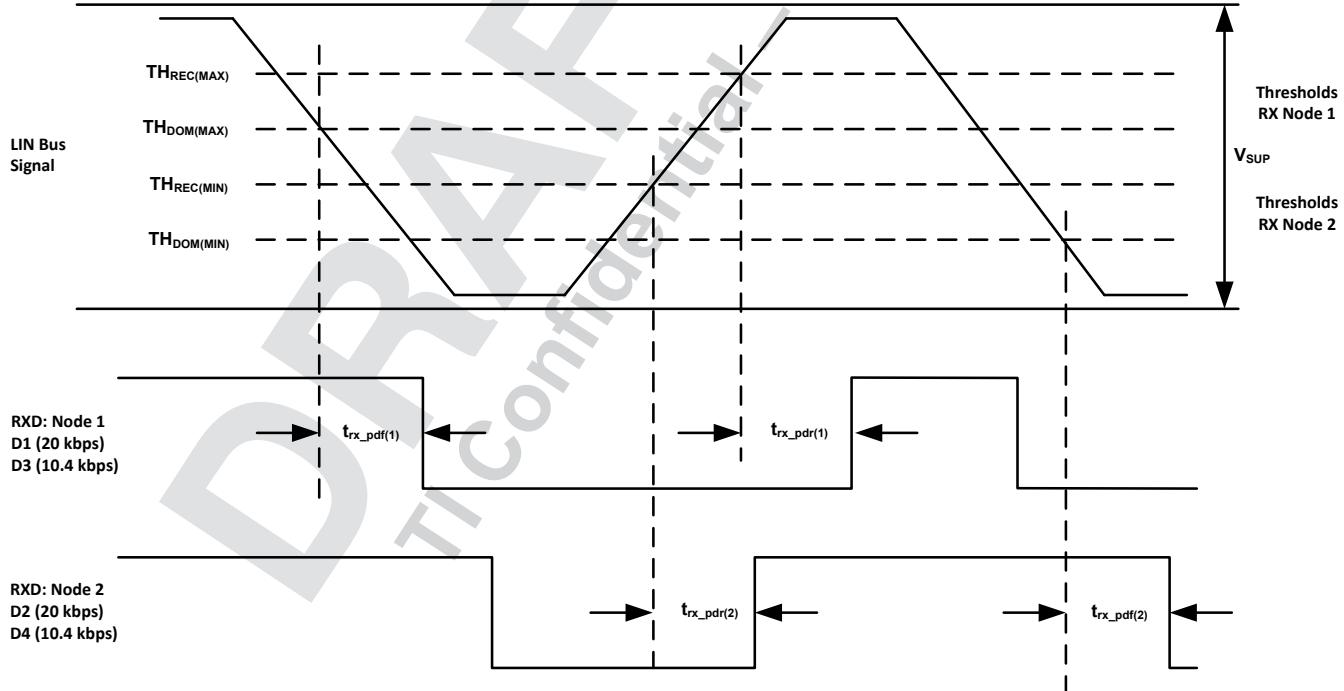


Figure 7-14. LIN Propagation Delay

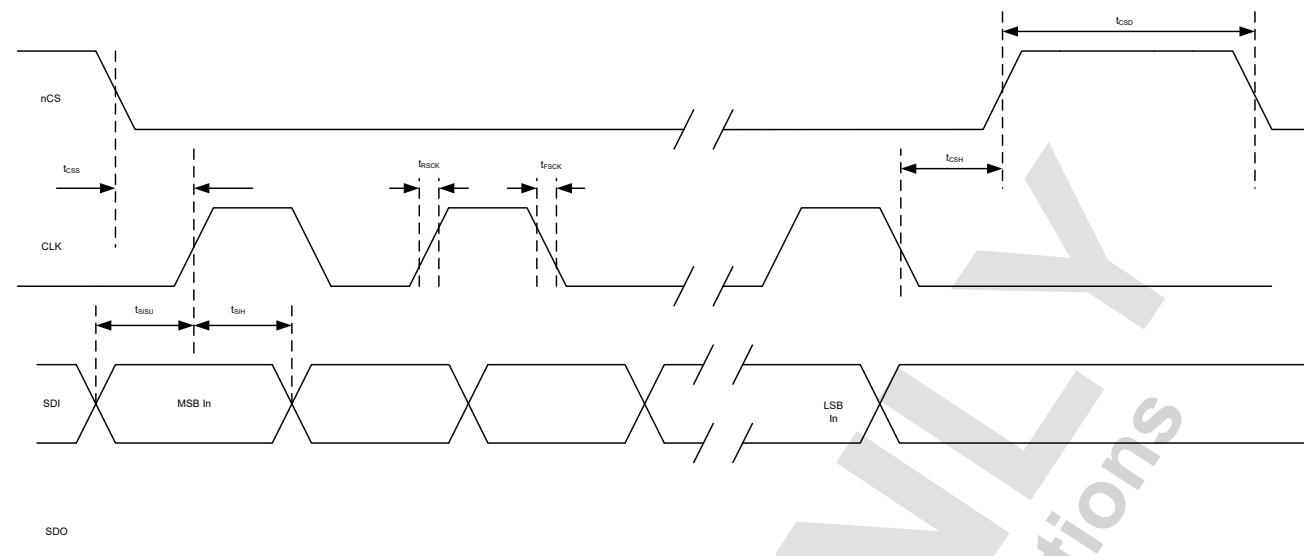


Figure 7-15. SPI AC Characteristic Write

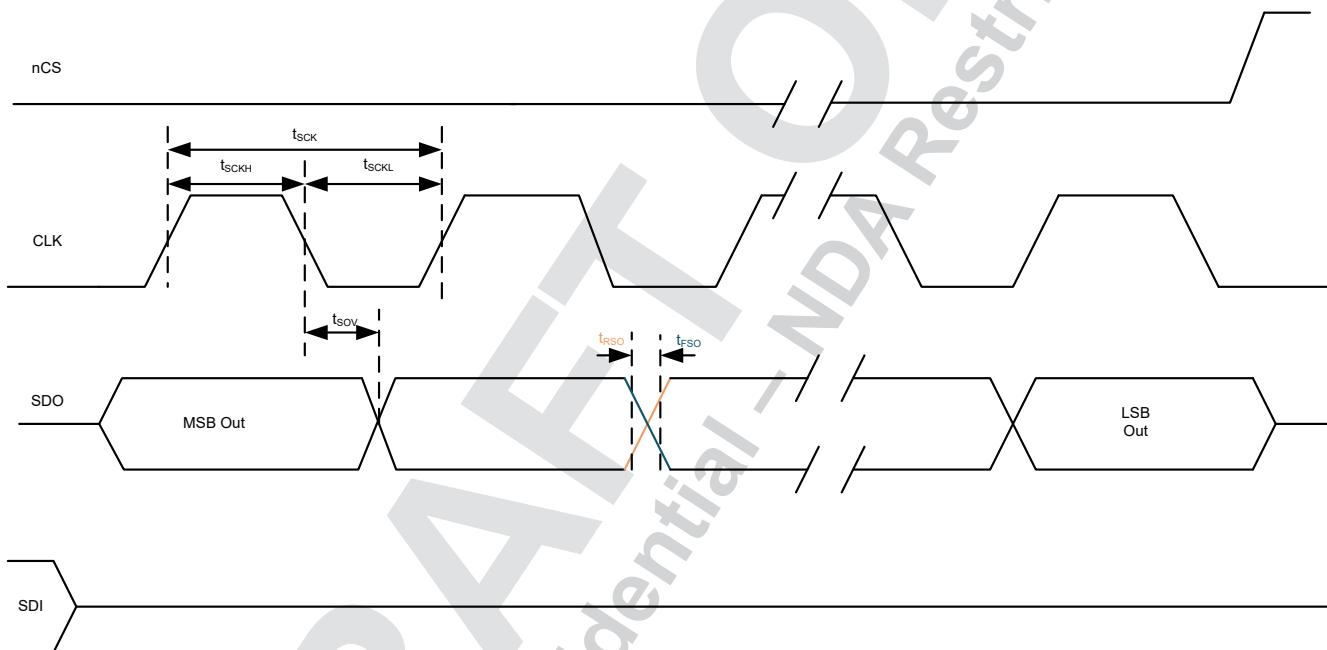
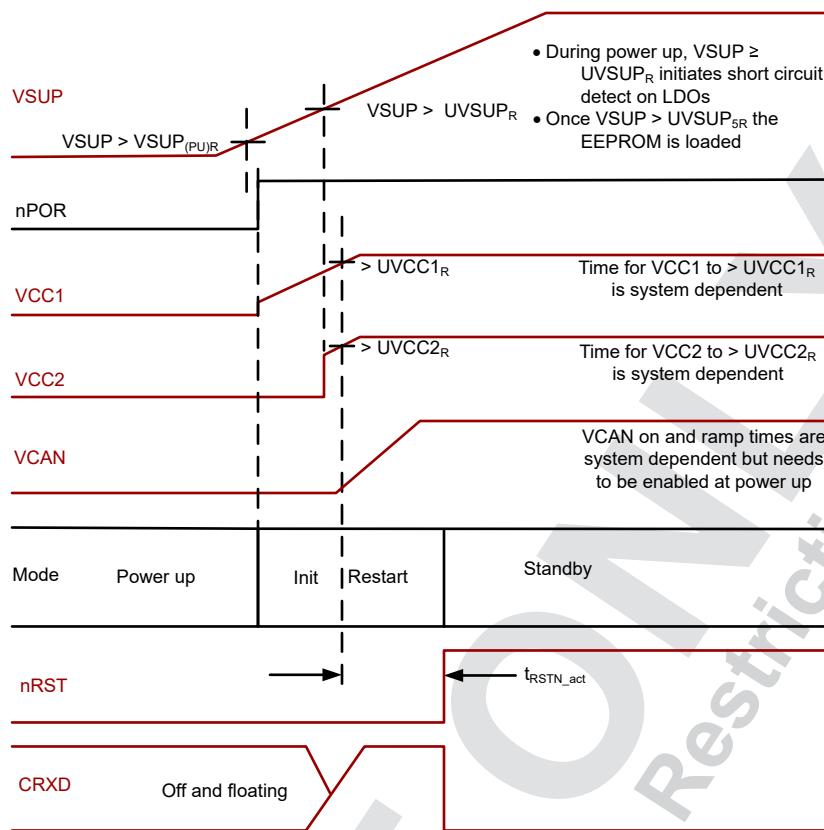
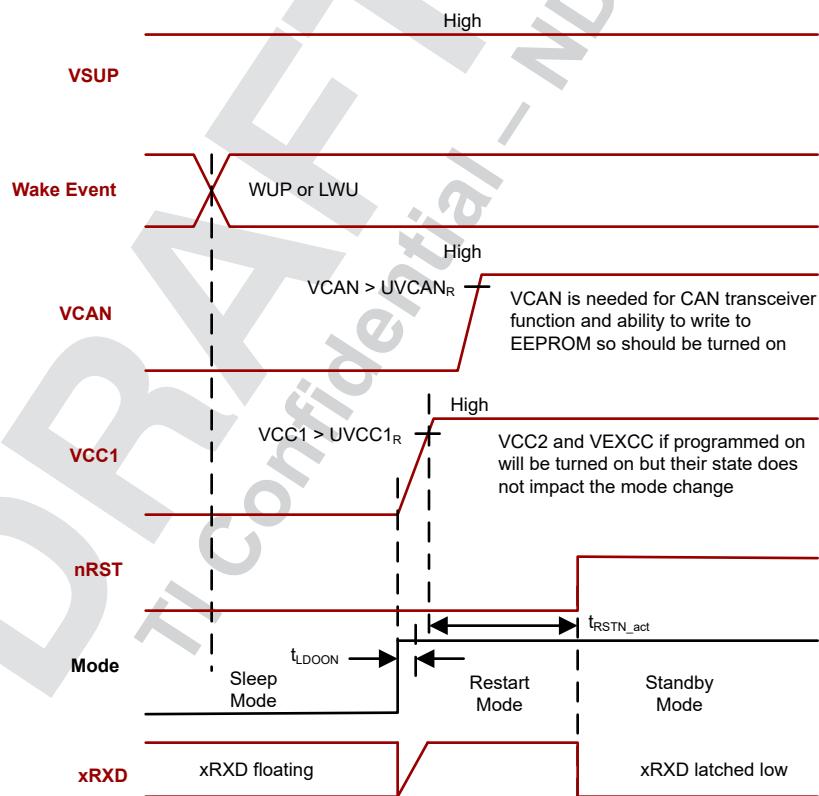


Figure 7-16. SPI AC Characteristic Read

ADVANCE INFORMATION

**Figure 7-17. Power Up Timing****Figure 7-18. Sleep to Restart Timing**

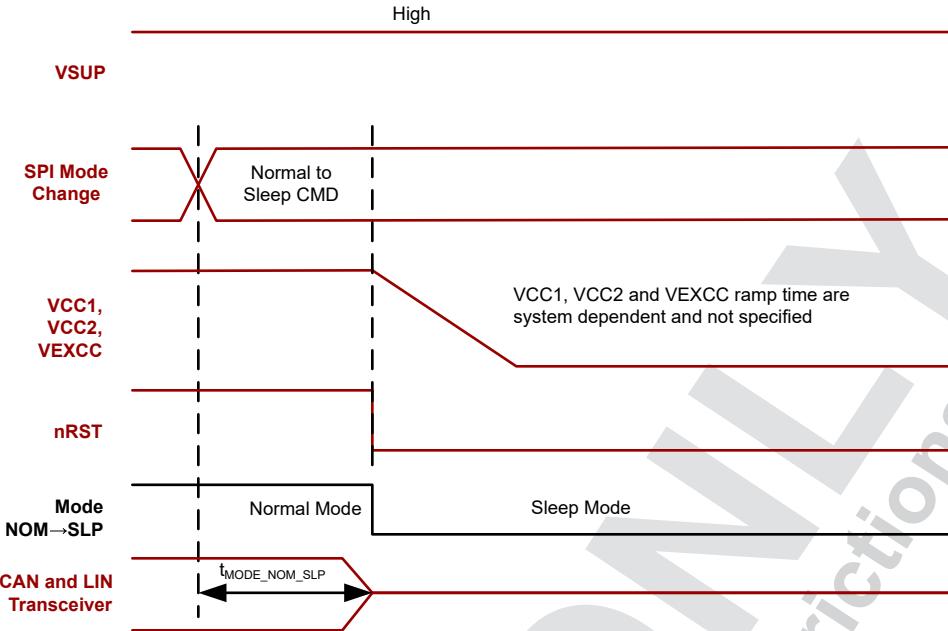


Figure 7-19. Normal to Sleep Timing

Note

The CAN and LIN transceiver can be independently controlled. The timing diagram shown shows the transceivers configured to change states based upon the mode.

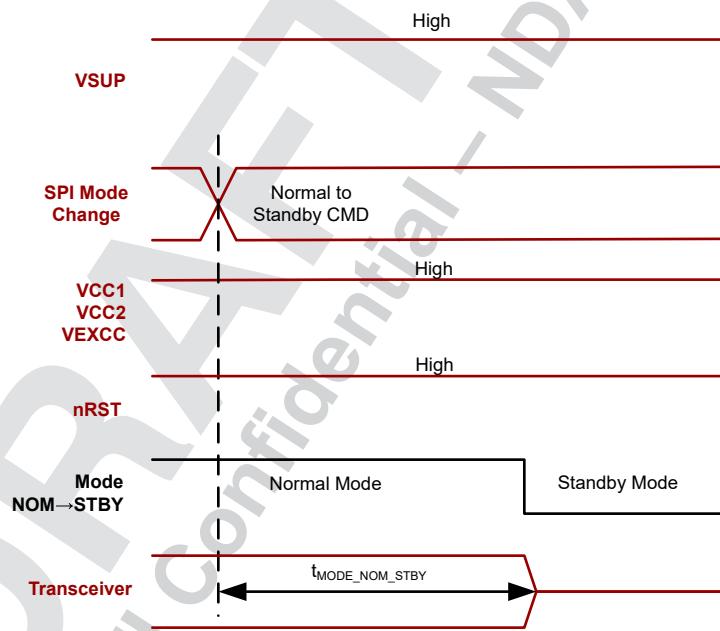


Figure 7-20. Normal to Standby Timing

Note

The CAN and LIN transceiver can be independently controlled. The timing diagram shown shows the transceivers configured to change states based upon the mode.

Note

The red signals are input or output of the TCAN284xx-Q1 and the black signals are internal to the TCAN284xx-Q1. This is for any timing diagram in the data sheet that has red and black colors.

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8 Detailed Description

8.1 Overview

The TCAN284xx-Q1 is a family of system basis chips (SBC) that integrate the CAN FD transceiver. The CAN FD transceiver supports data rates up to 5 Mbps while meeting the high-speed CAN physical layer standards: ISO 11898-2:2016. The TCAN2846x-Q1 and TCAN2847x-Q1 integrate a LIN transceiver that supports data rates up to 200 kbps when slope control is disabled and programmed for fast mode. The LIN transceiver physical layer transceiver is compliant to LIN 2.2 A and ISO/DIS 17987-4 and SAE J2602 standards. These data rates support end of line programming. The TCAN2845x-Q1 and TCAN2847x-Q1 supports selective wake up on dedicated CAN-frames. The device can also wake up via remote wake up using CAN bus implementing the ISO 11898-2:2016 Wake Up Pattern (WUP). The TCAN284xx-Q1 supports 3.3 V and 5 V processors based upon VCC1 voltage. The device has a Serial Peripheral Interface (SPI) that connects to a local microprocessor for configuration. The SPI interface supports clock rates up to 4 MHz. The TCAN284xx-Q1 provide a software development pin to help implementer with development. In this mode the watchdog is still active but only sets a flag.

The TCAN284x3-Q1 variant of the devices provide a VCC1 of 3.3 V output capable of supporting 250 mA. The TCAN284x5-Q1 variant of the device provides a VCC1 of 5 V output capable of supporting 250 mA, VCC1. These devices have a separate 5 V LDO, VCC2, that provides up to 200 mA externally. The ability to control an external PNP power transistor is provided to support up to 350 mA with output voltage from 1.8 V, 2.5 V, 3.3 V and 5 V if needed. VCC2 and VEXCC are short to battery protected. A 5 V input supply is needed for the CAN FD transceiver, VCAN.

The CAN bus has two logical states during operation: recessive and dominant. See [Figure 7-1](#) and [Figure 7-2](#).

Recessive bus state is when the bus is biased to a common mode of about 2.5 V via the high resistance internal input resistors of the receiver of each node on the bus across the termination resistors. Recessive is equivalent to logic high and is typically a differential voltage on the bus of almost 0 V. Recessive state is also the idle state.

Dominant bus state is when the bus is driven differentially by one or more drivers. Current is induced to flow through the termination resistors and generate a differential voltage on the bus. Dominant is equivalent to logic low and is a differential voltage on the bus greater than the minimum threshold for a CAN dominant. A dominant state overwrites the recessive state.

During arbitration, multiple CAN nodes may transmit a dominant bit at the same time. In this case, the differential voltage of the bus is greater than the differential voltage of a single driver.

Transceivers with low power Standby Mode have a third bus state where the bus terminals are weakly biased to ground via the high resistance internal resistors of the receiver. See [Figure 7-1](#) and [Figure 7-2](#).

8.2 Functional Block Diagram

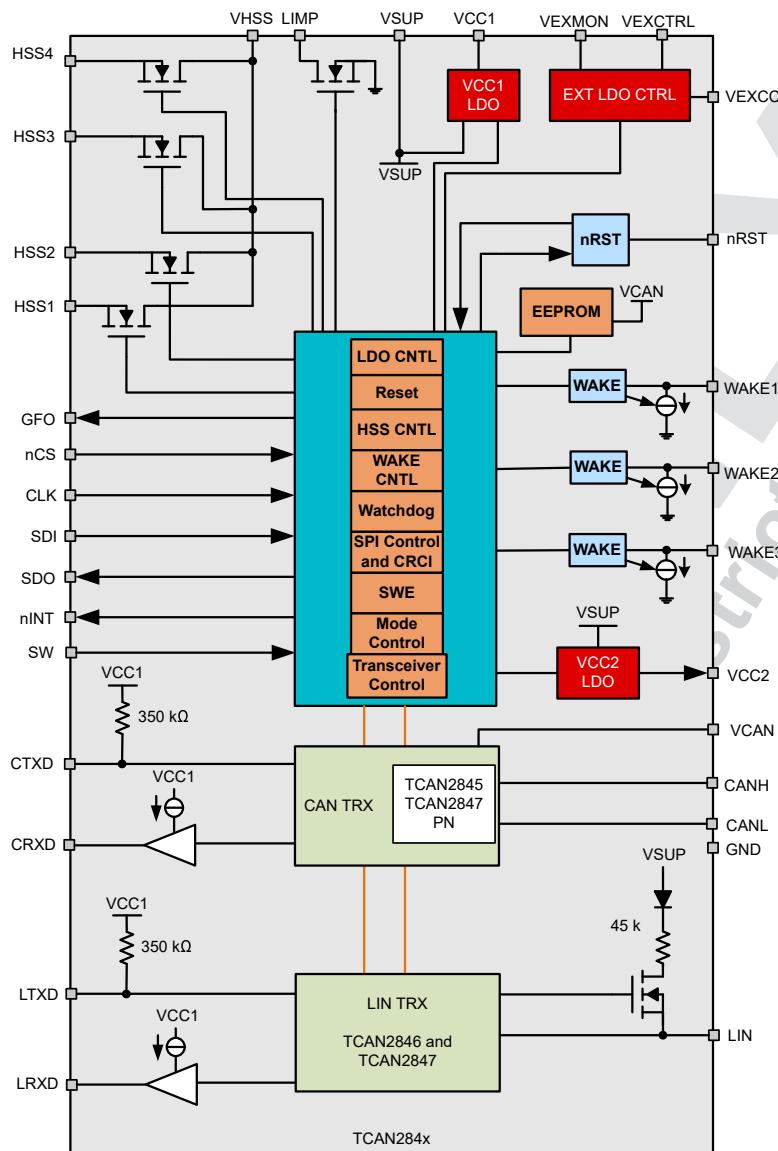


Figure 8-1. TCAN284x Functional Block Diagram

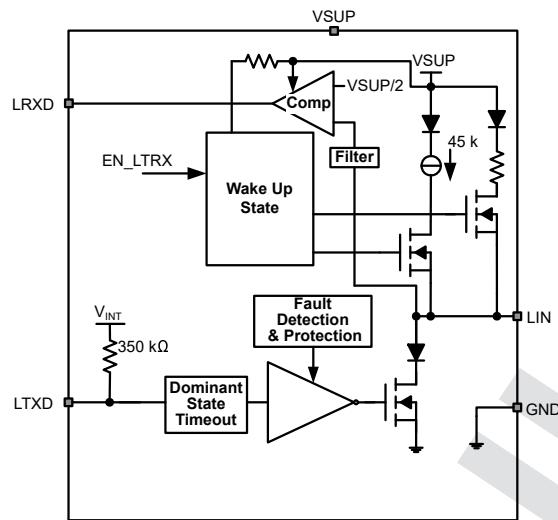


Figure 8-2. TCAN284xx-Q1 LIN Transceiver Block Diagram

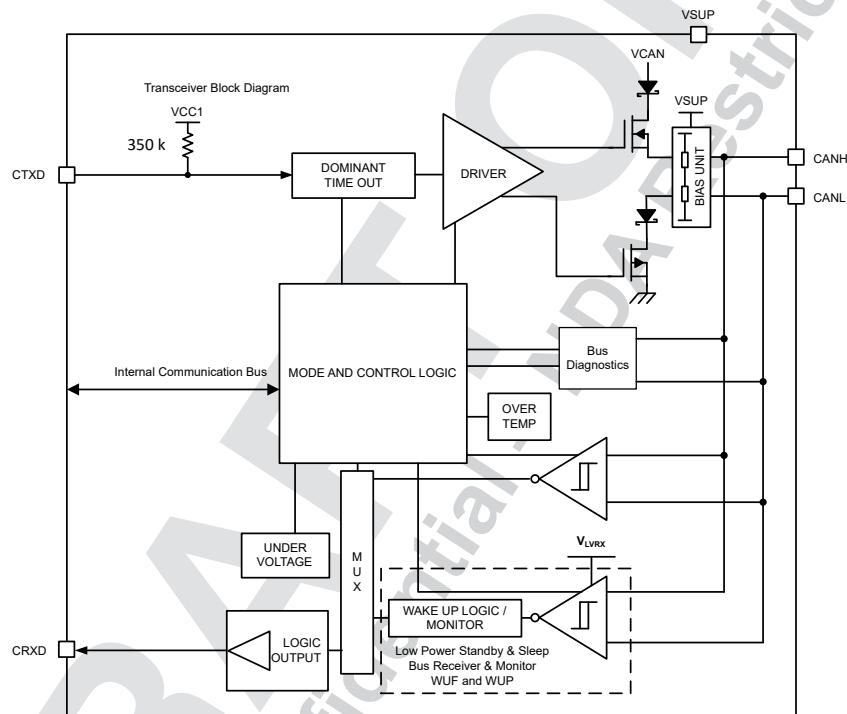


Figure 8-3. CAN Transceiver Block Diagram

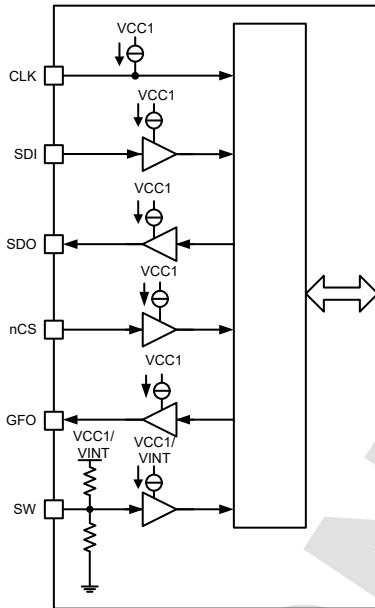


Figure 8-4. Digital Input/output Block Diagram

8.3 Pin Description

8.3.1 VSUP Pin

VSUP is the power supply pin. VSUP is connected to the battery through an external reverse battery-blocking diode. The VSUP pin is a high-voltage-tolerant pin. Decoupling capacitor with a value of 100 nF is recommended to be connected close to this pin to better the transient performance. The TCAN284xx-Q1 family of devices are designed to function with an extended VSUP range, 4.5 V to 28 V, with parametric performance and LDO regulation between 5.5 V and 28 V. If there is a loss of power at the ECU level, the device has extremely low leakage from the CAN and LIN pins, which does not load the bus down. This is optimal for systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

There are three VSUP voltage levels monitored by the device, power on reset ($VSUP_{(PU)R/F}$) and undervoltage ($UVSUP_{33R/F}$ and $VSUP_{5R/F}$), where both ramping up and down values are monitored. UVSUP is also broken down to two different thresholds depending upon VCC1 voltage level. UVSUP is covered in [Section 8.6.9](#). For power up, [Figure 8-5](#) provides information on what voltage levels and functions are available and when.

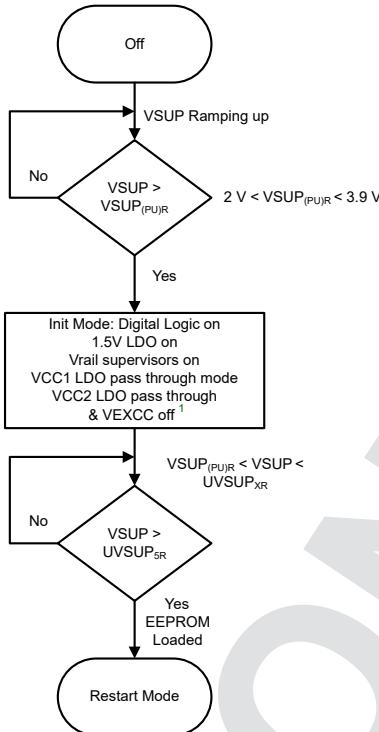


Figure 8-5. Power Up State Diagram

Note

- After initial powerup and configuration saved to EEPROM, the LDOs may not perform as shown, example would be these are programmed off
- VEXCC will always be off until EEPROM has been loaded and then it will behave as configured
- VCAN must be > UVCAN in order to write to EEPROM and not considered here

8.3.2 VHSS

The VHSS pin is a dedicated supply pin for the high-side switches outputs. Over-voltage and under-voltage is monitored for this pin. An over-voltage event will be indicated by interrupt register 8'h5A[2], OVHSS. An under-voltage event will be indicated by interrupt register 8'h5A[0], UVHSS.

8.3.3 VCAN Pin

The VCAN pin is the 5 V supply input for the CAN FD transceiver. VCAN is monitored for under-voltage events, UVCAN. When VCAN is present and not in a fault state, register 8'h4F[1], VCAN_STATUS, will indicate this by being set to 1b. For the CAN FD transceiver to be available VCAN must be present. This pin is also used for EEPROM writing so must be on for this function to happen.

8.3.4 VCC1 Pin

The VCC1 output pin sources either 3.3 V or 5 V to external circuits with up to 250 mA of current. The VCC1 pin is capable of sinking either 10 μA or 100 μA of current depending upon the setting of register 8'h0D[3] and is active when VCC1 is on. An external capacitor to ground is required on this pin. There are three monitors on VCC1, under-voltage (UVCC1), over-voltage (OVCC1) and short to ground (VCC1_{SC}). When load sharing with VEXCC, VCC1 fault monitors are utilized for both. VCC1 is the main LDO output and sets the digital IO voltage levels. Any fault on VCC1 will cause a state change.

8.3.5 VCC2 Pin

The VCC2 pin provides 5 V with up to 200 mA to external circuitry and requires an external capacitor to ground. This pin is short to battery protected and if connected to VCAN or an external CAN transceiver should not be

taken off board where a short to battery can take place. There are three monitors on VCC2, under-voltage (UVCC2), over-voltage (OVCC2) and short to ground (VCC2_{SC}). When these faults are detected an interrupt is provided and the LDO may or may not be turned off. No mode change will take place. When VCC2 is on and not in a fault state, register 8'h4F[2], VCC2_STATUS, will indicate this by being set to 1b.

8.3.5.1 V_{CC2} Short to Battery Protection

The output stage of V_{CC2} is short to battery protected. No inverse current flow if external voltage is at or above OVCC2. This protection is for 28 V with the ability to handle up to 40 V for less than 300 ms. If the device powers up with a short to battery that is above 28 V for more than 300 ms, the device can be damaged or reliability issues can occur.

8.3.6 nRST Pin

The nRST pin is a bi-directional open-drain low side driver that serves several functions, an LDO monitor output for under-voltage events, an indicator to the processor that restart has been entered and a device input reset.

nRST is connected to VCC1 through a 30 kΩ resistor, see [Figure 8-6](#). When a VCC1 under-voltage (UVCC1) event takes place, the device will transition to restart mode and nRST pin will be latched low. nRST pin behavior is shown in [Figure 8-7](#) based upon the SBC mode of operation and how it was entered.

When the device enters restart mode this pins behavior depends upon the method of entry. If entering restart mode turns on the LDO the nRST is latched low until the device enters standby mode. This will be t_{RSTN_act} after the LDO(s) exceed their rising under-voltage level. If the LDO is already on when entering restart mode, the pin will be pulled low for t_{NRST_TOG}. After this time the device will transition to standby mode and nRST returns to high.

The pin can determine when an input pulse of t_{NRSTIN} is applied causing the device to reload EEPROM, set other registers to factory default and enters restart mode.

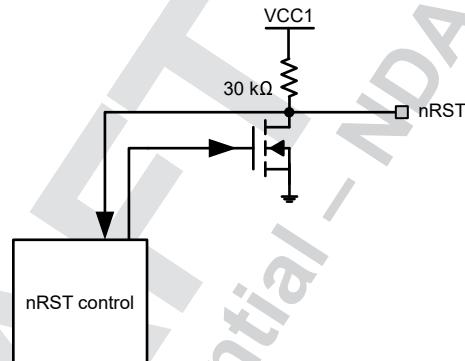


Figure 8-6. nRST Block Diagram

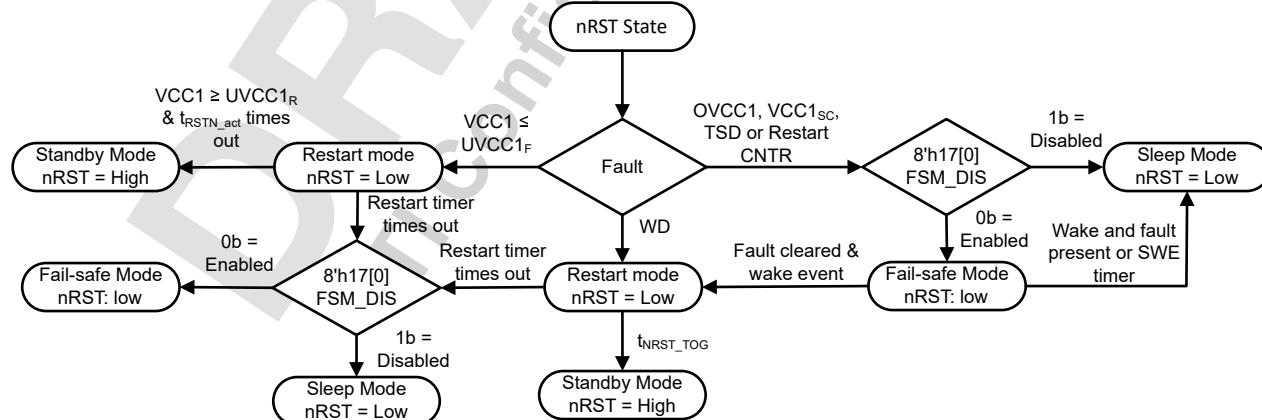


Figure 8-7. nRST State Diagram

8.3.7 VEXMON, VEXCTRL and VEXCC Pins

These pins control an external PNP power transistors with β between 50 and 500 to support higher currents and wider voltage needs. The TCAN284x-Q1 can support 1.8 V, 2.5 V, 3.3 V and 5 V output with up to 350 mA.

The voltage is selected using SPI register 8'h0D[2:0] and defaults to 1.8 V. There are three monitors on VEXCC, under-voltage (UVEXCC), over-voltage (OVEXCC) and short to ground (VEXCC_{SC}). The external PNP will not be turned on until register 8'h0D[5:4] is configured and is default off. When VEXCC is on and not in a fault state, register 8'h4F[3], VEXCC_STATUS, will indicate this by being set to 1b. When load sharing is selected, the device will automatically configure the voltage level to match the VCC1 voltage and follow the programming state of VCC1.

For stability, an external capacitance of $\geq 4.7 \mu\text{F}$ with an ESR between 1 mΩ and 500 mΩ is needed on the VEXCC pin to ground. When external PNP load shares with the VCC1 pin to provide higher current. To limit the current through the PNP transistor, one external resistor is needed. The shunt resistor, Rshunt, is between VSUP and VEXMON and serves two purposes depending upon configuration. When used as an stand-alone configuration, see [Figure 8-8](#), Rshunt set the current limit for the PNP FET. The value for Rshunt is typically 500 mΩ but is dependent upon the current limit needs. The value of this resistor is determined by the VEXMON threshold divided by the current limit. The typical value was determined by 0.25V/500mA. When configured for load sharing with VCC1, see [Figure 8-9](#), it sets the ratio of current between VEXCC and VCC1. See [Equation 1](#) and [Equation 2](#) to determine how to calculate the Rshunt value.

$$\text{Ratio} = \left(\frac{IVEXCC}{IVCC1} \right) \quad (1)$$

$$Rshunt = \left(\frac{8.824}{\text{Ratio}} \right) - \left(\left(\frac{1 + \text{Ratio}}{\text{Ratio}} \right) \times \left(\frac{0.8}{Iload} \right) \right) \quad (2)$$

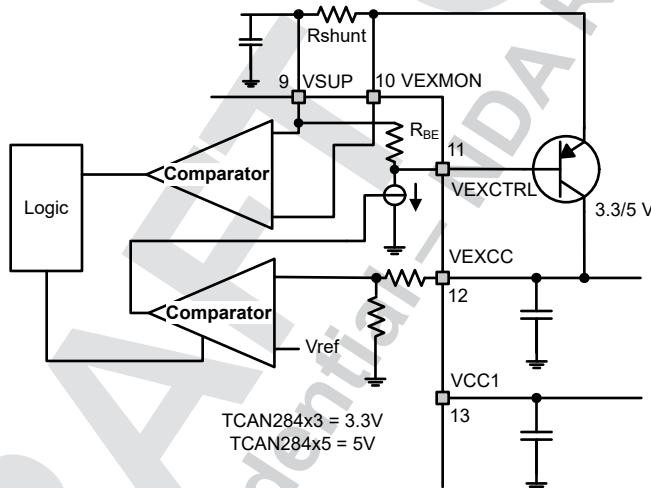
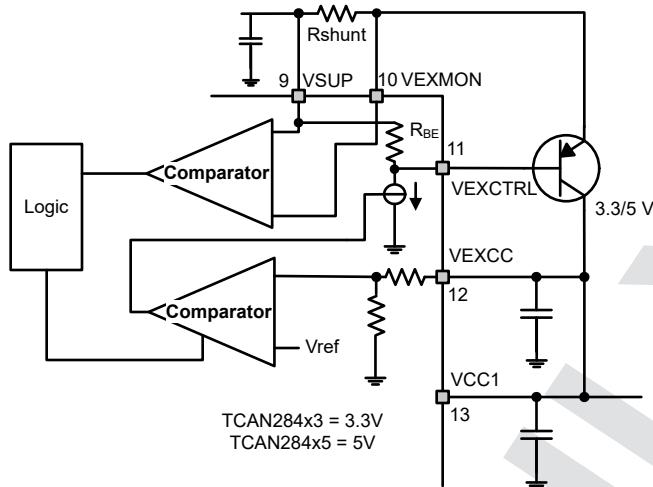
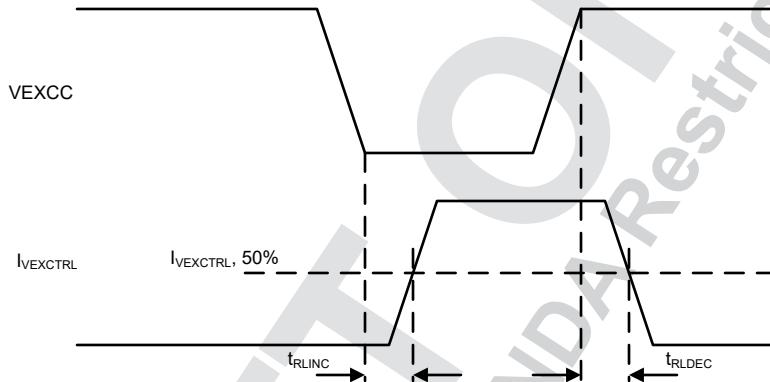


Figure 8-8. Stand-alone External PNP Example

**Figure 8-9. External PNP Example with Load Sharing****Figure 8-10. VEXCC versus $I_{VEXCTRL}$ Timing Diagram****Note**

The external PNP transistor power handling capabilities are application specific and must therefore be designed according to the selected PNP device along with the PCB properties to prevent thermal damage as the SBC is not able to make sure the thermal protection of the external PNP transistor.

8.3.8 GND

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the VSUP below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has extremely low leakage from the CANL/H and LIN pins, which does not load the bus down. This is optimal for CAN and LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered.

8.3.9 LIMP Pin

The LIMP pin is for the limp home function and is an open-drain, active low, output. It is used for a limp home mode if the watchdog has timed out causing a reset. The pin should be pulled up with an external resistor connected to the battery supply, VSUP. For the LIMP pin to be turned off, the watchdog error counter must reach zero from correct input triggers. If programmed any event that triggers the fail-safe mode will also turn on the LIMP pin.

8.3.10 HSS1, HSS2, HSS3 and HSS4 Pins

These pins are based upon a high-side switch configuration supporting up to 100 mA load with 60 mA being typical with a 14 V VHSS. When a over current is detected there is a filter time, t_{OCFLTR} , to determine if

over current is valid. If valid there is a shut off time, t_{COFF} , time for the HSS to shut off. The pins can be programmed to support a 200 Hz or 400 Hz 10-bit PWM. PWM1, PWM2, PWM3 or PWM4 can be assigned to the HSSx. HSS4 can be configured to utilize one of two timers that allows it to work with WAKE1, WAKE2 and WAKE3 pins supporting cyclic sensing. Cyclic sensing is used for sleep mode thus reducing sleep mode current. HSS1 and HSS2 can be connected together and synchronized by configuring registers 8'h1F[6] = 1b. The timing mechanism for the synchronized pair will be determined by the selected HSS1 timing configuration by register 8'h1E[6:4], HSS1_CNTL. This will allow higher current loads to be used. The high side switches are monitored for open loads and over-current. The VHSS pin is also monitored for a high-side switch over-voltage condition based upon OVHSS thresholds. If VHSS exceeds this threshold the high-side switches will be turned off. When VHSS drops below this threshold the high-side switches will automatically be enabled to its previous state. Register 8'h4F[7:6] disables the high-side switches from automatically shutting down due to an OVHSS or UVHSS event. HSS_OV_UV_REC, register 8'h4F[5] = 1b enables the high-side switches to go back to the programmed state. If HSS_OV_UV_REC = 0b, the high-side switches will stay off due to an over-voltage or under-voltage event on VHSS.

To configure HSS3 and HSS4, register 8'h4D[7:0] is used. To configure PWM3 and PWM4 SBC_CONFIG0 register 8'h0C[5:4] = 01b. and then use the PWM1 and PWM2 configuration registers to program them. This changes the PWM1 control registers to PWM3 and the PWM2 control registers to PWM4. After configuring the registers it is best to change 8'h0C[5:4] = 00b thus converting the PWM registers back to PWM1 and PWM2.

Note

- For resistive loads an external capacitor to ground in not required.
 - For inductive loads an external 100 nF capacitor to ground is needed.
 - When using the 10-bit PWM with the HSS it is possible to select values that are unrealizable due to the on and off times of the switch. An example of this would be 00 0000 0001b
 - When HSS1 and HSS2 are synchronized and connected together, open load is disabled
-

8.3.11 WAKE1, WAKE2 and WAKE3 Pins

WAKE1, WAKE2 and WAKE3 pins are ground biased local wake up (LWU) input pins that are high voltage tolerant. This function is explained further in [Section 8.4.6.1.3](#) section. The pins can be both rising and falling edge trigger, meaning it recognizes a LWU on either edge of WAKE pin transition. The pin can be configured to accept a pulse, see [Figure 8-28](#) for timing diagram of this behavior. The WAKE pins are default enabled but can be disabled by using register 8'h2A[7:5], WAKE_PIN_SET, to turn off individual ones. Register 8'h11[7:6] sets the method the pins will utilize to register a wake event. These pins can be configured for cyclic sensing wake, see [Section 8.4.6.1.3.2](#), or static wake.

The WAKE pins have four individual thresholds that can be set for a state change.

- Register 8'h12[1:0], WAKE1_LEVEL
 - Register 8'h2B[5:4], WAKE2_LEVEL
 - Register 8'h2B[1:0], WAKE3_LEVEL
-

Note

If WAKE_x_LEVEL = 10b or 11b is selected and uses static wake, the system designer needs to make sure that VSUP does not cross the wake pin threshold otherwise a false wake up can take place. Normal undervoltage events on VSUP will not cause this to take place.

Register 8'h2A[4:0], MULTI_WAKE_STAT, provides which WAKE pin or combination of WAKE pins caused the LWU event. The individual status of the pins, low or high, can be read via SPI in any mode that SPI is available.

- Register 8'h11[5], WAKE1_STAT
- Register 8'h2B[6], WAKE2_STAT
- Register 8'h2B[2], WAKE3_STAT

8.3.12 CTXD and LTXD Pins

The CTXD and LTXD are the inputs from the processor that controls the state of the CAN FD and LIN busses. When TXD is low, the bus output is dominant. When TXD is high, the bus output is recessive which is a logic 0.

The TXD input structure is compatible with processors with 3.3 V to 5 V V_O . TXD has an internal pull-up resistor to VCC1. The bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state time-out timer.

For TCAN2844-Q1 and TCAN2845-Q1 LTXD pin is not present and is a NU for not used pin. This pin should not be connected on the board.

8.3.13 CRXD and LRXD Pins

These pins are the outputs to the processor from the CAN FD and LIN busses. When a CAN wake event takes place the CRXD pin is latched low. When a LIN wake event takes place the LRXD is latched low. CRXD is the LWU indicator for the system. LRXD will only latch low when a LIN bus WUP takes place. The CRXD and LRXD pins are push-pull buffers and as such an external pull-up is not needed. In restart mode, the RXD pins are driven high. When VCC1 is $>$ UVCC1 for t_{RSTN_act} , the device will automatically transition to standby mode. The RXD pins are then pulled low to indicate a wake up request. The CRXD pin can be programmed to toggle low/high with a pulse width of t_{TOGGLE} , see [Section 8.4.6.1.3.1](#) as an example of this feature.

For TCAN2844-Q1 and TCAN2845-Q1 LRXD pin is not present and is a NU for not used pin. This pin should not be connected on the board.

8.3.14 SDO Pin

The SPI data output (SDO) function provides the requested data from the device to the processor. Upon nCS state changing states to low the global interrupts information is placed SDO.

8.3.15 nCS Pin

The nCS pin is the SPI chip select pin. When pulled low and a clock is present, the device can be written to or read from.

8.3.16 CLK Pin

The CLK pin is the SPI clock to the TCAN284xx-Q1. The max clock rate is 4 MHz.

8.3.17 SDI Pin

When nCS is low, this pin is the SPI data input pin used for programming the device or requesting data.

8.3.18 nINT Pin

This pin is the interrupt output pin to the processor. When the TCAN284xx-Q1 requires the attention of the processor, this pin is pulled low. After the interrupt is cleared and the nINT pin is released back to high a 1ms delay will take place before another interrupt can take place and latch the nINT pin low again.

8.3.19 SW Pin

During debug or development this pin can be used to disable the watchdog actions. When the pin is active, the device will expect normal WD triggers, but will ignore any mode changes or actions outside of setting the watchdog failure interrupt flag and incrementing and decrementing the watchdog counter. When the pin is released, the flags will self-clear and the watchdog counter will either go back to default or programmed value. The pin is default active high but can be configured active low by using register 8'h0E[0] = 0b.

When the TCAN284xx-Q1 is in sleep or fail-safe mode, this pin can be used as a digital wake up pin by enabling this feature using register 8'h0E[1] = 1b and 8'h0E[2] = 1b. If VCC1 is present in sleep mode, the thresholds will be based on VCC1 levels. If VCC1 is not present, the levels will be based off an internal voltage rail, $V_{IH\text{SWINT}}$ and $V_{IL\text{SWINT}}$. This pin can then be used to wake up when an external CAN FD or LIN transceiver is wake capable or MCU to wake up the TCAN284xx-Q1. This can be accomplished in several ways. If the external transceiver has an inhibit pin, external circuitry can be utilized to provide a wake input to this pin. The processor can connect directly to this pin and initiate the wake up without utilizing a SPI command.

[Figure 8-11](#) provides a state diagram on how the SW pin behaves.

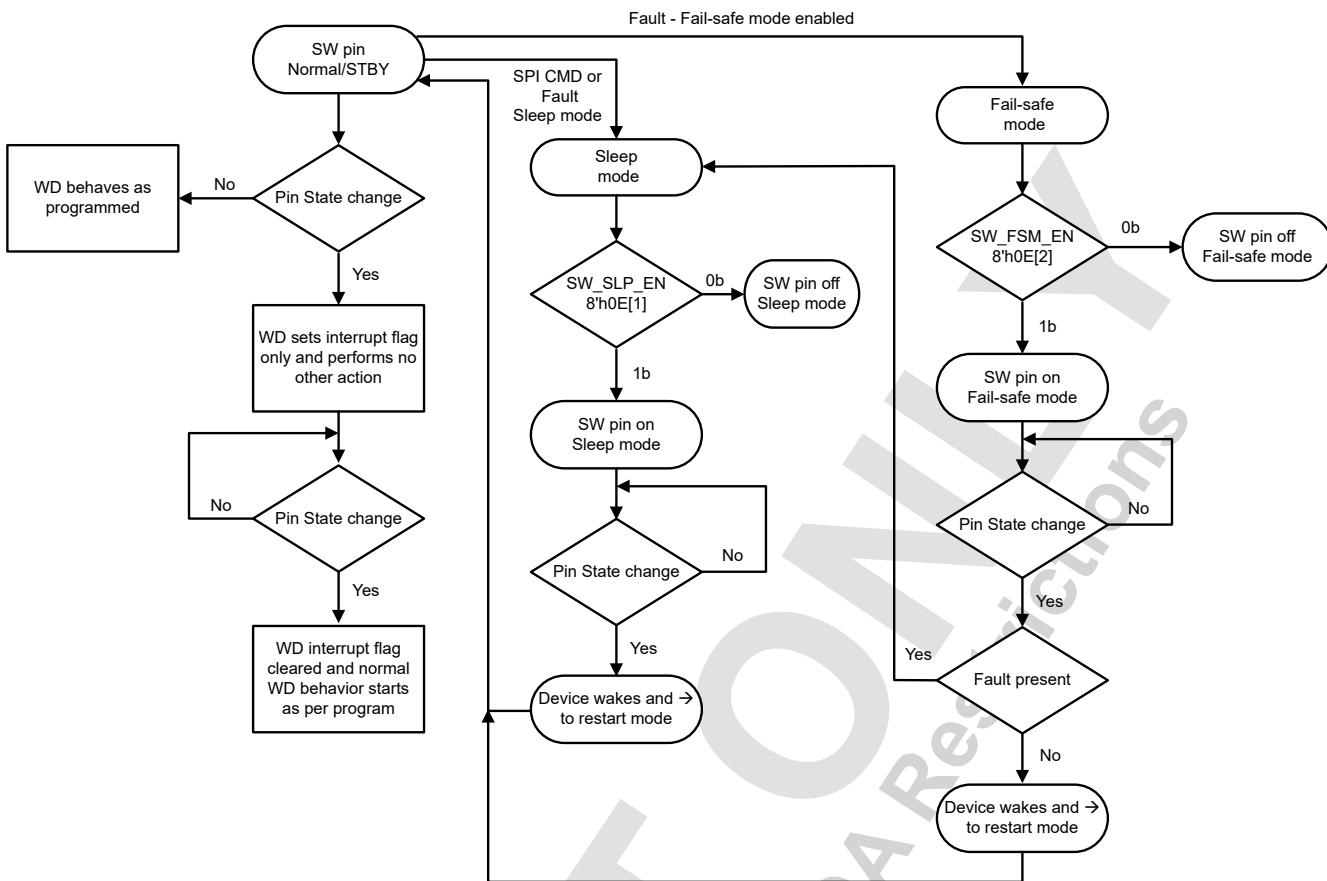


Figure 8-11. SW Pin State Diagram

Note

- The SW pin has a filter timer that the state change has to be at least $t_{SW} = 140 \mu s$
 - The pull-up and pull-down resistor will be self-configured based upon register 8'h0E[0] setting. Active high means pull-down active, active low means pull-up active.
 - If the device is powered up with the SW pin connected high the device will treat this as no watchdog actions to take place.

8.3.20 GFO Pin

This pin is can be programmed to provide certain information back to the processor. These can be considered interrupts such as a UVCC1 or watchdog failures. The pin can be configured to state which wake event has taken place, bus or local via WAKE pin. Configurable to indicate device has entered fail-safe mode.

Pin can also be configured to act as an enable pin to control an external LIN or CAN transceiver. This is accomplished by configuring the pin to support the correct polarity and then programming the external device mode.

8.3.21 CANH and CANL Bus Pins

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transceiver and the low voltage WUP CAN receiver. The functionality of these is explained throughout the document. See [Section 9.1.2.2](#) for can bus biasing.

8.3.22 NU/LIN Bus Pin

This high voltage input or output pin is a single wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 58 V. Reverse currents from the LIN to supply (VSUP) are minimized with blocking

diodes, even in the event of a ground shift or loss of supply (VSUP). The LIN bus has bus short circuit current limiter shown by I_{BUS_LIM} in the electric specification table.

For TCAN2844x-Q1 and TCAN2845x-Q1 LIN pin is not present and is a NU for not used pin. This pin should not be connected on the board.

8.3.22.1 LIN Transmitter Characteristics

The transmitter meets thresholds and AC parameters according to the LIN specification. The transmitter is a low side transistor with internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to VSUP, so no external pull-up components are required for the LIN peripheral node applications. An external pull-up resistor and series diode to VSUP must be added when the device is used for a controller node application. In fast mode the transmitter can support 200 kbps data rates.

8.3.22.2 LIN Receiver Characteristics

The receiver's characteristic thresholds are ratio-metric with the device supply pin according to the LIN specification.

The receiver is capable of receiving higher data rates (> 100 kbps) than supported by LIN or SAEJ 2602 specifications. This allows the TCAN2846x-Q1 and TCAN2847x-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system. In fast mode the receiver can support 200 kbps.

8.3.22.3 LIN Termination

There is an internal pull-up resistor with a serial diode structure to VSUP, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor (1 k Ω) and a series diode to VSUP must be added when the device is used for commander node applications as per the LIN specification.

Figure 8-12 shows a commander node configuration and how the voltage levels are defined.

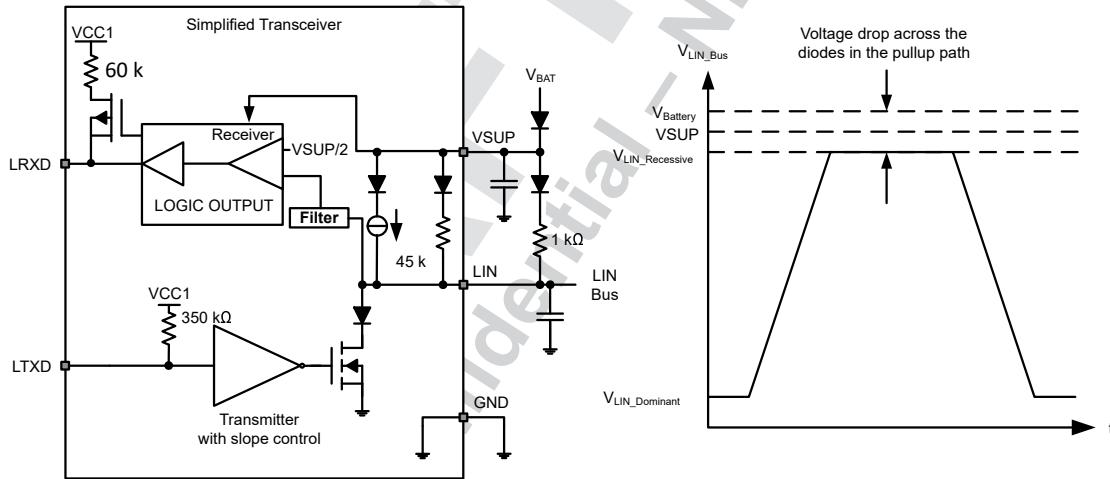


Figure 8-12. Commander node configuration with voltage levels

8.3.23 CAN FD and LIN Transceiver

The CAN FD and LIN transceiver can be separately programmed outside of the SBC mode control or tied to the SBC mode control. When tied to the SBC mode control, changing the SBC mode to normal mode will automatically change the transceivers to on. All other states will be wake capable. When programmed separately than the SBC modes, there are certain states that the transceivers cannot be in for the mode. **If a mode change is initiated and the transceiver is not in an allowed state the mode change will not take place and the MODE_ERR interrupt at 8'h5A[3] will be set to 1b.** Here are a few specific cases for consideration.

- A transceiver in Normal mode configured for listen, wake capable and off can transition to standby mode and the state will be the same.
- Transitioning to restart mode will be wake capable unless the transceiver was programmed off.
- Transitioning from restart mode to standby mode will be wake capable unless the transceiver was programmed off.
- When using the SWE timer and it times out, the transceivers will automatically become wake capable when entering sleep mode or fail-safe mode.

Note

If the device is in SBC normal mode and the transceivers are programmed on, the TXD pin will be checked. If the TXD pin is dominant, the transceiver will not turn on the transmitter until the TXD pin has transitioned to recessive.

The CAN FD transceiver supports off, on, listen and wake capable. The state of the transceiver is programmed using register 8'h10[2:0]. On represents what would be normal mode for a stand-alone transceiver. The CAN transceiver defaults to wake capable when entering fail-safe mode but can be disabled for this mode by using CAN1_FSM_DIS at register 8'h10[3] = 1b.

Table 8-1. CAN FD Transceiver Programmable State by SBC Mode

SBC Mode	On	Listen	Wake Capable	Off	SBC Mode Control
Normal	✓	✓	✓	✓	On
Standby		✓	✓	✓	Wake Capable
Sleep			✓ default	✓	Wake Capable
Restart			✓ default	✓	Wake Capable
Fail-safe			✓ default	✓	Wake Capable

Note

- When entering SBC restart mode, the transceiver will change wake capable
- When entering SBC fail-safe mode, the transceiver will default to wake capable.

The TCAN2846x-Q1 and TCAN2847x-Q1 provides a LIN transceiver which supports on, fast, listen, off and wake capable. The state of this transceiver is programmed using register 8'h1D[7:5]. The LIN transceiver defaults to wake capable when entering fail-safe mode but can be disabled for this mode by using LIN1_FSM_DIS at register 8'h1C[1] = 1b.

Table 8-2. LIN Transceiver Programmable State by SBC Mode

SBC Mode	On	Fast	Listen	Wake Capable	Off	SBC Mode Control
Normal	✓	✓	✓	✓	✓	On
Standby			✓	✓	✓	Wake Capable
Sleep				✓ default	✓	Wake Capable
Restart				✓ default	✓	Wake Capable
Fail-safe				✓ default	✓	Wake Capable

Note

- When entering SBC restart mode, the transceiver will change to wake capable
- When entering SBC fail-safe mode, the transceiver will default to wake capable

8.4 Device Functional Modes

The TCAN284xx-Q1 has several SBC operating modes: normal, standby, sleep, restart and fail-safe. The first three mode selections are made by the SPI register, 8'h10[2:0]. Fail-safe mode if enabled is entered due to

various fault conditions. The CAN FD and LIN transceivers are independently controlled. The TCAN284xx-Q1 automatically goes from sleep to restart and then to standby mode when receiving a WUP or LUP event. When selective wake is enabled, the device looks for a WUF and if not received the TCAN2845/7x-Q1 remains in sleep mode. See [Table 8-3](#) for the various modes and what parts of the device are active during each mode.

Table 8-3. Mode Overview

Block	Restart	Sleep	Standby	Normal	Fail-safe
nINT	High (VCC1 present) off others	High (VCC1 present) High-Z others	Active	Active	High-Z
GFO	High (VCC1 present) off others	High-Z	Active	Active	High-Z
SW	Off	Wake capable/Off	Active	Active	Wake capable/Off
HSSx	Off	Off - HSS4 can be on if WAKE pins setup for cyclic sensing	As Programmed	As Programmed	Off - HSS4 can be on if WAKE pins setup for cyclic sensing
LIMP (Open-drain active low)	Same as previous state unless from fail-safe mode. Off (high from external pull-up) from fail- safe mode unless WD error and then Low	High	Previous state prior to entering STBY	Previous state prior to entering normal mode	Low
WAKE _x	Off	Active	Active	Off	Active
CRXD	High (VCC1 present)	High (VCC1 present) High-Z others	Transceiver configuration dependent	Transceiver configuration dependent	High-Z
LRXD	High (VCC1 present)	High (VCC1 present) High-Z others	Transceiver configuration dependent	Transceiver configuration dependent	High-Z
nRST	Low	Low unless VCC1 programmed to be on in sleep mode, then high.	High	High	Off
SPI	Off	Active if VCC1 present	Active	Active	Off
Watchdog	Off	Off	Default on with long first pulse but programmable off - Timeout only	Active	Off
Low Power CAN RX	Default on for Wake capable	Default on for Wake capable	On if Wake capable	On if Wake capable	Default on for Wake capable
CAN Transceiver	Off	Off	Programmable - Receiver only	Programmable	Off
Low Power LIN RX	Default on for Wake capable	Default on for Wake capable	On if Wake capable	On if Wake capable	Default on for Wake capable
LIN Transceiver	Off	Off	Programmable - Receiver only	Programmable	Off
LIN Bus Termination	Weak current pull-up	Weak current pull-up	45 kΩ (typical)	45 kΩ (typical)	Weak current pull-up
VCC1	Ramping	Off (default); programmable on	On (default); programmable off	On (default); programmable off	Off
VCC2	Ramping	Off (default); programmable on	On (default); programmable off	On (default); programmable off	Off
VEXCC	Ramping after initial configuration	Off (default); programmable on	Programmable	Programmable	Off

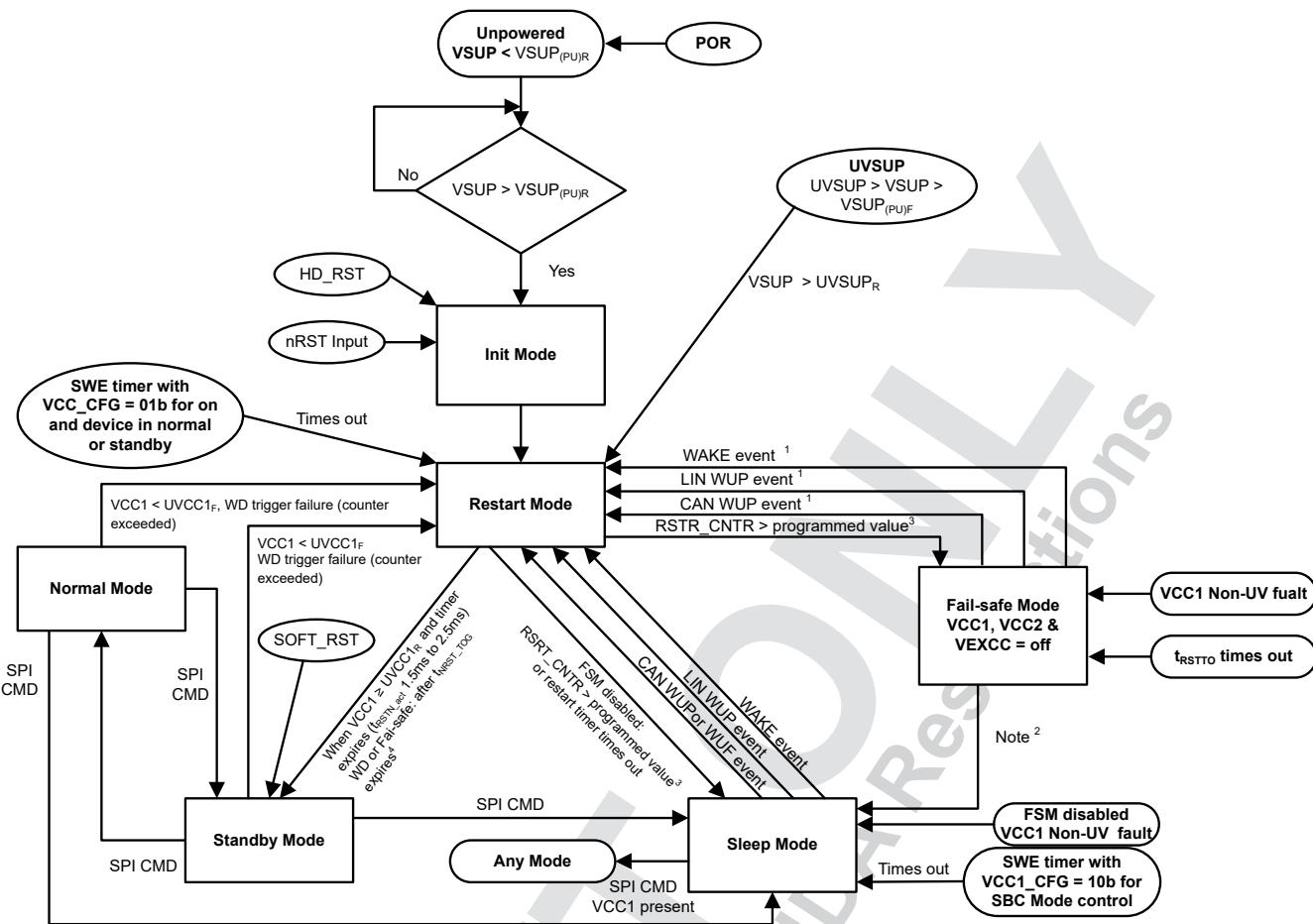


Figure 8-13. Device State Diagram

Note

Figure notes for the device state diagram figure.

1. To exit fail-safe mode the fault must be cleared and a wake event take place
 - The exception to this is when fail-safe mode is entered due to a TSD event on VCC1 and VEXCC
2. SWE timer starts upon entering fail-safe mode and if timer times out the device will transition to sleep mode regardless of VCC1 configuration
3. Restart counter increments when entered from Normal or Standby modes
4. Exiting Restart mode to standby mode can take place due to these two actions
 - VCC1 must be $>$ UVCC1_R
 - WD failure or FSM cause device to enter Restart mode, pulling nRST low for t_{NRST_TOG} and then will transition to standby mode releasing nRST

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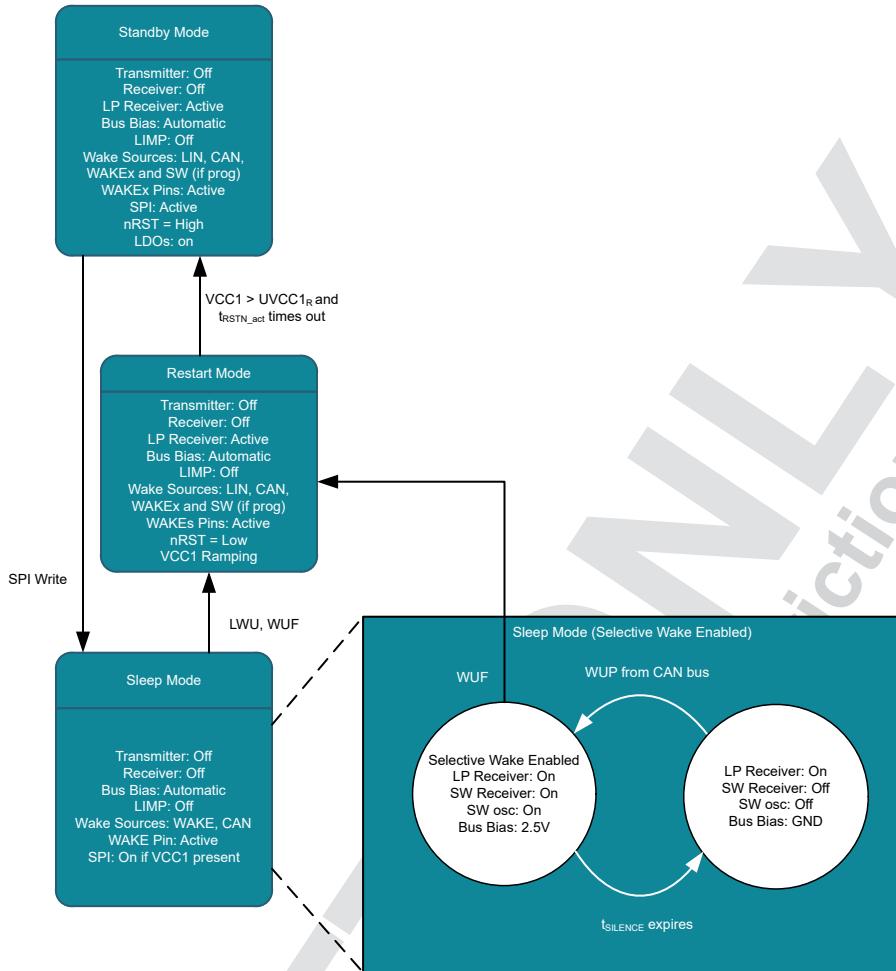


Figure 8-14. Selective Wake Enabled Sleep Mode

Note

For the state diagrams by default SPI is off in sleep mode. SPI can be configured to work in sleep mode which would include selective wake sub state as shown in [Figure 8-14](#).

8.4.1 Init Mode

This is the initial mode of operation upon powering up. This is a transitional mode that is entered once VSUP is above $VSUP_{(PU)R}$ threshold. The device will transition to restart mode once the device defaults are set.

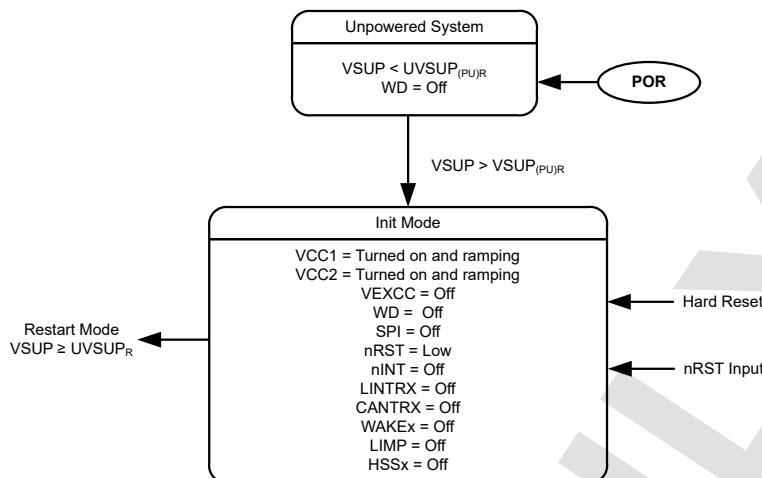


Figure 8-15. Init Mode

8.4.2 Normal Mode

In normal mode, the CAN FD transceiver can be configured as on, listen, wake capable or off. The LIN transceiver can be configured as on, fast, listen, wake capable or off. The transmitters are translating digital inputs on the LTXD and CTXD signals from the controller to LIN and or CAN signals on their bus. The receivers are translating signals from the bus to a digital output on the LRXD and CRXD to the processor. Normal mode is enter by a SPI command and does not change the programmed configuration of the transceivers. If the watchdog is disabled in standby mode when entering normal mode, a long timeout window is used prior to utilizing the programmed watchdog type and timing.

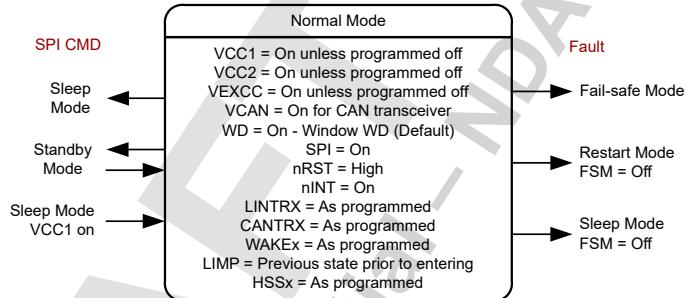


Figure 8-16. Normal Mode

8.4.3 Standby Mode

The device automatically enters standby mode from restart mode. Upon initial power up, this transition happens when $VCC1 > UVCC1$ and t_{RSTN_act} time has expired. $VCC2$ is turned on at power up but is not required to be greater than $UVCC2$ in order to transition to standby mode. The TCAN284xx-Q1 can enter standby mode by writing a 00b to register 8'h0B[7:6] from normal mode. The watchdog function is default on in standby mode. Standby mode only supports timeout watchdog and automatically changes to this when entered. When WD_STBY_DIS , register 8'h14[0] = 0b (default value) entrance to standby mode has a long timeout window, t_{INITWD} , that a WD trigger event must take place when entered from restart mode. The watchdog can be disabled for standby mode by setting 8'h14[0] = 1b. In this mode, the transceiver can be programmed to meet the applications requirements. There are several blocks that are active in this mode. In standby mode, the CAN FD transceiver can be configured as listen, wake capable or off. The LIN transceiver can be configured as listen, wake capable or off. If programmed as wake capable, the low power CAN and LIN receivers are actively monitoring the bus for the wake up pattern (WUP). The WAKEEx pins monitor is active. The SPI interface is active so that the microprocessor can read and write registers in the memory for status and configuration. The device goes from sleep mode to restart mode to standby mode automatically upon a bus WUP event, WUF (TCAN2845x-Q1 and TCAN2847x-Q1) or a local wake up from the WAKEEx pins and when $VCC1 > UVCC1_R$. If $VCC1$ is disabled, the device will enter standby mode after t_{RSTN_act} timer times out.

Upon entering standby mode, the SWE timer, $t_{INACTIVE}$, starts and any SPI command from the processor will clear the SWE timer. This feature makes sure the node will be in the lowest power mode if the processor does not come up properly. This automatic mode change also takes place when the device has been put into sleep mode and receives a wake event, WUP, WUF or LWU. To disable this feature for sleep events, register 8'h10[3] (SWE_DIS) must be set to one. This does not disable the feature when powering up or when a power on reset takes place.

The following provides the description on how selective wake interacts between sleep and standby modes for the TCAN2845x-Q1 and TCAN2847x-Q1.

- At power up, the device is in standby. Clear all Wake flags (PWRON, WUP/LWU), configured the Selective Wake registers, and then set selective wake config (SWCFG = 1) and selective wake enable (SW_EN = 1).
- When SWCFG = 1 and the device is placed into sleep mode the low power WUP receiver is active and waiting for a WUP.
- Once a WUP is received the WUF receiver is active.
- The device receives the wake-up frame and determine if it is the node requested to wake up.
 - If the WUF address is correct, the device wakes up the node entering standby mode.
 - If the WUF is not address is incorrect, the device stays in sleep mode.
- A wake interrupt occurs from any type – WUF (CANINT), FRAME_OVF or LWU (if enabled), the device enters standby mode.

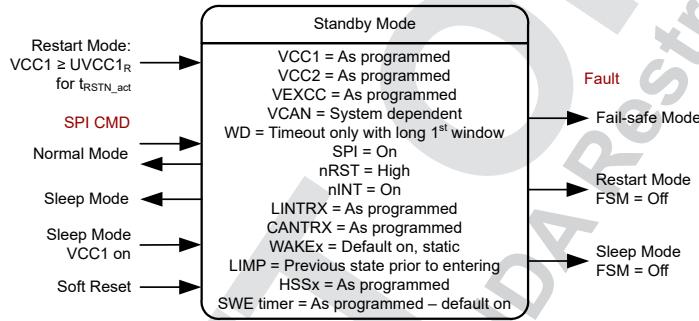


Figure 8-17. Standby Mode

8.4.4 Restart Mode

Restart mode is a transitional mode. This mode can be entered from any of the other modes depending upon whether fail-safe mode is disabled. In this mode the enabled LDOs are ramping or are on. At initial power up, once $VCC1 \geq UVCC1_R$ for t_{RSTN_act} (~2 ms) the device will transition to standby mode. While in restart mode, nRST will be latched low. When restart mode is entered, a restart timer is started. This timer can be selected between t_{RSTTO} and $t_{INACTIVE}$ (SWE) timer time by programming register 8'h4F[0], RSTART_TMR_SEL. The default is t_{RSTTO} . If the device has not exited restart mode prior to the timer timing out, the device will transition to fail-safe mode if enabled or sleep mode if fail-safe mode is disabled. Each time restart mode is entered from normal or standby modes, the restart mode counter, RSRT_CNTR, is incremented. The exception to this is if exceeding the restart counter caused the device to enter fail-safe or sleep mode. When re-entering restart mode due to this event, the counter is ignored and device will enter standby mode. Once in standby mode, the counter should be cleared. This counter is programmable from register 8'h28[7:4], which sets the number of times restart can be entered before transitioning to sleep or fail-safe mode, up to 15 times. The default value is 4. Register 8'h28[3:0] is RSRT_CNTR. The counter can be disabled by programming the counter to 0000b. To prevent the transition to sleep or fail-safe mode, the counter should be cleared periodically.

The nRST output pin behavior depends upon the reason the device entered restart mode. When entered due a watchdog failure, from fail-safe mode or an external nRST toggle, the nRST pin is pulled low for t_{NRST_TOG} which defaults to 20 ms. This pulse width can be configured to 2 ms by changing register 8'h29[5] = 0. After this time the device will transition to standby mode and release nRST pin to high. When restart mode is entered from sleep mode or due to an under-voltage event the device will latch nRST low until $VCC1 > UVCC1_R$ for t_{RSTN_act} and then will transition to standby mode and release nRST high. See [Figure 8-18](#) on how restart mode is entered and exited.

The nRST pin is the TCAN284xx-Q1 reset input which transitions the device into restart mode when the pin is pulled low for t_{nRST_TOG} , see Figure 8-19

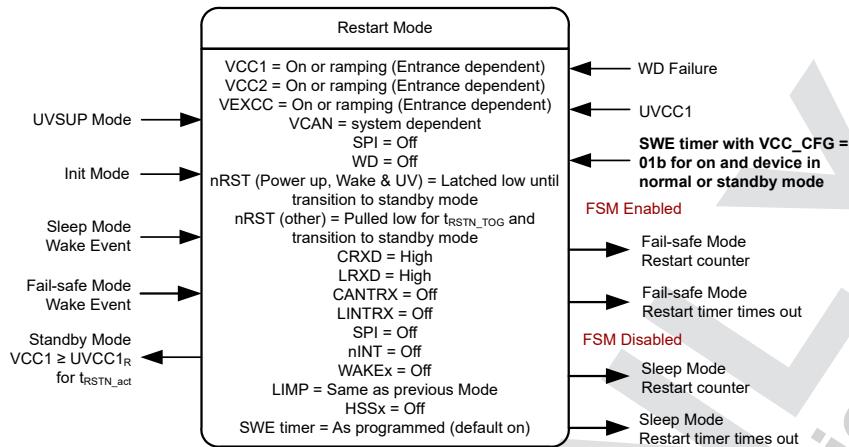


Figure 8-18. Restart Mode

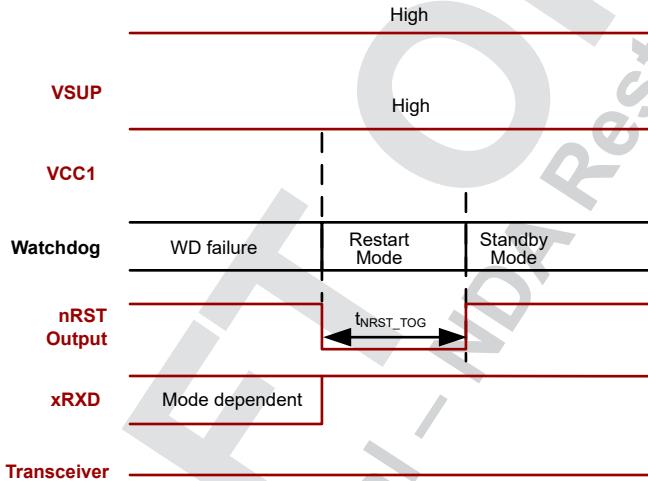


Figure 8-19. WD Failure to Restart Timing Diagram

8.4.5 Fail-safe Mode

The TCAN284x-Q1 has a fail-safe mode, default on, which is entered when certain fault events take place. When fail-safe mode is entered, a global interrupt is issued and the sleep wake error (SWE) timer, $t_{INACTIVE}$, if enabled starts and VCC1, VCC2 and VEXCC are turned off. The reason for entering fail-safe mode is provided by register 8'h17[3:1] and expanded further with other interrupt flags. This mode can be disabled by utilizing register 8'h17[0] but it is recommended to keep enabled as fault monitoring is active in fail-safe mode and not sleep mode. This mode turns on LIMP and brings other functions into lower power mode states. When entering fail-safe mode the LDOs are kept off for at least t_{LDOOFF} , ~ 300ms. During this time wake events are monitored and preserved. After t_{LDOOFF} times out wake events will cause the device to transition to restart mode. If the SWE timer times out prior to faults being cleared and a wake event taking place, the device will transition to sleep mode. Figure 8-20 shows the various fault conditions that will cause the device to enter fail-safe mode. If the fault conditions are cleared and a wake event takes place, the device will transition to restart mode. Figure 8-21 provides a high level flow chart for fail-safe mode.

A fail-safe mode counter is available allowing a set number of fail-safe events in a row which then causes the device to perform the programmed action which can include going to sleep where a WUP, WUF or LWU event does not wake the device. A power on reset is required. The counter is default disabled and can be enabled at 8'h17[7:4] ≠ 0000b. The counter expiration action is at 8'h17[7:4]. The number of events before action is

programmed is set at 8'h18[7:4] with a value up to 16 events. 8'h18[3:0] is the running up/down fail-safe event counter that can be read and cleared.

There are multiple ways to exit fail-safe mode depending upon the fault and programmed configuration.

- By default, the SWE timer is enabled and these are the transition paths out of fail-safe mode.
 - A wake event and cleared fault will send the device into restart mode.
 - SWE timer timing out will cause the device to transition to sleep mode
- and VCC1 will remain off even if VCC1_CFG = 01b for on
- If FSM_CYC_WK_EN, 8'h1A[0] = 1b, the device will wake up during the on time of the selected timer and check to see if the fault has cleared. If so, it will transition to restart mode.

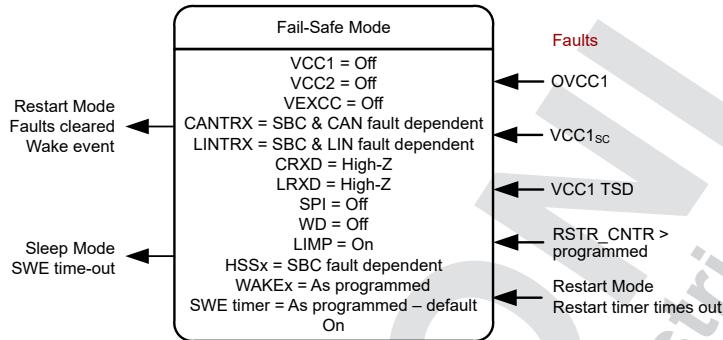


Figure 8-20. Fail-safe Mode

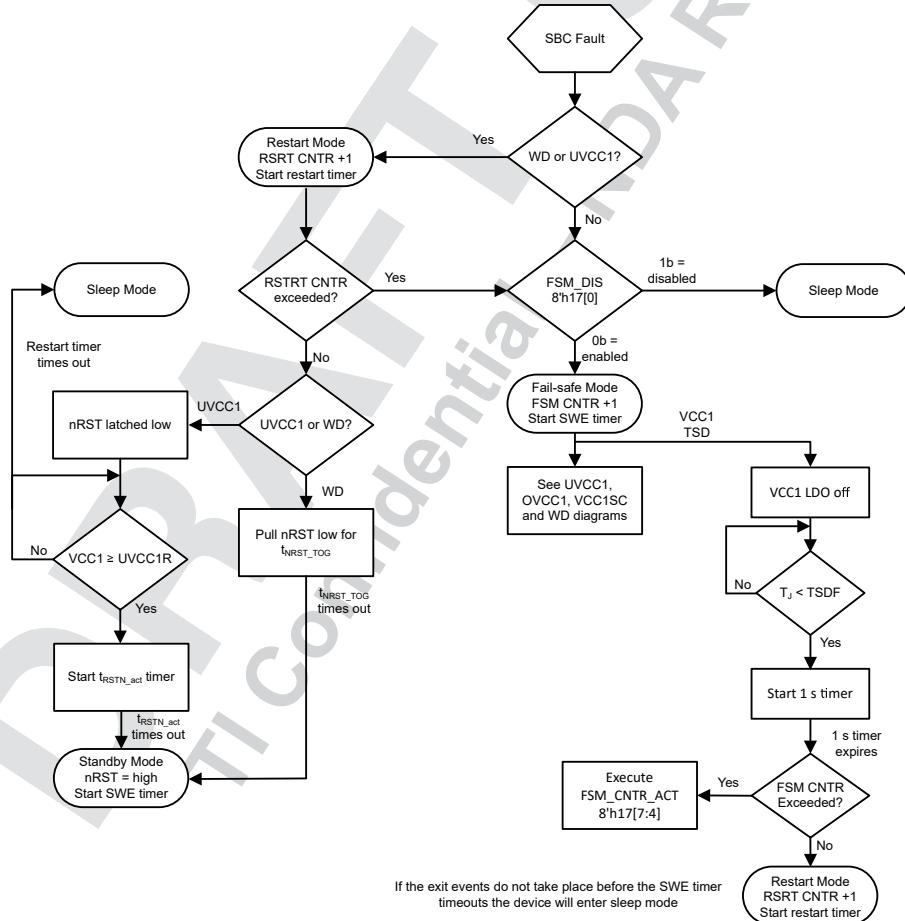


Figure 8-21. Fail-safe mode flow chart

Note

For the device to enter fail-safe mode there has to be a method for the device to wake up. This can be by the communication bus or a WAKE pin. If these are all disabled for fail-safe mode the device will automatically make the CAN FD and LIN transceivers wake capable.

When the device enters fail-safe mode, the SWE timer automatically starts.

- If SWE timer times out the device will enter sleep mode
- If a wake event takes place prior to the SWE timer timing out the device will determine if fault is still present.
 - If fault is present the device stays in fail-safe mode monitoring the fault.
 - If fault has cleared the device will enter restart mode.

When fail-safe mode is entered due to any condition other than TSD the following takes place.

- The VCC1 LDO is turned off. If the fault impacts load sharing; both will be turned off.
 - If the device receives a wake event, the LDO will be turned on for t_{LDOON} to determine if the short circuit event is still present.
 - At the end of t_{LDOON} , if a short circuit is detected the device will turn off the LDO and wait for next wake event.
 - Over-voltage is continuously monitored will immediately enter sleep mode.
 - If fault is cleared the device will enter restart mode.
-

8.4.5.1 SBC Faults

SBC faults are faults that cause the device to change the mode the device is in. If fail-safe mode is enabled these faults will cause the device to enter either restart or fail-safe mode. If fail-safe mode is disabled the faults will cause the device to enter either restart or sleep mode. SBC Faults are:

- Over-voltage for VCC1
- Under-voltage for VCC1
- Short circuit on VCC1
- Thermal Shutdown due to VCC1
- Watchdog failure
- Restart counter exceeds programmed value
- SWE timer expires
- Under-voltage on VSUP is an SBC fault but does not cause the device to enter fail-safe mode

8.4.5.2 CAN Transceiver Faults

CAN transceiver faults are ones that impact the transceiver and doesn't cause the device to enter fail-safe mode but does turn off the CAN transmitter. CAN Transceiver Faults:

- VCC2 thermal shutdown
- CAN transceiver thermal shutdown
- CTXD pin stuck dominant - CTXD dominant timeout
- UVCAN

Note

If VCC2 is connected to VCAN, faults on VCC2 may cause a CAN fault.

8.4.5.3 LIN Transceiver Faults (TCAN2846-Q1 and TCAN2847-Q1)

LIN transceiver faults are ones that impact the transceiver and doesn't cause the device to enter fail-safe mode. The faults include dominant state timeout and thermal shut down.

8.4.6 Sleep Mode

Sleep mode is the power saving mode for the TCAN284x-Q1. In this mode the device can wake up from the CAN bus, LIN bus, WAKEx pins or SW pin (if programmed). If VCC1 is present, SPI is available to change

modes and nRST will be high. If sleep mode is entered due to a fault condition, INT_2 register 8'h52[7] (SMS) will be set to 1. [Figure 8-22](#) shows the various ways that sleep mode is entered and left.

While the device is in sleep mode, the following conditions exist.

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake up events in case an external connection to the LIN bus is lost.
- The CAN bus driver is disabled and the internal CAN bus termination is switched to a weak ground.
- The CAN and LIN transceiver receivers are disabled.
- The CAN and LIN low power wake up receivers are as programmed.
- WAKE pin is active.
- If cyclic sensing is enabled the selected high side switch will periodically turn on.
- SW pin if programmed as a digital wake input will be on.

Note

To enter sleep mode at least one method to wake up has to be available. If all have been disabled the device will not enter sleep mode and will set an interrupt, 8'h5A[3].

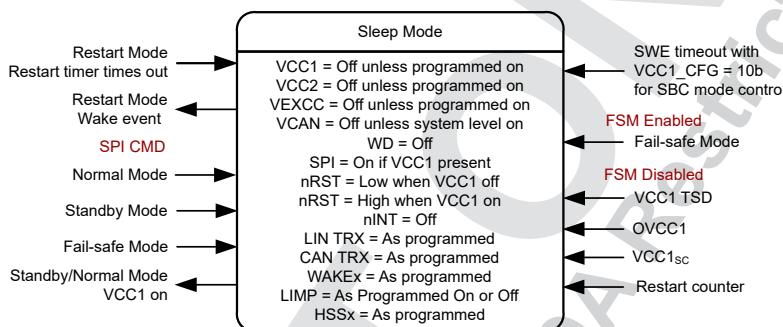


Figure 8-22. Sleep Mode

8.4.6.1 Wake Events

There are multiple ways to wake up from sleep mode.

- CAN bus wake using BWRR
- CAN bus wake using selective wake (TCAN2845-Q1 and TCAN2847-Q1)
- LIN bus wake (TCAN2846-Q1 and TCAN2847-Q1)
- Local wake up through the WAKEx pins
- SW pin if programmed as a digital wake input

8.4.6.1.1 CAN Bus Wake via CRXD Request (BWRR) in Sleep Mode

The TCAN284xx-Q1 supports low power sleep and standby modes and uses a wake up from the CAN bus mechanism called bus wake via CRXD Request (BWRR). Once this pattern is received, the TCAN284xx-Q1 automatically switches to standby mode from sleep mode and insert an interrupt onto the nINT pin, if enabled, to indicate to a host microprocessor that the bus is active, and the processor should wake up and service the TCAN284xx-Q1. The low power receiver and bus monitor are enabled in sleep mode to allow for CRXD Wake Requests via the CAN bus. A wake-up request is output to the CRXD (driven low) as shown in [Figure 8-23](#). The external CAN FD controller monitors CRXD for transitions (high to low) and reactivate the device to normal mode based on the CRXD Wake Request. The CAN bus terminals are weakly pulled to GND during this mode, see [Figure 7-2](#).

This device uses the wake-up pattern (WUP) from ISO 11898-2: 2016 to qualify bus traffic into a request to wake the host microprocessor. The bus wake request is signaled to the integrated CAN FD controller by a falling edge and low corresponding to a “filtered” bus dominant on the CRXD terminal (BWRR).

The wake-up pattern (WUP) consists of

- A filtered dominant bus of at least t_{WK_FILTER} followed by

- A filtered recessive bus time of at least t_{WK_FILTER} followed by
- A second filtered dominant bus time of at least t_{WK_FILTER}

Once the WUP is detected, the device starts issuing wake up requests (BWRR) on the CRXD pin. The behavior of this pin is determined by register 8'h12[2]. If 8'h12[2] = 0b the CRXD pin is pulled low once the WUP pattern has been received that meets the dominant, recessive, dominant filtered times. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive, other bus traffic does not reset the bus monitor. Once a filtered recessive is received, the bus monitor is now waiting on a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon receiving of the second filtered dominant the bus monitor recognizes the WUP and transition to BWRR output. Immediately upon verification receiving a WUP the device transitions the bus monitor into BWRR mode. This is indicated on the CRXD pin by latching it low, thus the CRXD output during BWRR matches the classical 8 pin CAN devices that used the single filtered dominant on the bus as the wake-up request mechanism from ISO 11898-2: 2016.

For a dominant or recessive to be considered “filtered”, the bus must be in that state for more than t_{WK_FILTER} time. Due to variability in the t_{WK_FILTER} the following scenarios are applicable.

- Bus state times less than $t_{WK_FILTER(MIN)}$ are never detected as part of a WUP, and thus no BWRR is generated.
- Bus state times between $t_{WK_FILTER(MIN)}$ and $t_{WK_FILTER(MAX)}$ may be detected as part of a WUP and a BWRR may be generated.
- Bus state times more than $t_{WK_FILTER(MAX)}$ is always detected as part of a WUP; thus, a BWRR is always generated.

See [Figure 8-23](#) for the timing diagram of the WUP.

The pattern and t_{WK_FILTER} time used for the WUP and BWRR prevents noise and bus stuck dominant faults from causing false wake requests while allowing any CAN or CAN FD message to initiate a BWRR. If the device is switched to normal mode or an under-voltage event occurs on V_{CC} the BWRR is lost. The WUP pattern must take place within the $t_{WK_TIMEOUT}$ time; otherwise, the device is in a state waiting for the next recessive and then a valid WUP pattern.

If 8'h12[2] = 1, the CRXD pin toggles low too high too low for $t_{TOGGLE} = 10 \mu\text{s}$ until the device is put into normal mode or listen mode. BWRR is active in standby mode upon power up and once coming out of sleep mode or certain fail-safe mode conditions. If a SPI write puts the device into standby mode, the CRXD pin is high until a wake event takes place. The CRXD pin then behaves like it would when in sleep mode.

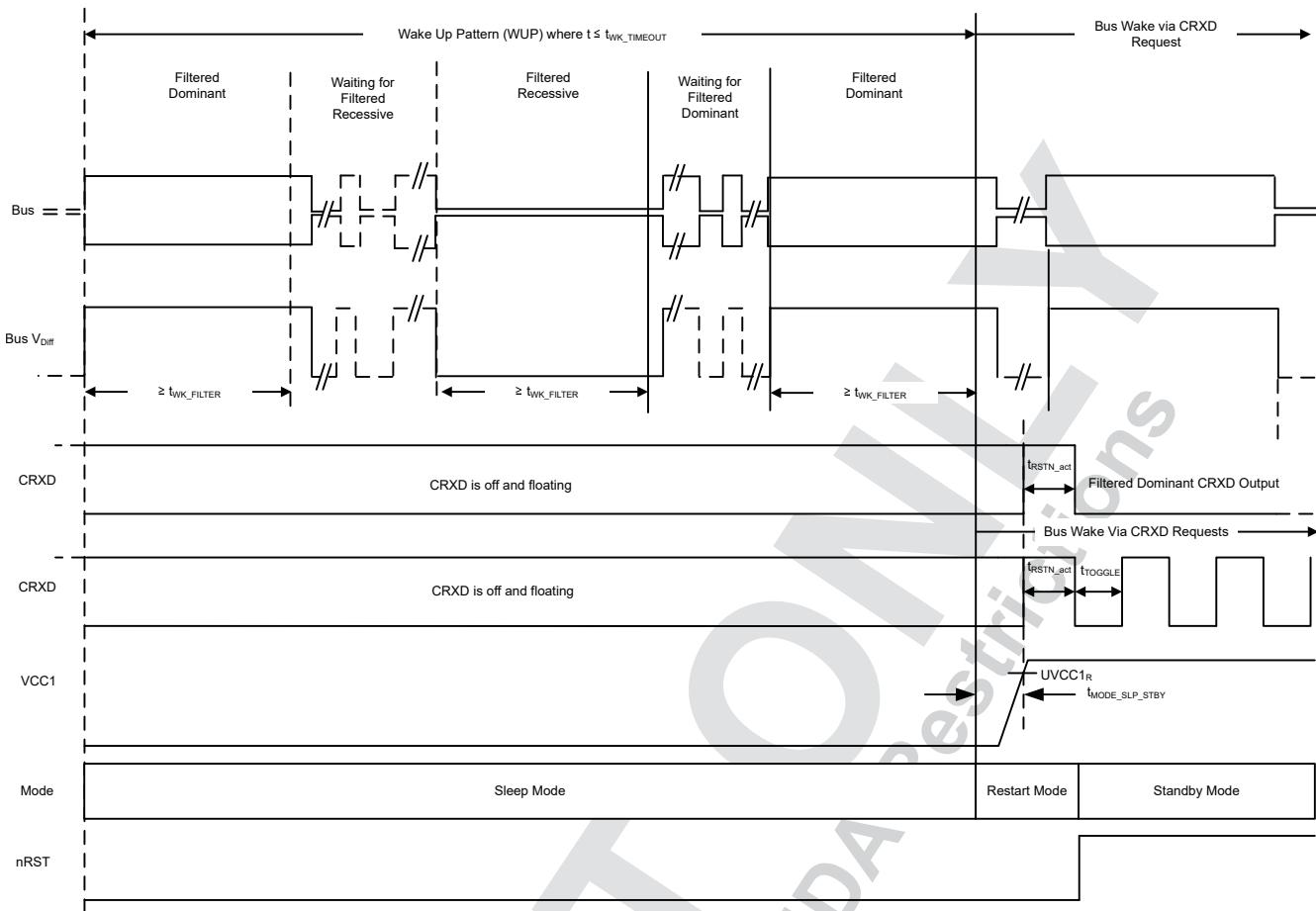


Figure 8-23. Wake Up Pattern (WUP) and Bus Wake via CRXD Request (BWRR)

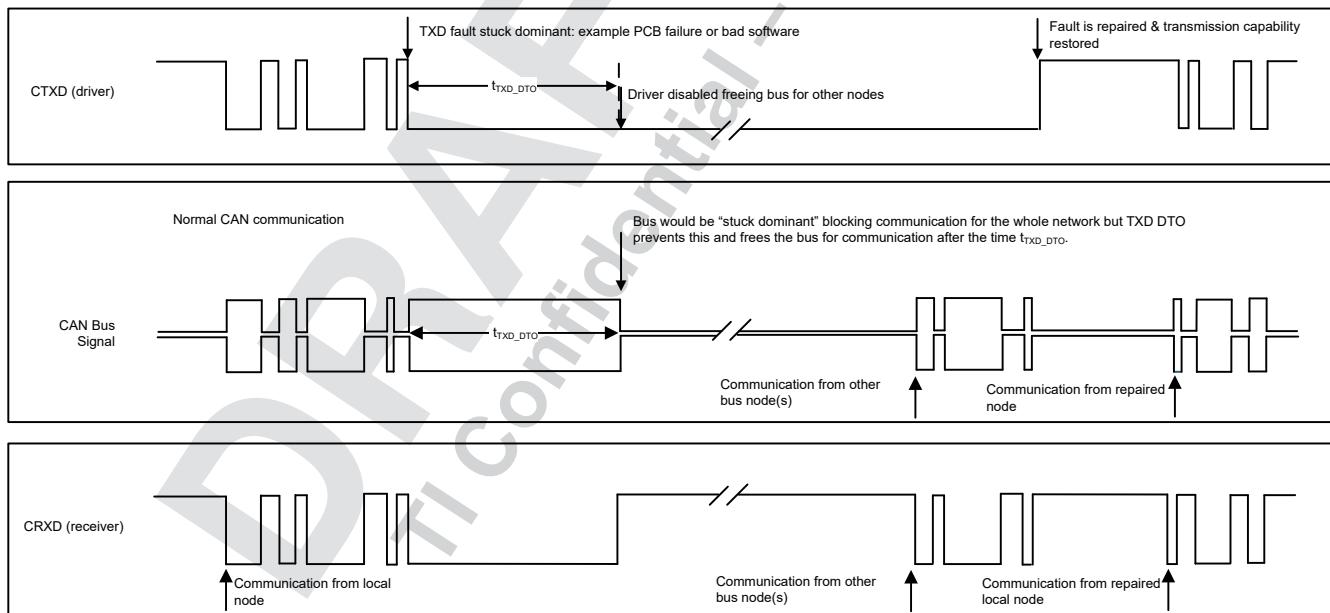


Figure 8-24. Example timing diagram with CTXD DTO

8.4.6.1.2 LIN Bus Wake

Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on the LIN bus where the dominant state is held for the t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake up event eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground. The LIN bus wake event will be indicated by L_RXD being pulled low once the device enters standby mode.

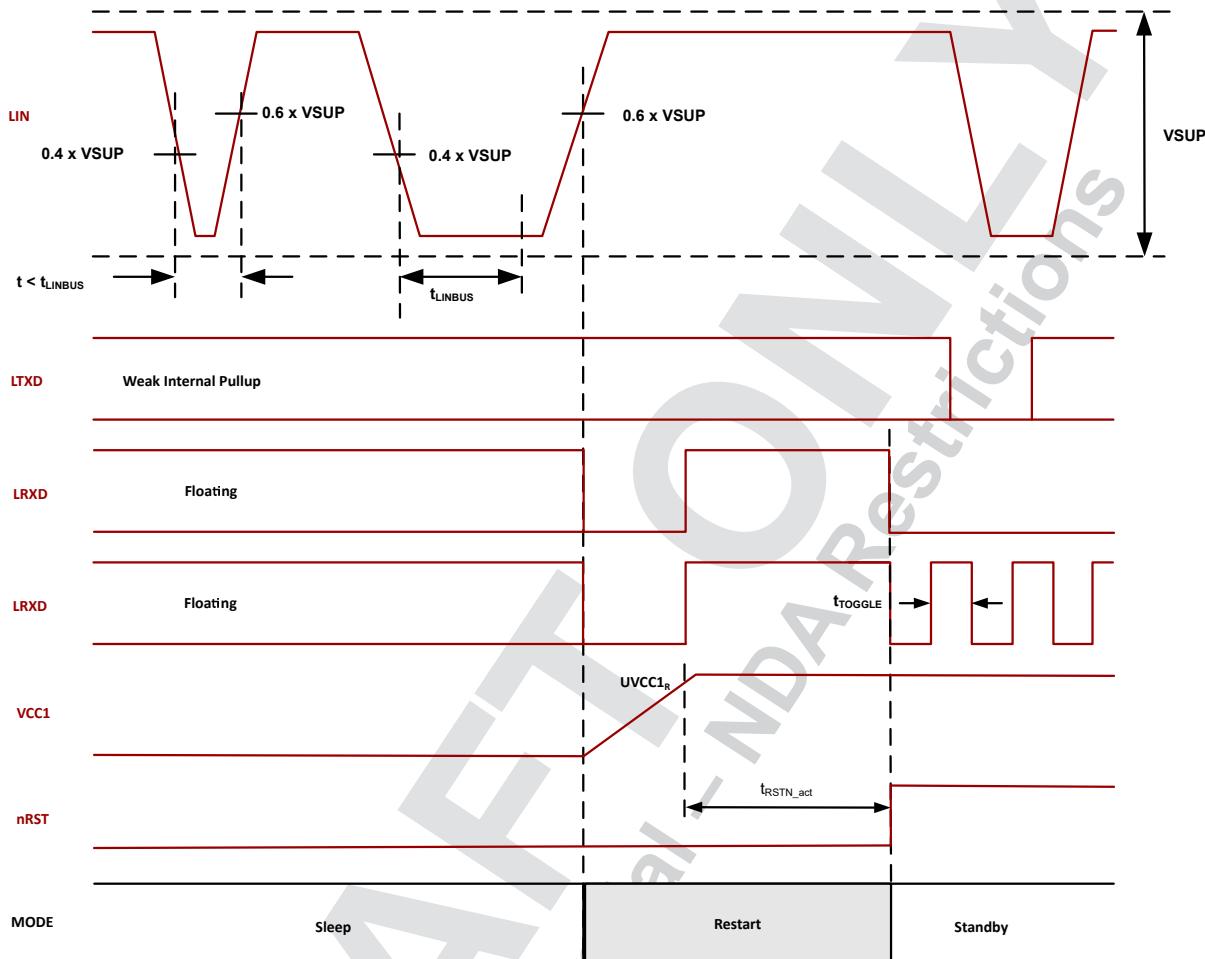


Figure 8-25. LIN bus wake

8.4.6.1.3 Local Wake Up (LWU) via WAKE_x Input Terminal

The WAKE_x terminals are a highly configurable ground based, high voltage capable inputs which can be used for local wake up (LWU) request via a voltage transition. There are two methods for this wake event. A static wake based on a level changed on the pin or a timing based, cyclic sensing where the WAKE_x pin is periodically turned on and a change during this on time is the trigger event is checked.

The device provides a WAKE pin status change update using reg 2Ah[4:0] showing which WAKE pin has changed states.

There are two methods of utilizing the WAKE pins:

- Static wake
- Cyclic sensing wake

The WAKE pins have a global control for which method a wake takes place, rising edge, falling edge, bi-directional, pulse or filtered pulse. The WAKE pins have programmable thresholds

8.4.6.1.3.1 Static Wake

The WAKE_x pins default to bi-directional input but can be configured for rising edge and falling edge transitions, see [Figure 8-26](#) and [Figure 8-27](#), by using WAKE_CONFIG register 8'h11[7:6]. WAKE pins are ground based wake inputs and can be used with a switch to ground or V_{SUP}. The WAKE_x pins input thresholds can be based on VCC1 levels which would allow a direct connection to the processor or a switch to the VCC1 rail. If the terminal is not used, it should be connected to ground to avoid unwanted parasitic wake up. Once the device enters sleep mode the WAKE_x terminals voltage level need to be at either a low state or high state for t_{WAKE} before a state transition for a WAKE input can be determined. A pulse width less than t_{WAKE_INVALID} is filtered out.

The LWU circuitry is active in sleep mode, standby mode and transition state off going to sleep. If a valid LWU event occurs the device transitions to standby mode. The LWU circuitry is not active in normal mode.

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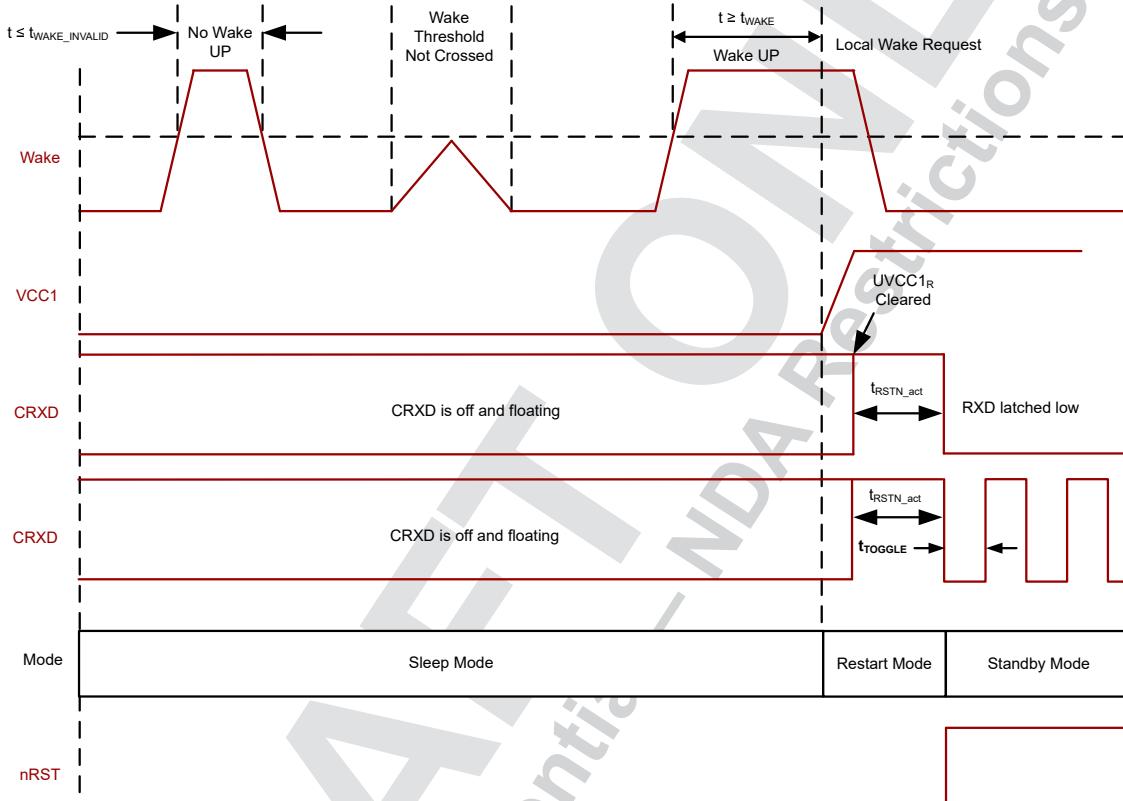


Figure 8-26. Local Wake Up – Rising Edge

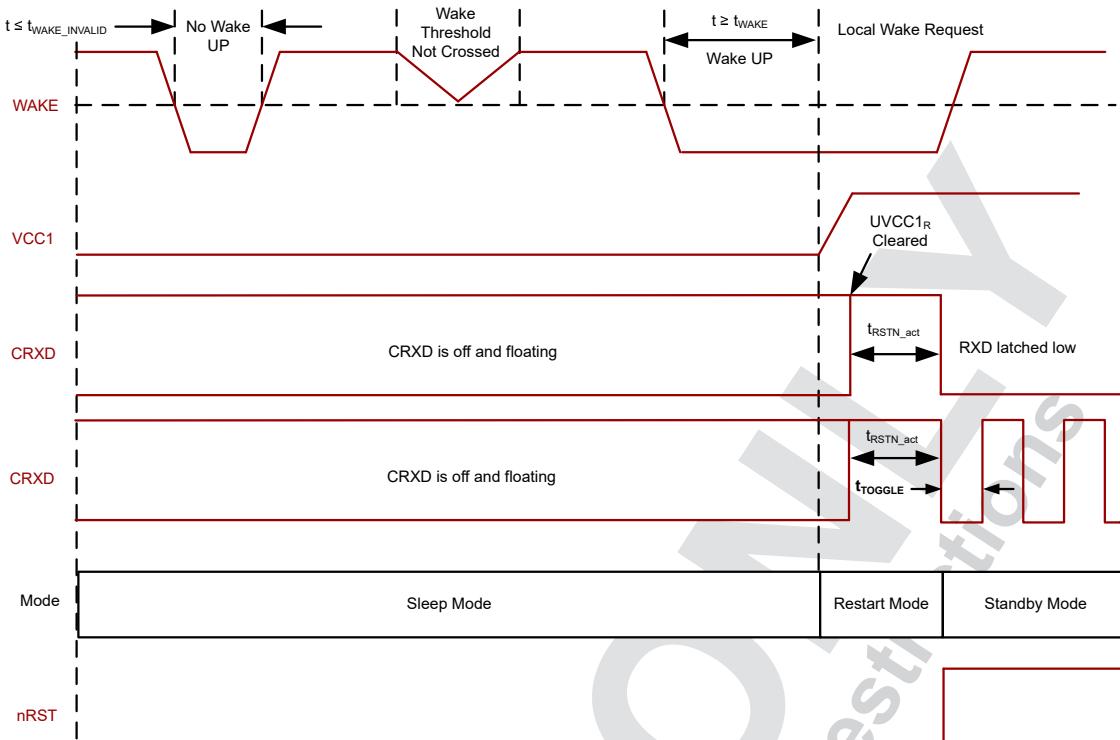


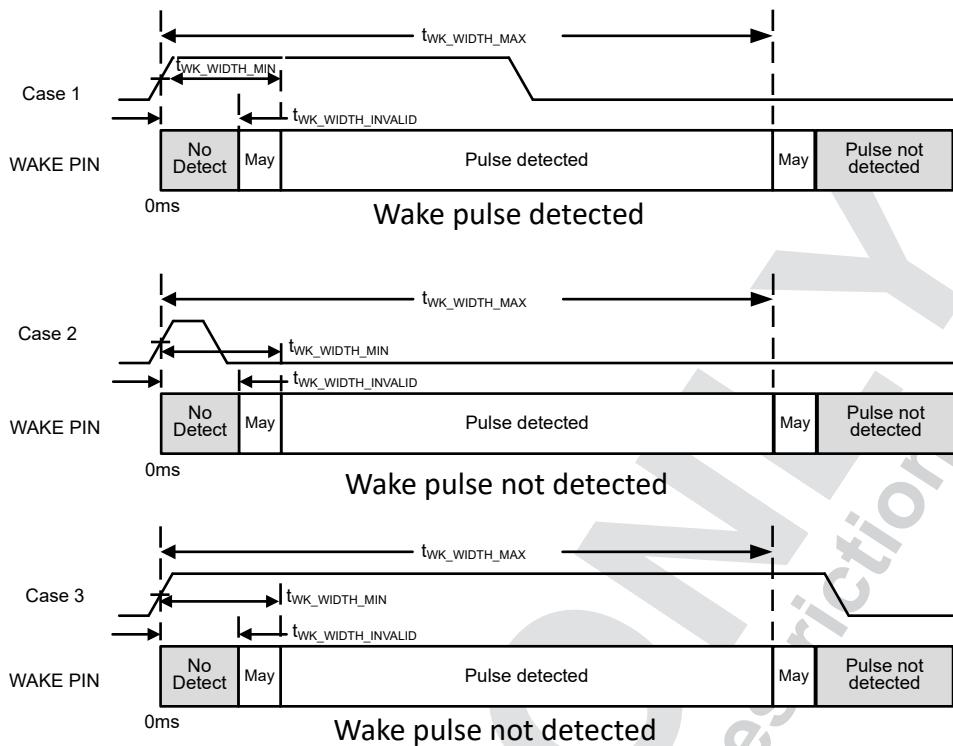
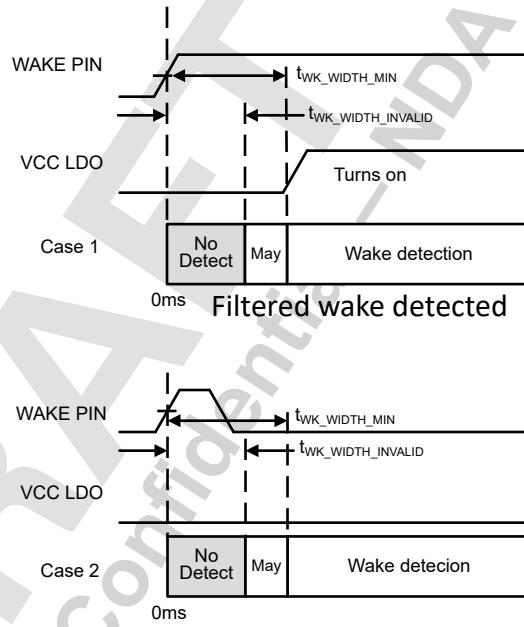
Figure 8-27. Local Wake Up – Falling Edge

Note

When either a rising or falling edge is selected for the WAKE pins the state prior to the edge requires a t_{WAKE} period of time.

- If a rising edge is selected and the device goes to sleep with WAKE high, a low of at least t_{WAKE} must be present prior to the rising edge wake event
- If a falling edge is selected and the device goes to sleep with WAKE low, a high of at least t_{WAKE} must be present prior to the falling edge wake event
- This requirement is not necessary for a bidirectional edge (default)
- [Figure 8-26](#) and [Figure 8-27](#) provide examples of a rising or falling edge WAKE input. RXD will be pulled low once VCC1 > UVCC1 and standby mode is entered.

The WAKE terminal can be configured for a pulse, see [Figure 8-28](#), by using WAKE_CONFIG register 8'h11[7:6]. The terminal can be configured to work off a pulse only. The pulse must be between $t_{WK_WIDTH_MIN}$ and $t_{WK_WIDTH_MAX}$. This figure provides three examples of pulses and whether the device will wake or not wake. $t_{WK_WIDTH_MIN}$ is determined by the value for $t_{WK_WIDTH_INVALID}$ is set to in register 8'h11[3:2]. There are two regions where a pulse may or may not be detected. By using register 8'h1B[1], WAKE_WIDTH_MAX_DIS, the pulse mode can be configured as a filtered wake input. Writing a 1 to this bit will disable $t_{WK_WIDTH_MAX}$ and the WAKE input will be based upon the configuration of register 8'h11[3:2] which selects a $t_{WK_WIDTH_INVALID}$ and $t_{WK_WIDTH_MIN}$ value. A WAKE input of less than $t_{WK_WIDTH_INVALID}$ will be filtered out and if longer than $t_{WK_WIDTH_MIN}$ the device will enter restart mode and turn on the LDOs. The region between the two may or may not be counted, see [Figure 8-29](#). Register 8'h12[7] determines the direction of the pulse or filter edge that is recognized. The status of the WAKE pin can be determined from register 8'h11[5:4]. When a WAKE pin change takes place the device will register this as a rising edge or falling edge. This will be latched until a 00 is written to the bits.

**Figure 8-28. WAKE Pin Pulse Behavior****Figure 8-29. WAKE Pin Filtered Behavior**

8.4.6.1.3.2 Cyclic Sensing Wake

When utilizing cyclic sense WAKE, the quiescent current of the device in sleep mode is reduced as the WAKE circuitry is only active during the on time of the selected HSS4 pin, see Figure 8-30 as an example for this. Periodically the HSS4 pin turns on applying VSUP to the external local wake circuitry. Each time this is done WAKE sets a bit stating the pin is high or low and compares the bit to the previous state. If there has been a change then the device will wake up, otherwise it will remain in sleep mode. See Figure 8-31 for a timing

diagram. The wake time is based upon t_{WK_CYC} as shown in Figure 8-31. The period and pulse width are determined by register 8'h12[5].

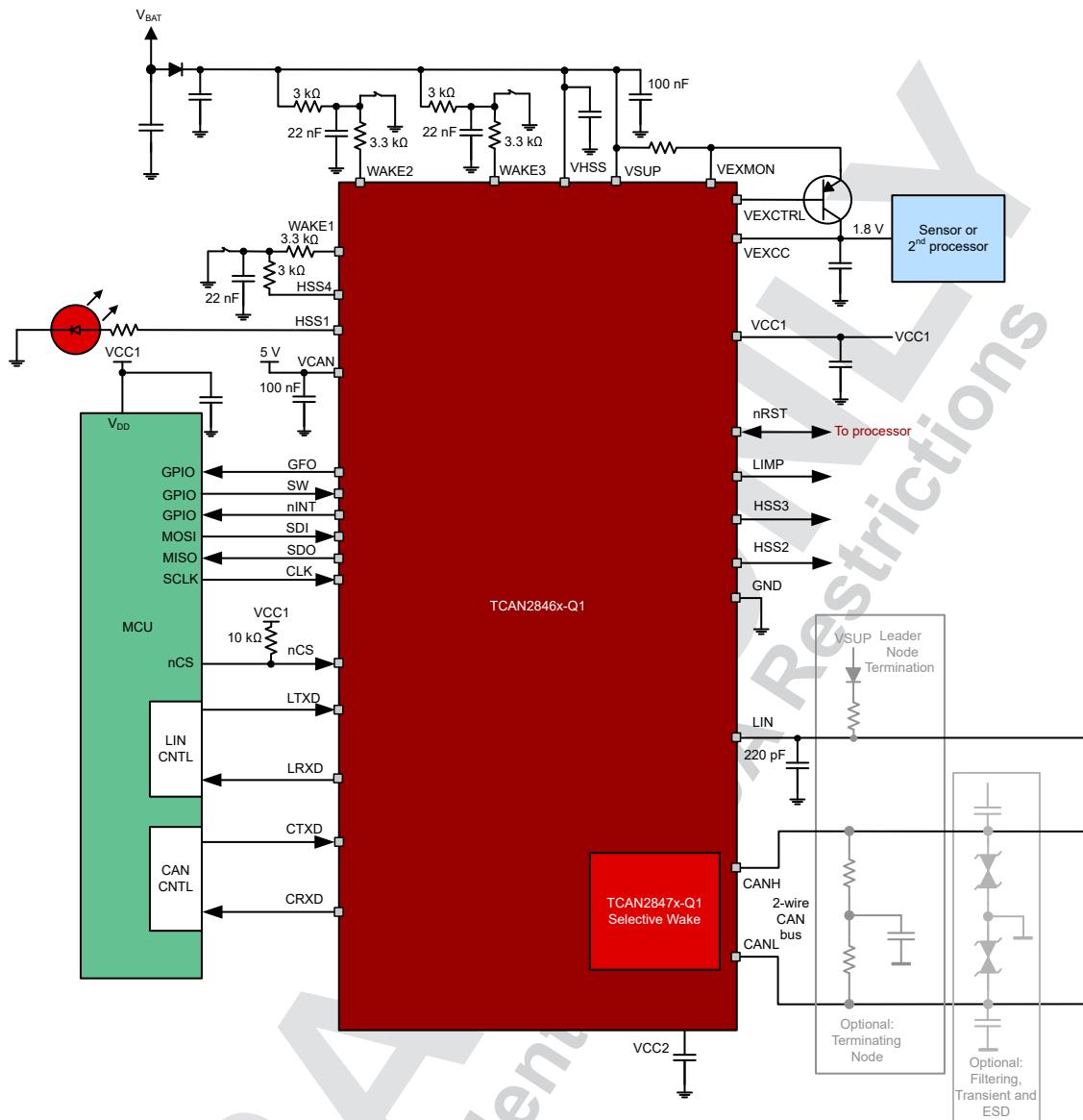


Figure 8-30. Application drawing with cyclic sensing configuration

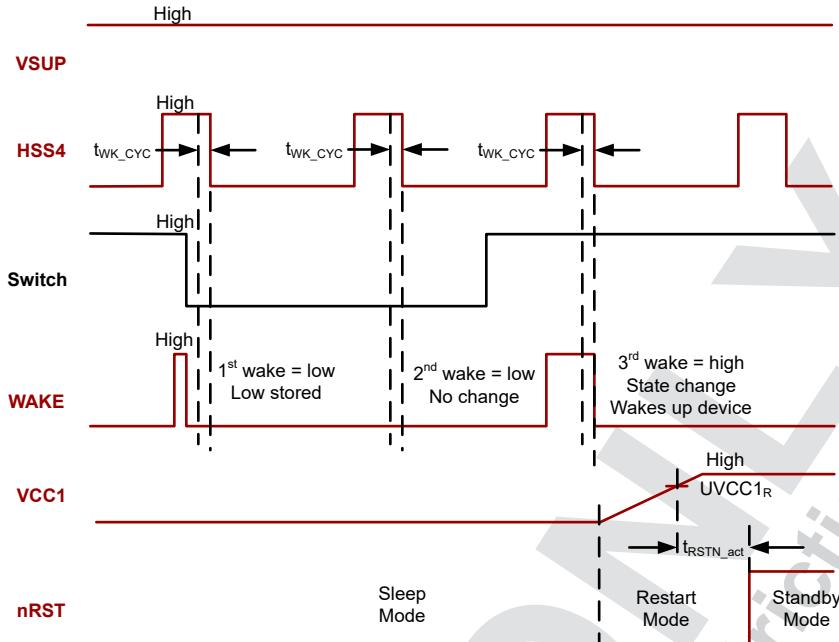


Figure 8-31. Cyclic sensing timing diagram

8.4.6.1.4 Cyclic Wake

Cyclic Wake is similar to cyclic sensing wake in that it uses timer1 or timer2 to periodically wake. For Cyclic Wake, at the start of the programmed on time, the device will pull nINT low for programmed-on time and release. The first on time pulse is ignored but each afterwards causes the interrupt. Cyclic wake is enabled by using register 8'h25[3] for timer1 or 8'h26[3] for timer2. When enabled, this function will work in normal and standby mode. This can be enabled in fail-safe, register 8'h1A[0]=1b. As VCC1 is off in fail-safe mode, nINT pin will not be utilized. When enabled, in fail-safe mode the period selected for the timer needs to be 500 ms, 1 s or 2 s. When the on time takes place, the device will determine if a fault is still present. If fault has not cleared the device stays in fail-safe mode and will repeat the process until the SWE timer times out at which time the device will transition to sleep mode. If fault has cleared, this will be treated like a wake event and the device will transition to restart mode. This can be enabled in sleep mode, register 8'h4F[4]=1b, if VCC1 is present.

8.5 Selective Wake-up

The TCAN284xx-Q1 performs CAN communication according to ISO 11898-1 and Bosch CAN protocol specification 3.2.1.1.

8.5.1 Selective Wake Mode (TCAN2845x-Q1 and TCAN2847x-Q1)

This is the medium level of power saving mode of the device. The WUF receiver is turned on and connected internally to the frame detection logic is looking for a Wake-Up Frame (WUF) as outlined in the Frame Detection section of the datasheet. The CAN bus data is not put on the RXD pin in this state. The device is supplied via the VSUP supply coming from the system battery.

The valid wakes up sources in selective wake mode are:

- Wake-Up Frame (WUF)
- WAKE pin local wake up (LWU). Event on WAKE pin must match the programmed requirements for WAKE pin in register 8'h11[7:6]
- Frame Overflow (FRAME_OVF)
- SPI command to another state

If a WUF and/or LWU event occurs, the corresponding wake event flag (WUF and/or LWU) flag is set. At this point, an interrupt is provided to the MCU using the nINT pin if enabled or by pulling down the RXD pin.

To enter selective wake mode, the following conditions must be met:

- Selective Wake Configured, SWCFG, flag is set
 - All Selective Wake registers must be written followed by a read to ensure they are programmed correctly for the proper frame detection and selective wake configuration. Once configured, the SWCFG bit should be set to 1b.
- Selective Wake Error, SWERR, flag is cleared
- Set Selective Wake Enable (SW_EN) = 1b, register 8'h10[7] = 1b

If a frame is incoming during the transition it may be lost and frame detection may not sync to the frames for an additional four incoming CAN frames.

Note

If a fault condition or FRAME_OVF forces the device into sleep mode, fail-safe mode disabled, or into fail-safe mode; SW_EN is disabled turning off selective wake function.

8.5.2 Frame Detection

The frame detection logic is what enables processing of serial data, or CAN frames, from the CAN bus. The device has Selective Wake Control Registers to set up the device to look for a programmed match using either the CAN ID (11 bit or 29 bit), or the CAN ID plus the data frame including data masking. If the detected CAN frame received from the bus matches the configured requirements in the frame detection logic it is called a Wake-Up Frame (WUF).

Before Frame Detection may be enabled or used the data needed for validation, or match, of the WUF needs to be correctly configured in the device registers. Once the device has been correctly configured to allow frame detection, or selective wake function the SWCFG (Selective Wake Configuration) must be set to load the parameters for WUF for the device. If a valid WUF is detected it is shown via the CANINT flag, including selective wake up.

When Frame Detection is enabled several other actions may take place as the logic is decoding the CAN frames the device receives on the bus. These include error detection and counting and the indication of reception of a CAN frame via the CAN_SYNC and CAN_SYNC_FD flags.

If a Frame Overflow (FRAME_OVF) occurs while in Frame Detection mode, it is disabled, clearing the SW_EN bit.

When Frame Detection is enabled transitioning from a mode where the receiver bias is not on up to four CAN frames for 500kbps and slower data rates and up to eight CAN frames for greater than 500kbps may be ignored by the device until the Frame Detection is stabilized.

The procedure to correctly configure the device to use frame detection and selective wake up is:

- Write all control registers for frame detection (selective wake), Selective Wake Config 1-4 (Registers 8'h44 through 8'h47), and ID and ID mask (Registers 8'h30 and 8'h40)
- Recommend reading all Selective Wake registers, allowing the software to confirm the device was written and thus configured properly
- Set Selective Wake Configured (SWCFG) bit to 1b, register 8'h4F[7] = 1b
- Set Selective Wake Enable = 1b, register 8'h10[7] = 1b
- Set device into standby mode by SPI write to 8'h10[2:0] = 100b. Step must be done even if already in standby mode.

If a SWERR interrupt then occurs from the Frame Overflow flag, the Frame Overflow interrupt needs to be cleared, and then the SWCFG bit must be set again to 1b.

8.5.3 Wake-Up Frame (WUF) Validation

When the following conditions are all met the received frame shall be valid as a Wake-Up Frame (WUF):

- The received frame is a Classical CAN data frame when DLC (Data Length Code) matching is not disabled. The frame may also be a remote frame when DLC matching is disabled.

- The ID (as defined in ISO 11898-1:2015, 8.4.2.2) of the received Classical CAN frame is exactly matching a configured ID in the relevant bit positions. The relevant bit positions are given by an ID-mask illustrated in [Section 8.5.5](#)
- The DLC (as defined in ISO 11898-1:2015, 8.4.2.4) of the received Classical CAN data frame is exactly matching a configured DLC. See the mechanism illustrated in [Section 8.5.6](#). Optionally, this DLC matching condition may be disabled by configuration in the implementation.
- When the DLC is greater than 0 and DLC matching is enabled, the data field (as defined in ISO 11898-1:2015, 8.4.2.5) of the received frame has at least one bit set in a bit position which corresponds to a set bit in the configured data mask. See the mechanism illustrated in [Section 8.5.5](#).
- A correct cyclic redundancy check (CRC) has been received, including a recessive CRC delimiter, and no error (according to ISO 11898-1:2015, 10.11) is detected prior to the acknowledgment (ACK) Slot.

8.5.4 WUF ID Validation

The ID of the received frame matches the configured ID in all required bit positions. The relevant bit positions are determined by the configured ID in 8'h30 through 8'h33 and the programmed ID mask in 8'h34 and 8'h38. Classic Base Frame Format (CBFF) 11-bit Base ID and Classic Extended Frame Format (CEFF) 29-bit Extended ID and ID masks are supported. All masked ID bits except "do not care" must match exactly the configured ID bits for a WUF validation. If the masked ID bits are configured as "do not care" then both "1" and "0" are accepted in the ID. In the ID mask register a 1 represents "do not care".

[Figure 8-32](#) shows an example for valid WUF ID and corresponding ID Mask register

Configured ID	1	0	0	0	1	0	1	0	0	1	0																																																
Mask Register	c	c	c	c	c	c	c	c	d	d	d																																																
<i>d = don't care</i> <i>c = care</i>																																																											
Valid WUF IDs																																																											
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td></td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td></td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td></td></tr> </table>												1	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	1		1	0	0	0	1	0	1	0	0	1	0		1	0	0	0	1	0	1	0	0	1	1	
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1	0	0	0	1	0	1	0	1	x	x																																																	
1	0	0	0	1	0	1	1	0	x	x																																																	
1	0	0	0	1	0	1	1	1	x	x																																																	
1	0	0	0	1	0	0	0	0	x	x																																																	

Figure 8-32. ID and ID Mask Example for WUF

8.5.5 WUF DLC Validation

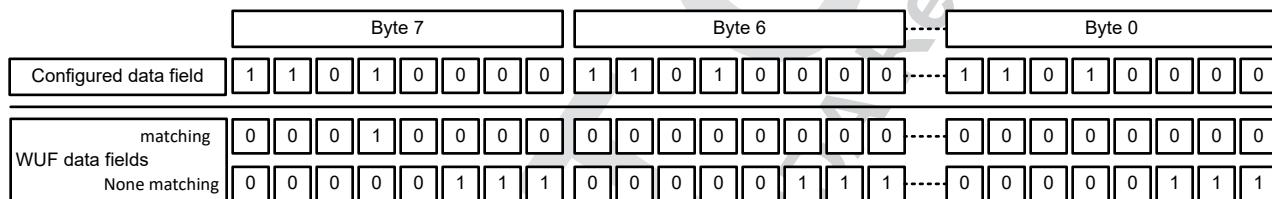
The DLC (Data Length Code) of the received frame must match exactly the configured DLC if the data mask bit is set. The DLC is configured in 8'h38[4:1]. The data mask bit is set in 8'h38[0].

Table 8-4. DLC

Frames	Data Length Code				Number of Data Bytes
	DLC3	DLC2	DLC1	DLC0	
Classical Frames & FD Frames	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
Classical Frames	1	0 or 1	0 or 1	0 or 1	8

8.5.6 WUF Data Validation

When the Data mask is enabled via the data mask bit, the data of the received frame must match the configured Data where at least one logic high (1) bit within the data field of the received frame matches a logic high (1) of the data field within the configured data. The relevant bit positions are determined by the configured Data in 8'h39 through 8'h40 and enabled by Data mask enable in 8'h38[0]. An example of a matching and non-matching Data is shown in [Figure 8-33](#)


Figure 8-33. Data Field Validation for WUF Example

The selective wake data validation ensures that the last byte sent on the bus will be interpreted as data mask byte 0. This means for 8 bytes of data, the first byte sent is interpreted as data mask byte 7. For a DLC of 3, the last byte sent on the bus will be interpreted as data mask byte 0 and the first byte sent is interpreted as data mask byte 2. [Figure 8-34](#) provides a few examples of which bytes would be used for various bytes sent and received.

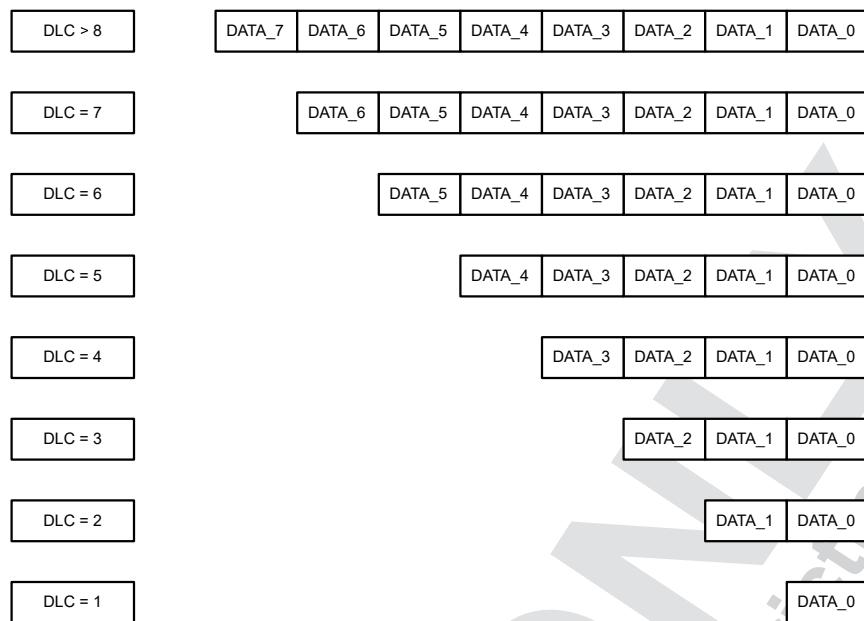


Figure 8-34. Data register mask values for different DLC values

8.5.7 Frame error counter

Upon activation of the selective wake up function and upon the expiration of $t_{SILENCE}$ the CAN frame error counter is set to zero. This error counter determines the CAN frame errors detected by the device. It is in $8'h45$ and the error counter is called FRAME_CNTx.

The initial counter value is zero and is incremented by 1 for every received frame error detected (stuff bit, CRC or CRC delimiter form error). The counter is decremented by 1 for every correctly received CAN frame assuming the counter is not zero. If the device is set for passive on CAN with flexible data rate frames, any frame detected as a CAN FD frame has no impact on the frame error counter (no increment or decrement). If a valid Classical CAN frame has been received and the counter is not zero the counter shall be decremented by one. Dominant bits between the CRC delimiter and the end of the intermission field does not increase the frame error counter.

On each increment or decrement of the error counter, the decoder unit waits for nBits_idle recessive bits before considering a dominant bit as a start of frame (SOF). See [Figure 8-35](#) for the position of the mandatory start of frame detection when classic CAN frame was received and in case of error scenario.

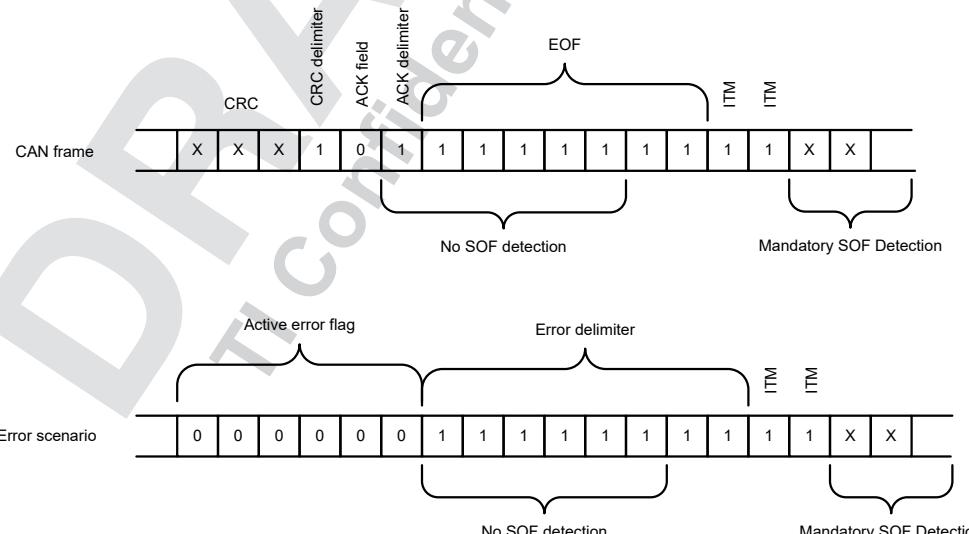


Figure 8-35. Mandatory SOF Detection after Classic CAN Frames and Error Scenarios

The default value for the frame error counter threshold is 31, so that on the 32nd error, the frame overflow flag (FRAME_OVF) is set.

Up to four (or eight when bit rate > 500 kbps) consecutive Classic CAN data and remote frames that start after the bias reaction time, t_{Bias} , has elapsed might be either ignored, no error counter increase or failure, or judged as erroneous (error counter increases even in case of no error).

Received a frame in CEFF with non-nominal reserved bits (SRR, r0) are not led to an increase of the error counter.

The frame error counter is compared to the frame error counter threshold, FRAME_CNT_THRESHOLD in 8'h46. If the counter overflows the threshold the frame error overflow flag, FRAME_OVF, is set. The default value for the frame error counter threshold is 31 so that on the 32nd error the overflow flag is set. However, if the application requires a different frame error count overflow threshold the required value may be programmed into the FRAME_CNT_THRESHOLD register.

The counter is reset by the following: disabling the frame detection, CANSLNT flag set, and setting register 8'h51[2] = 1b.

The description for the errors detected:

- **Stuff bit error:** A stuff bit error is detected when the 6th consecutive bit of the same state (level) is received. CAN message coding should have had a stuff bit at this bit position in the data stream.
- **CRC error:** The CRC sequence consists of the result of the CRC calculation by the transmitting node. This device calculates the CRC with the same polynomial as the transmitting node. A CRC error is detected if the calculated result is not the same as the result received in the CRC sequence.
- **CRC delimiter error:** The CRC delimiter error is detected when a bit of the wrong state (logic low / dominant) is received in the CRC delimiter bit position which is defined as logic high (recessive).

8.5.8 CAN FD Frame Tolerance

After receiving a FD Format indicator (FDF) followed by a dominant res bit, the decoder unit waits for n_{Bits_idle} recessive bits before considering a further dominant bit as a SOF as per [Figure 8-35](#). [Table 8-5](#) defines n_{Bits_idle} .

Table 8-5. Number of Recessive Bits Prior to Next SOF

Parameter	Notation	Value	
		Min	Max
Number of recessive bits before a new SOF is accepted	n_{Bits_idle}	6	10

There are two bitfilter options available to support different combinations of arbitration and data phase bit rates. Register 8'h47[4] is where the pBitfilter option is selected.

- Bitfilter 1: A data phase bit rate \leq four times the arbitration rate or 2 Mbps whichever is lower shall be supported
- Bitfilter 2: A data phase bit rate \leq ten times the arbitration rate or 5 Mbps whichever is lower shall be supported

Dominant signals \leq the minimum pBitfilter, see [Table 8-6](#), of the arbitration bit time in duration is not considered valid and does not restart the recessive bit counter. Dominant signals \geq the maximum of pBitfilter of the arbitration bit time duration restart the recessive bit counter.

Table 8-6. Number of Recessive Bits Prior to Next SOF

Parameter	Notation	Value	
		Min	Max
CAN FD data phase bitfilter 1	pBitfilter1	5.00%	17.50%
CAN FD data phase bitfilter 2	pBitfilter2	2.50%	8.75%

8.5.9 8Mbps Filtering

- Bitfilter 3: A data phase bit rate \leq 16 times the arbitration rate or 8 Mbps whichever is lower shall be supported
- pBitfilter 3 Min 1.25% to Max 4.375%

8.6 Protection Features

The TCAN284xx-Q1 has several protection features that are described as follows.

8.6.1 Fail-safe Features

The TCAN284xx-Q1 has a fail-safe mode that can be used to reduce node power consumption for a node system issue. This can be separated into two operation modes, sleep and failsafe modes.

8.6.1.1 Sleep Mode via Sleep Wake Error

The sleep wake error (SWE) timer ($t_{INACTIVE}$) is a timer used to determine if specific functions are not working or if communication between the device and processor is valid. This feature cannot be disabled for power up. At power up with VCC1_CFG = 10b for SBC mode control, if the device has not had the PWRON flag cleared or been placed into normal mode, it will enter sleep mode when $t_{INACTIVE}$ times out. If VREG_CONFIG1 register 8'h0D[7:6], VCC1_CFG has been set to 01b for always on and the SWE timer times out while the device is in normal or standby modes, the device will transition to restart mode. The SWE timer can be disabled for the other scenarios that causes the device to enter fail-safe mode by setting SWE_DIS; 8'h10[5] = 1b and FS_DIS at 8'h10[6] = 1b. See [Figure 8-36](#) for information on which modes the SWE timer start in and when.

The device wakes up if the CAN or LIN bus provides a WUP or a local wake event takes place thus entering standby mode. Once in standby mode, the $t_{SILENCE}$ and $t_{INACTIVE}$ timers start. If the $t_{INACTIVE}$ expires the device re-enter sleep mode. When the device receives a CANINT, LWU or FRAME_OVF such that the device leaves sleep mode, entering restart mode and then enters standby mode, the processor has the programmed SWE timer time to clear the flags or place the device into normal mode. If this does not happen, the device will enter either restart mode or sleep mode depending upon the programmed value of VCC1_CFG. When in standby or normal mode and the CANSLNT flag persists for $t_{INACTIVE}$, the device enters sleep mode. Examples of events that could create this are the processor is no longer working and not able to exercise the SPI bus, a go to sleep command comes in and the processor is not able to receive it or is not able to respond. See [Figure 8-37](#).

Note

- When VCC1 is enabled on for sleep mode a SWE timer time-out will cause the device to transition to restart mode instead of sleep mode. This will cause the nRST pin to be pulled low to reset the processor and set the WKERR and SMS interrupt flags.
- A SWE timer time-out does not impact VCC2 or VEXCC if enabled on for sleep mode.

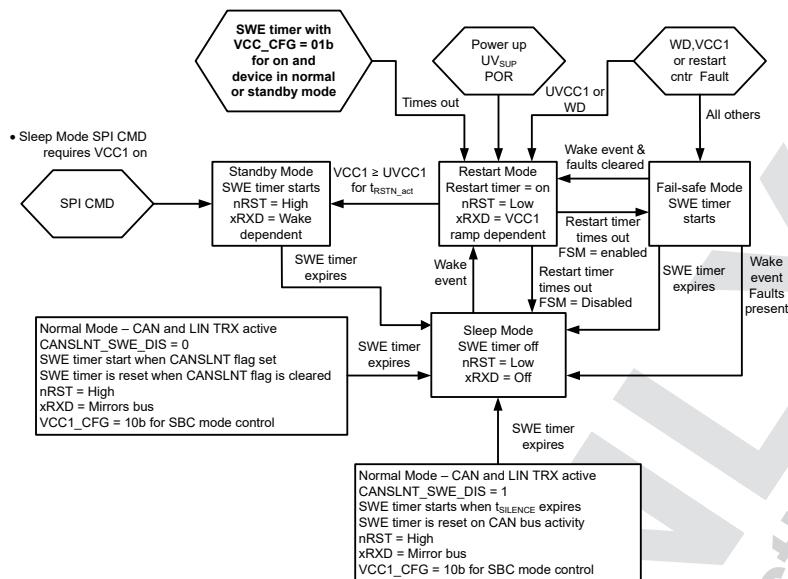
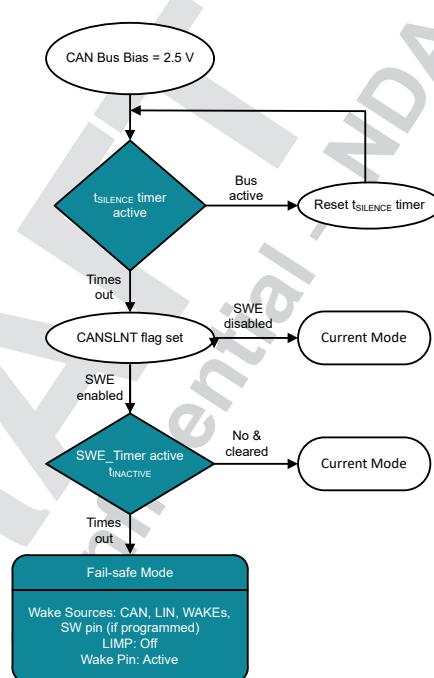


Figure 8-36. SWE Timer by Mode

Note

The restart counter can be either t_{RSTTO} or $t_{INACTIVE}$ (SWE timer) and is selected using register 8'h4F[0], RSTRT_TMR_SEL.



Note

This figure is based upon the CAN FD transceiver being on or in listen only states.

Figure 8-37. Normal and Standby to Fail-safe Mode

8.6.2 Device Reset

The TCAN245x-Q1 family has three methods to reset the device. Two are accomplished with SPI commands and are a soft reset and hard reset. Soft reset and hard reset are accomplished by writing a 1b to DEVICE_RST register 8'h19[1] for soft reset or to 8'h19[0] for hard reset. nRST can be used as a full power on reset by pulling nRST low for t_{NRSTIN} .

When performing a soft reset, the following takes place:

- Saved EEPROM registers are reloaded
- All other registers are reset to default values
- VCC1 and VCC2 do not change state
- Device transitions to standby mode

When performing a hard reset, the following takes place:

- Device transitions to Init mode
- Saved EEPROM registers are reloaded
- All other registers are reset to default values
- Most of the internal device logic is reset to default
- VCC1 and VCC2 do not change state
- Device then transitions to restart mode and finally to standby mode where the device can be reprogrammed

When pulling nRST pin low and releasing, the following takes place:

- Device transitions to Init mode
- Saved EEPROM registers are reloaded
- All other registers are reset to default values
- Most of the internal logic is reset to default
- VCC1 and VCC2 do not change state
- Device then transitions to restart mode and finally to standby mode where the device can be reprogrammed

Note

It is recommended that any changes to registers that are stored into EEPROM should be saved to EEPROM as a reset causes these registers to be loaded from EEPROM. This would overwrite unsaved changes with the last-saved register values from EEPROM.

8.6.3 Driver and Receiver Function

The TXD and RXD pins are input and output between the processor and the CAN FD and LIN physical layer transceivers. The digital logic input and output levels for these devices are TTL levels with respect to VCC1 for compatibility with protocol controllers having 3.3 V or 5 V logic. [Table 8-7](#) and [Table 8-8](#) provides the states of the CAN driver and CAN receiver in each mode.

Table 8-7. Driver Function Table

Transceiver State	TXD Input	Bus Outputs			Driven Bus State
		CANH	CANL	LIN	
CAN On	L	H	L	NA	Dominant
	H or Open	Z	Z	NA	Biased Recessive
LIN On	L	NA	NA	L	Dominant
	H or Open	NA	NA	H	Biased Recessive
Wake capable (CAN)	X	Z	Z	Z	Weak Pull to GND
Wake capable (LIN)	X	NA	NA	H	
Off	X	Z	Z	Z	

Table 8-8. CAN Receiver Function Table

Transceiver State	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus States	RXD Terminal
On/Listen	$V_{ID} \geq 0.9 \text{ V}$	Dominant	L
	$0.5 \text{ V} < V_{ID} < 0.9 \text{ V}$	Undefined	Undefined
	$V_{ID} \leq 0.5 \text{ V}$	Recessive	H
Wake capable	$V_{ID} \geq 1.15 \text{ V}$	Dominant	See Figure 8-23
	$0.4 \text{ V} < V_{ID} < 1.15 \text{ V}$	Undefined	
	$V_{ID} \leq 0.4 \text{ V}$	Recessive	
Off	Open ($V_{ID} \approx 0 \text{ V}$)	Open	H

8.6.4 Floating Terminals

There are internal pull ups and pull downs on critical terminals to place the device into known states if the terminal floats. See [Table 8-9](#) for details on terminal bias conditions.

Table 8-9. Terminal Bias

TERMINAL	PULL-UP or PULL-DOWN	COMMENT
SW	350 kΩ Pull-down or Pull-up	When SW pin is active high pin weakly biases input to GND When SW pin is active low pin weakly biases input to either VCC1 or internal voltage rail
CLK	350 kΩ Pull-up	Weakly biases input
SDI	350 kΩ Pull-up	Weakly biases input
nCS	350 kΩ Pull-up	Weakly biases input so the device is not selected
nRST	30 kΩ Pull-up	Pulled-up to VCC1
LIN	45 kΩ Pull-up	Weakly biases
LTXD	350 kΩ Pull-up	Weakly biases input
CTXD	350 kΩ Pull-up	Weakly biases input

Note

The internal bias should not be relied upon as only termination, especially in noisy environments but should be considered a fail-safe protection. Special care needs to be taken when the device is used with MCUs utilizing open drain outputs.

8.6.5 TXD Dominant Time Out (DTO)

The TCAN284xx-Q1 supports dominant state time out on both the LIN and CAN busses. This is an internal function based upon the TXD path. The TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant (LOW) longer than the time out period t_{TXD_DTO} . The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time out constant of the circuit, t_{TXD_DTO} , the bus driver is disabled. This frees the bus for communication between other nodes on the network. The driver is re-activated when a recessive signal (HIGH) is seen on TXD terminal; thus, clearing the dominant time out. The receiver remains active and the RXD terminal reflects the activity on the CAN bus and the bus terminals is biased to recessive level during a TXD DTO fault. This feature can be disabled by using register 8'h10[6] TXD.DTO.DIS for CAN and 8'h1D[5] LIN1.TXD.DTO.DIS for LIN.

Note

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame.

8.6.6 LIN Bus Stuck Dominant System Fault: False Wake Up Lockout

The device contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current use. [Figure 8-38](#) and [Figure 8-39](#) show the behavior of this protection.

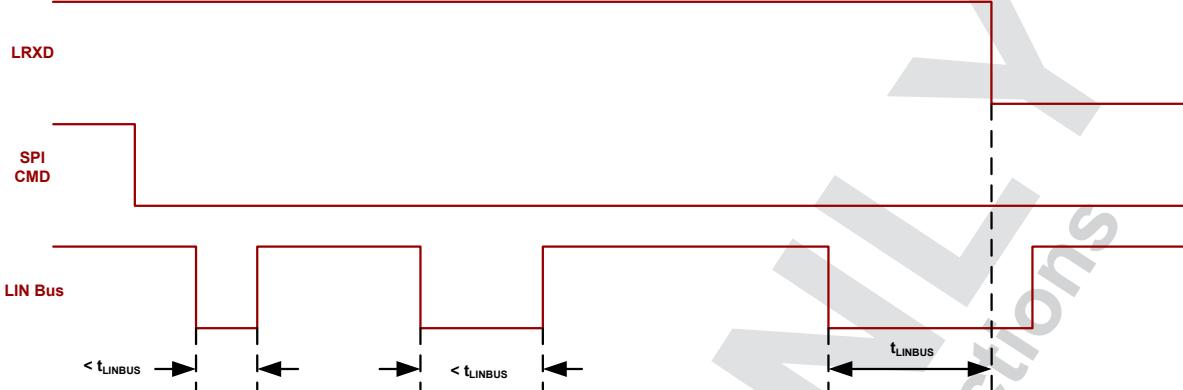


Figure 8-38. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wake Up

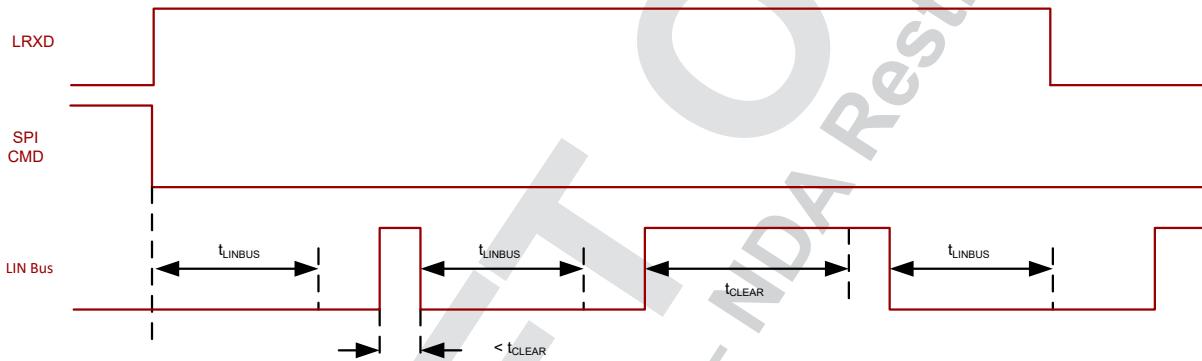


Figure 8-39. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wake Up

8.6.7 CAN Bus Short Circuit Current Limiting

These devices have several protections features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting (dominant and recessive). The device has TXD dominant time out which prevents permanently having the higher short circuit current of dominant state for a system fault. During CAN communication the bus switches between dominant and recessive states; thus, the short circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings the average short circuit current should be used. The percentage dominant is limited by the TXD dominant time out and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and inter frame space. These make sure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

Note

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated using [Equation 3](#).

$$I_{OS(AVG)} = \%Transmit \times [(\%REC_Bits \times I_{OS(SS)}_REC) + (\%DOM_Bits \times I_{OS(SS)}_DOM)] + [\%Receive \times I_{OS(SS)}_REC] \quad (3)$$

Where

- $I_{OS(AVG)}$ is the average short circuit current.
- %Transmit is the percentage the node is transmitting CAN messages.
- %Receive is the percentage the node is receiving CAN messages.
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages.
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages.
- IOS(SS)_REC is the recessive steady state short circuit current and IOS(SS)_DOM is the dominant steady state short circuit current.

Note

The short circuit current and possible fault cases of the network should be taken into consideration when sizing the power ratings of the termination resistance, other network components, and the power supply used to generate VSUP.

8.6.8 Thermal Shutdown

The TCAN284x-Q1 has two thermal sensors in the device to monitor the junction temperature of the die.

1. Coveres VCC1 LDO and external PNP control, VEXCC
2. Covers VCC2 LDO, CAN transceiver and LIN transceiver

There is a thermal shutdown pre-warning provided that is set when the junction temperature of VCC1 LDO, and external PNP control, VEXCC, hits the warning temperature level. When this temperature sensor reaches the pre-warning rising, TSDWR, an interrupt will be set for pre-warning. There are three interrupts a thermal event. The behavior of the device depends upon which sensor hits the thermal event. This is a device preservation feature.

- INT_6 register 8'h5C[7] is TSDW interrupt
- INT_2 register 8'h52[1] is TSD_VCC1_VEXCC interrupt
- INT_3 register 8'h53[1] is TSD_CAN_LIN interrupt which includes VCC2 LDO

Exceeding the maximum junction temperature for $> t_{TSD}$ will cause interrupt flags to be set and is indicated by pulling nINT low. If VCC1 or VEXCC causes the TSD event; the device will turn off these LDOs and enter either fail-safe mode (if enabled) or sleep mode. The nRST pin is pulled to ground during this TSD event. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the TSDF temperature for 1s, the device will transition from fail-safe mode to restart mode and turn on VCC1 and VEXCC (if enabled). A thermal shut down interrupt flag is set but not indicated on nINT pin as VCC1 is off. This event will turn off the high side switches by resetting the HSS1-4_CNTL registers. If thermal shutdown event happens while the device is in fail-safe or sleep mode and cyclic sensing is enabled, the cyclic sensing function will be lost as HSS4 will be turned off.

If TSD is detected by the second sensor which covers the transceivers and VCC2. Both CAN and LIN transmitters will be disabled placing them into listen mode. VCC2 LDO will be disabled and the interrupt flag will be set. This does not cause an SBC state change. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the TSDF temperature, the CAN and LIN transmitters will be re-enabled. After 1s of further wait time, VCC2 LDO will be turned on. Note that UVCC2 will not get set here because the LDO has been disabled. Read VCC2_STATUS at register 8'h4F[2] to determine when VCC2 has been re-enabled. If VCC2 is used in the system as the supply source for VCAN, then the VCC2 off condition will create a UVCAN condition. The CAN transceiver will change to wake capable, and will cannot be re-enabled until VCC2 is fully powered again. VCC2_STATUS is also indicating the status of VCAN. When VCC2_STATUS=1b, the CAN transceiver is re-enabled and UVCAN interrupt flag can be cleared.

8.6.9 Under/Over Voltage Lockout and Unpowered Device

The TCAN284xx-Q1 monitors all of the supply rails of the device, both input (VSUP, VHSS and VCAN) and output (VCC1, VCC2 and VEXCC). For the input supply rails, all are monitored for under-voltage and VHSS can be monitored for over-voltage. For the output supply rails, all are monitored for under-voltage, over-voltage and short circuit failures. Each of these fault events have a corresponding interrupt with VSUP and VCC1 faults causing device SBC mode changes. See [Table 8-10](#) for the relationship between VSUP, VCC1, VCC2 and VEXCC faults.

The TCAN284xx-Q1 monitors VCC1, VCC2 and VEXCC for over-voltage condition. Over-voltage is represented by OVCC1, OVCC2 and OVEXCC. The TCAN284xx-Q1 monitors VCC1, VCC2 and VEXCC for short to ground conditions. Short to ground is represented by VCC_{133SC}, VCC_{15SC}, VCC_{2SC} and VEXCC_{SC}.

The TCAN284xx-Q1 monitors the high-side switches supply voltage, VHSS, for over-voltage events. This can be disabled by writing 1b to 8'h4F[7], HSS_OV_DIS. Under-voltage is monitored on the HVSS supply, UVHSS. This can be disabled by writing 1b to 8'h4F[6], HSS_UV_DIS. The HSS switches will automatically recover from an OVHSS or UVHSS unless disabled by writing 1b to 8'h4F[5], HSS_OV_UV_REC.

Table 8-10. VSUP, VCC1, VCC2 and VEXCC Faults and Device Mode

VSUP	VCC1	VCC2	VEXCC	Device Mode
> UVSUP	> UVCC1	> UVCC2	NA	Normal or Standby
> UVSUP	< UVCC _{1PR}	> UVCC2	NA	Previous Mode
> UVSUP	< UVCC1	> UVCC2	NA	Restart
> UVSUP	> UVCC1	< UVCC2	NA	Previous Mode
> UVSUP	> UVCC1	> UVCC2	< UVEXCC	Previous Mode
< UVSUP	NA	NA	NA	UVSUP
> UVSUP	> OVCC1	NA	NA	Fail-safe or Sleep
> UVSUP	> UVCC1	> OVCC2	NA	Previous Mode
> UVSUP	> UVCC1	NA	< OVEXCC	Previous Mode
> UVSUP	< VCC _{1SC}	NA	NA	Fail-safe or Sleep
> UVSUP	> UVCC1	< VCC _{2SC}	NA	Previous Mode
> UVSUP	> UVCC1	NA	< VEXCC _{SC}	Previous Mode

Note

If a permanent fault on VCC1 takes place and fail-safe mode is disabled, it is possible to get into a loop between restart and sleep mode due to wake events and VCC1 SBC fault.

- It is recommended to enable fail-safe mode when VCC1 is programmed on for sleep mode.
- To avoid the loop situation for a permanent fault with fail-safe mode enabled, it is recommended to use FSM_CONFIG register 8'h17[7:4] = 0100b which is FSM_CNT_R_ACT and places the device into sleep mode with LDOs off until a power cycle reset takes place.

8.6.9.1 Under-voltage

The device monitors VSUP, VHSS, VCAN, VEXCC, VCC1 and VCC2 for under-voltage events. Under-voltage events are represented by UVSUP_{xR/F}, UVHSS_{R/F}, UVCAN_{R/F}, VCC1_{xR/F}, UVCC2_{R/F} and UVEXCC_{xR/F}. The x represents the voltage level, R is when voltage level is ramping up and F is when voltage level is ramping down. Behavior of the device is dependent upon when supply rail is in under-voltage.

VCC1 is the LDO that provides power for the digital input/output pins and is expected to be connected to the node processor. VCC1 has a under-voltage pre-warning threshold and four programmable under-voltage threshold. When the under-voltage pre-warning event takes place an interrupt will be set, INT_6 register 8'h5C[6] and the nINT pin will be pulled low. Once VCC1 reaches one of the programmed thresholds, SBC_CONFIG1 register 8'h0E[4:3], the device to transition to restart mode and latch nRST low until the LDO voltage exceeds the under-voltage rising threshold. nRST will remain latched low and the device will stay in restart mode for t_{RSTN_act} after clearing the UV threshold. For UVCC1, there is a filter time, t_{UVFLTR}, that under-voltage event must last longer than for the device to enter restart mode.

8.6.9.1.1 VSUP and VHSS Under-voltage

VSUP is the primary input supply rail required for the device to function properly. There are three voltage levels monitored by the device, power on reset and two under-voltage level. For all functions and output voltage rails

to be in regulation the device must exceed UVSUP_{5R}. A UVSUP event places the device into a protected state, UVSUP. If VSUP is in under-voltage, the device loses the supply source needed to keep the internal regulators in regulation. This causes the device to go into a state where communication between the microprocessor and the TCAN284xx-Q1 is disabled. In this mode the device is still active but VCC1, VCC2 and VEXCC may be experiencing under voltage events and other functions will not be active, like watchdog. No mode change can take place. The TCAN284xx-Q1 is not able to receive information from the bus; and thus, does not pass any signals from the bus, including any Bus Wake via BWRR signals to the microprocessor. VCC1 determines which UVSUP level, UVSUP_{33R/F} or UVSUP_{5R/F}, is utilized for this. If VSUP keeps ramping down and drops below VSUP_{(PU)F}, the device will enter powered off state. When VSUP returns, the device comes up as if it is an initial power on. All registers are cleared and the device has to be reconfigured from the stored EEPROM values that were retained. In UVSUP state, the device will have some functionality. The LDOs will be in pass through mode until VSUP ≥ UVSUP_{xxR} and VCC1 exceeds its UVCC1_{xRx} level. At this time, the device will transition to restart mode.

For devices where VCC1 is 5 V, UVSUP_{5R/F} is the only VSUP under-voltage rail monitored. When VSUP drops below UVSUP_{5F}, The CAN and LIN transceivers are turned off and the device enters a protected UVSUP state and LDOs are in pass thru mode. See [Table 8-11](#) for relationship between VSUP, VCC1₅, VCAN, device mode and transceivers.

When VCC1 is 3.3 V, both UVSUP_{33R/F} and UVSUP_{5R/F} are monitored. When powering up, VSUP has to exceed UVSUP_{33R} for VCC1 to be in regulation and above UVSUP_{5R} for VCC2 and other functions of the device to work properly. When VSUP is ramping down, UVSUP_{5F} is the first UVSUP level that will set an UVSUP5 interrupt flag, register 8'h52[4], and will turn off the CAN transceiver but the LIN transceiver is still functioning but may not meet the data sheet electrical and timing specifications. If VSUP keeps dropping, the next level is UVSUP_{33F}. When this is reached, the UVSUP₃₃ interrupt flag will be set, register 8'h52[3]. When this level is reached, the LIN transceiver is turned off and the device enters UVSUP mode. See [Table 8-12](#) for relationship between VSUP, VCC1₃₃, VCAN, device mode and transceivers.

Under-voltage on the high-side switches power, VHSS, is indicated by interrupt INT_4 register 8'5A[0] UVHSS. How the high-side switches behave due to an UVHSS event is determined by HSS_CNTL3 register 8'h4F[6:5].

Table 8-11. Under-voltage Events for VCC1₅, Device State and Transceiver State

VSUP	VCC1	VCAN	DEVICE STATE	CAN TRANSCEIVER	LIN TRANSCEIVER
> UVSUP ₅	> UVCC1 ₅	> UVCAN	Normal or Standby	As Programmed	As Programmed
> UVSUP ₅	< UVCC1 ₅	NA	Restart	Wake capable or off	Wake capable or off
> UVSUP ₅	> UVCC1 ₅	> UVCAN	Previous State	As Programmed	As Programmed
> UVSUP ₅	> UVCC1 ₅	> UVCAN	Previous State	As Programmed	As Programmed
< UVSUP ₅	> NA	NA	UVSUP	Off	Off
> UVSUP ₅	< UVCC1 ₅	< UVCAN	Previous State	Wake capable or off	As Programmed

Table 8-12. Under-voltage Events for VCC1₃₃, Device State and Transceiver State

VSUP	VCC1	VCAN	DEVICE STATE	CAN TRANSCEIVER	LIN TRANSCEIVER
> UVSUP ₅	> UVCC1 ₃₃	> UVCAN	Normal or Standby	As Programmed	As Programmed
> UVSUP ₅	< UVCC1 ₃₃	NA	Restart	Wake capable or off	Wake capable or off
> UVSUP ₅	> UVCC1 ₃₃	> UVCAN	Previous State	As Programmed	As Programmed
< UVSUP ₅ > UVSUP ₃₃	> UVCC1 ₃₃	NA	Normal or Standby	Off	As Programmed
< UVSUP ₅ > UVSUP ₃₃	< UVCC1 ₃₃	NA	Restart	Off	Off
< UVSUP ₃₃	NA	NA	UVSUP	Off	Off
> UVSUP ₅	> UVCC1 ₃₃	< UVCAN	Normal or Standby	Wake capable or off	As Programmed

Note

- If a thermal shut down or short circuit event takes place while the regulator is in UV, the device transitions to sleep mode (fail-safe mode disabled) or fail-safe mode if enabled.
- When UVCC1 does not clear by the time the restart timer expires, the device will determine if fail-safe mode is enabled. If not enabled the device will transition to sleep mode and turn off VCC1. When VCC1 is enabled on for sleep mode, an UVCC1 event will proceed in the same manner.
- OVSUPHSS is not shown in the table as it only impacts the high-side switches.

8.6.9.1.2 VCC1 Under-voltage

VCC1 is the LDO that provides power for the digital input/output pins and is expected to be connected to the node processor. VCC1 is monitored for under-voltage and has two levels that are monitored, pre-warning ($UVCC1_{XPR}$) and under-voltage ($UVCC1_{XXR/FX}$). The under-voltage has one of four levels that can be programmed using register 8'h0E[4:3], $UVCC1_SEL$. Of the supply rails providing external power, VCC1 is the only one considered an SBC fault which will cause a state change. When the under-voltage pre-warning event takes place an interrupt will be set, INT_6 register 8'h5C[6] and the nINT pin will be pulled low. Once VCC1 reaches one of the programmed thresholds, SBC_CONFIG1 register 8'h0E[4:3], the device will transition to restart mode and latch nRST low until VCC1 exceeds the under-voltage rising threshold. nRST will remain latched low and the device will stay in restart mode for t_{RSTN_act} after clearing the UV threshold. For UVCC1, there is a filter time, t_{UVFLTR} , that the under-voltage event must last longer than for the device to enter restart mode. See [Figure 8-40](#) for UVCC1 behavior.

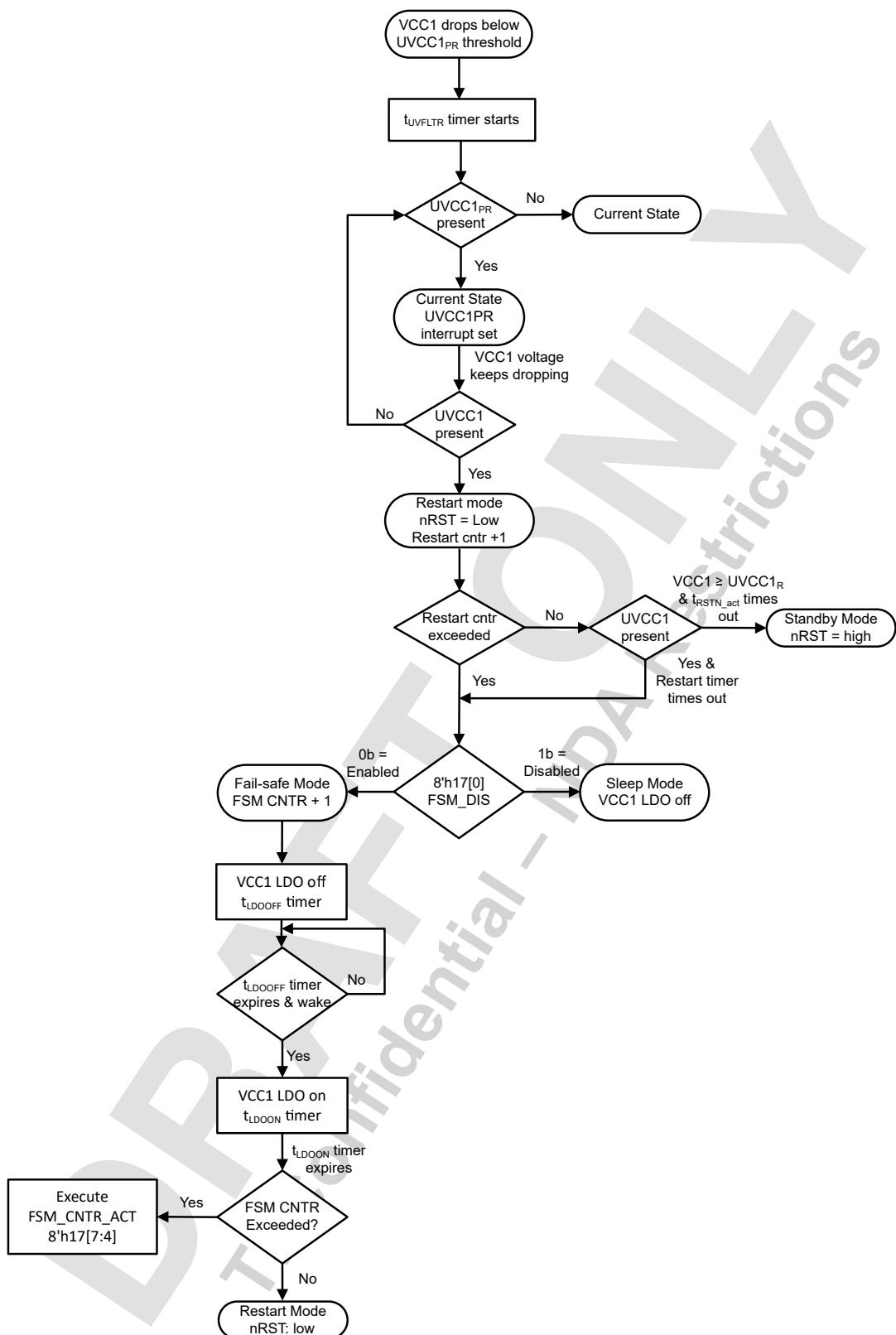


Figure 8-40. UVCC1 State Diagram

Note

When VCC1_CFG = 01b for VCC1 always on, a wake event is not needed to exit fail-safe mode.

8.6.9.1.3 VCC2 and VEXCC Under-voltage

A UVCC2 or UVEXCC will set interrupt flags but do not cause a mode change. See [Figure 8-41](#) and [Figure 8-42](#) for under-voltage behavior

- Register INT_6; 8'h5C[5] is the interrupt for UVEXCC
- Register INT_6; 8'h5C[2] is the interrupt for UVCC2

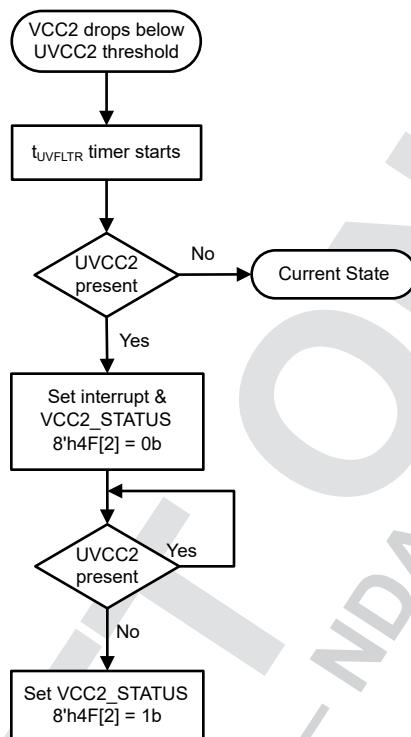


Figure 8-41. UVCC2 State Diagram

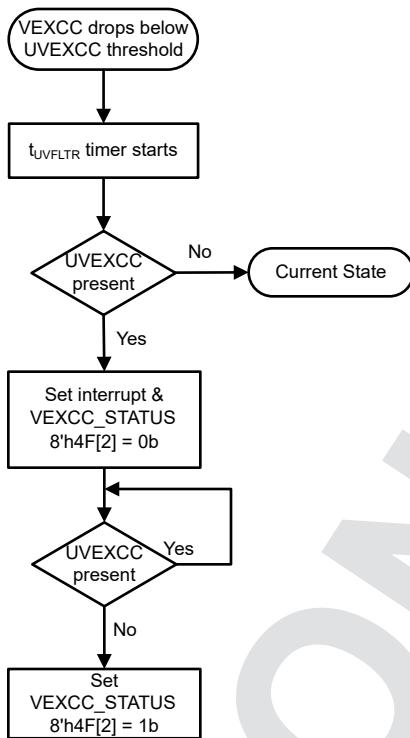
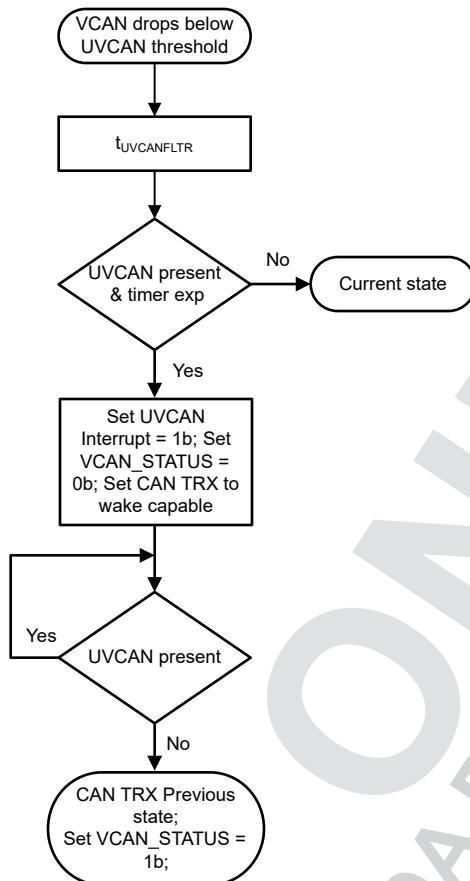


Figure 8-42. UVEXCC State Diagram

8.6.9.1.4 VCAN Under-voltage

If VCAN drops below UVCAN under-voltage detection the CAN transceiver switches off and disengage from the bus until VCAN has recovered. See [Figure 8-43](#) on how the device behaves. The device is designed to be an "ideal passive" or "no load" to the CAN bus if the device is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the network remains operational. Logic terminals also have extremely low leakage currents when the device is unpowered, so they do not load other circuits which may remain powered.

The UVLO circuit monitors both rising and falling edge of a power rail when ramping and declining.

**Figure 8-43. UVCAN State Diagram****Note**

- UVCAN comparator is only enabled when the CAN transceiver is programmed on or in listen.
- VCAN is required for EEPROM writes so VCAN_STATUS = 1b at register 8'h4F[1] needs to be checked before writing to the EEPROM.

8.6.9.2 VCC1, VCC2 and VEXCC Over-voltage

TCAN284xx-Q1 monitors VCC1, VEXCC and VCC2 for over-voltage condition. Over-voltage is represented by OVCC1, OVCC2 and OVEVCC. When OVCC1 occurs, the device enters either fail-safe mode, if enabled, or sleep mode. When OVCC2 or OVEVCC takes place, the LDOs are turned off and an interrupt flag is set but no mode change takes place. When entering fail-safe mode, the device turns off all the LDOs and starts the t_{LDOOFF} timer. After this timer times out, OVCC1 is checked for over-voltage. If the OV event has cleared, and a wake event has taken place, the device enters restart mode. If OVCC1 is still present, the device enters sleep mode. Wake events are monitored but not acted upon until t_{LDOOFF} time out. If no wake event has taken place and the OV event has cleared, the device is still in fail-safe mode until the SWE timer times out or a wake event takes place. See [Figure 8-44](#), [Figure 8-45](#) and [Figure 8-46](#) for device behavior during an over-voltage event.

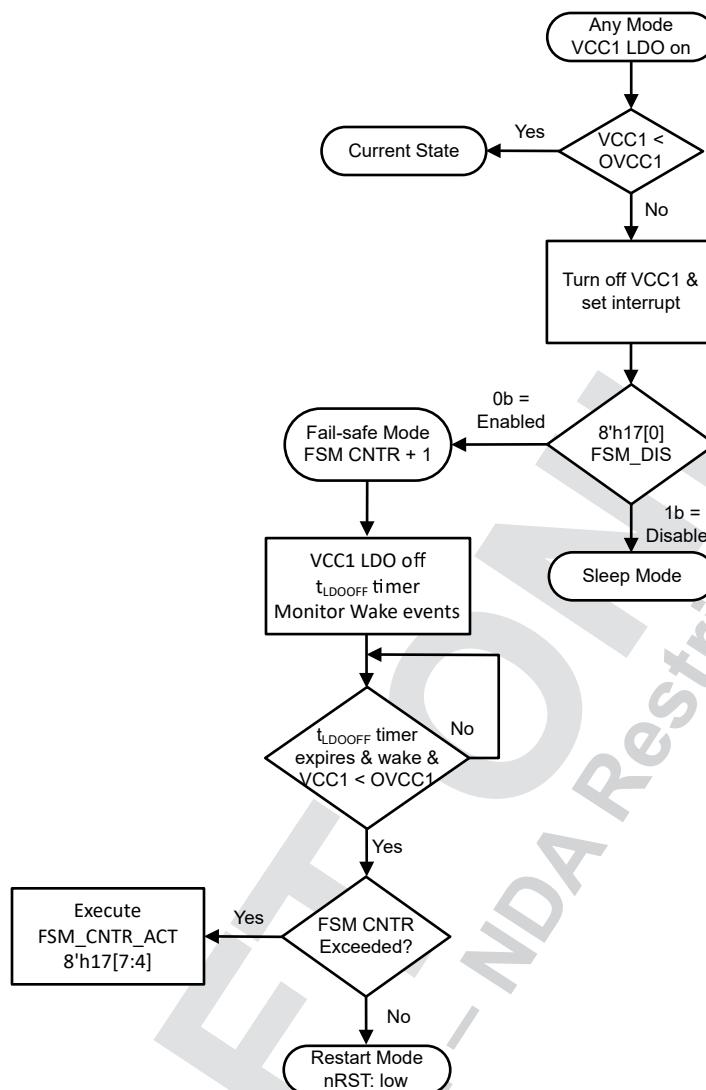


Figure 8-44. OVCC1 State Diagram

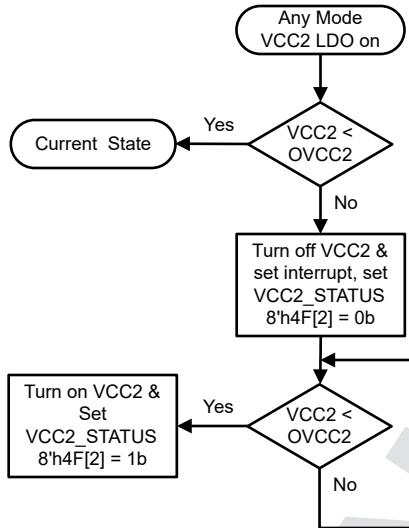


Figure 8-45. OVCC2 State Diagram

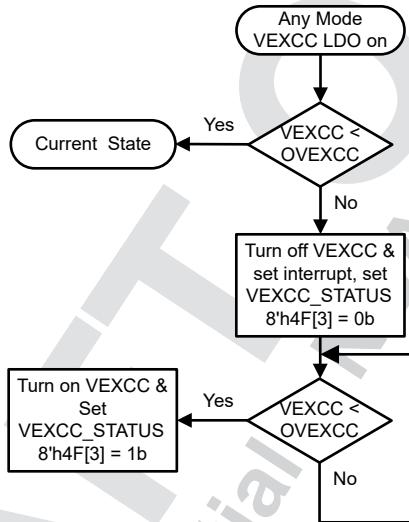


Figure 8-46. OVEXCC State Diagram

8.6.9.3 VCC1, VCC2 and VEXCC Short Circuit

The TCAN284xx-Q1 monitors VCC1, VEXCC and VCC2 (CAN LDO) for short to ground conditions. Short to ground is represented by $VCC1_{33SC}$, $VCC1_{5SC}$, $VCC2_{SC}$ and $VEXCC_{SC}$. A short to ground turns off the LDO. When a $VCC1_{SC}$ occurs, VCC1 is turned off for a minimum of t_{LDOOFF} , and the device enters fail-safe mode (if enabled) or sleep mode. During this time, wake events are monitored and preserved. A short circuit event cannot be monitored while the LDO is off. A wake event causes VCC1 to be turned on for t_{LDOON} to see if the SC event is still present. If still present, the device transitions to sleep mode. If not present, the device transitioned to restart mode. While in fail-safe mode, the SWE timer starts and if the fault is not cleared and a wake event has not taken place before the timer times out the device transitions to sleep mode. If fail-safe mode is disabled, the device transitions to sleep mode. See Figure 8-47, Figure 8-48 and Figure 8-49 for device behavior during a short to ground event.

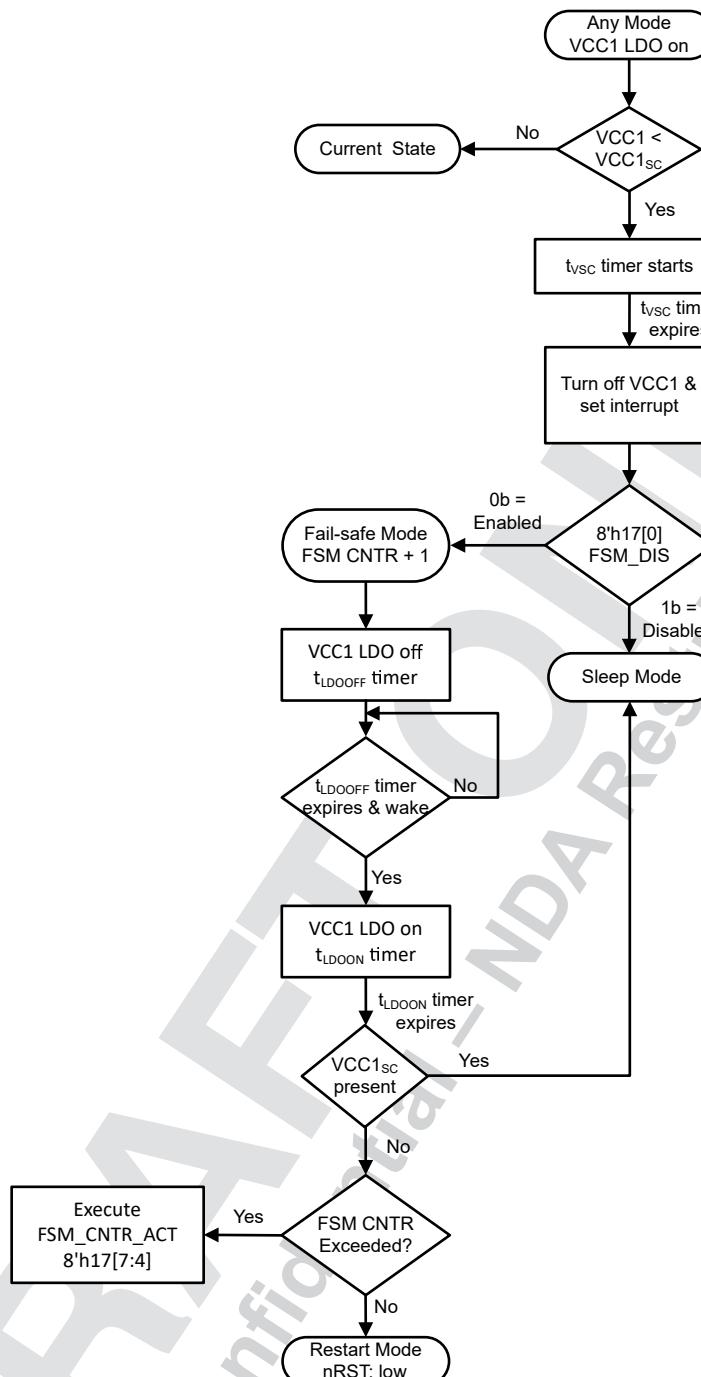
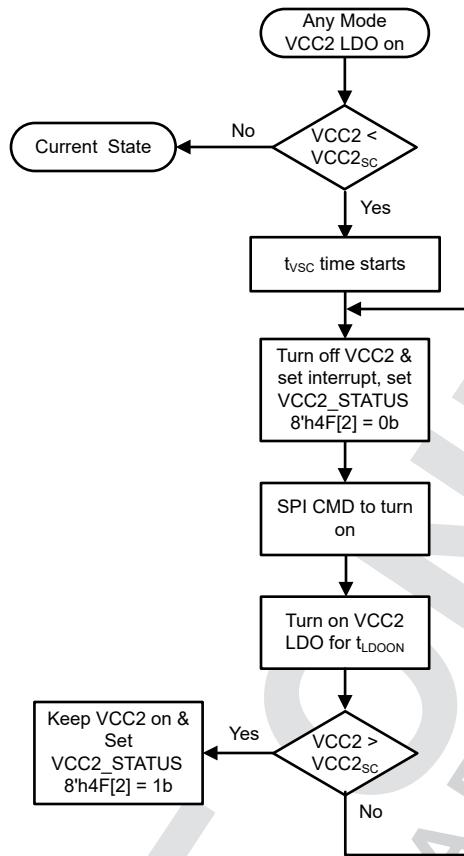


Figure 8-47. VCC1_{SC} State Diagram

Figure 8-48. VCC2_{SC} State Diagram

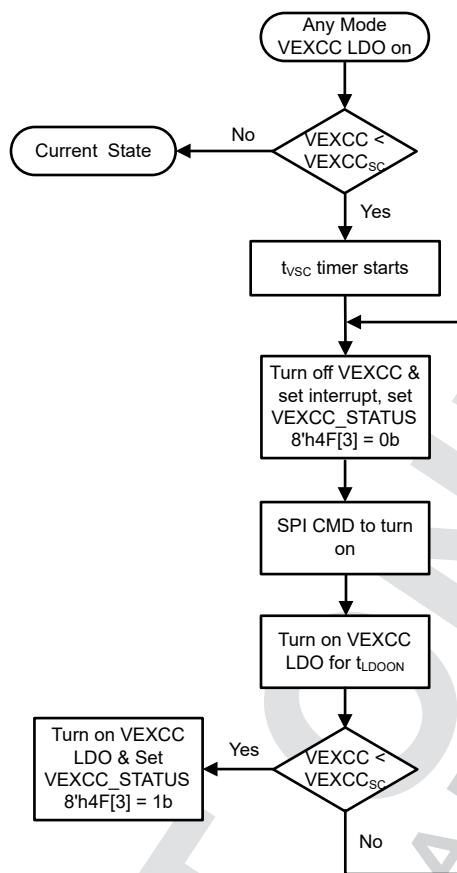


Figure 8-49. VEXCC_{sc} State Diagram

8.6.10 Watchdog

The TCAN284x-Q1 has an integrated watchdog function. The device provides a default window based, time-out and question and answer (Q&A) watchdog using SPI programming. The watchdog configuration and type can only be programmed when the device is in standby mode. Normal mode supports all three watchdog configurations while standby mode only supports time-out. When the device enters standby mode the watchdog configuration automatically changes to a time-out watchdog. When entering standby mode from restart mode, there is a nRST transition from low to high. This transition starts the t_{INITWD} timer, and includes the t_{RSTN_act} timer in restart mode. A WD trigger input must take place prior to this initial long window times out. When entering normal mode, the programmed watchdog timer starts based upon the programmed configuration. The watchdog timer is off in sleep, restart and fail-safe modes. The LIMP pin provides a limp home capability. When in sleep mode, the LIMP pin is off. When the error counter exceeds the watchdog trigger event level, the LIMP pin turns pulling the LIMP pin to ground as described in the LIMP pin section.

The watchdog has extensive configurability including the ability to select the time-out or Q&A watchdog. Watchdog is default enabled for standby mode, but can be disabled by setting register 8'h14[0] = 1b. Register 8'h13[7:6] can be set to 00b to disable the WD. There is a WD error counter available, see [Section 8.6.10.1](#) for description of this counter.

[Figure 8-50](#) and [Figure 8-51](#) provide a state diagram on the watchdog with and without it being active in standby mode.

ADVANCE INFORMATION

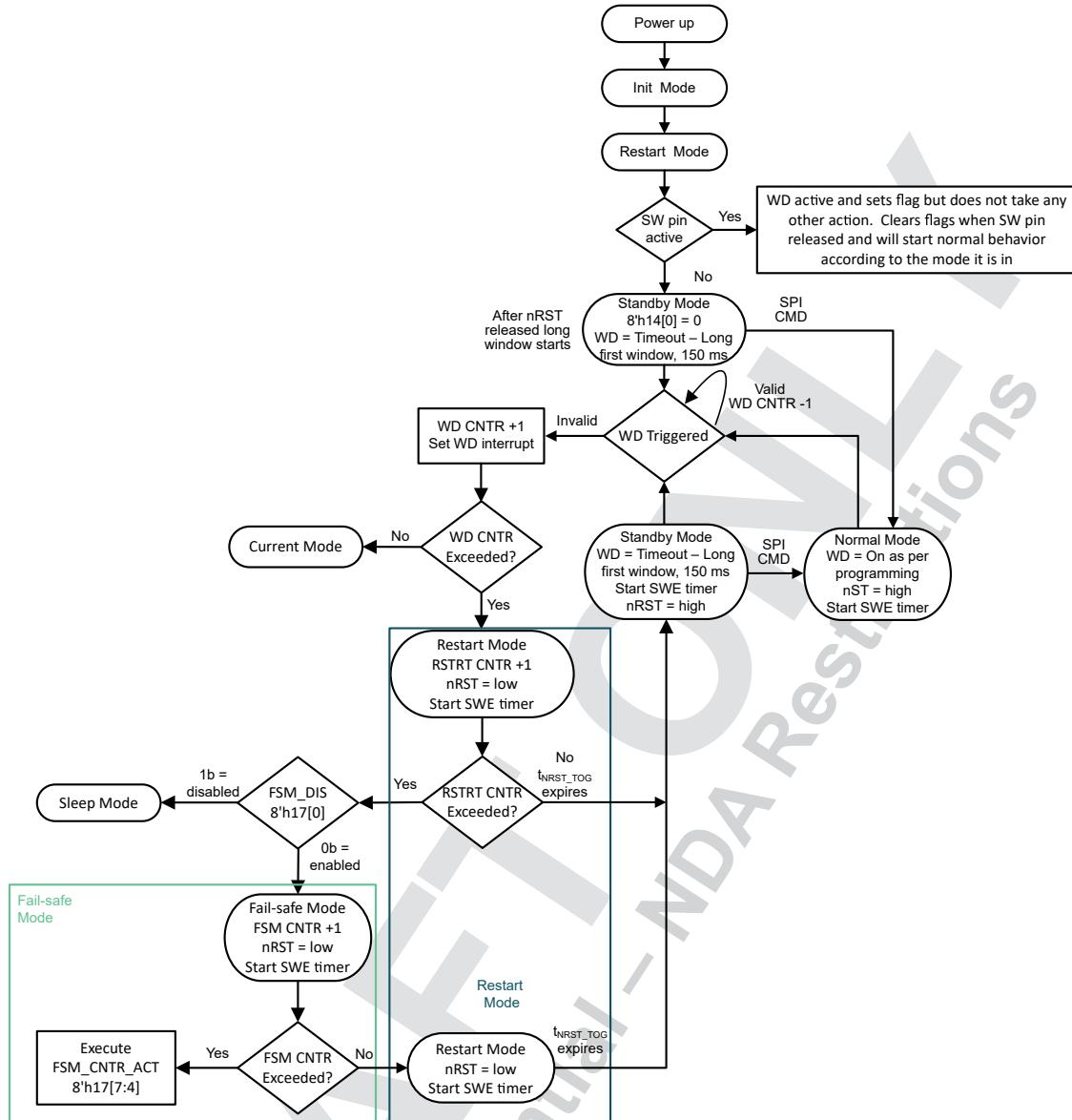


Figure 8-50. Watchdog State Diagram; Standby Mode Enabled

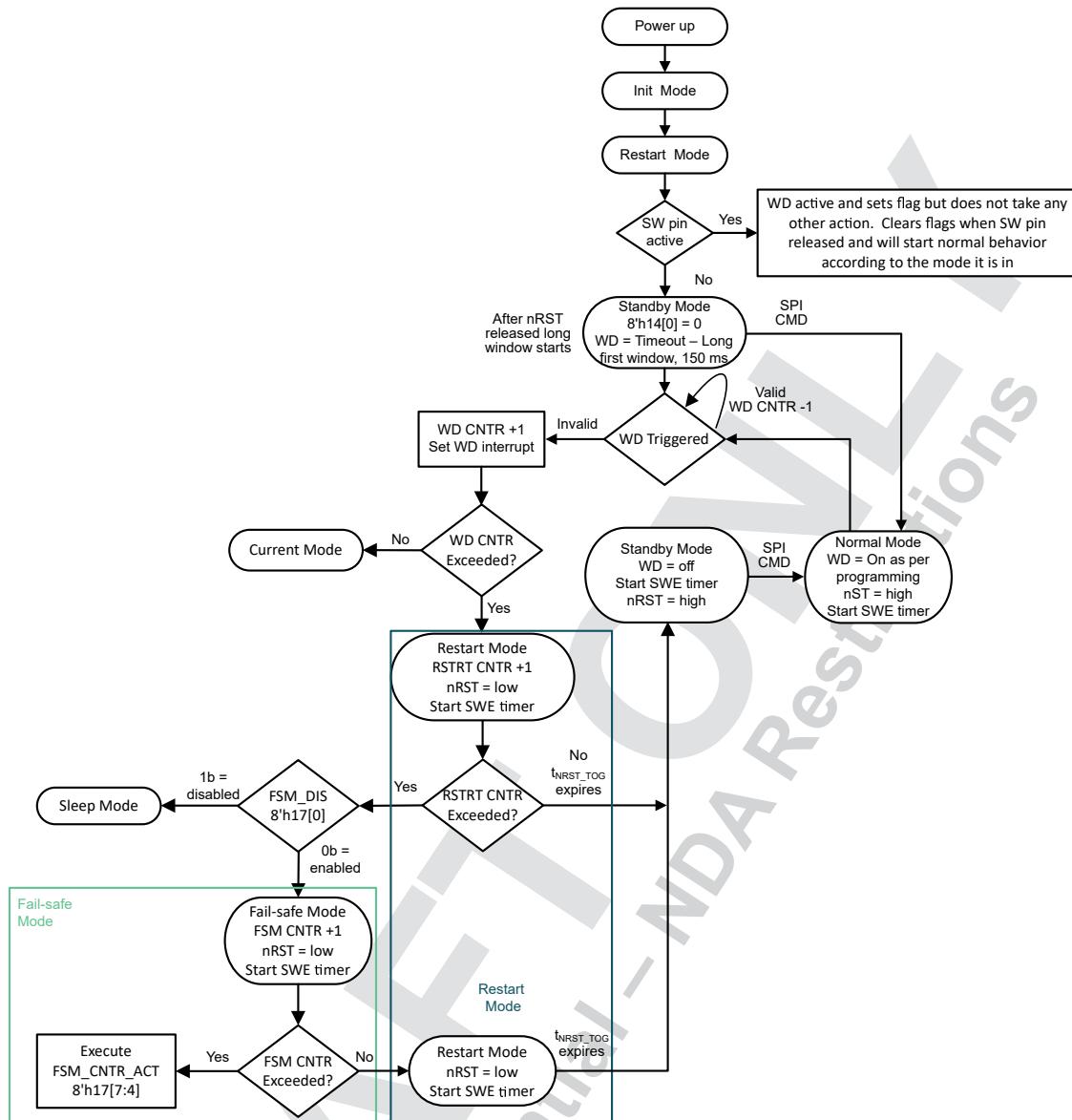


Figure 8-51. Watchdog State Diagram; Standby Mode Disabled

Note

- When the mode is changed while the timeout or window watchdog is running it will restart once entering the new mode, normal and standby.
- If the watchdog configuration is changed on-the-fly while the watchdog is running will reset the error counter to 0 and resets the watchdog timers.

8.6.10.1 Watchdog Error Counter and Action

The TCAN284x-Q1 has a watchdog error counter. This counter is an up down counter that increments for every missed window or incorrect input watchdog trigger event. For every correct input trigger, the counter decrements but does not drop below zero. The default trigger for this counter is to trigger a watchdog event is for every event. This counter can be configured at register 8'h16[7:4] which sets the limit for incorrect input triggers up to 15. The error counter can be read at register 8'14[4:1].

Once the programmed WD error counter limit has been exceeded, the device will transition to restart mode which will pull nRST low for t_{NRST_TOG} . The error counter resets back to 0 at this point. Once t_{NRST_TOG} times out

the device will transition back to standby mode releasing nRST high. If the WD failure causes the restart counter to exceed its programmed limit, the device will transition to either fail-safe mode if enabled or to sleep mode.

8.6.10.2 Watchdog SPI Programming

Registers 8'h13 through 8'h15 control the watchdog function. The TCAN284xx-Q1 watchdog can be set as a time-out watchdog or window watchdog by setting 8'h13[6] to the method of choice. The timer is based upon registers 8'h13[5:4] WD prescaler and 8'h14[7:5] WD timer and is in ms. See [Table 8-13](#) for the achievable times. If using smaller time windows, it is suggested to use the Time-out version of the watchdog. This is for times between 4 ms and 64 ms.

Table 8-13. Watchdog Window and Time-out Timer Configuration (ms)

WD_TIMER	8'h13[5:4] WD_PRE			
	00	01	10	11
000	4	8	12	16
001	32	64	96	128
010	128	256	384	512
011	256	384	512	768
100	512	1024	1536	2048
101	2048	4096	6144	8192
110	10240	20240	RSVD	RSVD
111	RSVD	RSVD	RSVD	RSVD

Note

If timing parameters are changed while the watchdog is running, the WD timer restarts to the new window automatically.

8.6.10.3 Watchdog Timing

The TCAN284xx-Q1 provides three methods for setting up the watchdog, window, time-out and question and answer. Question and Answer watch dog is covered in [Section 8.6.10.4](#). If more frequent, < 64 ms, input trigger events are desired it is suggested to us the time-out timer as this is an event within the time event and not specific to an open window.

When using the window watchdog, it is important to understand the closed and open window aspects. The TCAN284xx-Q1 is set up with a 50%/50% open and closed window and is based on an internal oscillator with a $\pm 10\%$ accuracy range. To determine when to provide the input trigger, this variance needs to be considered. Using the 64 ms nominal total window, t_{WINDOW} , provides a closed and open window that are each 32 ms. Taking the $\pm 10\%$ internal oscillator into account means t_{WINDOW} could be between 57.6 ms and 70.4 ms. The closed, t_{CLOSED} , and open window, t_{OPEN} , would then be between 22.4 ms and 35.2 ms. Using t_{WINDOW} of 57.6 ms and t_{CLOSED} of 35.2 ms, the total t_{OPEN} is 22.4 ms. The safe trigger area needs to happen at the 46.4 ms ± 11.2 ms which is half the t_{OPEN} min + t_{CLOSED} max. The same method is used for the other window values. [Figure 8-52](#) provides the above information graphically.

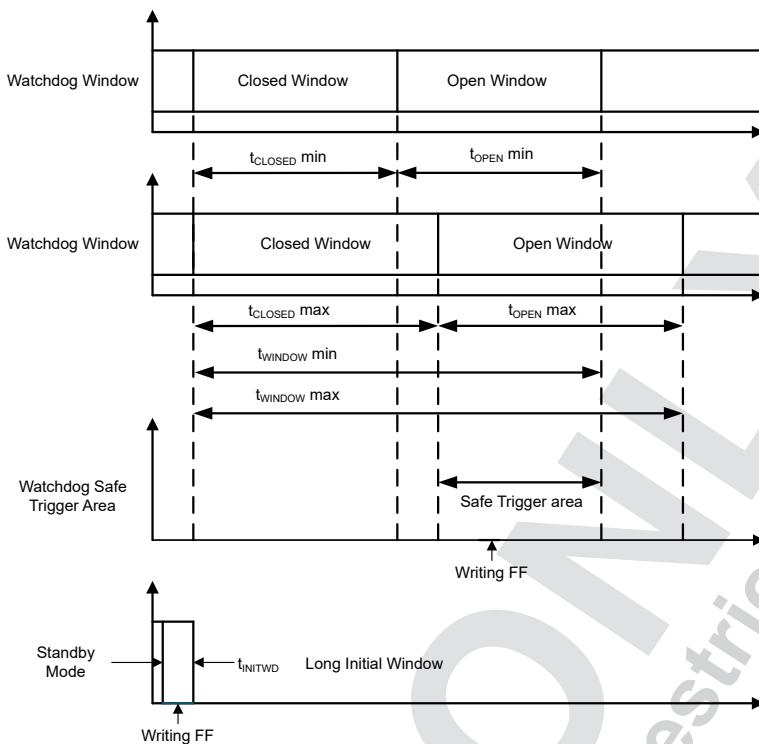


Figure 8-52. Watchdog Timing Diagram

8.6.10.4 Question and Answer Watchdog

The TCAN284x-Q1 devices include a question and answer watchdog selectable from SPI. Device defaults to window watchdog.

Section 8.6.10.4.3.1 explains the WD initialization events.

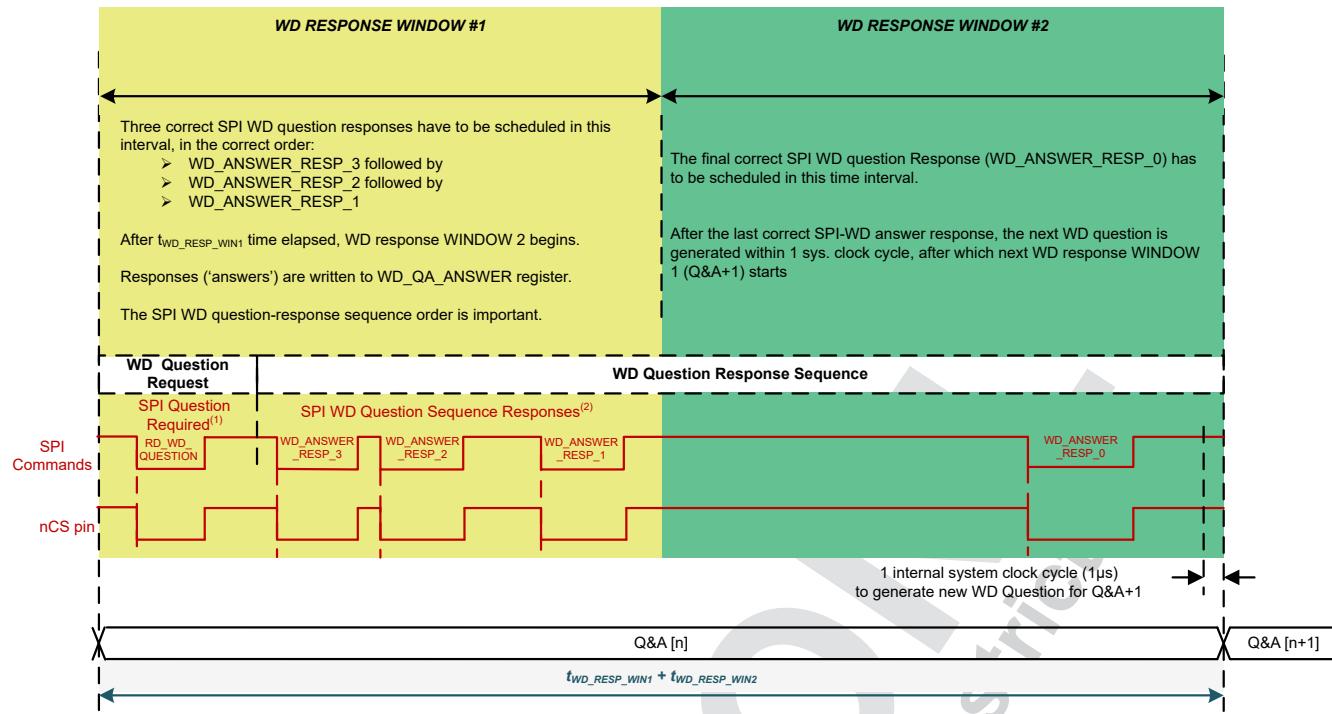
8.6.10.4.1 WD Question and Answer Basic Information

A Question and Answer (Q&A) watchdog is a type of watchdog where instead of simply resetting the watchdog via a SPI write, the MCU must read a ‘question’ from the TCAN284x-Q1, do math based on the question and then write the computed answers back to the TCAN284x-Q1. The correct answer is a 4-byte response. Each byte must be written in order and with the correct timing to have a correct answer.

There are 2 watchdog windows, referred to as WD Response window #1 and WD Response window #2 (Figure 8-53 WD QA Windows as example). The size of each window will be 50% of the total watchdog window time, $t_{WD_RESP_WIN1} + t_{WD_RESP_WIN2}$, which is selected from the WD_TIMER and WD_PRE register bits.

Each watchdog question and answer is a full watchdog cycle. The general process is that the MCU reads the question during WD Response Window #1. The CPU must perform a mathematical function on the question, resulting in 4 bytes of answers. 3 of the 4 answer bytes must be written to the answer register within the WD Response Window #1, in correct order. The last answer must be written to the answer register after the first response window, inside of WD Response Window #2. If all 4 answer bytes were correct and in the correct order, then the response is considered good, the error counter is decremented and a new question is generated, starting the cycle over again.

If anything is incorrect or missed, the response is considered bad and the watchdog question will NOT change. In addition, an error counter will be incremented. Once this error counter exceeds the threshold (defined in the WD_ERR_CNT_SET register field), the watchdog failure action will be performed. Examples of actions are an interrupt, or reset toggle, etc.



- The MCU is not required to request the WD question. The MCU can start with correct answers, WD_ANSWER_RESP_x bytes anywhere within RESPONSE WINDOW 1. The new WD question is always generated within one system clock cycle after the final WD_ANSWER_RESP_0 answer during the previous WD Q&A sequence run.
- The MCU can schedule other SPI commands between the WD_ANSWER_RESPx responses (even a command requesting the WD question) without any impact to the WD function as long as the WD_ANSWER_RESP[3:1] bytes are provided within the RESPONSE WINDOW 1 and WD_ANSWER_RESP_0 is provided within the RESPONSE WINDOW 2.

Figure 8-53. WD Q&A Sequence Run for WD Q&A Multi-Answer Mode

8.6.10.4.2 Question and Answer Register and Settings

There are several registers used to configure the watchdog registers, see [Table 8-14](#).

Table 8-14. List of Watchdog Related Registers

Register Address	Register Name	Description
0x16	WD_RST_PULSE	Sets error counter threshold
0x2D	WD_QA_CONFIG	Configuration related to the QA configuration
0x2E	WD_QA_ANSWER	Register for writing the calculated answers
0x2F	WD_QA_QUESTION	Reading the current QA question

The WD_CONFIG_1 and WD_CONFIG_2 registers mainly deal with setting up the watchdog window time length. Refer to [Table 8-13](#) to see the options for window sizes, and the required values for the WD_TIMER values and WD_PRE values. Take note that each of the 2 response windows are half of the selected value. Due to the need for several bytes of SPI to be used for each watchdog QA event, it is recommended that windows greater than 64 ms be used when using the QA watchdog functionality.

There are also different actions that can be performed when the watchdog error counter exceeds the error counter threshold.

8.6.10.4.3 WD Question and Answer Value Generation

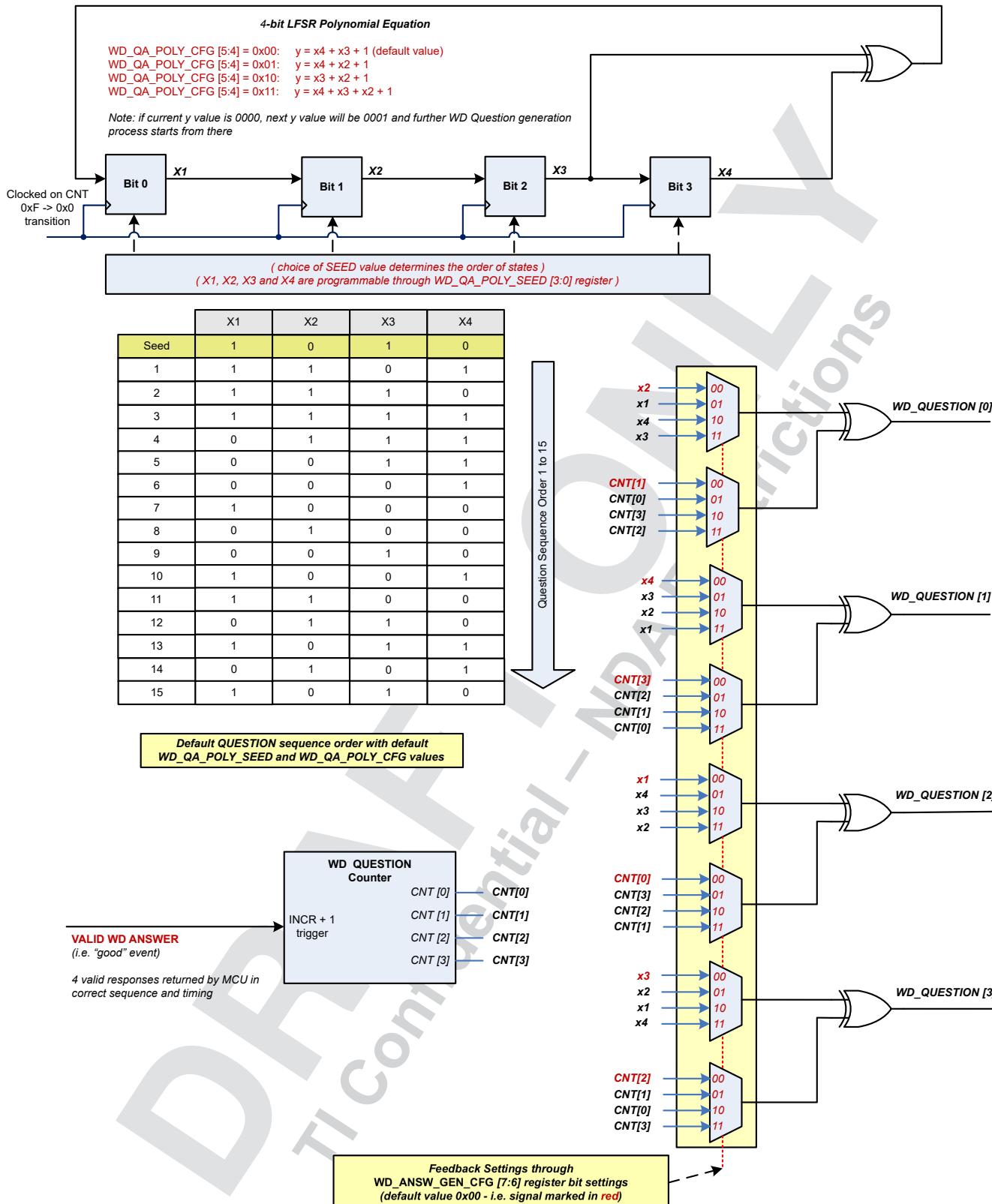
The 4-bit WD question, WD_QA_QUESTION[3:0], is generated by 4-bit Markov chain process. A Markov chain is a stochastic process with Markov property, which means that state changes are probabilistic, and the future state depends only on the current state. The valid and complete WD answer sequence for each WD Q&A mode is as follows:

- In WD Q&A multi-answer mode:
 1. Three correct SPI WD answers are received during RESPONSE WINDOW 1.
 2. One correct SPI WD answer is received during RESPONSE WINDOW 2.
 3. In addition to the previously listed timing, the sequence of four responses shall be correct.

The WD question value is latched in the WD_QUESTION bits of the WD_QA_QUESTION register and can be read out at any time.

The Markov chain process is clocked by the 4-bit Question counter at the transition from 1111b to 0000b. This includes the condition of a correct answer (correct answer value and correct timing response). The logic combination of the 4-bit questions WD_QA_QUESTION [3:0] generation is given in [Figure 8-54](#). The question counter is reset to default value of 0000b and the Markov chain is re-initialized to programmed register value when a watchdog fail puts the device in restart mode.

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- A. If the current y value is 0000, the next y value is 0001. The next watchdog question generation process starts from that value. Any changes to WD_QA_CONFIG register in Standby mode will re-initialize the Markov chain to the current register value. The question counter is not affected.

Figure 8-54. Watchdog Question Generation

Answer Comparison

The 2-bit, watchdog-answer counter, WD_ANSW_CNT[1:0], counts the number of received answer-bytes and controls the generation of the reference answer-byte as shown in [Figure 8-55](#). At the start of each watchdog sequence, the default value of the WD_ANSW_CNT[1:0] counter is 11b to indicate that the watchdog expects the MCU to write the correct Answer-3 in WD_QA_ANSWER[7:0].

The device sets the WD_QA_ERR status bit as soon as one answer byte is not correct. The device clears this status bit only if the MCU writes a '1' to this bit.

Sequence of the 2-bit Watchdog Answer Counter.

The sequence of the 2-bit, watchdog answer-counter is as follows for each counter value:

- WD_ANSW_CNT[1:0] = 11b:
 1. The watchdog calculates the reference Answer-3.
 2. A write access occurs. The MCU writes the Answer-3 byte in WD_QA_ANSWER[7:0].
 3. The watchdog compares the reference Answer-3 with the Answer-3 byte in WD_QA_ANSWER[7:0].
 4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 10b and sets the WD_QA_ERR status bit to 1 if the Answer-3 byte was incorrect.
- WD_ANSW_CNT[1:0] = 10b:
 1. The watchdog calculates the reference Answer-2.
 2. A write access occurs. The MCU writes the Answer-2 byte in WD_QA_ANSWER[7:0].
 3. The watchdog compares the reference Answer-2 with the Answer-2 byte in WD_QA_ANSWER[7:0].
 4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 01b and sets the WD_QA_ERR status bit to 1 if the Answer-2 byte was incorrect.
- WD_ANSW_CNT[1:0] = 01b:
 1. The watchdog calculates the reference Answer-1.
 2. A write access occurs. The MCU writes the Answer-1 byte in WD_QA_ANSWER[7:0].
 3. The watchdog compares the reference Answer-1 with the Answer-1 byte in WD_QA_ANSWER[7:0].
 4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 00b and sets the WD_QA_ERR status bit to 1 if the Answer-1 byte was incorrect.
- WD_ANSW_CNT[1:0] = 00b:
 1. The watchdog calculates the reference Answer-0.
 2. A write access occurs. The MCU writes the Answer-0 byte in WD_QA_ANSWER[7:0].
 3. The watchdog compares the reference Answer-0 with the Answer-0 byte in WD_QA_ANSWER[7:0].
 4. The watchdog sets the WD_QA_ERR status bit to 1 if the Answer-0 byte was incorrect.
 5. The watchdog starts a new watchdog sequence and sets the WD_ANSW_CNT[1:0] to 11b.

The MCU needs to clear the bit by writing a '1' to the WD_QA_ERR bit

Table 8-15. Set of WD Questions and Corresponding WD Answers Using Default Setting

QUESTION IN WD_QA_QUESTION REGISTER	WD ANSWER BYTES (EACH BYTE TO BE WRITTEN INTO WD_QA_ANSWER REGISTER)			
	WD_ANSWER_RESP_3	WD_ANSWER_RESP_2	WD_ANSWER_RESP_1	WD_ANSWER_RESP_0
WD_QUESTION	WD_ANSW_CNT[1:0] 11b	WD_ANSW_CNT[1:0] 10b	WD_ANSW_CNT[1:0] 01b	WD_ANSW_CNT[1:0] 00b
0x0	FF	0F	F0	00
0x1	B0	40	BF	4F
0x2	E9	19	E6	16
0x3	A6	56	A9	59
0x4	75	85	7A	8A
0x5	3A	CA	35	C5
0x6	63	93	6C	9C
0x7	2C	DC	23	D3
0x8	D2	22	DD	2D
0x9	9D	6D	92	62

Table 8-15. Set of WD Questions and Corresponding WD Answers Using Default Setting (continued)

QUESTION IN WD_QA_QUESTION REGISTER	WD ANSWER BYTES (EACH BYTE TO BE WRITTEN INTO WD_QA_ANSWER REGISTER)			
	WD_ANSWER_RESP_3	WD_ANSWER_RESP_2	WD_ANSWER_RESP_1	WD_ANSWER_RESP_0
WD_QUESTION	WD_ANSW_CNT[1:0] 11b	WD_ANSW_CNT[1:0] 10b	WD_ANSW_CNT[1:0] 01b	WD_ANSW_CNT[1:0] 00b
0xA	C4	34	CB	3B
0xB	8B	7B	84	74
0xC	58	A8	57	A7
0xD	17	E7	18	E8
0xE	4E	BE	41	B1
0xF	01	F1	0E	FE

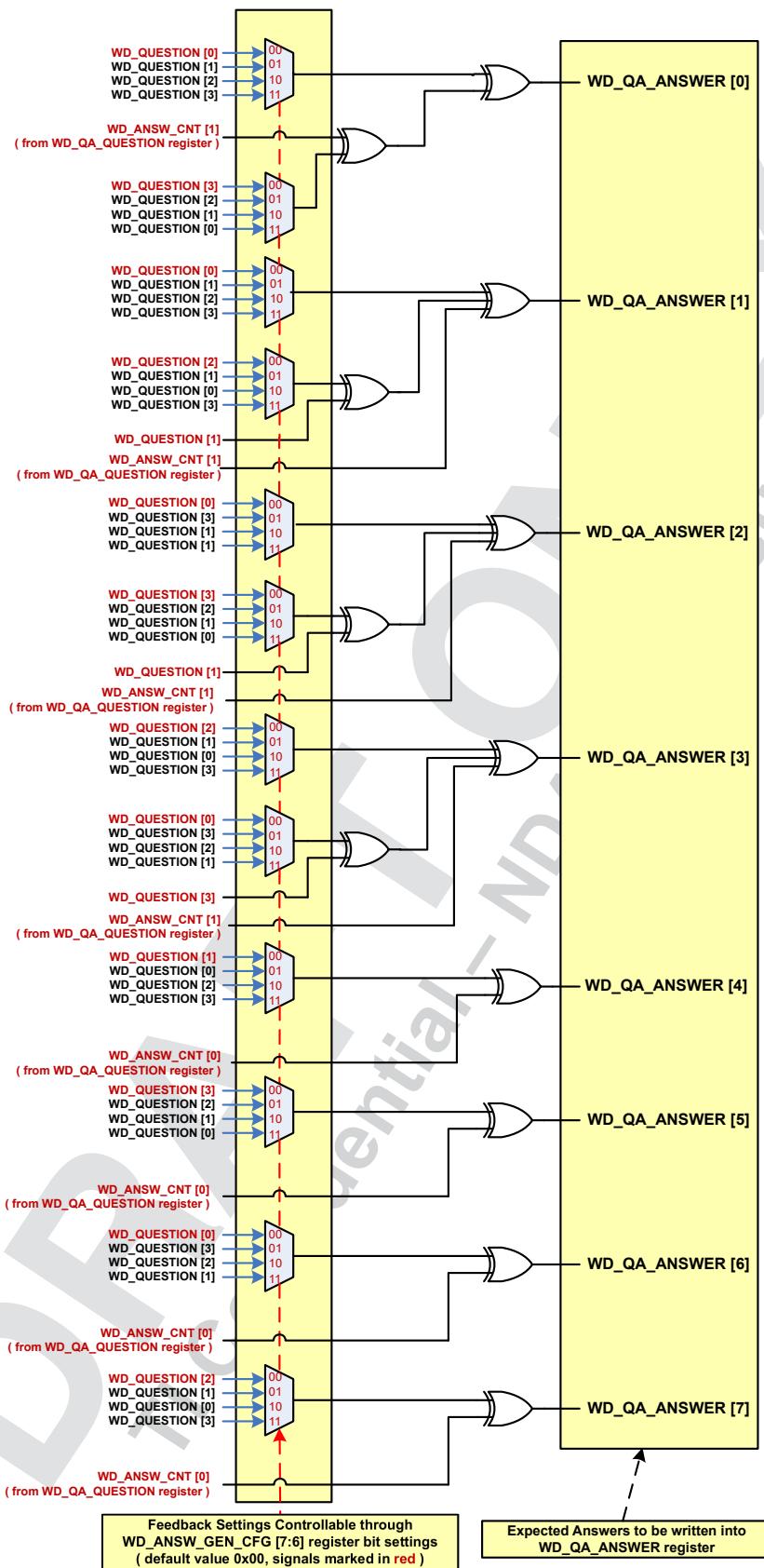


Figure 8-55. WD Expected Answer Generation

Table 8-16. Correct and Incorrect WD Q&A Sequence Run Scenarios for WD Q&A Multi-Answer Mode

NUMBER OF WD ANSWERS		ACTION	WD_QA_ERR (in WD_QA_QUESTION Register) ⁽¹⁾	COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2			
0 answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	No answers
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
0 answer	1 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question		
2 CORRECT answer	1 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question		
0 answer	1 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question		
2 CORRECT answer	1 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question		
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWER in WIN1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question		
2 CORRECT answer	2 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question		
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question		
2 CORRECT answer	2 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question		
0 answer	3 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question		
2 INCORRECT answer	1 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question		
0 answer	3 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question		
2 INCORRECT answer	1 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question		
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question		
2 INCORRECT answer	2 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question		
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question		
2 INCORRECT answer	2 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question		
3 CORRECT answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD Question	1b	Less than 4 CORRECT ANSWER in RESPONSE WINDOW 1 and more than 0 ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
2 CORRECT answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD Question		
1 CORRECT answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD Question		
3 CORRECT answer	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Decrement WD failure counter -New WD cycle starts with a new WD question	0b	CORRECT SEQUENCE
3 CORRECT answer	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
3 INCORRECT answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received < 4
3 INCORRECT answer	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4

**Table 8-16. Correct and Incorrect WD Q&A Sequence Run Scenarios for WD Q&A Multi-Answer Mode
(continued)**

NUMBER OF WD ANSWERS		ACTION	WD_QA_ERR (in WD_QA_QUESTION Register) ⁽¹⁾	COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2			
3 INCORRECT answer	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
4 CORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	
3 CORRECT answer + 1 INCORRECT answer	Not applicable			
2 CORRECT answer + 2 INCORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	4 CORRECT or INCORRECT ANSWER in RESPONSE WINDOW 1
1 CORRECT answer + 3 INCORRECT answer	Not applicable			

(1) WD_QA_ERR is the logical OR of all QA watchdog errors

8.6.10.4.3.1 Question and Answer WD Example

For this example, we'll walk through a single sequence with the following configuration settings, [Table 8-17](#).

Table 8-17. WD Function Initialization

Item	Value	Description
Watchdog window size	1024 ms	Window size of 1024 ms
Answer Generation Option	0 (default)	Answer generation configuration
Question Polynomial	0 (default)	Polynomial used to generate the question
Question polynomial seed	A (default)	Polynomial seed used to generate questions
WD Error Counter Limit	15	On the 15th fail event, do the watchdog action

8.6.10.4.3.1.1 Example configuration for desired behavior

[Table 8-18](#) register writes will configure the part for the example behavior specified above. Most of the settings are power on defaults.

Table 8-18. Example Register Configuration Writes

Step	Register	Data
1	WD_CONFIG_1 (0x13)	[W] 0b11010000 / 0xD0
2	WD_CONFIG_2 (0x14)	[W] 0b10000000 / 0x80
3	WD_RST_PULSE (0x16)	[W] 0b11110000 / 0xF0
4	WDT_QA_CONFIG (0x2D)	[W] 0b00001010 / 0xA

8.6.10.4.3.1.2 Example of performing a question and answer sequence

The normal sequence summary is as follows:

1. Read the question
2. Calculate the 4 answer bytes
3. Send 3 of them within the first response window
4. Wait and send the last byte in the second response window

See [Table 8-19](#) for an example of the first loop sequence.

Table 8-19. Example First Loop

Step	Register	Data	Description
1	WD_QA_QUESTION (0x2F)	[R] 0x0C	Read the question. Question is 0x0C
2	WD_QA_ANSWER (0x2E)	[W] 0x58	Write answer 3 (See Table 8-15 Example answers to questions with default settings to see answers)
3	WD_QA_ANSWER (0x2E)	[W] 0xA8	Write answer 2
4	WD_QA_ANSWER (0x2E)	[W] 0x57	Write answer 1
5	WD_QA_ANSWER (0x2E)	[W] 0xA7	Write answer 0 once window 2 has started

At this point, you can read the WD_QA_QUESTION[6] (0x2F) register to see if WD_QA_ERR is set.

8.6.11 Bus Fault Detection and Communication

The TCAN284xx-Q1 provides advanced bus fault detection. The device can determine certain fault conditions and set a status/interrupt flag so that the MCU can understand what the fault is. As with any bus architecture where termination resistors are at each end not every fault can be specified to the lowest level, meaning exact location. The fault detection circuitry is monitoring the CANH and CANL pins (currents) to determine if there

is a short to battery, short to ground, short to each other or opens. From a system perspective the location of the device will also determine what can be detected. See [Figure 8-56](#) as an example of node locations and how they can impact the ability to determine the actual fault location. [Figure 8-57](#) through [Figure 8-60](#) show the various bus faults based upon the three-node configuration. [Table 8-20](#) shows what can be detected and by which device.

Bus fault detection is a system level situation. If the fault is occurring at the ECU then the general communication of the bus is compromised. For complete coverage of a node a system level diagnostic step is needed for each node and the ability to communicate this back to a central point.

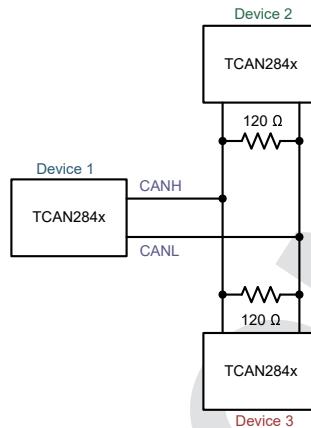


Figure 8-56. Three Node Example

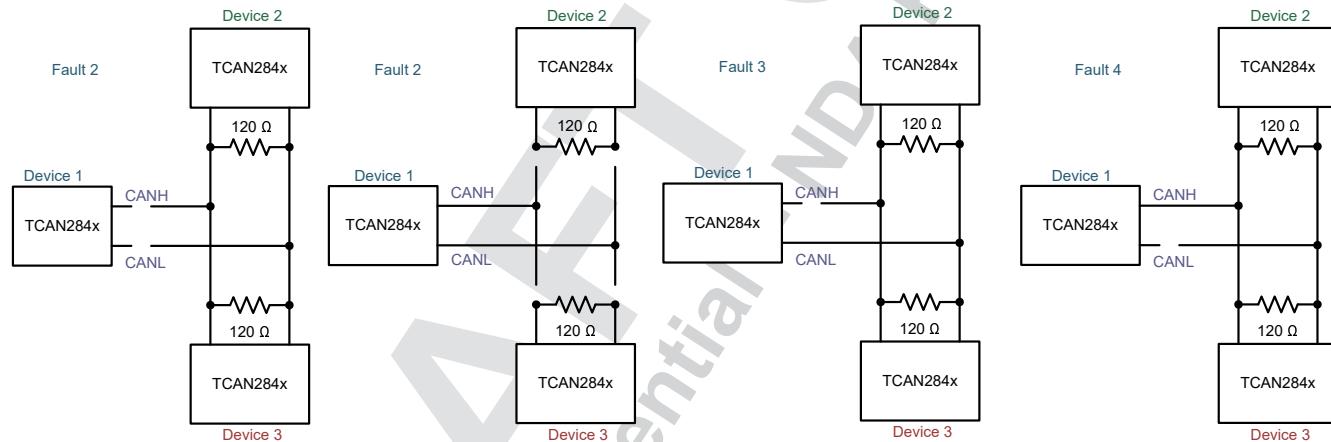


Figure 8-57. Open Fault Examples

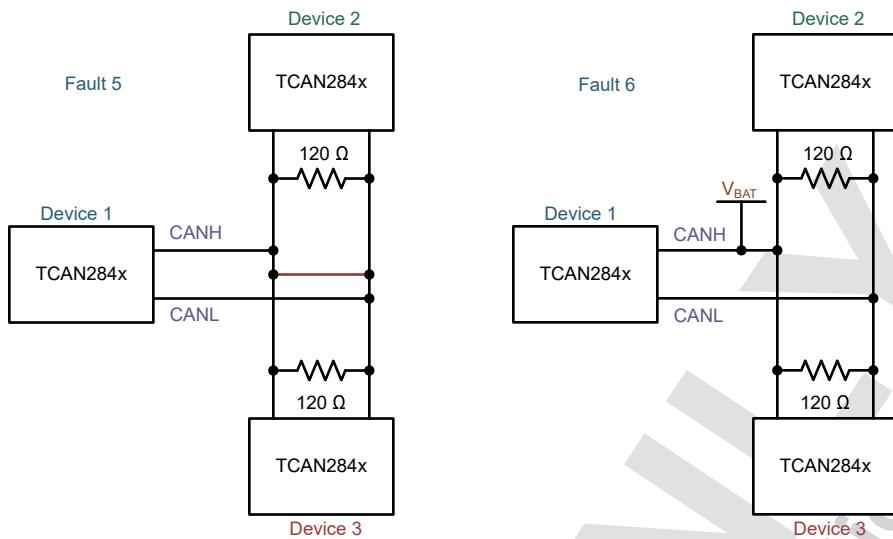


Figure 8-58. Short Faults 5 and 6 Examples

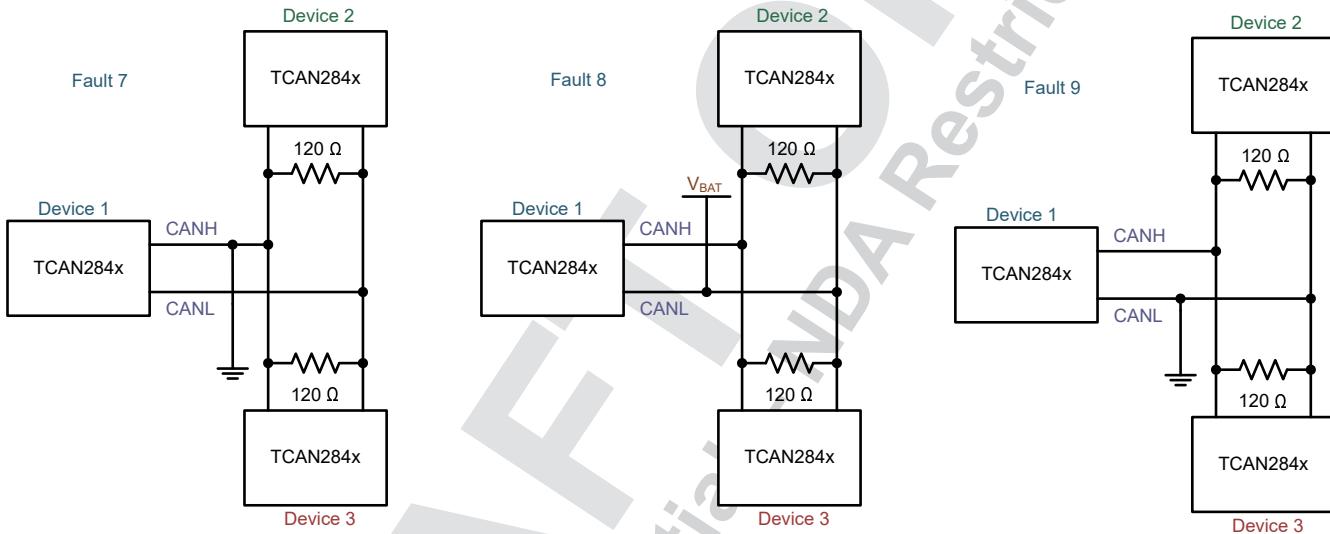


Figure 8-59. Short Faults 7, 8 and 9 Examples

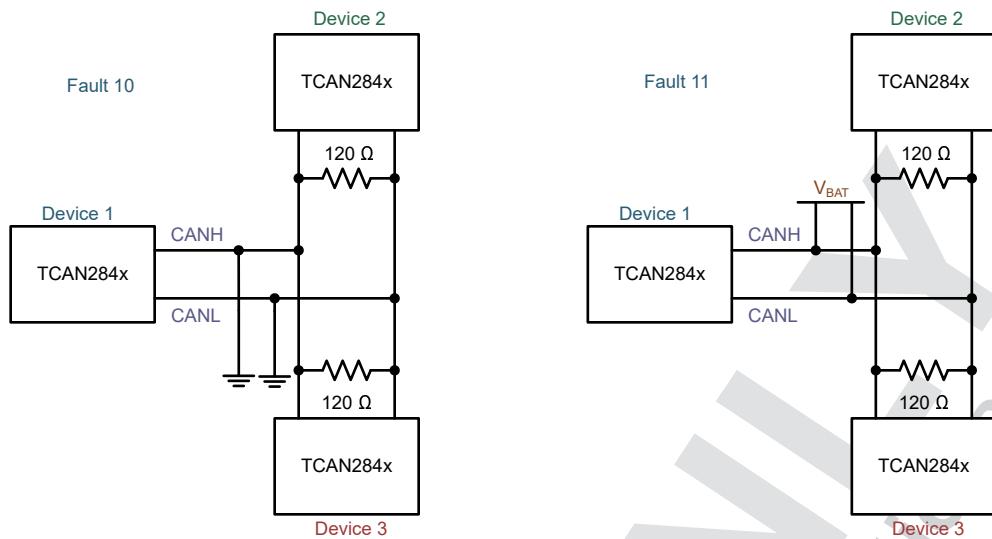


Figure 8-60. Short Faults 10 and 11 Examples

Table 8-20. Bus Fault Pin State and Detection Table

Fault #	CANH	CANL	Fault Detected
2	Open	Open	Depending upon open location the device detects this as no termination.
3	Shorted to CANL	Shorted to CANH	Yes, but not location
4	Normal	Open	<ul style="list-style-type: none"> Device 1 detects this fault but cannot tell the difference between it and Fault 2 and 5 Device 2 and Device 3 does not see this fault
5	Open	Normal	Yes, but cannot tell the difference between it and Fault 2 and 4; Device 2 and Device 3 does not see this fault
6	Shorted to V_{BAT}	Normal	Yes, but not location
7	Shorted to GND	Normal	Yes, but cannot tell the difference between this and Fault 10
8	Normal	Shorted to V_{BAT}	Yes, but cannot tell the difference between this and Fault 11
9	Normal	Shorted to GND	Yes, but not location
10	Shorted to GND	Shorted to GND	Yes, but cannot tell the difference between this and Fault 7
11	Shorted to V_{BAT}	Shorted to V_{BAT}	Yes, but cannot tell the difference between this and Fault 8

Table 8-21. Bus Fault Interrupt Flags Mapping to Fault Detection Number

Address	BIT(S)	DEFUALT	FLAG	DESCRIPTION	FAULT DETECTED	ACCESS
8'h54	7	1'b0	UVCAN	VCAN under-voltage interrupt	Normal Operation	R/W1C
	6	1'b0	RSVD	Reserved	NA	R
	5	1'b0	CANHCANL	CANH and CANL Shorted Together	Fault 3	R/W1C
	4	1'b0	CANHBAT	CANH Shorted to V_{BAT}	Fault 6	R/W1C
	3	1'b0	CANLGND	CANL Shorted to GND	Fault 9	R/W1C
	2	1'b0	CANBUSOPEN	CAN Bus Open (One of three possible places)	Faults 2, 4 and 5	R/W1C
	1	1'b0	CANBUSGND	CANH Shorted to GND or Both CANH & CANL Shorted to GND	Faults 7 and 10	R/W1C
	0	1'b0	CANBUSBAT	CANL Shorted to V_{BAT} or Both CANH & CANL Shorted to V_{BAT}	Faults 8 and 11	R/W1C

8.7 Programming

The TCAN284xx-Q1 is a 7-bit address access SPI communication port.

8.7.1 SPI Communication

The SPI communication uses a standard SPI interface. Physically the digital interface pins are nCS (Chip Select Not), SDI (SPI Data In), SDO (SPI Data Out) and CLK (SPI Clock). Each SPI transaction is initiated by a seven bit address with a R/W bit. The data shifted out on the SDO pin for the transaction always starts with the register 8'h50[7:0] which is the global interrupt register. This register provides the high-level interrupt status information about the device. The data byte which are the ‘response’ to the address and R/W byte are shifted out next.

The SPI data input data on SDI is sampled on the low to high edge of CLK. The SPI output data on SDO is changed on the high to low edge of CLK.

See [Figure 8-61](#) and [Figure 8-62](#) for read and write method when cyclic redundancy is disabled.

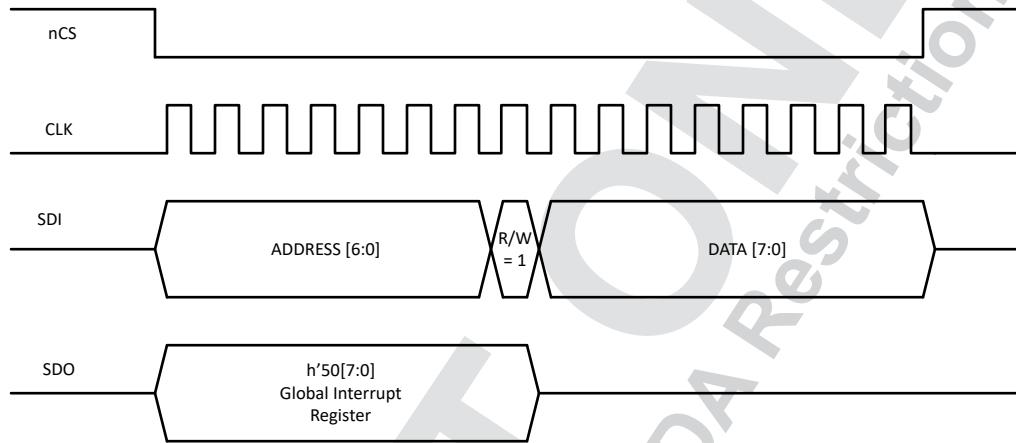


Figure 8-61. SPI Write

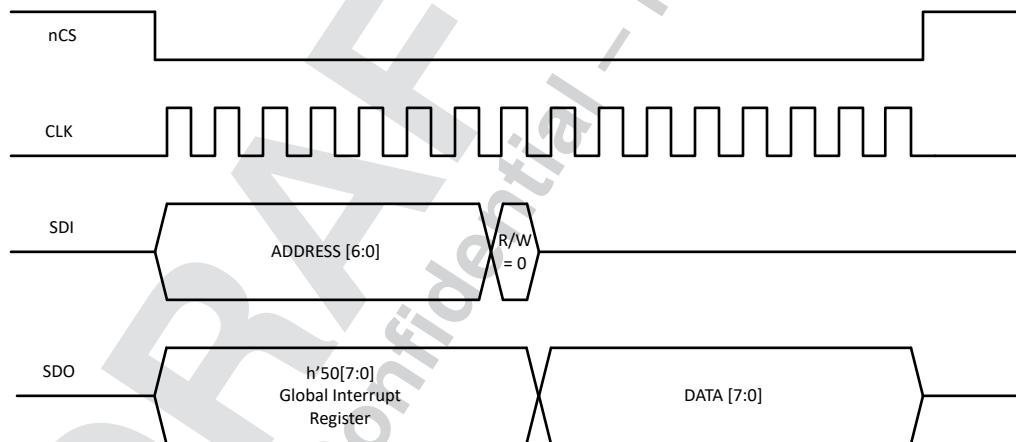


Figure 8-62. SPI Read

8.7.1.1 Cyclic Redundancy Check

The TCAN284xx-Q1 family cyclic redundancy check (CRC) for SPI transactions, default disabled. Register 'h0A[0] can be used to enable this feature. The default polynomial supports AutoSAR CRC8H2F, $X^8 + X^5 + X^3 + X^2 + X + 1$, see [Table 8-22](#). CRC8 according to SAE J1850 is also supported and can be selected at register 8'h0B[0]. When CRC is enabled the a filler byte of 00h is utilized to calculate the CRC value during a read/write operation, see [Figure 8-63](#) and [Figure 8-64](#).

Table 8-22. CRC8H27

SPI Transactions	
CRC result width	8 bits
Polynomial	2Fh
Initial value	FFh
Input data reflected	No
Result data reflected	No
XOR value	FFh
Check	DFh
Magic Check	42h

Table 8-23. CRC8 SAE J1850

SPI Transactions	
CRC result width	8 bits
Polynomial	1Dh
Initial value	FFh
Input data reflected	No
Result data reflected	No
XOR value	FFh
Check	4Bh
Magic Check	C4h

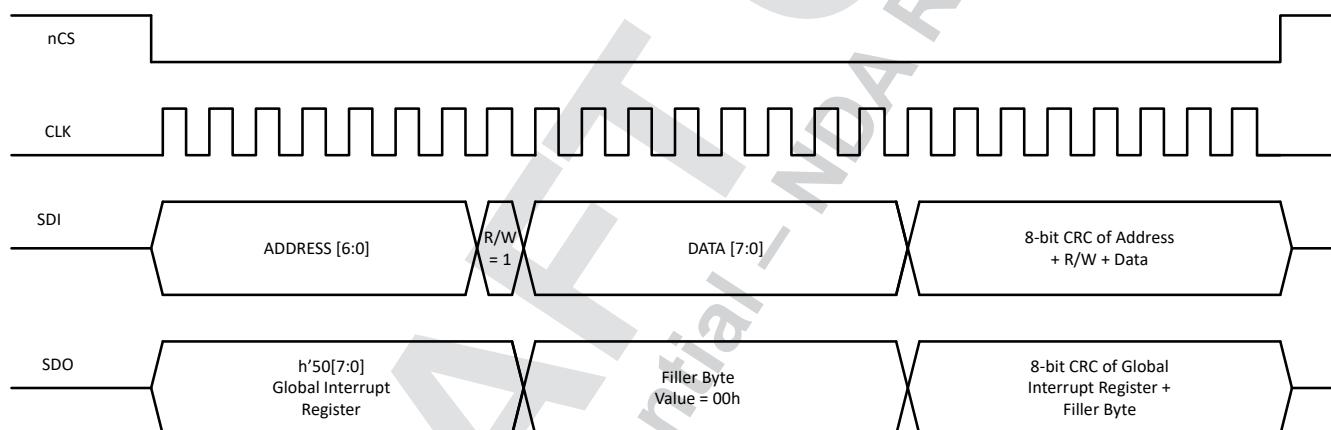


Figure 8-63. CRC SPI Write

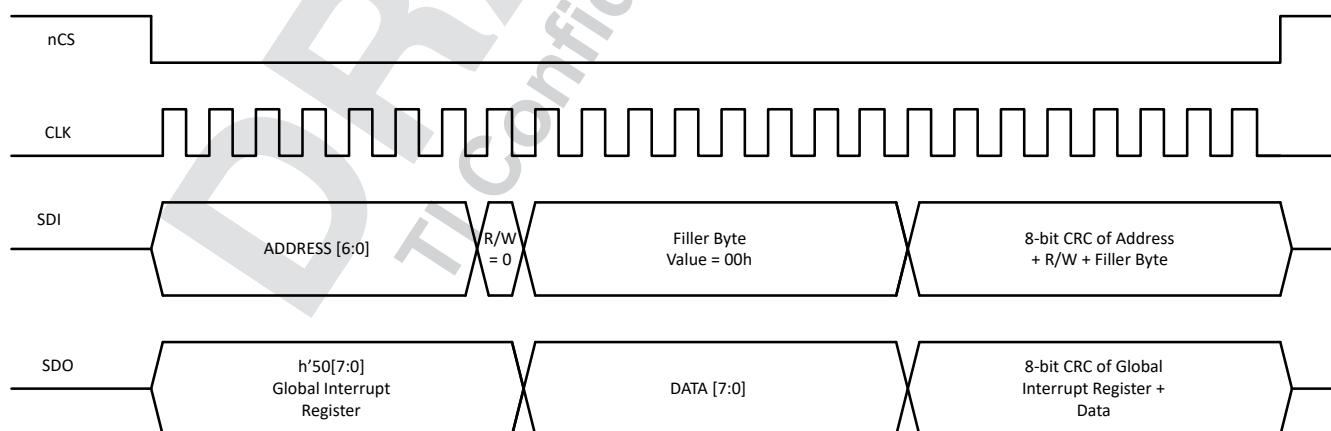


Figure 8-64. CRC SPI Read

8.7.1.2 Chip Select Not (nCS):

This input pin is used to select the device for a SPI transaction. The pin is active low, so while nCS is high the SPI Data Output (SDO) pin of the device is high impedance allowing an SPI bus to be designed. When nCS is low the SDO driver is activated and communication may be started. The nCS pin is held low for a SPI transaction. A special feature on this device allows the SDO pin to immediately show the Global Fault Flag on a falling edge of nCS.

8.7.1.3 SPI Clock Input (CLK):

This input pin is used to input the clock for the SPI to synchronize the input and output serial data bit streams. The SPI data input is sampled on the rising edge of CLK and the SPI data Output is changed on the falling edge of the CLK. See [Figure 8-65](#).

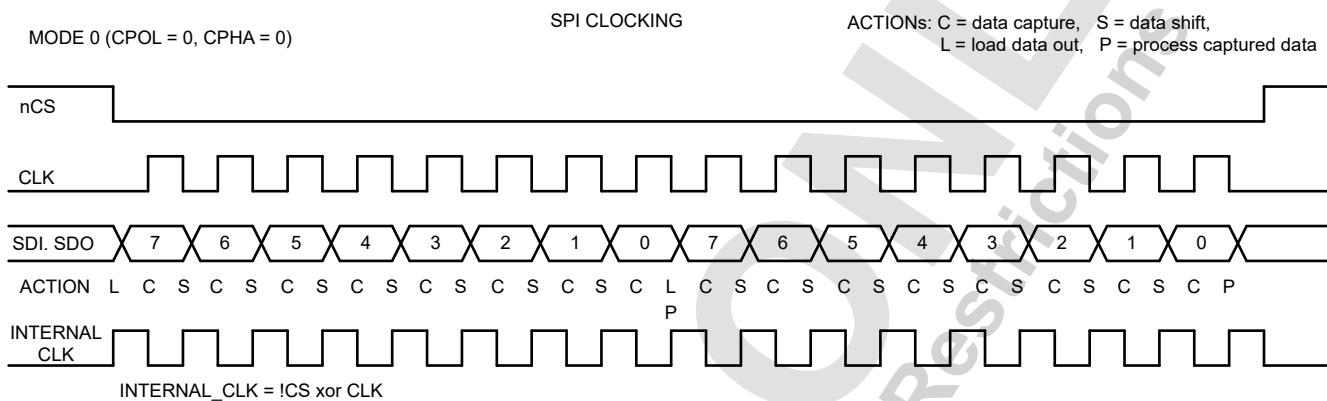


Figure 8-65. SPI Clocking

8.7.1.4 SPI Data Input (SDI):

This input pin is used to shift data into the device. Once the SPI is enabled by a low on nCS, the SDI samples the input shifted data on each rising edge of the SPI clock (CLK). The data is shifted into an 8-bit shift register. After eight (8) clock cycles and shifts, the addressed register is read giving the data to be shifted out on SDO. After eight clock cycles, the shift register is full and the SPI transaction is complete. If the command code is a write, the new data is written into the addressed register only after exactly 8 bits have been shifted in by CLK and the nCS has a rising edge to deselect the device. If there are not exactly 8 bits shifted in to the device during one SPI transaction (nCS low), the SPI command is ignored, the SPIERR flag is set and the data is not written into the device preventing any false actions by the device.

8.7.1.5 SPI Data Output (SDO):

This pin is high impedance until the SPI output is enabled via nCS. Once the SPI is enabled by a low on nCS, the SDO is immediately driven high or low showing the Global Fault Flag status which is also the first bit (bit 7) to be shifted out if the SPI is clocked. On the first falling edge of CLK, the shifting out of the data continues with each falling edge on CLK until all 8 bits have been shifted out the shift register.

8.7.2 EEPROM

The TCAN284x-Q1 family utilizes EEPROM for two purposes. The first is for device trimming and is not accessible. This portion of EEPROM is monitored and loaded upon power and when exiting sleep mode, checking for a valid CRC. If the CRC is not valid, this process will be performed a total of eight times. If still not valid, INT_3 register 8'h53[0] will be set to 1b. This means the device has an issue that may impact its performance and functionality.

The second use of the EEPROM is to allow the user to store specific device configurations. The configuration bits saved are provided in each register. In order to save the configuration to SPI CRC must be enabled for the save function at a minimum. Saving the configuration to EEPROM is accomplished by writing a 1b to register 8'h4E[7] and default code Ah to 8'h4E[3:0] followed by the CRC byte. See [Table 8-24](#) for procedure if the processor does not support CRC. Register 8'h4E[3:0] will read back 0h. Once the configuration bits have been

stored to EEPROM, a 0b will be read back from 8'h4E[7]. If a power on reset takes place the configuration of the device will be reloaded from EEPROM. [Table 8-25](#) provides the list of registers and the bits saved to EEPROM if utilized.

Note

The EEPROM can be reprogrammed a maximum of 500 times.

Table 8-24. Process for non-CRC capable processors

Step	Description	Register	Data	Second Data Byte (CRC POLY_8_SET = 0b)	Second Data Byte (CRC POLY_8_SET = 1b)
1	Configure device	See Table 8-25	NA	NA	NA
2	Set CRC Polynomial • 0x2F AutoSar • 0X1D SAE J11850	8'h0B[0]	• 00h • 01h	• Selected • NA	• NA • Selected
3	Enable SPI CRC if not enable	8'h0A[0]	01h	NA	NA
4	Save to EEPROM	8'h4E[7:0]	8Ah	36h	0Ch
5	Disable SPI CRC if not supported	8'h0A[0]	00h	5Eh	6Bh

The saved configuration can be forced to check if the saved configuration CRC is valid but using register 8'h4E[6], EEPROM_CRC_CHK, = 1b. This will take approximately 200 μ s to complete. If CRC is valid then no action is taken, If CRC is not valid the device will attempt this action eight times. If still not valid afterward the device will set an interrupt indicating there is an issue are INT_4 register 8'h5A[1], EEPROM_CRC_INT.

The following are power and reset scenarios and how the EEPROM is utilized.

- UVSUP event; no action as registers are not lost
- Power on reset event; EEPROM is read and registers restored in Init mode once VSUP > UVSUP_{5R}
- Soft reset; EEPROM is read and registers restored and device transitions to standby mode
- Hard reset; EEPROM is read and registers restored and device transitions to Init mode
- nRST input; EEPROM is read and register restored and device transitions to restart mode

Table 8-25. EEPROM Saved Registers and Bits

Register	Bits Saved
SBC_CONFIG (Address = Ch)	0-1, 4
VREG_CONFIG1 (Address = Dh)	0-7
SBC_CONFIG1 Register (Address = Eh)	0, 3-5, 7
WAKE_PIN_CONFIG1 Register (Address = 11h)	0-3
WAKE_PIN_CONFIG2 Register (Address = 12h)	0-1, 5
WD_CONFIG_1 Register (Address = 13h)	4-7
WD_CONFIG_2 Register (Address = 14h)	0, 5-7
WD_RST_PULSE Register (Address = 16h)	4-7
SWE_TIMER (Address = 1Ch)	3-6
nRST_CNTL (Address = 29h)	5
WAKE_PIN_CONFIG4 Register (Address = 2Bh)	0-1, 4-5
WD_QA_CONFIG Register (Address = 2Dh)	0-7
HSS_CNTL3 Register (Address = 4Fh)	0

8.8 Registers

Table 8-26 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 8-26 should be considered as reserved locations and the register contents should not be modified.

Table 8-26. Device Registers

Address	Acronym	Register Name	Section
0h + formula	DEVICE_ID_y	Device Part Number	Section 8.8.1
8h	REV_ID_MAJOR	Major Revision	Section 8.8.2
9h	REV_ID_MINOR	Minor Revision	Section 8.8.3
Ah	CRC_CNTL	SPI CRC control	Section 8.8.4
Bh	CRC_POLY_SET	Sets SPI CRC polynomial	Section 8.8.5
Ch	SBC_CONFIG	SBC, HSS and VCC2 select	Section 8.8.6
Dh	VREG_CONFIG1	Configures VCC1 and VEXCC regulators	Section 8.8.7
Eh	SBC_CONFIG1	SBC Configuration	Section 8.8.8
Fh	Scratch_Pad_SPI	Read and Write Test Register SPI	Section 8.8.9
10h	CAN_CTR1L_1	CAN transceiver 1 control	Section 8.8.10
11h	WAKE_PIN_CONFIG1	WAKE pin configuration 1	Section 8.8.11
12h	WAKE_PIN_CONFIG2	WAKE pin configuration 2	Section 8.8.12
13h	WD_CONFIG_1	Watchdog configuration 1	Section 8.8.13
14h	WD_CONFIG_2	Watchdog configuration 2	Section 8.8.14
15h	WD_INPUT_TRIGGER	Watchdog input trigger	Section 8.8.15
16h	WD_RST_PULSE	Watchdog output pulse width	Section 8.8.16
17h	FSM_CONFIG	Fail safe mode configuration	Section 8.8.17
18h	FSM_CNTR	Fail safe mode counter	Section 8.8.18
19h	DEVICE_RST	Device reset	Section 8.8.19
1Ah	DEVICE_CONFIG1	Device configuration 1	Section 8.8.20
1Bh	DEVICE_CONFIG2	Device configuration 2	Section 8.8.21
1Ch	SWE_TIMER	Sleep wake error timer configuration	Section 8.8.22
1Dh	LIN_CNTL	LIN transceiver control	Section 8.8.23
1Eh	HSS_CNTL	High side switch 1 and 2 control	Section 8.8.24
1Fh	PWM1_CNTL1	Pulse width modulation frequency select	Section 8.8.25
20h	PWM1_CNTL2	Pulse width modulation duty cycle two MSB select	Section 8.8.26
21h	PWM1_CNTL3	Pulse width modulation duty cycle eight LSB select	Section 8.8.27
22h	PWM2_CNTL1	Pulse width modulation frequency select	Section 8.8.28
23h	PWM2_CNTL2	Pulse width modulation duty cycle two MSB select	Section 8.8.29
24h	PWM2_CNTL3	Pulse width modulation duty cycle eight LSB select	Section 8.8.30
25h	TIMER1_CONFIG	High side switch timer 1 configuration	Section 8.8.31
26h	TIMER2_CONFIG	High side switch timer 2 configuration	Section 8.8.32
28h	RSRT_CNTR	Restart counter configuration	Section 8.8.33
29h	nRST_CNTL	nRST and GFO pin control	Section 8.8.34

Table 8-26. Device Registers (continued)

Address	Acronym	Register Name	Section
2Ah	WAKE_PIN_CONFIG3	Multi wake input configuration and reporting for WAKE pin	Section 8.8.35
2Bh	WAKE_PIN_CONFIG4	Multi wake input configuration and reporting for WAKE pin	Section 8.8.36
2Dh	WD_QA_CONFIG	Q and A Watchdog configuration	Section 8.8.37
2Eh	WD_QA_ANSWER	Q and A Watchdog answer	Section 8.8.38
2Fh	WD_QA_QUESTION	Q and A Watchdog question	Section 8.8.39
30h	SW_ID1	Selective wake ID 1	Section 8.8.40
31h	SW_ID2	Selective wake ID 2	Section 8.8.41
32h	SW_ID3	Selective wake ID 3	Section 8.8.42
33h	SW_ID4	Selective wake ID 4	Section 8.8.43
34h	SW_ID_MASK1	Selective wake ID mask 1	Section 8.8.44
35h	SW_ID_MASK2	Selective wake ID mask 2	Section 8.8.45
36h	SW_ID_MASK3	Selective wake ID mask 3	Section 8.8.46
37h	SW_ID_MASK4	Selective wake ID mask 4	Section 8.8.47
38h	SW_ID_MASK_DLC	ID Mask, DLC and Data mask enable	Section 8.8.48
39h + formula	DATA_y	CAN data byte 7 through 0	Section 8.8.49
41h + formula	SW_RSVD_y	SW_RSVD0 through SW_RSVD2	Section 8.8.50
44h	SW_CONFIG_1	CAN and CAN FD DR and behavior	Section 8.8.51
45h	SW_CONFIG_2	Frame counter	Section 8.8.52
46h	SW_CONFIG_3	Frame counter threshold	Section 8.8.53
47h	SW_CONFIG_4	Mode configuration	Section 8.8.54
48h + formula	SW_CONFIG_RSVD_y	SW_CONFIG_RSVD0 through SW_CONFIG_RSVD5	Section 8.8.55
4Dh	HSS_CNTL2	HSS3 and HSS4 control registers	Section 8.8.56
4Eh	EEPROM_CONFIG	EEPROM accessibility	Section 8.8.57
4Fh	HSS_CNTL3	Sets how HSS will behave to OL and OC	Section 8.8.58
50h	INT_GLOBAL	Global Interrupts	Section 8.8.59
51h	INT_1	Interrupts	Section 8.8.60
52h	INT_2	Interrupts	Section 8.8.61
53h	INT_3	Interrupts	Section 8.8.62
54h	INT_CANBUS_1	CAN transceiver 1 Bus fault interrupts	Section 8.8.63
55h	INT_7	Interrupts for high side switches	Section 8.8.64
56h	INT_EN_1	Interrupt mask for INT_1	Section 8.8.65
57h	INT_EN_2	Interrupt mask for INT_2	Section 8.8.66
58h	INT_EN_3	Interrupt mask for INT_3	Section 8.8.67
59h	INT_EN_CANBUS_1	Interrupt mask for INT_CANBUS	Section 8.8.68
5Ah	INT_4	Interrupts	Section 8.8.69
5Ch	INT_6	Interrupts	Section 8.8.71
5Eh	INT_EN_4	Interrupt mask for INT_4	Section 8.8.72
60h	INT_EN_6	Interrupt mask for INT_6	Section 8.8.73
62h	INT_EN_7	High side switch interrupt mask	Section 8.8.74

Complex bit access types are encoded to fit into small table cells. [Table 8-27](#) shows the codes that are used for access types in this section.

Table 8-27. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	H R	Set or cleared by hardware Read
Write Type		
H	H	Set or cleared by hardware
W	W	Write
W1C	1C W	1 to clear Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

8.8.1 DEVICE_ID_y Register (Address = 00h + formula) [reset = xxh]

DEVICE_ID_y is shown in [Table 8-28](#) and described in [Table 8-29](#).

Return to [Table 8-26](#).

Device Part Number, the xxh reset value depends upon device part number and register as shown in description table.

Offset = 00h + y; where y = 0h to 7h

Table 8-28. DEVICE_ID_y Register

7	6	5	4	3	2	1	0
DEVICE_ID							
R-xxh							

Table 8-29. DEVICE_ID_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEVICE_ID	R	xxh	The DEVICE_ID[1:8] registers determine the part number of the device. The reset values and value of each DEVICE_ID register are listed for the corresponding register address: Address 00h = 54h = T Address 01h = 43h = C Address 02h = 41h = A Address 03h = 32h = 2 Address 04h = 38h = 8 Address 05h = 34h = 4 Address 06h = 34h = 4 for TCAN2844-Q1 Address 06h = 35h = 5 for TCAN2845-Q1 Address 06h = 36h = 6 for TCAN2846-Q1 Address 06h = 37h = 7 for TCAN2847-Q1 Address 07h = 33h = 3 for 3.3 V VCC1 Address 07h = 35h = 5 for 5 V VCC1

8.8.2 REV_ID_MAJOR Register (Address = 08h) [reset = 00h]

REV_ID_MAJOR is shown in [Table 8-30](#) and described in [Table 8-31](#).

Return to [Table 8-26](#).

Major Revision

Table 8-30. REV_ID_MAJOR Register

7	6	5	4	3	2	1	0
Major_Revision							
R-00h							

Table 8-31. REV_ID_MAJOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Major_Revision	R	00h	Major die revision

8.8.3 REV_ID_MINOR Register (Address = 09h) [reset = 00h]

REV_ID_MINOR is shown in [Table 8-32](#) and described in [Table 8-33](#).

Return to [Table 8-26](#).

Minor Revision

Table 8-32. REV_ID_MINOR Register

7	6	5	4	3	2	1	0
Minor_Revision							
R-00h							

Table 8-33. REV_ID_MINOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Minor_Revision	R	00h	Minor die revision

8.8.4 CRC_CNTL Register (Address = 0Ah) [reset = 00h]

CRC_CNTL is shown in [Table 8-34](#) and described in [Table 8-35](#).

Return to [Table 8-26](#).

SPI CRC register controls the CRC function. CRC_EN bit can enable the CRC function.

Table 8-34. CRC_CNTL Register

7	6	5	4	3	2	1	0
CRC_CNTL_RSVD							CRC_EN
R-0000000b							R/W-0b

Table 8-35. CRC_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	CRC_CNTL_RSVD	R	0000000b	CRC control reserved bits
0	CRC_EN	R/W	0b	CRC enable 0b = Disable 1b = Enable

8.8.5 CRC_POLY_SET (Address = 0Bh) [reset = 00h]

CRC_POLY_SET is shown [Table 8-36](#) and described in [Table 8-37](#).

Return to [Table 8-26](#).

This register will set which polynomial will be set for CRC. Defaults to AutoSAR 8-bit 0x2F.

Table 8-36. CRC_POLY_SET

7	6	5	4	3	2	1	0
RSVD							POLY_8_SET
R-0000000b							R/W-1b

Table 8-37. CRC_POLY_SET Register Field Description

Bit	Field	Type	Reset	Description
7-1	RSVD	R	0000000b	Reserved
0	POLY_8_SET	R/W	0b	8 bit CRC polynomial set 0b = X^8 + X^5 + X^3 + X^2 + X + 1 (0x2F) 1b = X^8 + X^4 + X^3 + X^2 + 1 (0x1D SAE J1850)

8.8.6 SBC_CONFIG (Address = 0Ch) [reset = 06h]

SBC_CONFIG is shown [Table 8-38](#) and described in [Table 8-39](#).

Return to [Table 8-26](#).

The register programs which mode the SBC is in and which high side switches are being programmed. Configures VCC2 operation.

Bits 0, 1 and 4 are saved to EEPROM if used

Table 8-38. SBC_CONFIG

7	6	5	4	3	2	1	0
RSVD		PWM_SEL	VCC1_SNK_DIS	SBC_MODE_SEL		VCC2_CFG	
R-00b		R/W-0b	R/W-0b	R/W/H-01b		R/W-10b	

Table 8-39. SBC_CONFIG Register Field Description

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Reserved
5	PWM_SEL	R/W	0b	PWM select 0b = PWM1 and PWM2 1b = PWM3 and PWM4
4	VCC1_SNK_DIS	R/W	0b	VCC1 sink capability disable 0b = Sink enabled 1b = Sink disabled
3-2	SBC_MODE_SEL	R/W/H	01b	SBC mode select 00b = Sleep mode 01b = Standby mode 10b = Normal mode 11b = Reserved
1-0	VCC2_CFG	R/W	10b	VCC2 voltage regulator configuration 00b = Off 01b = On 10b = SBC mode controls VCC2 state 11b = RSVD

8.8.7 VREG_CONFIG1 (Address = 0Dh) [reset = 80h]

VREG_CONFIG1 is shown [Table 8-40](#) and described in [Table 8-41](#).

Return to [Table 8-26](#).

This register controls VCC1 and the external PNP configurations.

Bits 0-7 are saved to EEPROM if used

Table 8-40. VREG_CONFIG1

7	6	5	4	3	2	1	0
VCC1_CFG		VEXT_CFG		VCC1_SINK		VEXT_V_CFG	
R/W-10b		R/W-00b		R/W-0b		R/W-000b	

Table 8-41. VREG_CONFIG1 Register Field Description

Bit	Field	Type	Reset	Description
7-6	VCC1_CFG	R/W	10b	VCC1 voltage regulator configuration 00b = Reserved 01b = On 10b = SBC mode controls VCC1 state 11b = RSVD
5-4	VEXT_CFG	R/W	00b	VEXCC external PNP configuration 00b = Off 01b = On 10b = SBC mode controls VEXCC state 11b = RSVD
3	VCC1_SINK	R/W	0b	VCC1 sink current control 0b = 10 µA 1b = 100 µA
2-0	VEXT_V_CFG	R/W	000b	External PNP voltage control 000b = 1.8 V 001b = 2.5 V 010b = 3.3 V 011b = 5 V 100b = Load sharing 101b - 111b = Reserved

8.8.8 SBC_CONFIG1 Register (Address = 0Eh) [reset = 01h]

SBC_CONFIG1 is shown in [Table 8-42](#) and described in [Table 8-43](#).

Return to [Table 8-26](#).

Used to configure the SW. Bits 0, 3- 5 and 7 can be saved to EEPROM if used.

Table 8-42. SBC_CONFIG1 Register

7	6	5	4	3	2	1	0
CAN_SLOPE_CTRL_EN	FSM_CYC_WK_EN	VCC1_SLP_AC_T		UVCC1_SEL	SW_FSM_EN	SW_SLP_EN	SW_POL_SEL
R/W-0b	R/W-0b	R/W-0b		R/W-00b	R/W-0b	R/W-0b	R/W-1b

Table 8-43. SBC_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CAN_SLOPE_CTRL_EN	R/W	0b	Enables slope control on CAN transceiver 0b = Disabled 1b = Enabled
6	FSM_CYC_WK_EN	R/W	0b	Enables cyclic wake in fail-safe mode 0b = Disabled 1b = Enabled
5	VCC1_SLP_ACT	R/W	0b	Action to take when VCC1 is enabled on in sleep mode due to a wake event 0b = Transition to restart mode 1b = indicate wake event with nINT pin only
4-3	UVCC1_SEL	R/W	00b	VCC1 under-voltage threshold select 00b = Threshold 1 01b = Threshold 2 10b = Threshold 3 11b = Threshold 4
2	SW_FSM_EN	R/W	0b	Enables the SW pin to become a digital wake up pin when in fail-safe mode: 0b = Disabled 1b = Enabled
1	SW_SLP_EN	R/W	0b	Enables the SW pin to become a digital wake up pin when in sleep mode: 0b = Disabled 1b = Enabled
0	SW_POL_SEL	R/W	1b	Selects the input polarity of the SW pin 0b = Active low 1b = Active high

8.8.9 Scratch_Pad_SPI Register (Address = 0Fh) [reset = 00h]

Scratch_Pad_SPI is shown in [Table 8-44](#) and described in [Table 8-45](#).

Return to [Table 8-26](#).

Read and Write Test Register SPI

Table 8-44. Scratch_Pad_SPI Register

7	6	5	4	3	2	1	0
Scratch_Pad							
R/W-00h							

Table 8-45. Scratch_Pad_SPI Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Scratch_Pad	R/W	00h	Read and Write Test Register SPI

8.8.10 CAN_CNTRL_1 Register (Address = 10h) [reset = 04h]

CAN_CNTRL_1 is shown in [Table 8-46](#) and described in [Table 8-47](#).

Return to [Table 8-26](#).

Controls CAN1 modes and transceiver.

Table 8-46. CAN_CNTRL_1 Register

7	6	5	4	3	2	1	0
SW_EN	TXD.DTO.DIS	FD_EN	RSVD	CAN1_FSM_DIS		CAN1_TRX_SEL	
R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b		R/W-100b	

Table 8-47. CAN_CNTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SW_EN	R/W	0b	Selective wake enable 0b = Disabled 1b = Enabled
6	TXD.DTO.DIS	R/W	0b	CTXD Dominant time out disabled 0b = Enabled 1b = Disabled
5	FD_EN	R/W	0b	Bus fault diagnostic enable 0b = Disabled 1b = Enabled
4	RSVD	R	0b	Reserved
3	CAN1_FSM_DIS	R/W	0b	Sets the CAN transceiver operating state when device enters FSM 0b = Wake capable 1b = Disabled
2-0	CAN1_TRX_SEL	R/W	100b	CAN transceiver control 000b = Off 001b = Reserved 010b = Reserved 011b = Reserved 100b = Wake capable 101b = Listen 110b = SBC Mode Control 111b = On

8.8.11 WAKE_PIN_CONFIG1 Register (Address = 11h) [reset = 00h]

WAKE_PIN_CONFIG1 is shown in [Table 8-48](#) and described in [Table 8-49](#).

Return to [Table 8-26](#).

Device wake configuration register

Bits 0-3 are saved to EEPROM if used.

Table 8-48. WAKE_PIN_CONFIG1 Register

7	6	5	4	3	2	1	0
WAKE_CONFIG	WAKE1_STAT	RSVD		WAKE_WIDTH_INVALID		WAKE_WIDTH_MAX	
R/W-00b	R/H-0b	R-0b			R/W-00b		R/W-00b

Table 8-49. WAKE_PIN_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WAKE_CONFIG	R/W	00b	WAKE pin configuration: Note: Pulse requires more programming 00b = Bi-directional - either edge 01b = Rising edge 10b = Falling edge 11b = Pulse
5	WAKE1_STAT	R/H	0b	WAKE1 pin status when WAKE1 pin is configured on 0b = Low 1b = High
4	RSVD	R	0b	Reserved
3-2	WAKE_WIDTH_INVALID	R/W	00b	Pulses less than or equal to these pulses are considered invalid 0b = 5 ms and sets $t_{WAKE_WIDTH_MIN}$ to 10 ms 1b = 10 ms and sets $t_{WAKE_WIDTH_MIN}$ to 20 ms 10b = 20 ms and sets $t_{WAKE_WIDTH_MIN}$ to 40 ms 11b = 40 ms and sets $t_{WAKE_WIDTH_MIN}$ to 80 ms
1-0	WAKE_WIDTH_MAX	R/W	00b	Maximum WAKE pin input pulse width to be considered valid. 0b = 750 ms 1b = 1000 ms 10b = 1500 ms 11b = 2000 ms

8.8.12 WAKE_PIN_CONFIG2 Register (Address = 12h) [reset = 02h]

WAKE_PIN_CONFIG2 is shown in [Table 8-50](#) and described in [Table 8-51](#).

Return to [Table 8-26](#).

Device wake configuration register

Bits 0-1 and 5 are saved to EEPROM if used.

Table 8-50. WAKE_PIN_CONFIG2 Register

7	6	5	4	3	2	1	0
WAKE_PULSE_CONFIG	WAKE1_SENSE	TWK_CYC_SET	nINT_SEL		RXD_WK_CONFIG	WAKE1_LEVEL	
R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-10b	

Table 8-51. WAKE_PIN_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE_PULSE_CONFIG	R/W	0b	Set WAKE pin expected pulse direction for all WAKE pins 0b = Low → High → Low 1b = High → Low → High
6	WAKE1_SENSE	R/W	0b	WAKE1 pin configured for static or cyclic wake 0b = Static 1b = Cyclic
5	TWK_CYC_SET	R/W	0b	Sets the t_{WK_CYC} time (μs) for determining WAKE pin status for cyclic sensing for all WAKE pins 0b = 25 1b = 70
4-3	nINT_SEL	R/W	00b	nINT configuration selection: active low 00b = Global interrupt 01b = Watchdog failure output 10b = Bus fault interrupt 11b = Wake request
2	RXD_WK_CONFIG	R/W	0b	Configures RXD pin behavior from a wake event 0b = Pulled low 1b = Toggle
1-0	WAKE1_LEVEL	R/W	10b	WAKE1 pin threshold level; Mid-point value in 2 V window, except for 00b. 00b = VCC1 01b = 2.5 V 10b = 4 V 11b = 6 V

8.8.13 WD_CONFIG_1 Register (Address = 13h) [reset = 80h]

WD_CONFIG_1 is shown in [Table 8-52](#) and described in [Table 8-53](#).

Return to [Table 8-26](#).

Watchdog configuration register.

Register bits 4-7 are saved to EEPROM if used.

Table 8-52. WD_CONFIG_1 Register

7	6	5	4	3	2	1	0
WD_CONFIG		WD_PRE		RSVD			
R/W-10b		R/W-00b		R-0000b			

Table 8-53. WD_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_CONFIG	R/W	10b	Watchdog configuration 00b = Disabled 01b = Timeout 10b = Window 11b = Q&A
5-4	WD_PRE	R/W	00b	Watchdog prescalar 00b = Factor 1 01b = Factor 2 10b = Factor 3 11b = Factor 4
3-0	RSVD	R	0000b	Reserved

8.8.14 WD_CONFIG_2 Register (Address = 14h) [reset = 60h]

WD_CONFIG_2 is shown in [Table 8-54](#) and described in [Table 8-55](#).

Return to [Table 8-26](#).

Watchdog timer and error counter register.

Bits 0, 5-7 are saved to EEPROM if used.

Table 8-54. WD_CONFIG_2 Register

7	6	5	4	3	2	1	0
WD_TIMER				WD_ERR_CNT			
R/W-011b				RH-0000b			

Table 8-55. WD_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	WD_TIMER	R/W	011b	Sets window or timeout times based upon the WD_PRE setting, See WD_TIMER table
4-1	WD_ERR_CNT	RH	0000b	Watchdog error counter Running count of errors up to 15 errors
0	WD_STBY_DIS	R/W	0b	Disables the watchdog in standby mode. 0b = Enabled 1b = Disabled

8.8.15 WD_INPUT_TRIG Register (Address = 15h) [reset = 00h]

WD_INPUT_TRIG is shown in [Table 8-56](#) and described in [Table 8-57](#).

Return to [Table 8-26](#).

Writing FFh resets WD timer if accomplished at appropriate time

Table 8-56. WD_INPUT_TRIG Register

7	6	5	4	3	2	1	0
WD_INPUT							
R/W1C-00h							

Table 8-57. WD_INPUT_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_INPUT	R/W1C	00h	Write FFh to trigger WD

8.8.16 WD_RST_PULSE Register (Address = 16h) [reset = 00h]

WD_RST_PULSE is shown in [Table 8-58](#) and described in [Table 8-59](#).

Return to [Table 8-26](#).

The register sets the WD counter which determines the number of WD error events before the device enters restart mode. Can be programmed up to 15.

Bits 4-7 are saved to EEPROM if used.

Table 8-58. WD_RST_PULSE Register

7	6	5	4	3	2	1	0
WD_ERR_CNT_SET				Reserved			
R/W-0000b				R/W-0000b			

Table 8-59. WD_RST_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	WD_ERR_CNT_SET	R/W	0000b	Sets the number of watchdog error event threshold for the device to enter restart mode.
3-0	RSVD	R	0000b	Reserved

8.8.17 FSM_CONFIG Register (Address = 17h) [reset = 00h]

FSM_CONFIG is shown in [Table 8-60](#) and described in [Table 8-61](#).

Return to [Table 8-26](#).

Configures the fail-safe mode and provides status of what caused the device to enter fail-safe mode. When FSM is disabled 8'h17[3:1] provides the fault information that caused the device to enter sleep mode.

Table 8-60. FSM_CONFIG Register

7	6	5	4	3	2	1	0
FSM_CNTR_ACT				FSM_SLP_STAT			FSM_DIS
R/W-0000b				RH-000b			R/W-0b

Table 8-61. FSM_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FSM_CNTR_ACT	R/W	0000b	Action if fail-safe counter exceeds programmed value 0000b = Disabled 0001b - 0010b = Reserved 0011b = Perform hard reset - POR 0100b = Stop responding to wake events and go to sleep until power cycle reset 1001b - 1111b - Reserved
3-1	FSM_SLP_STAT	RH	000b	Reason for entering fail-safe or sleep mode 000b = Status clear 001b = Thermal shut down event 010b = Reserved 011b = VCC1 fault 100b = Reserved 101b = SWE timer (Sleep mode) 110b = Reserved 111b = Restart counter exceeded These values are held until cleared by writing 0h to FSM_CNTR_STAT
0	FSM_DIS	R/W	0b	Fail-safe mode disable: 0b = Enabled 1b = Disabled

Note

FSM_SLP_STAT provides information on what fault caused the device to enter fail-safe mode or sleep mode. The interrupt registers provide more information, example: if VCC1 fault is the reason, the interrupt registers will show if it was over-voltage or short circuit. When FSM is enabled INT_3 register 8'h53[5] will be set indicating that the device entered fail-safe mode. When VEXCC and VCC1 are load sharing, VCC1 will represent the fault condition.

When fail-safe mode is disabled FSM_SLP_STAT indicates which fault caused the device to enter sleep mode. The behavior is similar to when the device enters fail-safe mode but with the following differences:

- INT_2 register 8'h52[7] will be set indicating that the device entered sleep mode
- UVCC1 fault and watchdog failure events do not cause the device to enter sleep mode unless the event causes the restart counter to exceed its limit which will then be indicated by 111b restart counter exceeded. The under-voltage or watchdog interrupt will be set.

8.8.18 FSM_CNTR Register (Address = 18h) [reset = 00h]

FSM_CNTR is shown in [Table 8-62](#) and described in [Table 8-63](#).

Return to [Table 8-26](#).

Set fail safe counter and status.

Table 8-62. FSM_CNTR Register

7	6	5	4	3	2	1	0
FSM_CNTR_SET				FSM_CNTR_STAT			
R/W-0000b				RH-0000b			

Table 8-63. FSM_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FSM_CNTR_SET	R/W	0000b	Sets the number of times FS mode enters before action taken. Value is one less than the number of times FS mode is entered. Range is 0-15, representing entering Failsafe mode 1-16 times
3-0	FSM_CNTR_STAT	RH	0000b	Reads back the number of time FSM has been entered in a row up to 15. Can be cleared by writing 0h.

8.8.19 DEVICE_RST Register (Address = 19h) [reset = 00h]

DEVICE_RST is shown in [Table 8-64](#) and described in [Table 8-65](#).

Return to [Table 8-26](#).

Forces a soft or hard reset.

Table 8-64. DEVICE_RST Register

7	6	5	4	3	2	1	0
RESERVED						SF_RST	HD_RST
R-000000b						R/W1C-0b	R/W1C-0b

Table 8-65. DEVICE_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved
1	SF_RST	R/W1C	0b	Soft Reset: Writing a 1 causes a soft reset. Device registers are reloaded from EEPROM while keeping LDOs on.
0	HD_RST	R/W1C	0b	Hard Reset: Forces a power on reset when writing a 1. Note This will set the PWRON interrupt flag.

8.8.20 DEVICE_CONFIG (Address = 1Ah) [reset = 00h]

DEVICE_CONFIG is shown in [Table 8-66](#) and described in [Table 8-67](#).

Return to [Table 8-26](#).

LIMP pin configuration.

Table 8-66. DEVICE_CONFIG

7	6	5	4	3	2	1	0
	RSVD		LIMP_DIS	LIMP_SEL_RESET		LIMP_RESET	FSM_CYC_SE_N_EN
	R-000b		R/W - 0b	R/W - 00b		R/W1C - 0b	R/W - 0b

Table 8-67. DEVICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R	000b	Reserved
4	LIMP_DIS	R/W	0b	LIMP pin disable 0b = Enabled 1b = Disabled
3-2	LIMP_SEL_RESET	R/W	00b	Selects the method to reset/turn off the LIMP pin 00b = On third successful input trigger the error counter receives 01b = First correct input trigger 10b = Reserved 11b = Reserved
1	LIMP_RESET	R/W1C	0b	LIMP reset Writing a one to this location resets the LIMP pin to off state and bit automatically clears
0	FSM_CYC_SEN_EN	R/W	0b	Enables cyclic sensing wake up for fail-safe mode 0b = Disabled 1b = Enabled

8.8.21 DEVICE_CONFIG2 (Address = 1Bh) [reset = 00h]

DEVICE_CONFIG2 is shown in [Table 8-68](#) and described in [Table 8-69](#).

Return to [Table 8-26](#).

WAKE pin and channel expansion configuration and control.

Table 8-68. DEVICE_CONFIG2

7	6	5	4	3	2	1	0
RSVD						WAKE_WIDTH_MAX_DIS	RSVD
R-000000b						R/W-0b	R-0b

Table 8-69. DEVICE_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RSVD	R	000000b	Reserved
1	WAKE_WIDTH_MAX_DIS	R/W	0b	Disables the Max limit, $t_{WK_PULSE_WIDTH_MAX}$ detection when pulse is selected for WAKE pin wake up. 0b = Enabled 1b = Disabled
0	RSVD	R	0b	Reserved

8.8.22 SWE_TIMER (Address = 1Ch) [reset = 28h]

SWE_TIMER is shown in Table 8-70 and described in Table 8-71.

Return to [Table 8-26](#).

Sleep wake error timer configuration. Power up always sets to default value

Bits 3-6 are saved to EEPROM if used.

Table 8-70. SWE_TIMER

7	6	5	4	3	2	1	0
SWE_DIS				SWE_TIMER_SET	CANSLNT_SW_E_DIS	LIN1_FSM_DIS	RSVD
R/W-0b				R/W-0101b	R/W-0b	R/W-0b	R-0b

Table 8-71. SWE_TIMER Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SWE_DIS	R/W	0b	Sleep wake error disable: NOTE: This disables the device from starting the $t_{INACTIVE}$ timer when coming out of sleep mode on a wake event. If enabled, a SPI read or write must take place within this window or the device will go back to sleep. This does not disable the function for initial power on or in case of a power on reset. 0b = Enabled 1b = Disabled
6-3	SWE_TIMER_SET	R/W	0101b	Sets the timer used for $t_{INACTIVE}$ (minutes) 0000b = 2 0001b = 2.5 0010b = 3 0011b = 3.5 0100b = 4 0101b = 4.5 0110b = 5 0111b = 5.5 1000b = 6 1001b = 6.5 1010b = 8 1011b = 8.5 1100b = 10 1101b = Reserved 1111b = Reserved
				Note Note: This new $t_{INACTIVE}$ time does not impact the default used for power up, power on reset or brownout where VSUP goes low enough to be considered a power on reset
2	CANSLNT_SWE_DIS	R/W	0b	Disables the SWE timer connection with the CANSLNT flag. 0b = Enabled 1b = Disabled
1	LIN1_FSM_DIS	R/W	0b	Disables LIN transceiver when entering FSM 0b = Wake capable 1b = Off
0	RSVD	R	0b	Reserved

8.8.23 LIN_CNTL (Address = 1Dh) [reset = 20h]

LIN_CNTL is shown in [Table 8-72](#) and described in [Table 8-73](#).

Return to [Table 8-26](#).

LIN1 transceiver state and dominant timeout control.

Table 8-72. LIN_CNTL

7	6	5	4	3	2	1	0
LIN1_TRX_CNTRL			LIN1_TXD DTO_DIS	RSVD			
R/W/H-001b			R/W/H-0b	R-0000b			

Table 8-73. LIN_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	LIN1_TRX_CNTRL	R/W/H	001b	Channel 1 LIN transceiver control 000b = Off 001b = Wake Capable 010b = On 011b = Fast 100b = Listen 101b = SBC Mode Control 110b - 111b = Reserved
4	LIN1_TXD DTO_DIS	R/W/H	0b	Port 1 LIN LTXD1 dominant state timeout disable 0b = Enabled 1b = Disabled
3-0	RSVD	R	0000b	Reserved

8.8.24 HSS_CNTL (Address = 1Eh) [reset = 00h]

HSS_CNTL is shown in [Table 8-74](#) and described in [Table 8-75](#).

Return to [Table 8-26](#).

HSS1 and HSS2 high side switch control.

Table 8-74. HSS_CNTL

7	6	5	4	3	2	1	0
RSVD	HSS1_CNTL				RSVD	HSS2_CNTL	
R-0b	R/W-000b				R-0b	R/W-000b	

Table 8-75. HSS_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Reserved
6-4	HSS1_CNTL	R/W	000b	Control for HSS1 000b = Off 001b = PWM1 010b = PWM2 011b = Timer1 100b = Timer2 101b = On 110b = PWM3 111b = PWM4
3	RSVD	R	0b	Reserved
2-0	HSS2_CNTL	R/W	000b	Control for HSS2 000b = Off 001b = PWM1 010b = PWM2 011b = Timer1 100b = Timer2 101b = On 110b = PWM3 111b = PWM4

8.8.25 PWM1_CNTL1 (Address = 1Fh) [reset = 00h]

PWM1_CNTL1 is shown in [Table 8-76](#) and described in [Table 8-77](#).

Return to [Table 8-26](#).

Sets the pulse width modulation frequency, PWM1. When multiple high side switches are available more PWMs may be needed. PWM1 will become PWM3 if a HSS3 is available and these registers should be used.

Table 8-76. PWM1_CNTL1

7	6	5	4	3	2	1	0
PWM1_FREQ	HSS1_HSS2_SYNC	PWM1_FREQ_RSVD					
R/W-0b	R/W-0b	R-000000b					

Table 8-77. PWM1_CNTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM1_FREQ	R/W	0b	PWM frequency select (Hz) 0b = 200 1b = 400
6	HSS1_HSS2_SYNC	R/W	0b	Synchronization of HSS1 and HSS2: Which ever timing mechanism is used for HSS1 will be used for both HSS 0b = Stand alone 1b = Synchronized
5-0	PWM1_FREQ_RSVD	R	000000b	Reserved

Note

When configuring HSS3 it is best to align PWM3 if PWM is to be used. PWM1 control will change to PWM3 when register 8'hC[5:4] = 01b.

8.8.26 PWM1_CNTL2 (Address = 20h) [reset = 00h]

PWM1_CNTL2 is shown in [Table 8-78](#) and described in [Table 8-79](#).

Return to .

Set the two most significant bit for the 10-bit PWM1. These work with register h'21

Table 8-78. PWM1_CNTL2

7	6	5	4	3	2	1	0
PWM1_RSVD						PWM1_DC_MSB	
R-000000b						R/W-00b	

Table 8-79. PWM1_CNTL2L Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	PWM1_RSVD	R	000000b	Reserved
1-0	PWM1_DC_MSB	R/W	00b	Most significant two bits for 10-bit PWM1 duty cycle select. Works with 'h21[7:0] 00b = 100% off when used with 'h21[7:0] and it is 00h xxb = on time with an increase of ~ 0.1% when used with 'h21[7:0] 11b = 100% of when used with 'h21[7:0] and it is FFh

Note

When configuring HSS3 it is best to align PWM3 if PWM is to be used. PWM1 control will change to PWM3 when register 8'hC[5:4] = 01b.

8.8.27 PWM1_CNTL3 (Address = 21h) [reset = 00h]

PWM1_CNTL3 is shown in [Table 8-80](#) and described in [Table 8-81](#).

Return to [Table 8-26](#).

Bits 0 - 7 of the 10-bit PWM1 and PWM3. Used with register h'20[1:0]

Table 8-80. PWM1_CNTL3

7	6	5	4	3	2	1	0
PWM1_DC							
R/W-00h							

Table 8-81. PWM1_CNTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWM1_DC	R/W	00h	Bits 0 - 7 of the 10-bit PWM1 00h = 100% off when used with 'h20[1:0] = 00b xxh = On time with an increase of ~ 0.1% when used with 'h20[1:0] FFh = 100% on when used with 'h20[1:0] = 11b

Note

When configuring HSS3 it is best to align PWM3 if PWM is to be used. PWM1 control will change to PWM3 when register 8'hC[5:4] = 01b.

8.8.28 PWM2_CNTL1 (Address = 22h) [reset = 00h]

PWM2_CNTL1 is shown in [Table 8-82](#) and described in [Table 8-83](#).

Return to [Table 8-26](#).

Sets the pulse width modulation frequency, PWM2. When multiple high side switches are available more PWMs may be needed. PWM2 will become PWM4 if a HSS4 is available and these registers should be used.

Table 8-82. PWM2_CNTL1

7	6	5	4	3	2	1	0
PWM2_FREQ	PWM2_FREQ_RSVD						
R/W-0b	R-0000000b						

Table 8-83. PWM2_CNTL1 Register Field Descriptions

Bit	Filed	Type	Reset	Description
7	PWM2_FREQ	R/W	0b	PWM frequency select (Hz) 0b = 200 1b = 400
6-0	PWM2_FREQ_RSVD	R	0000000b	Reserved

Note

When configuring HSS4 it is best to align PWM4 if PWM is to be used. PWM2 control will change to PWM4 when register 8'hC[5:4] = 01b.

8.8.29 PWM2_CNTL2 (Address = 23h) [reset = 00h]

PWM2_CNTL2 is shown in [Table 8-84](#) and described in [Table 8-85](#).

Return to [Table 8-26](#).

Set the two most significant bit for the 10-bit PWM2. These work with register h'24

Table 8-84. PWM2_CNTL2

7	6	5	4	3	2	1	0
PWM2_RSVD						PWM2_DC_MSB	
R-000000b						R/W-00b	

Table 8-85. PWM2_CNTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	PWM2_RSVD	R	000000b	Reserved
1-0	PWM2_DC_MSB	R/W	00b	Most significant two bits for 10-bit PWM2 duty cycle select. Works with 'h24[7:0] 00b = 100% off when used with 'h24[7:0] and it is 00h xxb = on time with an increase of ~ 0.1% when used with 'h24[7:0] 11b = 100% of when used with 'h24[7:0] and it is FFh

Note

When configuring HSS4 it is best to align PWM4 if PWM is to be used. PWM2 control will change to PWM4 when register 8'hC[5:4] = 01b.

8.8.30 PWM2_CNTL3 (Address = 24h) [reset = 00h]

PWM2_CNTL3 is shown in [Table 8-86](#) and described in [Table 8-87](#).

Return to [Table 8-26](#).

Bits 0 - 7 of the 10-bit PWM2 and PWM4. Used with register h'23[1:0]

Table 8-86. PWM2_CNTL3

7	6	5	4	3	2	1	0
PWM2_DC							
R/W-00h							

Table 8-87. PWM2_CNTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWM2_DC	R/W	00h	Bits 0 - 7 of the 10-bit PWM2 00h = 100% off when used with 'h23[1:0] = 00b xxh = On time with an increase of ~ 0.1% when used with 'h23[1:0] FFh = 100% on when used with 'h23[1:0] = 11b

Note

When configuring HSS4 it is best to align PWM4 if PWM is to be used. PWM2 control will change to PWM4 when register 8'hC[5:4] = 01b.

8.8.31 TIMER1_CONFIG (Address = 25h) [reset = 00h]

TIMER1_CONFIG is shown in [Table 8-88](#) and described in [Table 8-89](#).

Return to [Table 8-26](#).

Sets timer 1 period and on time. Careful selection is important as selecting a 200ms on width and a 10ms period is not possible.

Table 8-88. TIMER1_CONFIG

7	6	5	4	3	2	1	0
TIMER1_ON_WIDTH				TIMER1_CYC_WK_EN	TIMER1_PERIOD		
R/W-0000b				R/W-0b	R/W-000b		

Table 8-89. TIMER1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TIMER1_ON_WIDTH	R/W	0000b	Sets the high side switch on time (ms) for timer 1 0000b = Off (HSS is high impedance) 0001b = 0.1 0010b = 0.3 0011b = 0.5 0100b = 1 0101b = 10 0110b = 20 0111b = 30 1000b = 40 1001b = 50 1010b = 60 1011b = 80 1100b = 100 1101b = 150 1110b = 200 1111b = On (HSS is on 100%)
3	TIMER1_CYC_WK_EN	R/W	0b	Enables timer1 for cyclic wake 0b = Disabled 1b = Enabled
2-0	TIMER1_PERIOD	R/W	000b	Sets the timer period (ms) for timer 1 000b = 10 001b = 20 010b = 50 011b = 100 100b = 200 101b = 500 110b = 1000 111b = 2000

8.8.32 TIMER2_CONFIG (Address = 26h) [reset = 00h]

TIMER2_CONFIG is shown in [Table 8-90](#) and described in [Table 8-91](#).

Return to [Table 8-26](#).

Sets timer 2 period and on time. Careful selection is important as selecting a 200ms on width and a 10ms period is not possible.

Table 8-90. TIMER2_CONFIG

7	6	5	4	3	2	1	0
TIMER2_ON_WIDTH				TIMER2_CYC_WK_EN	TIMER2_PERIOD		
R/W-0000b				R/W-0b	R/W-000b		

Table 8-91. TIMER2_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TIMER2_ON_WIDTH	R/W	0000b	Sets the high side switch on time (ms) for timer 2 0000b = Off (HSS is high impedance) 0001b = 0.1 0010b = 0.3 0011b = 0.5 0100b = 1 0101b = 10 0110b = 20 0111b = 30 1000b = 40 1001b = 50 1010b = 60 1011b = 80 1100b = 100 1101b = 150 1110b = 200 1111b = On (HSS is on 100%)
3	TIMER2_CYC_WK_EN	R/W	0b	Enables timer2 for cyclic wake 0b = Disabled 1b = Enabled
2-0	TIMER2_PERIOD	R/W	000b	Sets the timer period (ms) for timer 2 000b = 10 001b = 20 010b = 50 011b = 100 100b = 200 101b = 500 110b = 1000 111b = 2000

8.8.33 RSRT_CNTR (Address = 28h) [reset = 40h]

RSRT_CNTR is shown in [Table 8-92](#) and described in [Table 8-93](#).

Return to [Table 8-26](#).

Restart mode counter set and counter. Determines the number of times the device has entered restart mode and when it will transition to sleep mode once programmed counter value has been exceeded. Counter should be reset often to avoid this transition.

Table 8-92. RSRT_CNTR

7	6	5	4	3	2	1	0
RSRT_CNTR_SEL				RSRT_CNTR			
R/W-0100b				R/W1C-0000b			

Table 8-93. RSRT_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RSRT_CNTR_SEL	R/W	0100b	Selects the number of times the device can enter restart mode prior to device entering sleep mode, 1 to 15 times. Writing 0h here disables the restart counter.
3-0	RSRT_CNTR	R/W1C	0000b	Provides the number of times the device has entered restart mode and should be cleared prior to reaching the RSRT_CNTR_SEL value

8.8.34 nRST_CNTL (Address = 29h) [reset = 20h]

nRST_CNTL is shown in [Table 8-94](#) and described in [Table 8-95](#).

Return to [Table 8-26](#).

nRST and GFO pins control register.

Bit 5 is saved to EEPROM if used.

Table 8-94. nRST_CNTL

7	6	5	4	3	2	1	0
RSVD		nRST_PULSE_WIDTH	GFO_POL_SEL	GFO_SEL		RSVD	
R-00b		R/W-1b	R/W-0b	R/W-000b		R-0b	

Table 8-95. nRST_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	00b	Reserved
5	nRST_PULSE_WIDTH	R/W	1b	Sets the pulse width for toggling nRST from high-->low-->high when device enters restart mode (ms) 0b = 2 1b = 15
4	GFO_POL_SEL	R/W	0b	Selects the polarity for the GFO pin 0b = Active Low 1b = Active High
				Note Selects the output level when register 8'h29[3:1] = 110b making the pin a general-purpose output pin; 0 = Low and 1 = High
3-1	GFO_SEL	R/W	000b	Selects the information that will cause this pin to be pulled to the state selected by 'h29[4] for t_NRST_TOG except for when general purpose output is selected 000b = VCC1, VCC2 and/or VEXCC Interrupt (overvoltage, undervoltage or short) 001b = WD interrupt event 010b = Reserved 011b = Local wake request (LWU) 100b = Bus wake request (WUP) 101b = Restart counter exceeded (indicated in standby mode) 110b = General purpose output 111b = CAN Bus fault
0	RSVD	R	0b	RSVD

8.8.35 WAKE_PIN_CONFIG3 Register (Address = 2Ah) [reset = E0h]

WAKE_PIN_CONFIG3 is shown in [Table 8-96](#) and described in [Table 8-97](#).

Return to [Table 8-26](#)

Register to configure the number of inputs to the WAKE pin and which inputs caused the wake.

MULTI_WAKE_STAT provides which WAKE input state has changed based upon specific bits. Bits represent WAKE input so if multiple WAKE input bits are set, this indicates that those specific WAKE inputs cause the WAKE event. An example would be if h'2A[4:0] = 00101b then WAKE 0 and WAKE 2 have changed states.

Table 8-96. WAKE_PIN_CONFIG3

7	6	5	4	3	2	1	0
WAKE_PIN_SET			MULTI_WAKE_STAT				
R/W = 111b			R/W0C/H = 00000b				

Table 8-97. WAKE_PIN_CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	WAKE_PIN_SET	R/W	111b	Sets which WAKE input are on 000b = None 001b = WAKE1 on 010b = WAKE2 on 011b = WAKE1, WAKE2 on 100b = WAKE3 on 101b = WAKE1, WAKE3 on 110b = WAKE2, WAKE3 on 111b = WAKE1, WAKE2, WAKE3 on
4-0	MULTI_WAKE_STAT	R/W0C/H	00000b	Provides information on which individual or combination of wake input signal took place. 00000b = None 00001b = Wake1 00010b = Wake 2 00100b = Wake 3

Note

Note: The bit correspond to the WAKE pin will set to one allowing for multiple WAKE pins providing a local wake up input. An example would be if WAKE 1 and WAKE3 happened, this would show up as 00101b.

8.8.36 WAKE_PIN_CONFIG4 Register (Address = 2Bh) [reset = 22h]

CONFIG_RSVD_y is shown in [Table 8-98](#) and described in [Table 8-99](#).

Return to [Table 8-26](#).

Configures WAKE pins 2 and 3

Bits 0-1, 4-5 are saved to EEPROM if used.

Table 8-98. WAKE_PIN_CONFIG4

7	6	5	4	3	2	1	0
WAKE2_SENSE	WAKE2_STAT		WAKE2_LEVEL	WAKE3_SENSE	WAKE3_STAT		WAKE3_LEVEL
R/W-0b	R/H-0b		R/W-10b	R/W-0b	R/H-0b		R/W-10b

Table 8-99. WAKE_PIN_CONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE2_SENSE	R/W	0b	WAKE pin 2 sense configuration 0b = Static 1b = Cyclic
6	WAKE2_STAT	R/H	0b	WAKE2 pin status when WAKE2 pin is configured on 0b = Low 1b = High
5-4	WAKE2_LEVEL	R/W	10b	WAKE2 pin threshold level; Mid-point value in 2 V window, except for 00b. 00b = VCC1 01b = 2.5 V 10b = 4 V 11b = 6 V
3	WAKE3_SENSE	R/W	0b	WAKE pin 3 sense configuration 0b = Static 1b = Cyclic
2	WAKE3_STAT	R/H	0b	WAKE3 pin status when WAKE3 pin is configured on 0b = Low 1b = High
1-0	WAKE3_LEVEL	R/W	10b	WAKE3 pin threshold level; Mid-point value in 2 V window, except for 00b. 00b = VCC1 01b = 2.5 V 10b = 4 V 11b = 6 V

8.8.37 WD_QA_CONFIG Register (Address = 2Dh) [reset = 0Ah]

WD_QA_CONFIG is shown in [Table 8-100](#) and described in [Table 8-101](#).

Return to [Table 8-26](#).

Q&A watchdog configuration bits.

All bits are saved to EEPROM if used.

Table 8-100. WD_QA_CONFIG Register

7	6	5	4	3	2	1	0
WD_ANSW_GEN_CFG	WD_QA_POLY_CFG				WD_QA_POLY_SEED		
R/W-00b	R/W-00b				R/W-1010b		

Table 8-101. WD_QA_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_ANSW_GEN_CFG	R/W	00b	WD answer generation configuration
5-4	WD_QA_POLY_CFG	R/W	00b	WD Q&A polynomial configuration
3-0	WD_QA_POLY_SEED	R/W	1010b	WD Q&A polynomial seed value loaded when device is in the RESET state

8.8.38 WD_QA_ANSWER Register (Address = 2Eh) [reset = 00h]

WD_QA_ANSWER is shown in [Table 8-102](#) and described in [Table 8-103](#).

Return to [Table 8-26](#).

Q&A watchdog answer bits

Table 8-102. WD_QA_ANSWER Register

7	6	5	4	3	2	1	0
WD_QA_ANSWER							
R/W1C-00h							

Table 8-103. WD_QA_ANSWER Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_QA_ANSWER	R/W1C	00h	MCU watchdog Q&Aanswer response byte

8.8.39 WD_QA_QUESTION Register (Address = 2Fh) [reset = 00h]

WD_QA_QUESTION is shown in [Table 8-104](#) and described in [Table 8-105](#).

Return to [Table 8-26](#).

Q&A watchdog question bits

Table 8-104. WD_QA_QUESTION Register

7	6	5	4	3	2	1	0
WD_QA_RSVD	WD_QA_ERR	WD_ANSW_CNT				WD_QUESTION	
R-0b	W1C-0b	RH-00b				RH-0000b	

Table 8-105. WD_QA_QUESTION Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_QA_RSVD	R	0b	Reserved
6	WD_QA_ERR	W1C	0b	Watchdog Q&A answer error flag
5-4	WD_ANSW_CNT	RH	00b	Current state of received watchdog Q&A error counter When WD enabled value will show up as 2'h3
3-0	WD_QUESTION	RH	0000b	Current watchdog question value When WD is enabled value will show up as 4'hC

8.8.40 SW_ID1 Register (Address = 30h) [reset = 00h]

SW_ID1 is shown in [Table 8-106](#) and described in [Table 8-107](#).

Return to [Table 8-26](#).

Extended ID bits 17:10

Table 8-106. SW_ID1 Register

7	6	5	4	3	2	1	0
EXT_ID_17:10							
R/W-00h							

Table 8-107. SW_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_17:10	R/W	00h	Extended ID bits 17:10

8.8.41 SW_ID2 Register (Address = 31h) [reset = 00h]

SW_ID2 is shown in [Table 8-108](#) and described in [Table 8-109](#).

Return to [Table 8-26](#).

Extended ID bits 9:2.

Table 8-108. SW_ID2 Register

7	6	5	4	3	2	1	0
EXT_ID_9:2							
R/W-00h							

Table 8-109. SW_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_9:2	R/W	00h	Extended ID bits 9:2

8.8.42 SW_ID3 Register (Address = 32h) [reset = 00h]

SW_ID3 is shown in [Table 8-110](#) and described in [Table 8-111](#).

Return to [Table 8-26](#).

Extended ID bits 1:0, Extended ID Field, ID[10:6] and Extended ID[28:24]

Table 8-110. SW_ID3 Register

7	6	5	4	3	2	1	0
EXT_ID_1:0	IDE	ID_10:6__EXT_ID_28:24					
R/W-00b	R/W-0b	R/W-00000b					

Table 8-111. SW_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	EXT_ID_1:0	R/W	00b	Extended ID bits 1:0
5	IDE	R/W	0b	Extended ID field 0b = Standard ID (11-bits) 1b = Extended ID (29-bits)
4-0	ID_10:6__EXT_ID_28:24	R/W	00000b	ID[10:6] and Extended ID[28:24]

8.8.43 SW_ID4 Register (Address = 33h) [reset = 00h]

SW_ID4 is shown in [Table 8-112](#) and described in [Table 8-113](#).

Return to [Table 8-26](#).

ID[5:0] and Extended ID[23:18]

Table 8-112. SW_ID4 Register

7	6	5	4	3	2	1	0
ID_5:0__EXT_ID_23:18						RESERVED	
R/W-000000b						R-00b	

Table 8-113. SW_ID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	ID_5:0__EXT_ID_23:18	R/W	000000b	ID[5:0] and Extended ID[23:18]
1-0	RESERVED	R	00b	Reserved

8.8.44 SW_ID_MASK1 Register (Address = 34h) [reset = 00h]

SW_ID_MASK1 is shown in [Table 8-114](#) and described in [Table 8-115](#).

Return to [Table 8-26](#).

Extended ID Mask 17:16

Table 8-114. SW_ID_MASK1 Register

7	6	5	4	3	2	1	0
RESERVED						EXT_ID_MASK_17:16	
R-000000b						R/W-00b	

Table 8-115. SW_ID_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved
1-0	EXT_ID_MASK_17:16	R/W	00b	Extended ID Mask 17:16

8.8.45 SW_ID_MASK2 Register (Address = 35h) [reset = 00h]

SW_ID_MASK2 is shown in [Table 8-116](#) and described in [Table 8-117](#).

Return to [Table 8-26](#).

Extended ID Mask 15:8

Table 8-116. SW_ID_MASK2 Register

7	6	5	4	3	2	1	0
EXT_ID_MASK_15:8							
R/W-00h							

Table 8-117. SW_ID_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_MASK_15:8	R/W	00h	Extended ID Mask 15:8

8.8.46 SW_ID_MASK3 Register (Address = 36h) [reset = 00h]

SW_ID_MASK3 is shown in [Table 8-118](#) and described in [Table 8-119](#).

Return to [Table 8-26](#).

Extended ID Mask 7:0

Table 8-118. SW_ID_MASK3

7	6	5	4	3	2	1	0
EXT_ID_MASK_7:0							
R/W-00h							

Table 8-119. SW_ID_MASK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EXT_ID_MASK_7:0	R/W	00h	Extended ID Mask 7:0

8.8.47 SW_ID_MASK4 Register (Address = 37h) [reset = 00h]

SW_ID_MASK4 is shown in [Table 8-120](#) and described in [Table 8-121](#).

Return to [Table 8-26](#).

ID Mask 10:3 and Extended ID Mask 28:21 (Base ID)

Table 8-120. SW_ID_MASK4 Register

7	6	5	4	3	2	1	0
ID_MASK_10:3__EXT_ID_MASK_28:21							
R/W-00h							

Table 8-121. SW_ID_MASK4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ID_MASK_10:3__EXT_ID_MASK_28: 21	R/W	00h	ID Mask 10:3 and Extended ID Mask 28:21 (Base ID)

8.8.48 SW_ID_MASK_DLC Register (Address = 38h) [reset = 00h]

SW_ID_MASK_DLC is shown in [Table 8-122](#) and described in [Table 8-123](#).

Return to [Table 8-26](#).

ID Mask 2:0 and Extended ID Mask 20:18 (Base ID), DLC[3:0] and data mask enable

Table 8-122. SW_ID_MASK_DLC Register

7	6	5	4	3	2	1	0
ID_MASK[2:0]	EXT_ID_MASK[20:18]			DLC			DATA_MASK_EN
R/W-000b				R/W-0000b			R/W-0b

Table 8-123. SW_ID_MASK_DLC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	ID_MASK[2:0]_EXT_ID_MASK[20:18]	R/W	000b	ID Mask 2:0 and Extended ID Mask 20:18 (Base ID)
4-1	DLC	R/W	0000b	DLC[3:0]
0	DATA_MASK_EN	R/W	0b	Data mask enable 0b = DLC field and Data field are not compared and assumed valid. Remote frames are allowed. 1b = DLC field must match DLC[3:0] register and data field bytes are compared with DATAx registers for a matching 1. Remote frames are ignored

8.8.49 DATA_y Register (Address = 39h + formula) [reset = 00h]

DATA_y is shown in [Table 8-124](#) and described in [Table 8-125](#).

Return to [Table 8-26](#).

Register address 39h through 40h

Offset = 39h + (y x 1h); where y = 0h to 7h

Table 8-124. DATA_y Register

7	6	5	4	3	2	1	0
DATAx							
R/W-00h							

Table 8-125. DATA_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATAx	R/W	00h	CAN data byte x

8.8.50 SW_RSVD_y Register (Address = 41h + formula) [reset = 00h]

SW_RSVD_y is shown in [Table 8-126](#) and described in [Table 8-127](#).

Return to [Table 8-26](#).

Register address 41h through 43F

Offset = 41h + (y x 1h); where y = 0h to 2h

Table 8-126. SW_RSVD_y Register

7	6	5	4	3	2	1	0
RESERVED							
R-00h							

Table 8-127. SW_RSVD_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	00h	Reserved

8.8.51 SW_CONFIG_1 Register (Address = 44h) [reset = 50h]

SW_CONFIG_1 is shown in [Table 8-128](#) and described in [Table 8-129](#).

Return to [Table 8-26](#).

CAN and CAN FD DR

Table 8-128. SW_CONFIG_1 Register

7	6	5	4	3	2	1	0
SW_FD_PASSIVE	CAN_DR			FD_DR		RESERVED	
R/W-0b	R/W-101b			R/W-00b		R-00b	

Table 8-129. SW_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SW_FD_PASSIVE	R/W	0b	Selective Wake FD Passive: this bit modifies the behavior of the error counter when CAN with flexible data rate frames are seen. 0b = CAN with flexible data rate frame will be counted as an error frame 1b = CAN with flexible data rate frame are ignored (passive)
6-4	CAN_DR	R/W	101b	CAN bus data rate 0b = 50 Kbps 1b = 100 Kbps 10b = 125 Kbps 11b = 250 Kbps 100b = Reserved 101b = 500 Kbps 110b = Reserved 111b = 1 Mbps
3-2	FD_DR	R/W	00b	CAN bus FD data rate ratio verses CAN data rate 0b = CAN FD <= 4x CAN data rate 1b = CAN FD => 5x and <= 10x CAN data rate 10b = CAN FD 8 Mbps verses 500k CAN data rate 10b = Reserved 11b = Reserved
1-0	RESERVED	R	00b	Reserved

8.8.52 SW_CONFIG_2 Register (Address = 45h) [reset = 00h]

SW_CONFIG_2 is shown in [Table 8-130](#) and described in [Table 8-131](#).

Return to [Table 8-26](#)

Frame Error Counter: this error counter is incremented by 1 for every received frame error detected (stuff bit, CRC or CRC delimiter form error). The counter is decremented by 1 for every correctly received CAN frame assuming the counter is not zero. In case the device is set for passive on CAN with flexible data rate frames, any frame detected as a CAN FD frame will have no impact on the frame error counter (no increment or decrement). If the frame counter reaches FRAME_CNT_THRESHOLD[7:0] value the next increment will overflow the counter, set FRAME_OVF flag. The counter is reset by the following: enabling the frame detection or $t_{SILENCE}$ detection.

Table 8-130. SW_CONFIG_2 Register

7	6	5	4	3	2	1	0
FRAME_CNTx							
RH-00h							

Table 8-131. SW_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FRAME_CNTx	RH	00h	Frame Error Counter: this error counter is incremented by 1 for every received frame error detected (stuff bit, CRC or CRC delimiter form error). The counter is decremented by 1 for every correctly received CAN frame assuming the counter is not zero. In case the device is set for passive on CAN with flexible data rate frames, any frame detected as a CAN FD frame will have no impact on the frame error counter (no increment or decrement). If the frame counter reaches FRAME_CNT_THRESHOLD[7:0] value the next increment will overflow the counter, set FRAME_OVF flag. The counter is reset by the following: enabling the frame detection or $t_{SILENCE}$ detection.

8.8.53 SW_CONFIG_3 Register (Address = 46h) [reset = 1Fh]

SW_CONFIG_3 is shown in [Table 8-132](#) and described in [Table 8-133](#).

Return to [Table 8-26](#).

Frame Error Counter Threshold: these bits set the point at which the error counter reaches its maximum and on the next error frame will overflow and set the FRAME_OVF flag. Default is 31 so the 32nd error will set the overflow flag.

Table 8-132. SW_CONFIG_3 Register

7	6	5	4	3	2	1	0
FRAME_CNT_THRESHOLD							
R/W-1Fh							

Table 8-133. SW_CONFIG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FRAME_CNT_THRESHOLD	R/W	1Fh	Frame Error Counter Threshold: these bits set the point at which the error counter reaches its maximum and on the next error frame will overflow and set the FRAME_OVF flag. Default is 31 so the 32nd error will set the overflow flag.

8.8.54 SW_CONFIG_4 Register (Address = 47h) [reset = 00h]

SW_CONFIG_4 is shown in [Table 8-134](#) and described in [Table 8-135](#).

Return to [Table 8-26](#).

Table 8-134. SW_CONFIG_4 Register

7	6	5	4	3	2	1	0
SWCFG	CAN_SYNC_FD	CAN_SYNC			RESERVED		
RH/W-0b	RH-0b	RH-0b			R-00000b		

Table 8-135. SW_CONFIG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SWCFG	RH/W	0b	Selective wake configuration complete 0b = SW registers not configured 1b = SW registers configured Note: Make this the last step in configuring and turning on selective wake. Note Writing to any of these wake configuration registers (8'h30-8'h44, 8'h46) clears the SWCFG bit.
6	CAN_SYNC_FD	RH	0b	device is properly decoding CAN FD frames if frame detection is enabled. This flag is updated after every received frame. By polling this flag, the system may determine if the device is properly decoding CAN FD frames, up to but not including the Data Field. This flag is self-clearing.
5	CAN_SYNC	RH	0b	Synchronized to CAN data: this flag indicates the device is properly decoding CAN frames if frame detection is enabled. This flag is updated after every received frame. By polling this flag, the system may determine if the device is properly decoding CAN frames. This flag is self-clearing.
4-0	RESERVED	R	00000b	Reserved

8.8.55 SW_CONFIG_RSVD_y Register (Address = 48h + formula) [reset = 00h]

SW_CONFIG_RSVD_y is shown in [Table 8-136](#) and described in [Table 8-137](#).

Return to [Table 8-26](#).

Register address 48h through 4Dh

Offset = 48h + (y x 1h); where y = 0h to 5h

Table 8-136. SW_CONFIG_RSVD_y Register

7	6	5	4	3	2	1	0
RESERVED							
R-00h							

Table 8-137. SW_CONFIG_RSVD_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	00h	Reserved

8.8.56 HSS_CNTL2 (Address = 4Dh) [reset = 00h]

HSS_CNTL2 is shown in [Table 8-138](#) and described in [Table 8-139](#).

Return to [Table 8-26](#).

HSS3 and HSS4 high side switch control.

Table 8-138. HSS_CNTL2

7	6	5	4	3	2	1	0
RSVD	HSS3_CNTL			RSVD	HSS4_CNTL		
R-0b	R/W-000b			R-0b	R/W-000b		

Table 8-139. HSS_CNTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Reserved
6-4	HSS3_CNTL	R/W	000b	Control for HSS3 000b = Off 001b = PWM1 010b = PWM2 011b = Timer1 100b = Timer2 101b = On 110b = PWM3 111b = PWM4
3	RSVD	R	0b	Reserved
2-0	HSS4_CNTL	R/W	000b	Control for HSS4 000b = Off 001b = PWM1 010b = PWM2 011b = Timer1 100b = Timer2 101b = On 110b = PWM3 111b = PWM4

Note

When configuring HSS3 and HSS4 and they need to align PWM3 and PWM4 if PWM. PWM1 and PWM2 control will change to PWM3 and PWM4 when setting register 8'hC[5:4] = 01b.

8.8.57 EEPROM_CONFIG (Address = 4Eh) [reset = 00h]

EEPROM_CONFIG is shown in [Table 8-140](#) and described in [Table 8-141](#).

Return to [Table 8-26](#).

The register controls the access to the EEPROM.

Table 8-140. EEPROM_CONFIG

7	6	5	4	3	2	1	0
EEPROM_SAVE	EEPROM_CRC_CHK	EEPROM_REL_OAD	RSVD	EEPROM_CODE			
R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0000b			

Table 8-141. EEPROM_CONFIG Register Field Description

Bit	Field	Type	Reset	Description
7	EEPROM_SAVE	R/W	0b	Write a 1b & correct code to register 8'h4E[3:0] to save configuration bits to EEPROM. Self clears after EEPROM is written to.

Table 8-141. EEPROM_CONFIG Register Field Description (continued)

Bit	Field	Type	Reset	Description
6	EEPROM_CRC_CHK	R/W	0b	Write a 1b to force a EEPROM read and CRC check. Automatically clears upon completion
5	EEPROM_RELOAD	R/W	0b	Write a 1b to reload memory from the EEPROM
4	RSVD	R	0b	Reserved
3-0	EEPROM_CODE	W	0000b	Required code to update EEPROM. 0Ah is used and will read back 0h.

8.8.58 HSS_CNTL3 (Address = 4Fh) [reset = 00h]

HSS_CNTL3 is shown in Figure 8-66 and described in Table 8-142.

Return to [Table 8-26](#).

Used to determine HSS behavior during VHSS over/under-voltage and Register 8'h0E[7:5] provides the status of VEXCC, VCC2 and VCAN.

Bit 0 is saved to EEPROM if used

Figure 8-66. HSS_CNTL3

7	6	5	4	3	2	1	0
HSS_OV_DIS	HSS_UV_DIS	HSS_OV_UV_REC	SLP_CYC_WK_EN	VEXCC_STATUS	VCC2_STATUS	VCAN_STATUS	RSTRT_TMR_SEL
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/H-0b	R/H-0b	R/H-0b	R/W-0b

Table 8-142. HSS_CNTL3 Register Field Description

Bit	Field	Type	Reset	Description
7	HSS_OV_DIS	R/W	0b	Disables high-side switches from shutting down due to an OVHSS event 0b = Enabled 1b = Disabled
6	HSS_UV_DIS	R/W	0b	Disables high-side switches from shutting down due to an UVHSS event 0b = Enabled 1b = Disabled
5	HSS_OV_UV_REC	R/W	0b	Disables high-side switches from automatically recovering to previous state due to an OVHSS or UVHSS event 0b = Enabled 1b = Disabled
4	SLP_CYC_WK_EN	R/W	0b	Enables Cyclic Wake in sleep mode based upon timer 1 or timer 2 0b = Disabled 1b = Enabled
3	VEXCC_STATUS	R/H	0b	VEXCC status 0b = UVEXCC or off 1b = In regulation
2	VCC2_STATUS	R/H	0b	VCC2 status 0b = UVCC2 or off 1b = In regulation
1	VCAN_STATUS	R/H	0b	VCAN status 0b = UVCAN or off 1b = Good
0	RSTRT_TMR_SEL	R/W	0b	Selects the restart timer used to exit restart mode if VCC1 does not exceed UVCC1R 0b = t_{RSTTO} 1b = $t_{INACTIVE}$

8.8.59 INT_GLOBAL Register (Address = 50h) [reset = 00h]

INT_GLOBAL is shown in [Table 8-143](#) and described in [Table 8-144](#).

Return to [Table 8-26](#).

Logical OR of all to certain interrupts

Table 8-143. INT_GLOBAL Register

7	6	5	4	3	2	1	0
INT_7	INT_1	INT_2	INT_3	INT_CANBUS	INT_4	INT_5	INT_6
RH-0b	RH-0b	RH-0b	RH-0b	RH-0b	RH-0b	RH-0b	RH-0b

Table 8-144. INT_GLOBAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_7	RH	0b	Logical OR of INT_7 register
6	INT_1	RH	0b	Logical OR of INT_1 register
5	INT_2	RH	0b	Logical OR of INT_2 register
4	INT_3	RH	0b	Logical OR of INT_3 register
3	INT_CANBUS	RH	0b	Logical OR of INT_CANBUS register
2	INT_4	RH	0b	Logical OR of INT_4 register
1	INT_5	RH	0b	Logical OR of INT_5 register
0	INT_6	RH	0b	Logical OR of INT_6 register

8.8.60 INT_1 Register (Address = 51h) [reset = 00h]

INT_1 is shown in [Table 8-145](#) and described in [Table 8-146](#).

Return to [Table 8-26](#).

Table 8-145. INT_1 Register

7	6	5	4	3	2	1	0
WD	CANINT1	LWU	WKERR	FRAME_OVF_1	CANSLNT_1	CANTO_1	CANDOM_1
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 8-146. INT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD	R/W1C	0b	Watchdog event interrupt. Note This interrupt bit will be set for every watchdog error event and does not rely upon the Watchdog error counter
6	CANINT1	R/W1C	0b	CAN bus wake up interrupt
5	LWU	R/W1C	0b	Local wake up
4	WKERR	R/W1C	0b	Wake error bit is set when the SWE timer has expired and the state machine has returned to Sleep mode
3	FRAME_OVF_1	R/W1C	0b	Frame error counter overflow
2	CANSLNT_1	R/W1C	0b	CAN bus inactive for $t_{SILENCE}$
1	CANTO_1	R/W1C	0b	CAN bus inactive for $t_{SILENCE}$ while Selective Wake is enabled and in Sleep Mode
0	CANDOM_1	R/W1C	0b	CAN bus stuck dominant

8.8.61 INT_2 Register (Address = 52h) [reset = 40h]

INT_2 is shown in [Table 8-147](#) and described in [Table 8-148](#).

Return to [Table 8-26](#).

Table 8-147. INT_2 Register

7	6	5	4	3	2	1	0
SMS	PWRON	OVCC1	UVSUP5	UVSUP3	UVCC1	TSD_VCC1_VE XCC	RSVD
R/W1C-0b	R/W1C-1b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R-0b

Table 8-148. INT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SMS	R/W1C	0b	Sleep mode status flag. Sets whenever Sleep mode is entered from a WKERR or an SBC fault.
6	PWRON	R/W1C	1b	Power on
5	OVCC1	R/W1C	0b	VCC1 overvoltage
4	UVSUP5	R/W1C	0b	VSUP undervoltage for 5 V
3	UVSUP3	R/W1C	0b	VSUP undervoltage for 3.3 V
2	UVCC1	R/W1C	0b	VCC1 undervoltage
1	TSD_VCC1_VEXCC	R/W1C	0b	Thermal Shutdown due to VCC1 or VEXCC
0	RSVD	R	0b	Reserved

8.8.62 INT_3 Register (Address 53h) [reset = 00h]

INT_3 is shown in [Table 8-149](#) and described in [Table 8-150](#).

Return to [Table 8-26](#).

Interrupt set when the internal EEPROM used for trimming has a CRC error. Upon power up, the device loads an internal register from the EEPROM and performs a CRC check. If an error is present after eight attempts of loading valid data the CRC_EEPROM interrupt will be set. This will indicate an error that may impact device performance. This is repeated when the device leaves sleep mode or fail-safe mode due to a wake event.

Table 8-149. INT_3 Register

7	6	5	4	3	2	1	0
SPIERR	SWERR	FSM	CRCERR	VCC1SC	RSTR_CNT	TSD_CAN_LIN	CRC_EEPROM
R/W1C-0b	RH-0b	R/W1C-0b	R/W1C/H-0b	R/W1C/H-0b	R/W1C/H-0b	R/W1C-0b	R/W1C-0b

Table 8-150. INT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR	R/W1C	0b	Sets when SPI status bit sets
6	SWERR	RH	0b	Logical OR of (SW_EN=1 and NOT(SWCFG)) and FRAME_OVF. Selective Wake may not be enabled while SWERR is set
5	FSM	R/W1C	0b	Entered fail-safe mode.
4	CRCERR	R/W1C/H	0b	SPI CRC error detected
3	VCC1SC	R/W1C/H	0b	VCC1 short detected
2	RSTR_CNT	R/W1C/H	0b	Restart counter exceeded programmed count
1	TSD_CAN_LIN	R/W1C	0b	Thermal Shutdown due to VCC2, CAN or LIN transceiver
0	CRC_EEPROM	R/W1C	0b	EEPROM CRC error

8.8.63 INT_CANBUS_1 Register (Address = 54h) [reset = 00h]

INT_CANBUS is shown in [Table 8-151](#) and described in [Table 8-152](#).

Return to [Table 8-26](#).

CAN bus faults that include shorts and opens CAN port 1

Table 8-151. INT_CANBUS_1 Register

7	6	5	4	3	2	1	0
UVCAN	RSVD	CANHCANL	CANHBAT	CANLGND	CANBUSOPEN	CANBUSGND	CANBUSBAT
R/W1C-0b	R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 8-152. INT_CANBUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UVCAN	R/W1C	0b	VCAN undervoltage
6	RSVD	R	0b	Reserved
5	CANHCANL	R/W1C	0b	CANH and CANL shorted together
4	CANHBAT	R/W1C	0b	CANH shorted to Vbat
3	CANLGND	R/W1C	0b	CANL shorted to GND
2	CANBUSOPEN	R/W1C	0b	CAN bus open
1	CANBUSGND	R/W1C	0b	CAN bus shorted to GND or CANH shorted to GND
0	CANBUSBAT	R/W1C	0b	CAN bus shorted to Vbat or CANL shorted to Vbat

8.8.64 INT_7 (Address = 55h) [reset = 00h]

INT_7 is shown in [Table 8-153](#) and described in [Table 8-154](#).

Return to [Table 8-26](#).

High side switch interrupts.

Table 8-153. INT_7

7	6	5	4	3	2	1	0
HSSOC1	HSSOL1	HSSOC2	HSSOL2	HSSOC3	HSSOL3	HSSOC4	HSSOL4
R/W1C-0b							

Table 8-154. INT_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSSOC1	R/W1C	0b	High side switch 1 over current
6	HSSOL1	R/W1C	0b	High side switch 1 open load
5	HSSOC2	R/W1C	0b	High side switch 2 over current
4	HSSOL2	R/W1C	0b	High side switch 2 open load
3	HSSOC3	R/W1C	0b	High side switch 3 over current
2	HSSOL3	R/W1C	0b	High side switch 3 open load
1	HSSOC4	R/W1C	0b	High side switch 4 over current
0	HSSOL4	R/W1C	0b	High side switch 4 open load

8.8.65 INT_EN_1 Register (Address = 56h) [reset = FFh]

INT_EN_1 is shown in [Table 8-155](#) and described in [Table 8-156](#).

Return to [Table 8-26](#).

Interrupt mask for INT_1. CAN errors are for CAN port 1.

Table 8-155. INT_EN_1 Register

7	6	5	4	3	2	1	0
WD_EN	CANINT_EN_1	LWU_EN	WKERR_EN	FRAME_OVF_EN_1	CANSLNT_EN_1	CANTO_EN_1	CANDOM_EN_1
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 8-156. INT_EN_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_EN	R/W	1b	Watchdog event interrupt mask
6	CANINT_EN_1	R/W	1b	CAN bus wake up interrupt mask
5	LWU_EN	R/W	1b	Local wake up mask
4	WKERR_EN	R/W	1b	Wake error mask
3	FRAME_OVF_EN_1	R/W	1b	Frame error counter overflow mask
2	CANSLNT_EN_1	R/W	1b	CAN silent mask
1	CANTO_EN_1	R/W	1b	CAN timeout mask
0	CANDOM_EN_1	R/W	1b	CAN bus stuck dominant mask

8.8.66 INT_EN_2 Register (Address = 57h) [reset = 7Eh]

INT_EN_2 is shown in [Table 8-157](#) and described in [Table 8-158](#).

Return to [Table 8-26](#).

Interrupt mask for INT_2

Table 8-157. INT_EN_2 Register

7	6	5	4	3	2	1	0
SMS_EN	PWRON_EN	OVCC1_EN	UVSUP5_EN	UVSUP3_EN	UVCC1_EN	TSD_VCC1_VE_XCC_EN	RSVD
R-0b	R-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R-0b

Table 8-158. INT_EN_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SMS_EN	R	0b	SMS read only
6	PWRON_EN	R	1b	Power on read only
5	OVCC1_EN	R/W	1b	VCC1 over-voltage mask
4	UVSUP5_EN	R/W	1b	VSUP5 undervoltage mask
3	UVSUP3_EN	R/W	1b	VSUP3 undervoltage mask
2	UVCC1_EN	R/W	1b	VCC1 undervoltage mask
1	TSD_VCC1_VEXCC_EN	R/W	1b	VCC1 and VEXCC thermal shutdown mask
0	RSVD	R	0b	Reserved

8.8.67 INT_EN_3 Register (Address = 58h) [reset = FEh]

INT_EN_3 is shown in [Table 8-159](#) and described in [Table 8-160](#).

Return to [Table 8-26](#).

Interrupt mask for INT_3

Table 8-159. INT_EN_3 Register

7	6	5	4	3	2	1	0
SPIERR_EN	SWERR_EN	FSM_EN	CRCERR_EN	VCC1SC_EN	RSRT_CNT_EN	TSD_CAN_LIN_EN	RSVD
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R-1b	R-0b

Table 8-160. INT_EN_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR_ENABLE	R/W	1b	SPI error interrupt mask
6	SWERR_ENABLE	R/W	1b	Selective wake error interrupt mask
5	FSM_ENABLE	R/W	1b	Fail-safe mode interrupt mask
4	CRCERR_EN	R/W	1b	SPI CRC error interrupt mask
3	VCC1SC_EN	R/W	1b	VCC1 short circuit interrupt mask
2	RSRT_CNT_EN	R/W	1b	Restart counter exceeded programmed count mask
1	TSD_CAN_LIN_EN	R/W	1b	VCC2, CAN and LIN transceiver thermal shutdown mask
0	RSVD	R	0b	Reserved

8.8.68 INT_EN_CANBUS_1 Register (Address = 59h) [reset = BFh]

INT_EN_CANBUS is shown in [Table 8-161](#) and described in [Table 8-162](#).

Return to [Table 8-26](#).

Interrupt mask for CAN port 1 bus faults

Table 8-161. INT_EN_CANBUS_1 Register

7	6	5	4	3	2	1	0
UVCAN_EN	RSVD	CANHCANL_EN	CANHBAT_EN	CANLGND_EN	CANBUSOPEN_EN	CANBUSGND_EN	CANBUSBAT_EN
R/W-1b	R-0b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 8-162. INT_EN_CANBUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UVCAN_EN	R/W	1b	VCAN undervoltage mask
6	RSVD	R	0b	Reserved
5	CANHCANL_EN	R/W	1b	CANH and CANL shorted together mask
4	CANHBAT_EN	R/W	1b	CANH shorted to Vbat mask
3	CANLGND_EN	R/W	1b	CANL shorted to GND mask
2	CANBUSOPEN_EN	R/W	1b	CAN bus open mask
1	CANBUSGND_EN	R/W	1b	CAN bus shorted to GND mask
0	CANBUSBAT_EN	R/W	1b	CAN bus shorted to Vbat mask

8.8.69 INT_4 Register (Address = 5Ah) [reset = 00h]

INT_4 is shown in [Table 8-163](#) and described in [Table 8-164](#).

Return to [Table 8-26](#).

Interrupt for LIN and high side switches

Table 8-163. INT_4 Register

7	6	5	4	3	2	1	0
LIN1_WUP	LIN1.DTO	RSVD	RSVD	MODE_ERR	OVHSS	EEPROM_CRC_INT	UVHSS
R/W1C-0b	R/W1C-0b	R-0b	R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 8-164. INT_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LIN1_WUP	R/W1C	0b	LIN 1 bus wake
6	LIN1.DTO	R/W1C	0b	LIN 1 dominant state timeout, LTXD.DTO
5	RSVD	R	0b	Reserved
4	RSVD	R	0b	Reserved
3	MODE_ERR	R/W1C	0b	Illegal transceiver state for mode change request
2	OVHSS	R/W1C	0b	Over-voltage on VHSS pin for high-side switches
1	EEPROM_CRC_INT	R/W1C	0b	EEPROM saved configuration CRC error
0	UVHSS	R/W1C	0b	Under-voltage on VHSS pin for high-side switches

8.8.70 INT_5 Register (Address = 5Bh) [reset = 00h]

INT_5 is shown in [Table 8-165](#) and described in [Table 8-166](#).

Return to [Table 8-26](#).

Table 8-165. INT_5 Register

7	6	5	4	3	2	1	0
RSVD							
R-00h							

Table 8-166. INT_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RSVD	R	00h	Reserved

8.8.71 INT_6 Register (Address 5Ch) [reset = 00h]

INT_6 is shown in [Table 8-167](#) and described in [Table 8-168](#).

Return to [Table 8-26](#).

Table 8-167. INT_6 Register

7	6	5	4	3	2	1	0
TSDW	UVCC1PW	UVEXCC	OVEXCC	VEXCCSC	UVCC2	OVCC2	VCC2SC
R/W1C-0b							

Table 8-168. INT_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TSDW	R/W1C	0b	Thermal shutdown warning
6	UVCC1PW	R/W1C	0b	VCC1 under-voltage pre-warning
5	UVEXCC	R/W1C	0b	VEXCC undervoltage
4	OVEXCC	R/W1C	0b	VEXCC over-voltage
3	VEXCCSC	R/W1C	0b	VEXCC short circuit
2	UVCC2	R/W1C	0b	VCC2 under-voltage
1	OVCC2	R/W1C	0b	VCC2 over-voltage
0	VCC2SC	R/W1C	0b	VCC2 short circuit

8.8.72 INT_EN_4 Register (Address = 5Eh) [reset = CFh]

INT_EN_4 is shown in [Table 8-169](#) and described in [Table 8-170](#).

Return to [Table 8-26](#).

Interrupt mask for INT_4.

Table 8-169. INT_EN_4 Register

7	6	5	4	3	2	1	0
LIN1_WUP_EN	LIN1.DTO_EN	RSVD	RSVD	MODE_ERR_EN	OVHSS_EN	EEPROM_CRC_INT_EN	UVHSS_EN
R/W-1b	R/W-1b	R-0b	R-0b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 8-170. INT_EN_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LIN1_WUP_EN	R/W	1b	LIN 1 bus wake interrupt mask
6	LIN1.DTO_EN	R/W	1b	LIN 1 dominant state timeout interrupt mask
5	RSVD	R	0b	Reserved
4	RSVD	R	0b	Reserved
3	MODE_ERR_EN	R/W	1b	Illegal transceiver state for mode change request mask
2	OVHSS_EN	R/W	1b	VHSS over-voltage mask for high-side switches
1	EEPROM_CRC_INT_EN	R/W	1b	Mask for the saved configuration data to EEPROM error
0	UVHSS	R/W	1b	VHSS under-voltage mask for high-side switches

8.8.73 INT_EN_6 Register (Address = 60h) [reset = FFh]

INT_EN_6 is shown in [Table 8-171](#) and described in [Table 8-172](#).

Return to [Table 8-26](#).

Interrupt mask for INT_6.

Table 8-171. INT_EN_6 Register

7	6	5	4	3	2	1	0
TSDW_EN	UVCC1PW_EN	UVEXCC_EN	OVEXCC_EN	VEXCCSC_EN	UVCC2_EN	UVCC2_EN	VCC2SC_EN
R/W -1b	R/W -1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 8-172. INT_EN_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TSDW_EN	R/W	1b	Thermal shutdown warning mask
6	UVCC1PW_EN	R/W	1b	VCC1 under-voltage pre-warning mask
5	UVEXCC_EN	R/W	1b	VEXCC under-voltage mask
4	OVEXCC_EN	R/W	1b	VEXCC over-voltage mask
3	VEXCCSC_EN	R/W	1b	VEXCC short circuit mask
2	UVCC2_EN	R/W	1b	VCC2 pin under-voltage mask
1	OVCC2_EN	R/W	1b	VCC2 pin over-voltage mask
0	VCC2SC_EN	R/W	1b	VCC2 short circuit mask

8.8.74 INT_EN_7 Register (Address = 62) [reset = FFh]

INT_EN_7 is shown in [Table 8-173](#) and described in [Table 8-174](#).

Return to [Table 8-26](#).

Interrupt mask high side switch interrupts, INT_7.

Table 8-173. INT_EN_7 Register

7	6	5	4	3	2	1	0
HSSOC1_EN	HSSOL1_EN	HSSOC2_EN	HSSOL2_EN	HSSOC3_EN	HSSOL3_EN	HSSOC4_EN	HSSOL4_EN
R/W-1b							

Table 8-174. INT_EN_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSSOC1_EN	R/W	1b	High side switch 1 over current interrupt mask
6	HSSOL1_EN	R/W	1b	High side switch 1 open load interrupt mask
5	HSSOC2_EN	R/W	1b	High side switch 2 over current interrupt mask
4	HSSOL2_EN	R/W	1b	High side switch 2 open load interrupt mask
3	HSSOC3_EN	R/W	1b	High side switch 3 over current interrupt mask
2	HSSOL3_EN	R/W	1b	High side switch 3 open load interrupt mask
1	HSSOC4_EN	R/W	1b	High side switch 4 over current interrupt mask
0	HSSOL4_EN	R/W	1b	High side switch 4 open load interrupt mask

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TCAN284xx-Q1 family supports CAN FD communication while certain device also supports LIN communication

9.1.1 CAN BUS Loading, Length and Number of Nodes

The ISO11898-2:2016 standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes require a transceiver with high input impedance such as this transceiver family.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898-2:2016 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC825, CANopen, DeviceNet, SAEJ2284, SAEJ1939, and NMEA200.

A CAN network system design is a series of tradeoffs. In ISO11898-2 the driver differential output is specified with a $60\ \Omega$ bus load (the two termination resistors in parallel) where the differential output must be greater than 1.5 V. The TCAN284xx-Q1 is specified to meet the 1.5 V requirement with a across this load range and is specified to meet 1.4 V differential output at $45\ \Omega$ bus load. The differential input resistance of this family of transceiver is a minimum of $30k\Omega$. If 167 of these transceivers are in parallel on a bus, this is equivalent to an $180\ \Omega$ differential load in parallel with the $60\ \Omega$ from termination gives a total bus load of $45\ \Omega$. Therefore, this family theoretically supports over 167 transceivers on a single bus segment with margin to the 1.2 V minimum differential input voltage requirement at each receiving node. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is much lower. Bus length may also be extended beyond the original ISO11898-2:2016 standard of 40 m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of its key strengths allowing for these system level network extensions and additional standards to build on the original ISO11898-2 CAN standard. However, when using this flexibility, the CAN network system designer must take the responsibility of good network design to ensure robust network operation.

9.1.2 CAN Termination

The ISO11898-2:2016 standard specifies the interconnection to be a single twisted pair cable (shielded or unshielded) with $120\ \Omega$ characteristic impedance (Z_0).

9.1.2.1 Termination

Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be in a node but is generally not recommended, especially if the node may be removed from the bus. Termination must be carefully placed so that it is not removed from the bus. System level CAN implementations such as CANopen allow for different termination and cabling concepts for example to add cable length.

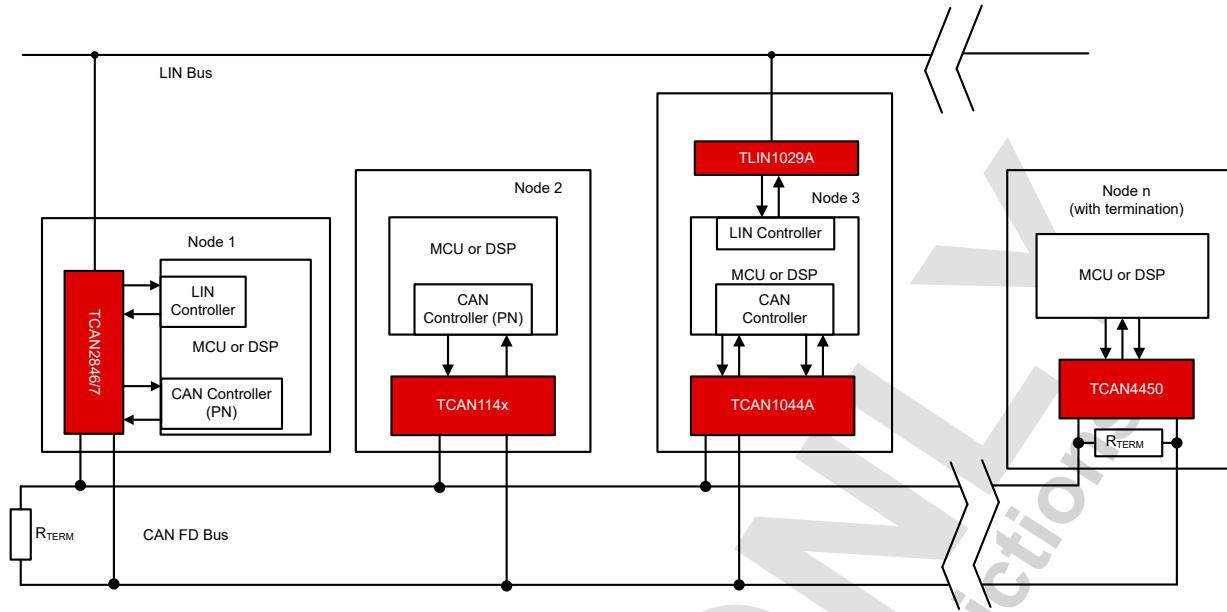


Figure 9-1. Typical CAN FD and LIN Bus

Termination may be a single 120Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired then “split termination” may be used, see [Figure 9-2](#). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltage levels at the start and end of message transmissions.

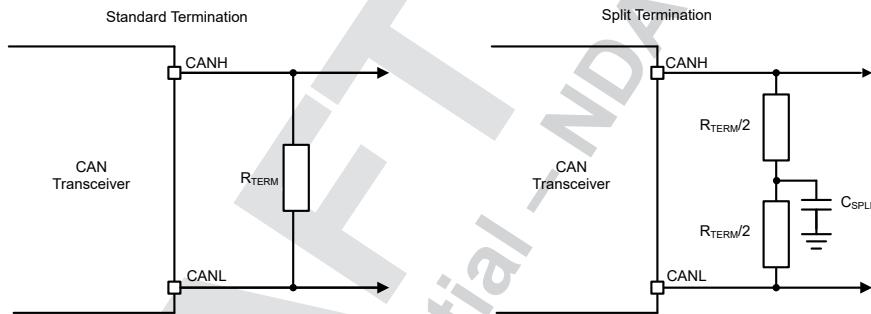


Figure 9-2. CAN Bus Termination Concepts

9.1.2.2 CAN Bus Biasing

Bus biasing can be normal biasing, active in normal mode and inactive in low-power mode. Automatic voltage biasing is where the bus is active in normal mode but is controlled by the voltage between CANH and CANL in lower power modes. See [Figure 9-3](#) for the state diagram on how the TCAN284xx-Q1 performs automatic biasing.

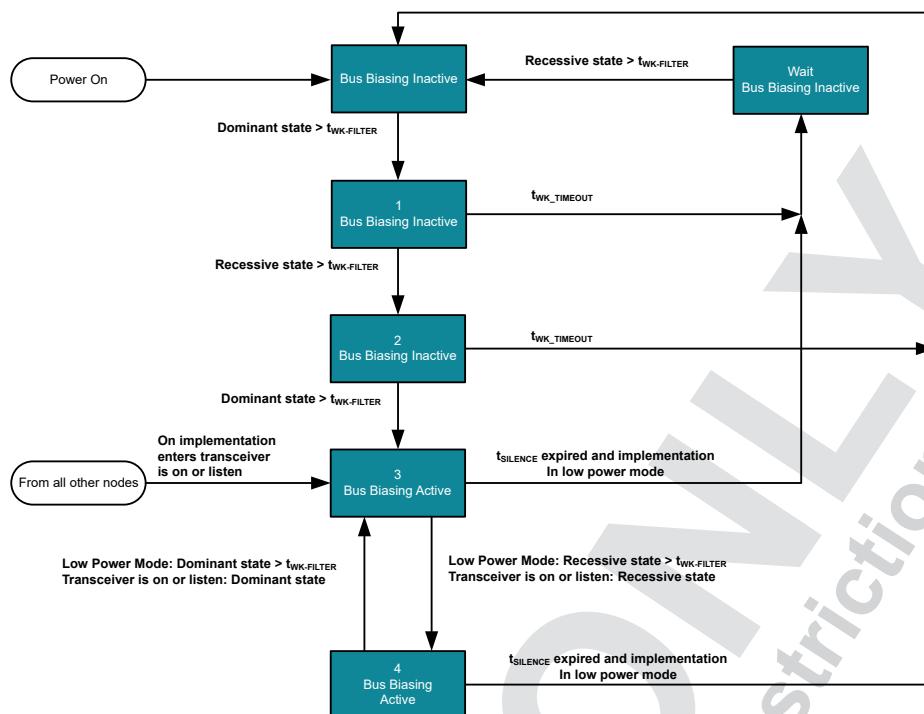


Figure 9-3. Automatic bus biasing state diagram

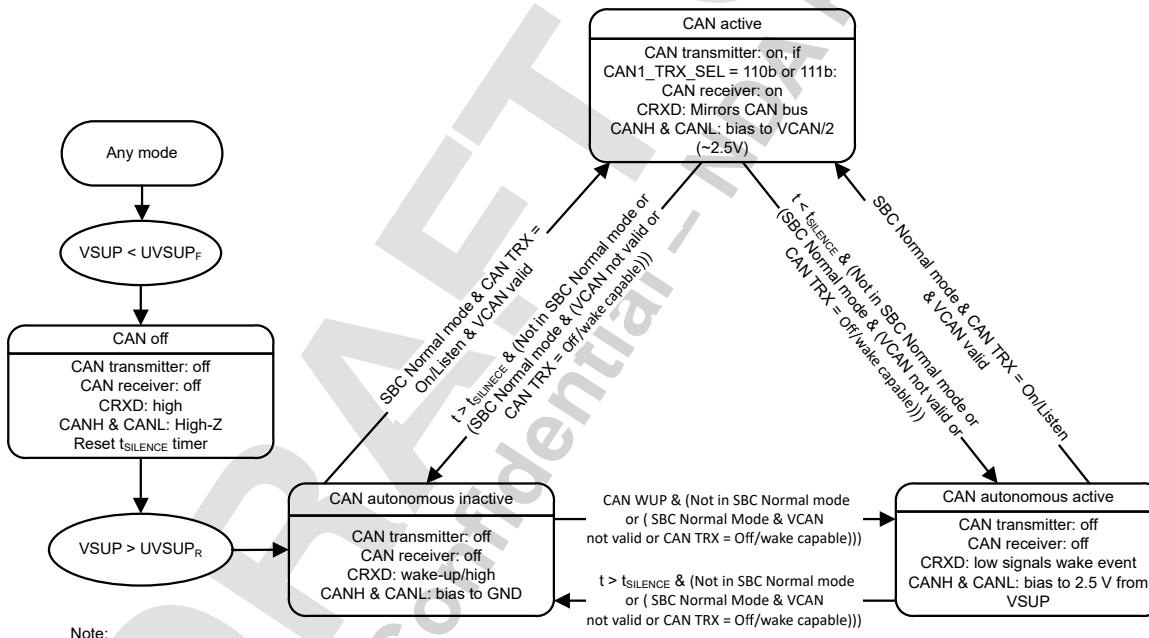


Figure 9-4. Bus biasing

9.1.3 Channel Expansion

The TCAN284xx-Q1 devices have the ability to control an external LIN or CAN FD transceiver or even other LIN and CAN FD SBCs. The processor controls the mode of the transceiver with the GFO pin as an EN/STB/nSTB/S pin. This capability allows the system implementer the ability to have many different configurations.

- Two CAN FD transceivers by using the TCAN2844x or TCAN2845x with an eight pin CAN FD transceiver

- Two CAN FD transceivers and a LIN transceiver by using the TCAN2846x or TCAN2847x with an eight pin CAN FD transceiver, see [Figure 9-8](#)
- On CAN FD transceiver and two LIN transceivers by using the TCAN2846x or TCAN2847x with a LIN transceiver, see [Figure 9-6](#)
- A second SBC with a LIN transceiver can be implemented by using the TCAN2844x through TCAN2847x and the TLIN1028x, see [Figure 9-7](#)
- A second SBC with a CAN transceiver can be implemented by using the TCAN2844x through TCAN2847x and the TCAN1162x, see [Figure 9-9](#)

9.1.3.1 Channel Expansion for LIN

[Figure 9-5](#) and [Figure 9-6](#) show high level diagrams on how the TCAN2844x through TCAN2847x can control an external LIN transceiver. Both of these show a high side switch (HSS) providing the power to the transceiver. When the TCAN284xx goes to sleep mode the HSS is turned off thus turning off the power to the transceiver. If this is not desired the transceiver VSUP can be connected to the same VSUP power as the TCAN284xx device. To configure the TCAN284xx to control the LIN transceivers the following register and bits need to be configured.

- Register 29h[3:1] = 110b sets the GFO pin a general purpose output pin
- Register 29h[4] sets the level of the GFO pin, high or low in order to control the EN pin of a LIN transceiver or LIN SBC
- To utilize the HSS as the power to the transceiver, turn on the selected HSS

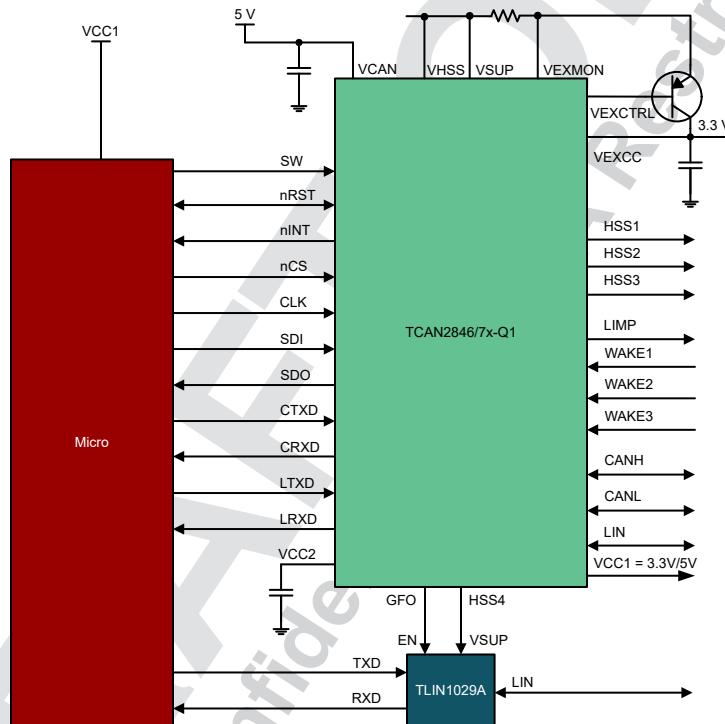


Figure 9-5. Channel Expansion Simple LIN Transceiver

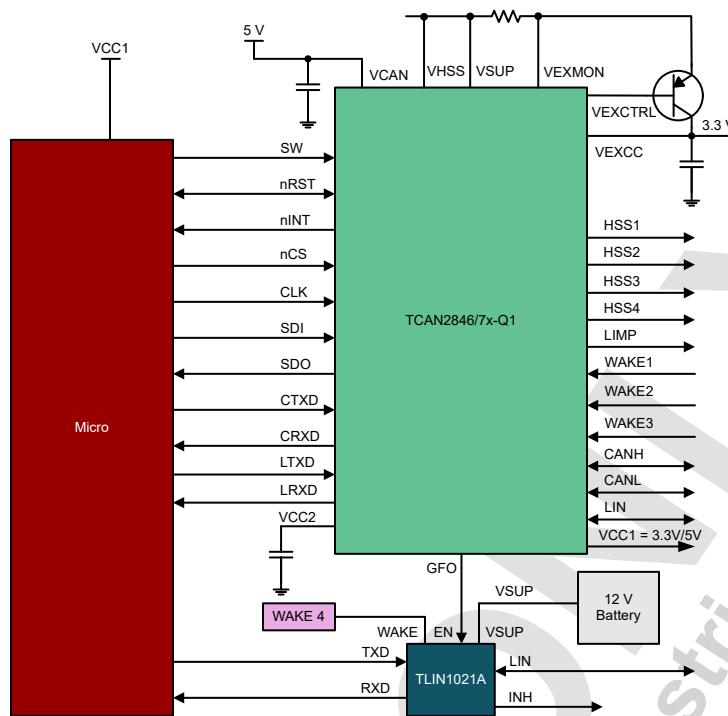


Figure 9-6. Channel Expansion Enhanced LIN Transceiver

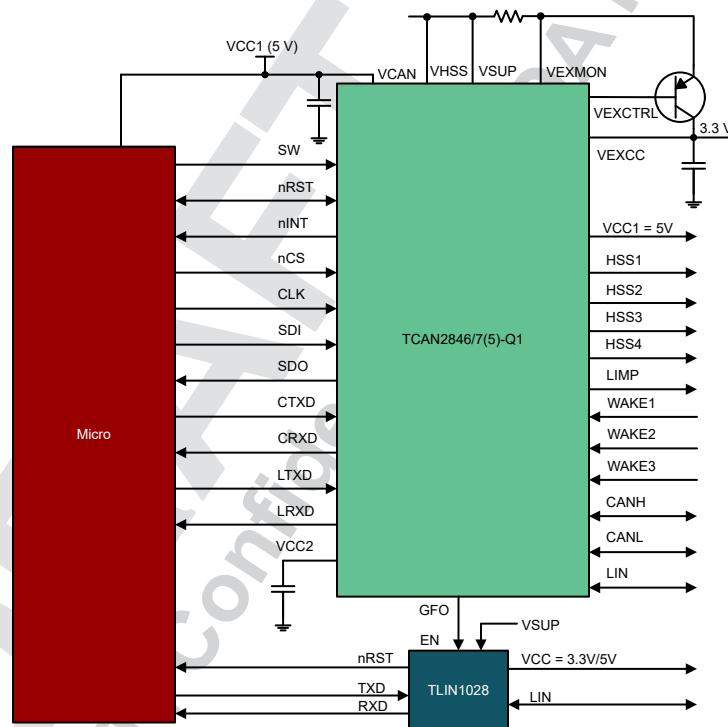


Figure 9-7. Channel Expansion with LIN SBC

9.1.3.2 Channel Expansion for CAN FD

Section 9.1.3.2 show high level diagrams on how the TCAN2846x or TCAN2847x can control an external CAN FD transceiver. As the LDO turns off in sleep mode or in various fault conditions like thermal shut down, the CAN FD transceiver will have its power shut off. To configure the TCAN284xx to control the CAN FD transceivers

the following register and bits need to be configured. If the 5 V variant shows VCC2 is used to power the CAN FD transceiver but VCC1 can also be used. A simple CAN SBC can also provide a second CAN transceiver as shown in [Figure 9-9](#)

- Register 29h[3:1] = 110b sets the GFO pin to a general purpose output pin
- Register 29h[4] sets the level of GFO pin to support an external CAN transceiver or SBC STB/nSTB/S pin.

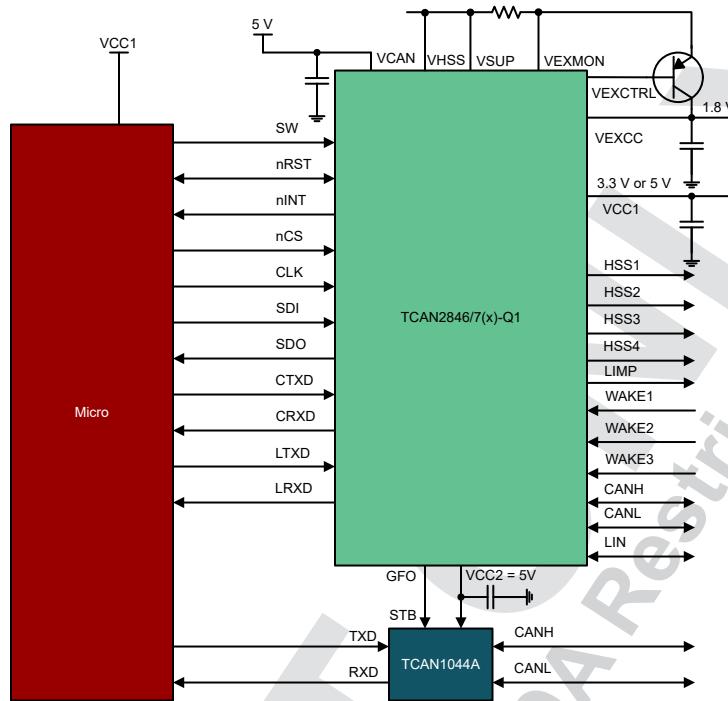


Figure 9-8. Channel Expansion with a CAN FD Transceiver

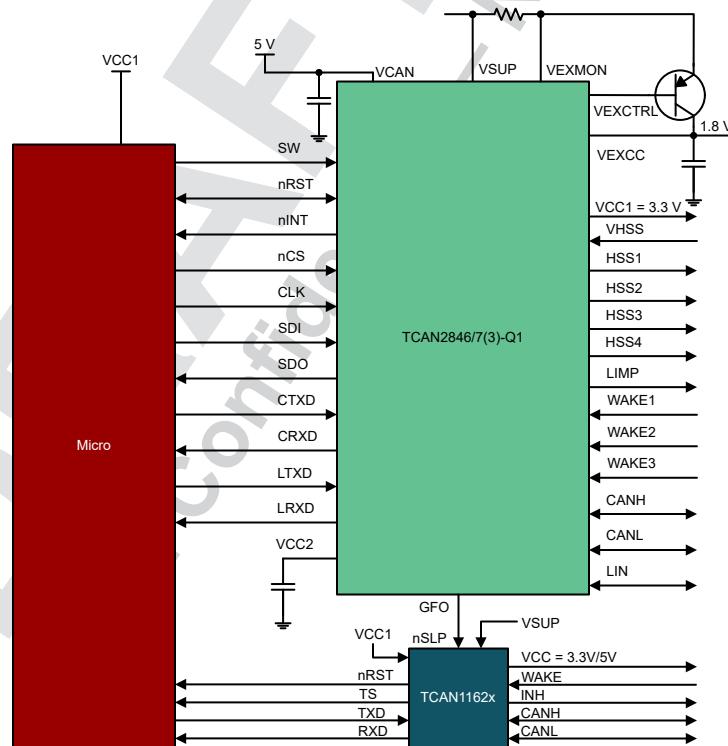


Figure 9-9. Channel Expansion with a CAN FD SBC

9.1.4 Device Brownout information

The brownout behavior of the TCAN284xx-Q1 depends upon VCC1 and whether VSUP drops below $VSUP_{(PU)F}$. For devices where $VCC1 = 5$ V, the device will behave as per Figure 9-10. When VSUP continues to fall to below $VSUP_{(PU)F}$, the device behaves as a power on reset as per Figure 9-11. UVSUP_{5F} is used for turning off VEXCC and UVSUP_{5R} is used to turn on VEXCC is programmed to be on.

When $VCC1 = 3.3$ V, Both UVSUP_{5R/F} and UVSUP_{33R/F} are utilized. The device will behave as per Figure 9-12 when VSUP drops below UVSUP_{33F} but stays above $VSUP_{(PU)F}$. When VSUP continues to fall to below $VSUP_{(PU)F}$, the device behaves as a power on reset as per Figure 9-13.

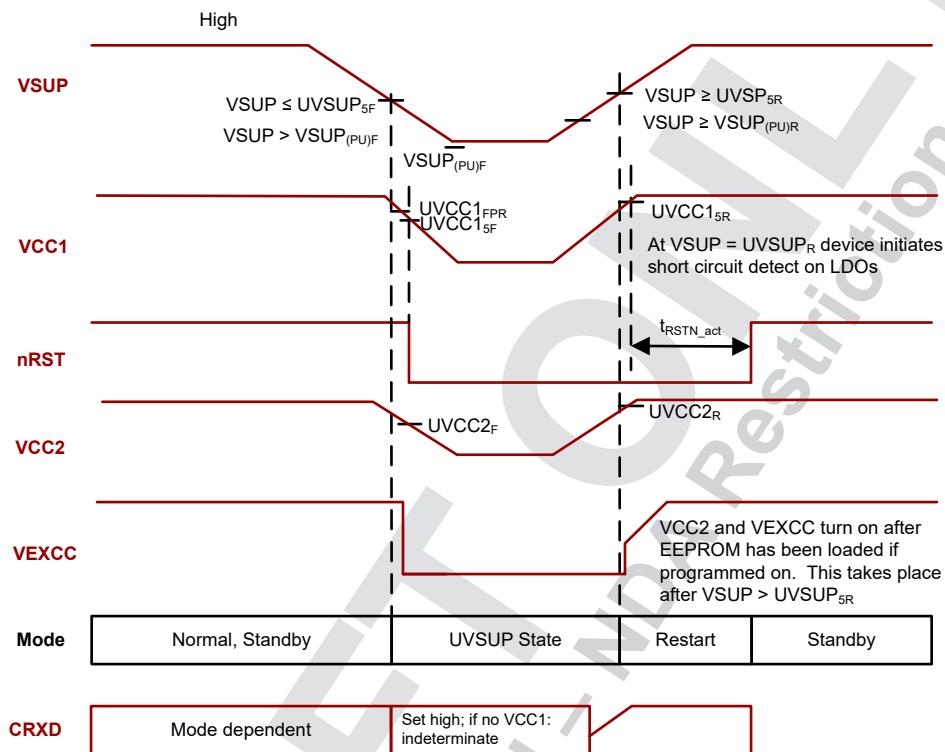
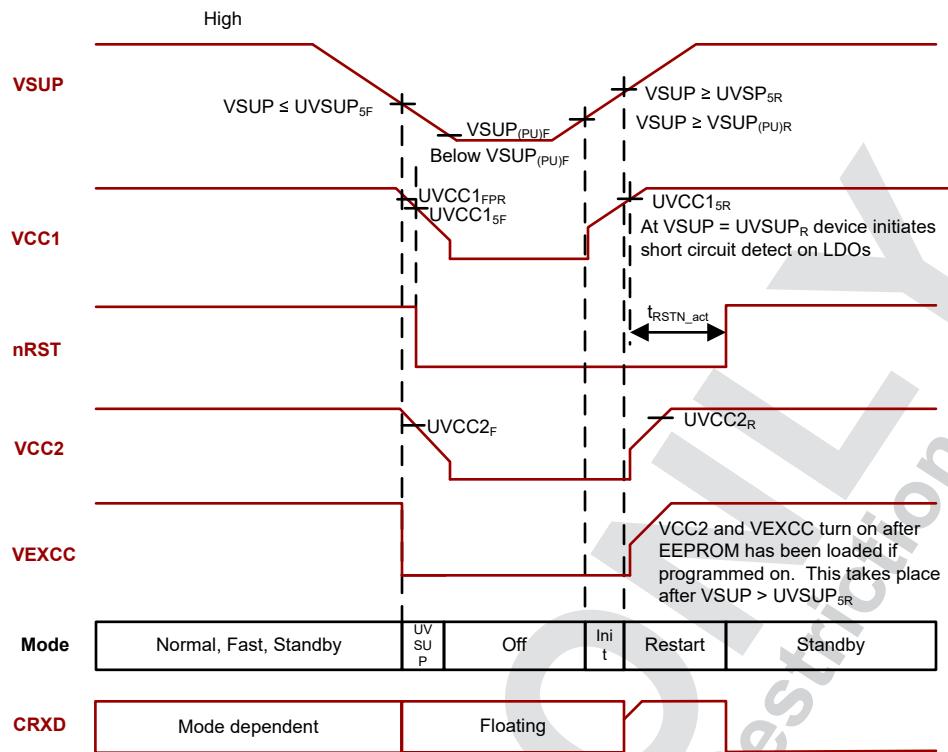
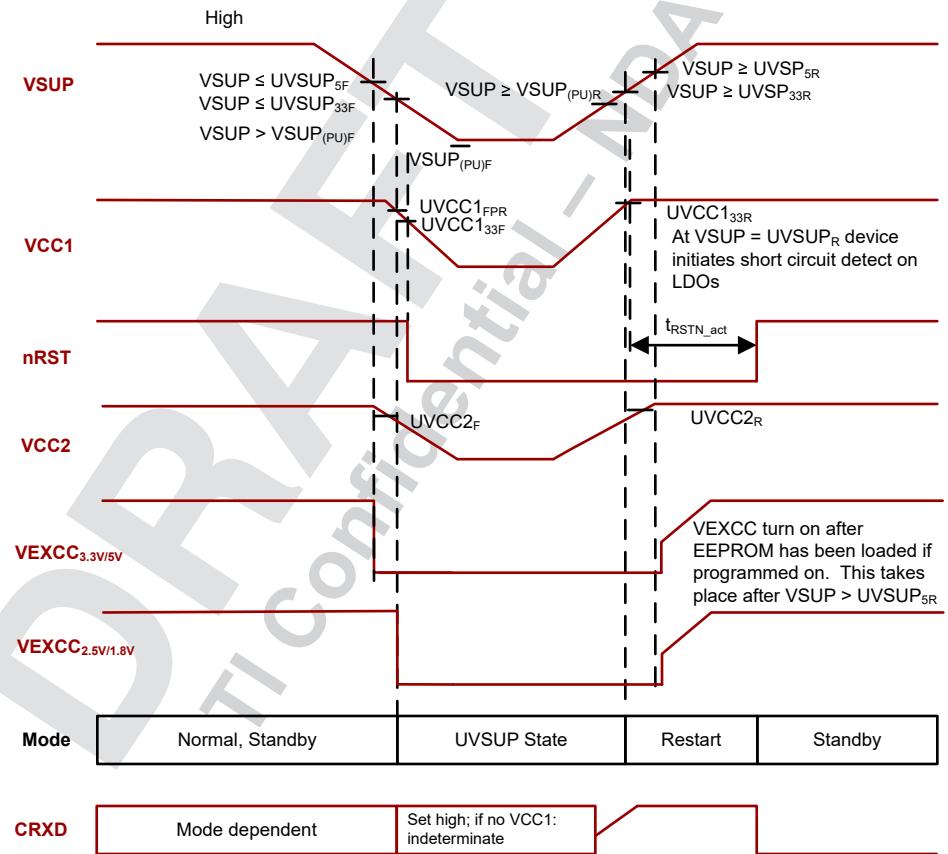


Figure 9-10. Brownout Above $VSUP_{(PU)F}$ for $VCC1 = 5$ V

**Figure 9-11. Brownout Below $VSUP_{(PU)F}$ for $VCC1 = 5\text{ V}$** **Figure 9-12. Brownout Above $VSUP_{(PU)F}$ for $VCC1 = 3.3\text{ V}$**

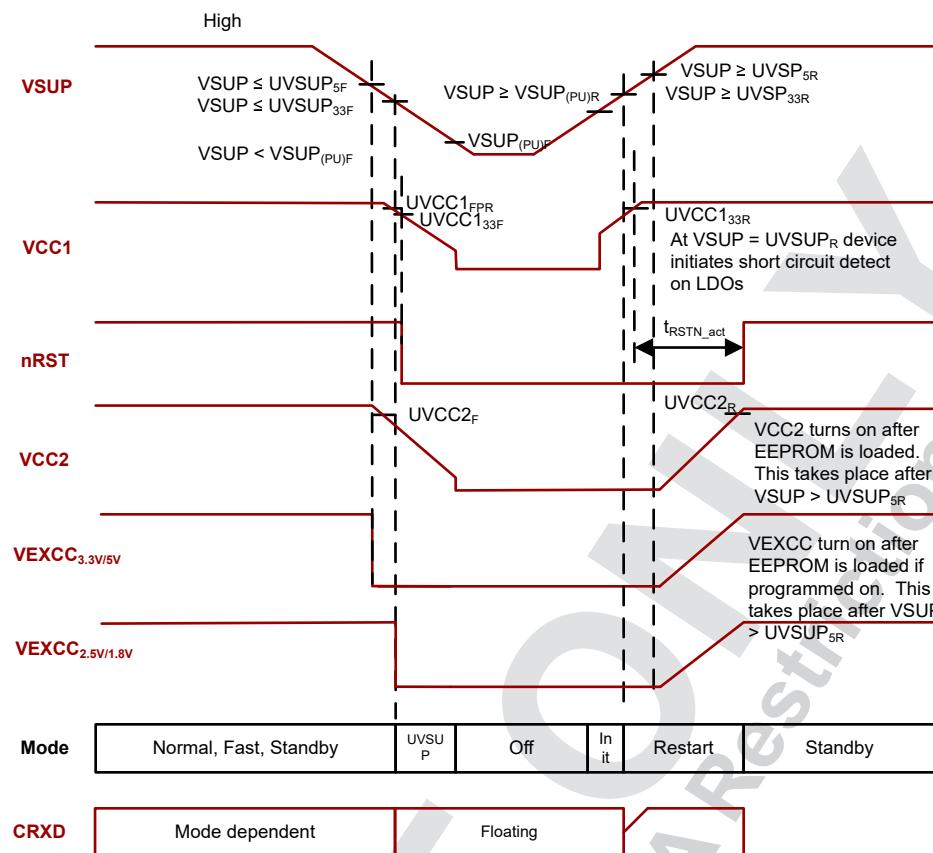


Figure 9-13. Brownout Below $VSUP_{(PU)F}$ for $VCC1 = 3.3\text{ V}$

9.1.5 Typical Application

The TCAN284xx-Q1 SBC family is typically used in applications with a host microprocessor or FPGA that requires CAN FD and LIN support while utilizing the devices many features like its watchdog, advanced bus fault diagnostics for CAN FD bus and high side switches. Below are typical applications configuration for 3.3 V microprocessor applications. These devices work with 3.3 V and 5 V microprocessors depending upon the value of VCC1. The bus termination is shown for illustrative purposes.

Figure 9-14 shows the TCAN2844x and TCAN2845x configured to support Cyclic sensing on WAKE pin and external PNP to support higher current for VCC1. Figure 9-15 shows the TCAN2846x and TCAN2847x supporting Cyclic sensing and three high side switches controlling LEDs.

Figure 9-16 shows the TCAN2846x and TCAN2847x with different functions than the previous application.

- VCC1 providing power to MCU
- External PNP providing power to a system sensor or second MCU
- HSS1 and HSS2 connected together to provide higher current to an external component.
- Cyclic sensing with the WAKE pin and HSS4

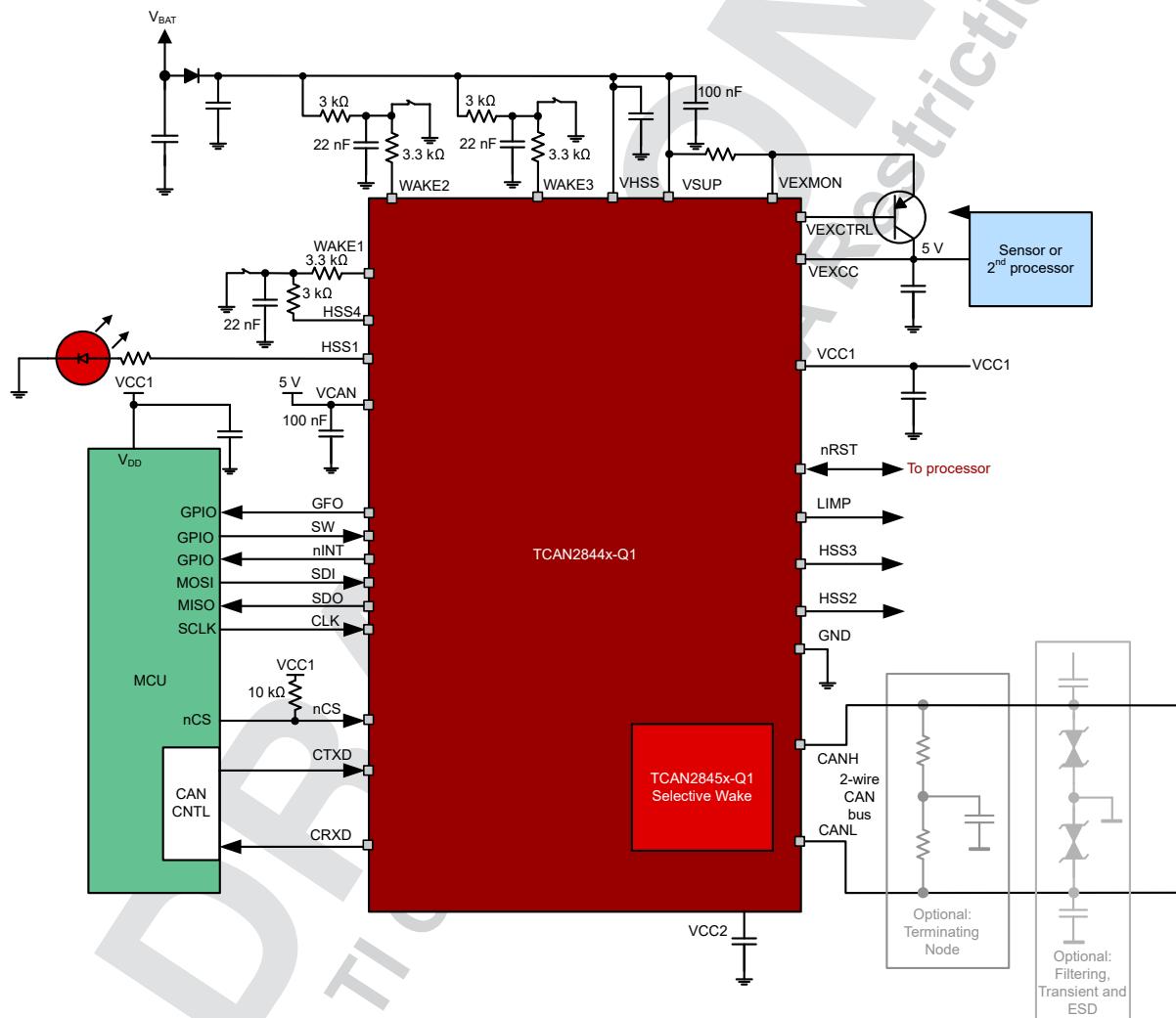


Figure 9-14. Typical CAN Applications for TCAN2844x and TCAN2845x

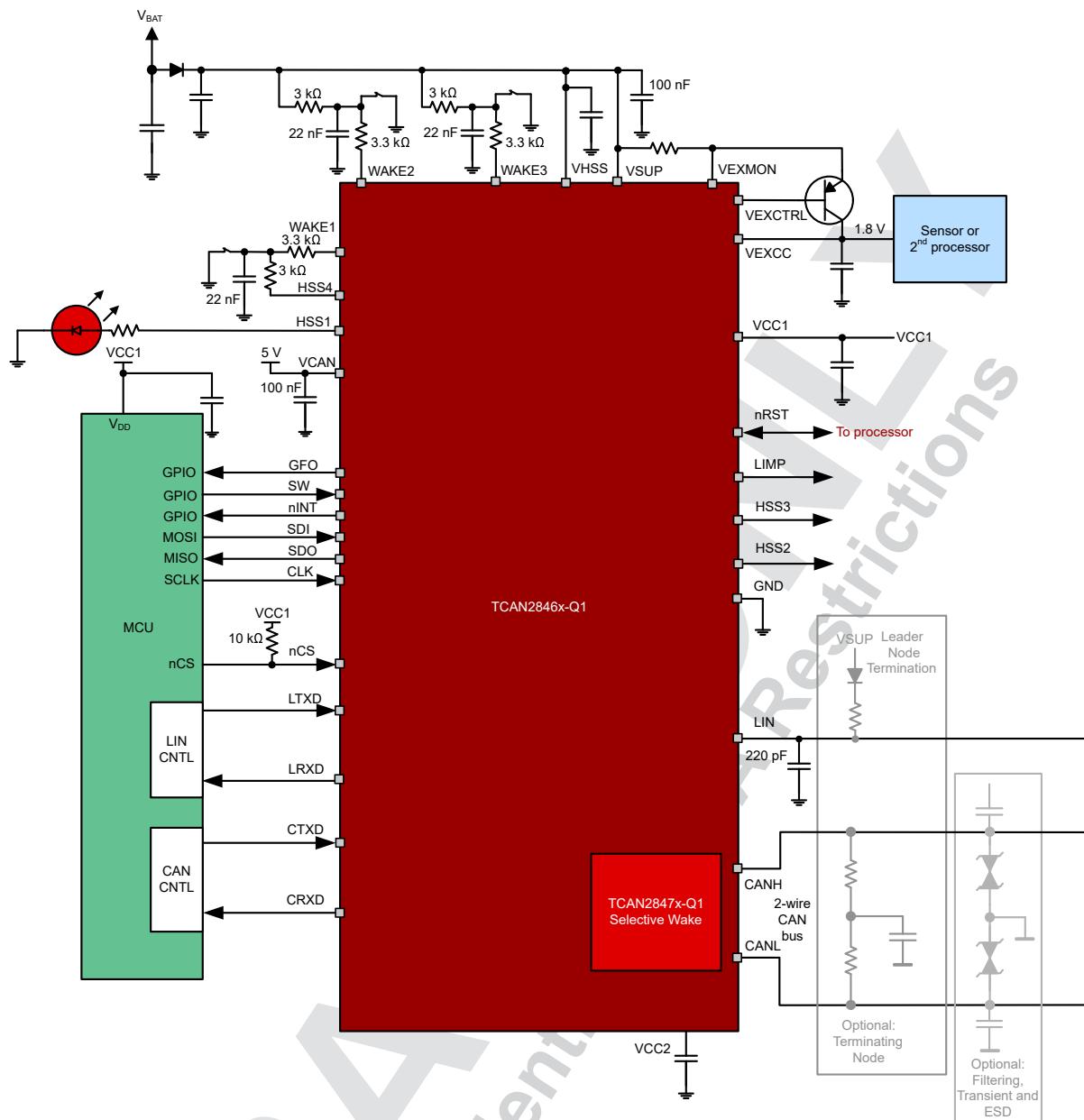


Figure 9-15. Typical CAN and LIN Applications for TCAN2846x or TCAN2847x

ADVANCE INFORMATION

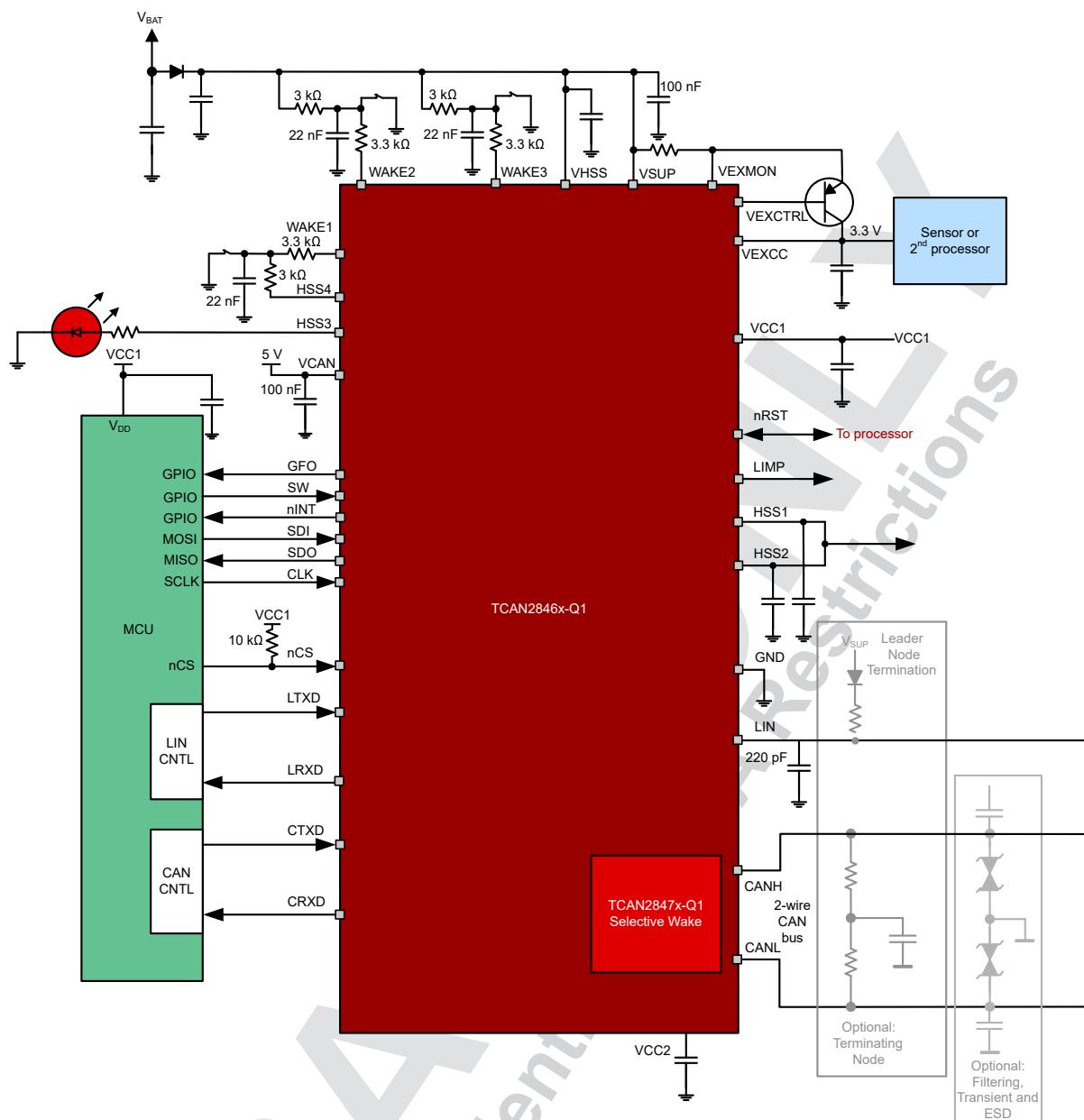


Figure 9-16. Typical CAN and LIN Applications for TCAN2846x or TCAN2847x with Synchronized High Side Switch

- A. Add decoupling capacitors as needed.

9.1.5.1 Design Requirements

The ISO 11898-2_2016 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the TCAN284xx-Q1. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2_2016. They have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. The TCAN284xx-Q1 is specified to meet the 1.5 V requirement with a 50 Ω load, incorporating the worst case including parallel transceivers. The differential input resistance of the TCAN284xx-Q1 is a minimum of 30 kΩ. If 100 the TCAN284xx-Q1 are in parallel on a bus, this is equivalent to a 300 Ω differential load worst case. That transceiver load of 300 Ω in parallel with the 60 Ω gives an equivalent loading of 50 Ω. Therefore, the TCAN284xx-Q1 theoretically supports up to 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO 11898-2_2016 standard of 40 m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate. This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2_2016 CAN standard. In using this flexibility comes the responsibility of good network design and balancing these tradeoffs.

9.1.5.1.1 Normal Mode Application Note

When using the T CAN284x in systems which monitor the CRXD or TRXD pin for a wake-up request, special care should be taken during the mode transitions. The output of the RXD pin is based upon the programmed state of the transceiver and will remain latched low, if wake capable, until the transceiver is placed into a different state.

9.1.5.1.2 Standby Mode Application Note

If the T CAN284x detects an under voltage on VSUP, the CRXD pin transitions low, and signals to the software that the device has transitioned to standby mode. nINT pin will be pulled low to indicate a UVSUP event. The device should be programmed to the expected mode. This includes the transceiver.

9.1.5.1.3 LTXD Dominant State Timeout Application Note

The maximum dominant LTXD time allowed by the TXD dominant state time out limits the minimum possible data rate of the device. The LIN protocol has different constraints for controller and peripheral node applications. Thus, there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

9.1.5.2 Detailed Design Procedures

9.1.5.2.1 CAN Detailed Design Procedure

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with $120\ \Omega$ characteristic impedance (Z_0). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that two terminations always exist on the network. Termination may be a single $120\ \Omega$ resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

9.1.5.2.2 LIN Detailed Design Procedures

Controller node applications require an external $1\ k\Omega$ pull-up resistor and serial diode.

10 Power Supply Recommendations

The TCAN284xx-Q1 is designed to operate off of the battery VSUP and VIO. In order to support a wide range of microprocessors the logic I/O and SPI are powered off of VCC1 which supports levels 3.3 V and 5 V. The CAN FD transceiver 5 V supply is powered from VCAN input. As VCAN is used for the CAN transceiver and needed for EEPROM writes it is recommended that VCC2 not be used to provide the 5 V if VCC2 is providing power off board. A bulk capacitance, typically 10 μ F, should be placed VSUP supply with a 100 nF cap place near the VSUP terminal. A 100 nF capacitor should be placed near the VCAN supply terminal in addition to bulk capacitors near the VCAN source. A bulk capacitance, typically 1 μ F, should be placed near the VCC1 and VCC2 pin. Depending upon an external connect to VCC2 a larger bulk capacitance may be needed.

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Layout

Robust and reliable bus node design often requires the use of external transient protection device in order to protect against EFT and surge transients that may occur in industrial environments. Because ESD and transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design. The family comes with high on-chip IEC ESD protection, but if higher levels of system level immunity are desired external TVS diodes can be used. TVS diodes and bus filtering capacitors should be placed as close to the on-board connectors as possible to prevent noisy transient events from propagating further into the PCB and system.

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Device and Documentation Support

This device will conform to the following CAN standards. The core of what is needed is covered within this system spec, however reference should be made to these standards and any discrepancies pointed out and discussed. This document should provide all the basics of what is needed. However, for a full understanding of CAN including the protocol these additional sources will be very helpful as the scope of CAN protocol in detail is outside the scope of this physical layer (transceiver) specification.

11.1 Documentation Support

11.1.1 CAN Transceiver Physical Layer Standards:

- ISO 11898-2:2016: High speed medium access unit with low power mode (super sets -2 standard electrically in several specs and adds the original wake up capability via the bus in low power mode)
- ISO 8802-3: CSMA/CD – referenced for collision detection from ISO11898-2
- SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
- SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps

11.1.2 LIN Transceiver Physical Layer Standards

- ISO/DIS 17987-1: Road vehicles -- Local Interconnect Network (LIN) -- Part 1: General information and use case definition
- ISO/DIS 17987-4: Road vehicles -- Local Interconnect Network (LIN) -- Part 4: Electrical Physical Layer (EPL) specification 12V
- SAEJ2602-1: LIN Network for Vehicle Applications
- LIN2.0, LIN2.1, LIN2.2 and LIN2.2A specification

11.1.3 EMC Requirements:

- SAEJ2962-2: US3 requirements for CAN Transceivers (-2, -5, GM will propose updates to address -6 + FD, but this is the best place for a working start)
- HW Requirements for CAN, LIN, FR V1.3: German OEM requirements for CAN and LIN
- ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
- ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
- ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
- ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
- IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method
- IEC 61000-4-2
- IEC 61967-4
- CISPR25

11.1.4 Conformance Test Requirements:

- HS_TRX_Test_Spec_V_1_0: GIFT / ICT CAN test requirements for High Speed Physical Layer
- ISO/DIS 17987-7.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
- SAEJ2602-2: LIN Network for Vehicle Applications Conformance Test

11.1.5 Related Documentation

- “A Comprehensible Guide to Controller Area Network”, Wilfried Voss, Copperhill Media Corporation
- “CAN System Engineering: From Theory to Practical Applications”, 2nd Edition, 2013; Dr. Wolfhard Lawrenz, Springer.

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.



ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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