Module 1: Why Use Concurrency?
Topic 1.2: Von Neumann Bottleneck

Speedup Without Parallelism

- Can we achieve speedup without parallelism?
- Design faster processors
  - Get speedup without changing software
- Design processors with more memory
  - Reduces the **von Neumann bottleneck**
  - Cache access time = 1 clock cycle
  - Main memory access time = ~100 clock cycles
  - Increasing on-chip cache improves performance

Moore's Law

- Predicted that transistor density would double every 2 years
- Not a physical law, just an observation
- **Smaller transistors switch faster**
- Exponential increase in density would lead to exponential increase in speed