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Predictions for 1977 and 1985
portray an evolutionary trend to a tenfold improvement
in circuits, simpler operating systems, somewhat more complicated
data management systems, and twenty times today's data traffic.

BEYOND 1984: A TECHNOLOGY FORECAST

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The computer industry's products are clearly in a state of transition, and many users faced with decisions about commitments to today's products need to know whatever they can about possible future successors. In early 1974 Arthur D. Little, Inc. prepared a comprehensive forecast of the nature of future data processing equipment, software, data communications services, and their costs for the Electronic Systems Div. of the U.S. Air Force, for use in a project called SADPR-85, which dealt with base-level data processing operations through 1985. A substantial effort involving 25 investigators, the study produced a report 284 pages long with a bibliography of over 500 titles. The full report is available to qualified defense contractors from the National Technical Information Service, 5285 Port Royal Road, Springfield, Va. It is Appendix VI, in vol. 3, of the six-volume report—"Support of Air Force Automatic Data Processing Requirements Through the 1980's," document number AD-783-768. This article summarizes the contents of that report, adding new material derived from subsequent studies and industry developments.

This article, like the report prepared for the Air Force, focuses on commercially available, general-purpose administrative data processing hardware and software. It covers the full spectrum of sizes and types, but omits specialized tools for scientific, industrial process, or dedicated commercial applications. Its objective is to provide forecasts of processing modules—computer, file and I/O subsystems, etc.—that can be used as building blocks in studying alternative configurations. Each building block requires a specific forecast of functions, power, and costs, but not a detailed discussion of the components within it. Therefore, the discussion of technologies as such is limited to those likely to be available in proven, commercially available modules by 1982. Also, in cases where alternative technologies might be used in a module without materially changing its price/performance, no effort is made to determine which will be the technology of choice. Constant dollars are used; no allowance is made for inflation. Forecasts for each type of module are made for two target years, 1977 and 1985.

formance level will cost about one-tenth the present price, while computers in today's medium-high price range will have speeds approaching 100 MIPS (million instructions per second).

However, an important factor in determining the architecture of tomorrow's processors derives from the desirability of manufacturing circuits in the most standardized form possible. It is and will remain expensive to design an individual integrated circuit, the more so as the scale of integration rises. On the other hand, the manufacturing cost of the individual circuit is extremely low, so it is more economical to effectively waste circuit functions than to design a new circuit. This influence, already visible in the design and functioning of electronic calculators, will be very important in determining the future architecture of computers. To the degree possible, modules at the microprocessor and even higher levels will be used in preference to the design of new specialized circuits.

Architecturally, increasing parallelism in commercial computers is likely to be used to reduce the wait times now encountered in interlinked data transfer and manipulation operations. This parallelism is likely to be realized in the form of specialized processors dedicated to I/O and file management, memory management, interrupt processing, and similar functions. Paralleling of many identical, multifunction processors as in ILLIAC is unlikely in general purpose computers, because the jobs to be done (many of them involving emulation of today's programs) do not conveniently subdivide into array form.

HARDWARE

Computers

Within the next five years, circuits for computer logic and storage will probably exist that have switching speeds on the order of 10^{-8} second, 10 to 50 times faster than today's devices. Beyond that level further improvements will become harder to achieve, though another order of magnitude could be obtained beyond 1985. How-

ever, appearance of improvements in the laboratory precedes their appearance in commercially usable, reliable computers by about five years. This suggests that the improvement in circuit performance per dollar cost will be no more than tenfold (relative to today's circuits) for computers being delivered in 1985. A rather simplistic inference is that circuits of today's per-

Microcoding

These specialized processors are likely to have their functions determined primarily by microcoded stored logic, with wired logic used only where high speed is essential. The use of microcode facilitates standardized manufacturing and maintenance, while permitting the functions of the processors to vary in support of system objectives.

The set of microcodes in the groups of processors forming a "computer" will, in addition to facilitating the basic scheduling and resource allocation functions, support the following system objectives now normally addressed by the operating system:

- Support of several run-time environments, both for the emulation of past programs (and related operating systems) and for the convenience of multiple users simultaneously desiring several modes of operation. Some version of virtual machine concepts will be involved.
- Separation of I/O, communications, and file processing from computational functions.
- Dynamic allocation of processor functions, both to meet varying workloads and to support fail-safe operations (which will, in some form, be all manufacturers' approach to increasing system availability).
- Automatic management of the memory and file device hierarchy at a symbolic level, to facilitate ease of programming, convenience of use, and (through access tables associated with individual run-time environments) security and privacy of data.
- Self measurement, including error logging. This function will support routine maintenance, fail-safe operation, job accounting, and system tuning.

Other functions now associated with operating systems are likely to continue to be performed primarily by software, and are discussed below.

This set of system objectives applies to computers to be available in both 1977 and 1985, and across most of the computer price range. Success and generality in meeting the objectives (and cost/effectiveness in doing so) will be evolutionary, obviously greatest in the larger computers and the later ones.

Processors become components

Computers of both 1977 and 1985 will, then, consist of complexes of component processors automatically sharing microcoded functions under control of the operating system in a manner largely invisible to the user. The throughput of computers will be

determined by that of their component processors. Three levels of component processors are defined here, designated level 1, level 2 and level 3, in order of increasing power. Then, four levels of end-user computers are defined in which they will be used. The four levels of end-user computers are enough to cover the normal price range for commercial data processing, and three levels of component processors appear to provide enough building blocks.

The price/performance forecasts for the component processors are summarized in Table 1, (page 56). The level 1 processor is similar to today's microprocessor, manufactured on one or a few semiconductor chips. Initially simple with a small programmable read-only memory (PROM) and minimal complexity, it will evolve in the direction of higher complexity and speed. Its speed in 1985 is forecast to be the same as that of the level 2 processor, reflecting the expectation that by then there will be no cost benefit in manufacturing circuits with cycle times any slower than 250 nanoseconds. The level 2 processor will evolve similarly, but will in both 1977 and 1985 be considerably more complex: it will be required to perform the functions currently associated with an I/O channel controller, or with the CPU of a small computer system.

The level 3 processors will correspond to the central computers in today's medium to high priced computer systems, but will have raw speed equivalent to that of today's largest computers. They will be used singly in batch-oriented monoprocessor computers as they are today, and in multiples under multiprocessor operating systems in large-scale systems with high power and automatic fail-safety. The cost (to the vendor) of level 3 processors is not expected to drop as much between 1977 and 1985 as the costs of smaller processors, because the complexity increase required to support the evolving microcode software is expected to be greater (as shown by the quadrupling of PROM size). Pipelined instruction interpretation and execution, probably used to achieve speeds approaching the microcode equivalent of 100 MIPS, will also serve to keep complexity high.

Larger, more powerful component processors than level 3 will be possible in both 1977 and 1985 and will probably be built for large scientific systems, but they will not be needed for even the largest commercial systems (partly because at least two CPU's will be needed in such systems to permit fail-safe operations).

These component processors will be

combined to form the "computers," or "processor systems," offered by the manufacturers. They will also be used in I/O subsystems (e.g., intelligent terminals and remote batch terminals) and in file storage subsystems; these are discussed below.

The expected characteristics of the four levels of computers are summarized in Table 2, (page 56). Conventional terminology is used to identify them, mostly because terms such as "minicomputer" are traditionally associated with a price range that will still exist (though the power provided in each price class will change). Each computer is described as a module incorporating an average amount of main memory and of backing storage for program residence and working space. All file storage is additional; file modules are described below.

Multiprocessing

The microcomputer, including one level 1 component processor, will typically be used in intelligent terminals or satellites. By 1985, however, the power of the processor and the low cost of relatively large memory will enable the microcomputer to support small stand-alone systems of considerable versatility. The costs of such systems will be dominated by their peripheral equipment costs (see below).

The minicomputer will in both 1977 and 1985 be able to support a fully capable data processing system. The CPU will be a single level 2 processor, and from three to (in 1985) as many as 20 level 1 processors will be associated with peripheral equipment. Ease of use in interactive applications will be the primary design objective of these machines. This accounts for the very large average storage size of the 1985 machine and resulting slow decline in price. One batch stream is assumed in the background, though the 1985 machine could easily run more batch streams at the expense of some interactive capability (particularly since virtual memory management will be generally used).

The mono-computer is designed primarily for users whose intent is to perform fairly large amounts of batch processing, though some interactive capability will be present. In the 1977 system a single level 3 CPU will be employed and two or three level 2 processors for high-volume peripheral device control; level 1 processors will be used as needed for individual or low-volume peripherals. Because no multiprocessing will be present, and because (for efficiency) fixed partitioning of memory into batch and interactive virtual environments will be used, the

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functional system objectives listed above will be only partly met. In the 1985 system, however, the low costs of component processors will permit a second level 3 processor to be included and several more level 2 processors. These, together with larger memories, will permit the mono-computer to meet almost all the system objectives (except, perhaps, multiple run-time environments) even though its price will decline.

The multi-computer will incorporate at least two level 3 processors in 1977 and three, four or more in 1985. Four to six level 2 processors will be in the 1977 system and perhaps twice as many in the 1985 system, together with multitudes of level 1 processors.

The multi-computer's price difference from the mono-computer is due not so much to having more processors as to the much larger storage of the multi-computer, particularly the large backing store (which may use magnetic bubble or charge-coupled device technology as early as 1977. See discussion of auxiliary storage). This very large storage is needed to provide numerous run-time environments (one or more emulating past generations, several running batch streams, several varieties of interactive environments, etc.). Also, the multi-computer will be designed to completely intermix a wide variety of file-based interactive, batch, and system development applications. The multi-computer will in fact be a network of computers providing a number of processing environments simultaneously. The common elements will be two: the central data base around which the processing is dis-

tributed, and a central system executive that controls the functions of each component computer and provides overall monitoring. It is these two common elements which prevent the multi-computer from being broken up into a "federated network" of physically dispersed minicomputers. Perhaps in the farther future ways will be found to provide these common system elements in a dispersed network, but this seems unlikely in products being delivered by 1982.

Comparing the estimated purchase costs of the different classes shown in Table 2, it appears that wide gaps will develop in the price spectrum. This is partly an illusion caused by this article's objective of providing standard cost forecasts for typical modules; as now, variations in configuration will cause wider variations in price than those shown here. Nevertheless, between the mono-computer and multi-computer, a genuine price gap seems likely; the implication is that there will be no high-priced batch processing computers (except perhaps specialized scientific ones), and that there will be a minimum cost of entry to the high volume, interactive, data base oriented environment.

Auxiliary Storage

A great deal of research is being performed into novel auxiliary storage technologies including magnetic bubbles, charge-coupled devices, laser-holographic devices, cryogenic devices, and others. This will gradually result in the introduction of new types of auxiliary storage subsystems. However, much improvement potential still exists

in conventional magnetic technology. Most of the improvement will be in the form of increased area density of recording: more tracks per inch laterally across a magnetic disc face, and more bits per inch longitudinally. An area density improvement factor of at least 40 appears theoretically possible. This will result in a much lower cost per bit for magnetic discs, lower through at least 1983 than newer technologies can match. However, access time to magnetic discs will remain a problem even if head-per-track arrangements become general. For this reason it seems likely that hierarchies of auxiliary storage devices will continue to be used through 1985, with the newer technologies appearing first at the high speed, low capacity end of the spectrum, and then gradually superseding slower technologies as their costs per bit drop. Either magnetic bubble or charge coupled device technology (or both) will be in widespread use by 1983, and are likely to appear in some product lines by 1977.

Table 3 summarizes the situation: four levels of auxiliary storage (in addition to the computer's main memory) are likely to remain in use in 1977 and beyond; only in the 1980s does the improvement potential of the new high speed technologies indicate that the number of levels of storage may be reduced. The multilevel hierarchy will be of less concern to the user than it is now, however, because virtual memory management techniques will be used to move data sets up and down the hierarchy depending on usage. The recent announcement of IBM's 3850 system exemplifies the trend in this direction.

	Level 1		Level 2		Level 3	
	1977	1985	1977	1985	1977	1985
Cycle time	2 usec	250 nsec	500 nsec	250 nsec	500 nsec	100 nsec
Bandwidth	4 bits	8-16 bits	16 bits	16-32 bits	32 bits	64 bits
Interrupt levels	0	1 level	1 level	2 level	2 level	4 level
PROM size	500 bytes	1,000 bytes	4,000 bytes	8,000 bytes	8,000 bytes	64,000 bytes
Cost to system vendor	\$100	\$50	\$4,000	\$2,000	\$50,000	\$30,000

Table 1. Future component processors.

	FUTURE COMPUTER CLASSES							
	Microcomputer		Minicomputer		Mono-computer		Multi-computer	
	1977	1985	1977	1985	1977	1985**	1977	1985
Typical use								
On-line (users)	1 or 1	5-10 or 1	6-10 and 1	10-20 and 1	10-20 and 4-6	20-40 and 6-8	complete intermixing, job determines limit	
Main memory (bytes)	4-8KB	32-64KB	32-64KB	0.2-0.5MB	0.5-2MB	2-4MB	2-16MB	8-64MB
Backing store* (bytes)	300KB	500KB	500KB	4MB	10MB	30MB	50-200MB	100-500MB
Operating system	minimal	minimal	real, fixed partitions \$10-20K	virtual	partitioned virtual	virtual	multiple virtual memory or machine	
User cost	\$1-2K	\$0.3-0.7K		\$7-10K	\$150-250K	\$75-100K	\$1.5-2.5M	\$1-2M

*Auxiliary storage for system programs, current application programs and data.

**This system will probably have multiple main processors by 1985.

Table 2. Future computer classes.

Auxiliary storage module performance and cost forecasts have been developed for 1977 and 1983, and compared with 1974 levels. These forecasts are summarized in Table 4. The modules were configured on the basis of the typical size and access time requirements assumed for the four classes of computers (multiple modules could, of course, be used to obtain higher capacity). Controllers are included in the cost of each module, ranging from a controller requiring a single level 1 component processor at the low end to a controller with dual level 2 processors at the high end.

In addition to the auxiliary storage modules for conventional random file access, forecasts are also summarized in Table 4 for very large, slow access archival storage systems that could be added to multi-computer configurations. These require advanced technology to obtain the very high capacities required; early models are available now and they are expected to see general use in the late 1970s. These modules are shown as if they are independent, for clarity and ease of reference. Their actual use in systems of both 1977 and 1985 will be in hierarchical arrangements, with data movements at least partially transparent to the user.

Forecasts for magnetic tape auxiliary storage modules are summarized in Table 5, (page 61). (The controller in each module is assumed capable of handling simultaneous data transfer to all drives). An eventual doubling of packing density (and therefore of data rate) and some reductions in cost are forecast, but the relatively mature electromechanical technology involved

seems to preclude major improvement.

Batch I/O Equipment

The spectrum of I/O device types, speeds, and functions is so broad that for purposes of the Air Force report individual devices were combined into clusters or "stations," each station forming a cost/performance module that could be used in configuring overall networks with approximate accuracy even though the exact number of readers, printers, etc., would probably be somewhat inaccurate. The same procedure is followed in this article. Forecasts were developed for two types of basic batch I/O stations in which a line printer is combined respectively with punched card and magnetic I/O equipment; then two optional, addi-

tional batch options were forecast: optical readers and computer output microfilm stations.

Punch card/line printer

The first of the batch I/O stations includes one card reader, one punch, and one line printer. Forecasts were developed for low, medium, and high speed versions of this station, and for 1977 and 1985. These are summarized in Table 6, (page 61).

During the last 10 years there has been little change in the price/performance of the card readers and punches offered for use with the larger computer systems. The only major innovation has been the 96-column card introduced by IBM; this did not cause a great deal of change in demand, and the price/performance of units de-

AUXILIARY STORAGE TECHNOLOGY PERFORMANCE CHARACTERISTICS

	Storage capacity (bits/unit)	Access time (sec)	Cost/bit (cents)
A. 1974 Technologies			
High speed/Low capacity (large core, hpt disc, drums)	$10^7\text{-}10^8$	$10^{-5}\text{-}10^{-8}$	0.1-2.0
Moderate speed/Moderate capacity (moving-head discs)	$10^8\text{-}10^9$	$10^{-1}\text{-}10^{-2}$	$10^{-3}\text{-}10^{-2}$
Low speed/High capacity (ultra-large storage devices)	$10^{11}\text{-}10^{12}$	1.0-10	$10^{-6}\text{-}10^{-4}$
Archival storage (magnetic tapes)	Unlimited ($10^8/\text{tape}$)	10-100	$10^{-6}\text{-}10^{-5}$
B. 1977 Technologies			
High speed/Low capacity (hpt discs, early bubbles or CCD)	$10^8\text{-}10^9$	$10^{-4}\text{-}10^{-3}$	0.1-1.0
Moderate speed/Moderate capacity (moving-head discs)	$10^9\text{-}10^{10}$	$10^{-3}\text{-}10^{-2}$	$10^{-4}\text{-}10^{-3}$
Low speed/High capacity (ultra-large storage devices)	$10^{11}\text{-}10^{13}$	1.0-10	$10^{-6}\text{-}10^{-4}$
Archival storage (magnetic tapes)	Unlimited ($10^8/\text{tape}$)	10-100	$10^{-7}\text{-}10^{-6}$
C. 1983 Technologies			
High speed/Moderate capacity (CCD, magnetic bubbles)	$10^8\text{-}10^9$	$10^{-7}\text{-}10^{-6}$	0.01-0.1
Moderate speed/Very high capacity (discs, holographic, cryogenic)	$10^9\text{-}10^{14}$	$10^{-8}\text{-}10^{-1}$	10^{-6}

Table 3. Auxiliary storage technology performance characteristics.

AUXILIARY STORAGE MODULE COST/PERFORMANCE FORECASTS

	1974	1977	1983
Microprocessor auxiliary storage			
Capacity	1 million bytes	5 million bytes	5 million bytes
Medium	small fixed disc	small fixed disc	semiconductor, CCD
Access time	10 msec	10 msec	10 usec
Cost	\$5,000	\$2,500-3,500	\$1,500-2,500
Minicomputer auxiliary storage			
Capacity	20 million bytes	50 million bytes	50 million bytes
Medium	small removable disc	small removable disc	bubble memory
Access time	100 msec	30 msec	100 usec
Cost	\$35,000	\$15-20,000	\$15-25,000
Product example	IBM S3/10 disc (5445)		
Monoprocessor auxiliary storage			
Capacity	200 million bytes	200 million bytes	500 million bytes
Medium	head/disc cartridge	head/disc cartridge	head/disc cartridge
Access time	25 msec	25 msec	20 msec
Cost	\$60,000	\$35-45,000	\$25-35,000
Product example	IBM 3340	IBM 3340	
Multiprocessor auxiliary storage			
Capacity	1 billion bytes	2 billion bytes	2 billion bytes
Medium	multiple disc unit	multiple disc unit	multiple discs
Access time	30 msec	25 msec	20 msec
Cost	\$260,000	\$180-220,000	\$90-130,000
Product example	IBM 3330		
Archival storage option			
Capacity	200 billion bytes	1 trillion bytes	10 trillion bytes
Medium	tape cartridge	laser, video recording	holographic systems
Access time	10 sec	10 sec	1 sec
Cost	\$1,000,000	\$400-600,000	\$700-1,200,000
Product example	IBM 3850		

Table 4. Auxiliary storage module cost/performance forecasts.

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signed to handle the 96-column card is comparable to that of conventional units. A check of devices offered by 15 vendors showed that maximum speed of punched card readers now available is 1,200 cpm, and the maximum punch speed is 300 cpm. These speeds were first achieved more than 10 years ago. Further speed increases obviously pose mechanical problems, but if there had been substantial market demand for units of higher speeds, it would have been technically possible to develop them. We infer that these speeds are regarded by the market as adequate for high-performance units. Prices of high-performance units have also changed little.

The growth of the minicomputer has brought with it a set of slower card readers and punches at lower prices designed to match the throughput capabilities and prices of the minicomputers. Readers capable of handling 400 cards per minute typically have a purchase price of about \$1,200, and punches capable of handling 100 cards per minute typically cost about \$9,000.

Price/performance evolution of these devices will be constrained by the fact that they are predominantly electromechanical and reflect a mature technology. We may expect manufacturers to substitute electronics for mechanical components wherever they can, and there is some possibility of using different technologies (such as

fluidics) for the direct control of mechanical modules. It is also likely that the manufacturers, faced with the inherent high failure rates of these devices, will continue to work to improve their reliability. However, their willingness to invest in either new technology or more reliable designs will be moderated by the fact that the total demand for card readers and punches will probably decrease; the popularity of data collection with other media should diminish the overall use of card readers and punches. We therefore forecast relatively little change in price/performance over the entire period 1977-1985.

Printers are similarly constrained by the limits of electromechanical technology, but nonimpact techniques (thermal, electrostatic, electrographic, inkjet and Xerographic) have led to a greater rate of change. In the time period of this article, the development of nonimpact devices may lead to improvements of 15%-30% in overall printer price/performance with greater improvements at speeds of 3,000 lpm and up. This improvement factor appears in Table 6 as an increase in speed for the medium and high speed printers without any decrease in cost; for the low speed printer, both speed and cost are forecast to improve.

The forecast for the second type of batch I/O station simply substitutes magnetic tape drives for the card

reader and punch, arriving at only slightly different cost forecasts.

OCR station

System designers are rapidly developing more sophisticated circuit designs that, combined with LSI technology, are producing character recognition logic components of much lower cost and smaller size. Electro-optics developments are also contributing very small, light, inexpensive scanning arrays for low-cost units, and also very fast, more accurate scanning elements (using such technologies as laser beam control) for the larger, more complex systems. The most difficult design barrier to dealing with the less constrained patterns of handprinting and script is still the development of a true "gestalt" pattern recognition methodology (probably of a software nature) with powerful heuristic capabilities. Little progress in this area is foreseen.

A combination of continued rapid development of newer electro-optic materials and improvements in the power, speed, and cost of integrated circuits will lead to an increase in the price/performance of all types of OCR's by an overall factor of at least 2 and, in some cases, as much as 4 by 1985. These assumptions are expressed in tabular form in Table 7. The most significant product development will be that of a family of multiple-font, medium-speed document readers in the

MAGNETIC TAPE COST/PERFORMANCE FORECASTS

Low performance (single drive with controller)		40,000 bytes/sec \$10,000 IBM 3411-2	40,000 bytes/sec \$7,500-8,500	40,000 bytes/sec \$6,500-7,500
Medium performance (three drives with controller)		600,000 bytes/sec \$75,000 IBM 3420-5	1.2 million bytes/sec \$45-60,000	1.2 million bytes/sec \$25-40,000
High performance (six drives with controller)		7.5 million bytes/sec \$220,000 IBM 3420-8	7.5 million bytes/sec \$140-180,000	15 million bytes/sec \$80-120,000

Table 5. Magnetic tape cost/performance forecasts.

COST/PERFORMANCE FORECASTS FOR BATCH STATION (PUNCH CARD/LINE PRINTER)

Low speed Performance	300 cpm read, 60 cpm punch, 100 lpm print (\$15,000-20,000)	400 cpm read, 100 cpm punch, 200 lpm print (\$12,000-16,000)	400 cpm read, 100 cpm punch, 300 lpm print (\$12,000-15,000)
Station Cost	900 cpm read, 200 cpm punch, 600 lpm print (\$32,000-37,000)	1,000 cpm read, 200 cpm punch, 800 lpm print (\$32,000-37,000)	1,000 cpm read, 200 cpm punch, 900 lpm print (\$32,000-37,000)
Medium speed Performance	1,200 cpm read, 300 cpm punch, 1,100 lpm print \$65,000-75,000	1,200 cpm read, 300 cpm punch, 1,300 lpm print \$65,000-75,000	1,200 cpm read, 300 cpm punch, 1,300 lpm print \$65,000-75,000
Station Cost			

Table 6. Cost/performance forecasts for batch station (punch card/line printer).

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\$50,000-75,000 price range with flexible software by 1985. In high-speed modules there should also be substantial improvement by 1985 in the reliability of recognition of more unconstrained, hand printed numeric information and some alphabetic forms.

The emergence of effective low-speed (and low-cost) OCR stations in the 1977-85 period should also enhance the development of sophisticated, modular, multi-media data entry systems combining low-speed, batch processing, character recognition stations with keyboard data entry and editing terminals, a local processor, and auxiliary memory.

A computer output microfilm station was assumed to include an off-line COM printer, a developer, a duplicator, and binding equipment. Significant price declines are believed likely because of reduction in LSI and electro-optical costs, and because of economies of scale as manufacturing vol-

cast, however.

Again, to simplify configuration details the forecast was developed on the basis of "stations" in which each basic terminal would have sufficient electronics to interface directly with a line connected to the host computer, whether the host be remote or a local satellite. The purpose of this assumption was to eliminate the need to allow for shared controllers and modems; this trend to integral electronics is visible in recent products. "Intelligent" terminals were assumed to contain a level 1 component processor and auxiliary memory in addition.

As Table 9 shows, three kinds of transaction terminal stations are considered. The two "standard" stations are the familiar combinations of keyboard with low speed, serial printer and of keyboard with "soft" display. Forecasts of the costs of these are shown for 1977 and for 1985, and for two versions: "basic," with only mini-

mal interface electronics, and "intelligent," incorporating a degree of independent processing capability. Two "optional" stations are also shown; these are in the form of optional additions to standard stations. (An intelligent hard-copy printer is considered nonexistent within these definitions since it would be associated with an intelligent standard station. Basic OCR units are also considered nonexistent since all OCR devices require at least the intelligence associated with a level 1 processor.) Finally, three kinds of "special stations" are shown: a small badge reader for credit checking, identification, and similar applications (no intelligent version needed), and voice input and response subsystems (both of which require intelligence).

Keyboard and low-speed serial printer mechanisms are not expected to change much in price. While thermal printers will largely replace mechanical ones and bring a substan-

COST/PERFORMANCE FORECASTS FOR OCR STATION

Low speed Performance Station Cost	50-100 lpm*	50-100 lpm \$25,000-50,000	50-100 lpm \$20,000-30,000
Medium speed Performance Station Cost	100-500 lpm \$75,000-100,000	100-500 lpm \$60,000-80,000	100-500 lpm \$50,000-75,000
High speed Performance Station Cost	500-1,200 lpm \$100,000-500,000	500-1,200 lpm \$100,000-250,000	500-1,200 lpm \$75,000-125,000

*average line length of 50 characters

Table 7. Cost/performance forecasts for OCR station.

COST/PERFORMANCE FORECASTS FOR COM STATION

Medium speed Performance: Station Cost	5,000-10,000 lpm \$50,000-\$75,000	5,000-10,000 lpm \$40,000-\$60,000	7,000-10,000 lpm \$25,000-\$50,000
High speed Performance: Station Cost	10,000-25,000 lpm \$75,000-\$125,000	12,000-25,000 lpm \$60,000-\$70,000	20,000-30,000 lpm \$50,000-\$65,000

*COM printer speed only, not system throughput

Table 8. Cost/performance forecasts for COM station.

umes rise. These are expected to be moderated by the highly electro-mechanical nature of the system, with the results summarized in Table 8. No low-speed units are shown, because developments in display devices are believed likely to satisfy any demand that may exist.

Terminals

Remote batch terminals require no separate forecast; a combination of the appropriate speed level of batch I/O station and a component processor (probably level 2) results in a price/performance forecast which should be grossly accurate. Interactive or "transaction" terminals were separately fore-

COST FORECASTS FOR TRANSACTION TERMINAL STATIONS

Standard stations	1977: \$ 700- 2,500	1985: \$ 2,000- 2,500	\$ 4,000- 9,000
Optional stations	1977: \$ 2,000- 5,000	1985: \$ 1,000- 4,000	nonexistent
Special stations	1977: \$ 500- 600	1985: \$ 300- 600	nonexistent
No. 1 keyboard/teleprinter	1977: \$ 700- 2,500	1985: \$ 2,000- 2,500	\$ 4,000- 9,000
No. 2 keyboard/display	1977: \$ 900- 3,000	1985: \$ 700- 1,500	\$ 2,000- 8,000
No. 3 hardcopy printer	1977: \$ 500- 1,000	1985: \$ 500- 1,000	\$ 2,000- 2,500
No. 4 low-cost OCR unit	1977: \$ 500- 1,000	1985: \$ 500- 750	\$ 2,000- 2,500
No. 5 minimal badge reader	1977: \$ 500- 600	1985: \$ 300- 600	\$ 2,000- 2,500
No. 6 voice input	1977: \$ 8,000- 12,000	1985: \$ 7,000- 10,000	\$ 2,000- 2,500
No. 7 voice response**	1977: \$ 50,000- 150,000	1985: \$ 25,000- 100,000	\$ 2,000- 2,500

*Including small processor and auxiliary memory

**A special case combining telephone receivers as remote I/O stations plus a specialized unit associated with the central system.

Table 9. Cost forecasts for transaction terminal stations.

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tial speed improvement, they will not cost much less. A somewhat greater cost reduction is forecast for "soft" displays, primarily because of the larger amount of circuitry associated with the displays which will drop in cost very sharply. For large displays (over 1,000 characters), the crt will remain the dominant technology in 1977 and perhaps in 1985. Planar gaseous displays and/or light-emitting diodes will become steadily more competitive, however, dominating the smaller displays (under 500 characters) and eventually challenging the crt.

The intelligent versions of the standard stations incorporate a level 1 component processor of very low cost. They also require a substantial memory, however, as well as interface electronics, power supply, etc., which add considerably more cost. Between 1977 and 1985 decreasing electronics cost and increased manufacturing volumes should bring these costs down sharply.

Nonimpact printing technology will have a major effect on the hard-copy printer option (number 3), not so much in price as in speed. A typical speed range of 120-200 cps is forecast for such printers in 1977, rising to 200-1,000 cps in 1985.

The low-speed ocr device (number 4) is assumed to be hand fed, often using a hand-held "wand" rather than an automatic scanner. The cost of a paper feed mechanism is thereby avoided, so the cost of the device is largely determined by its case, power supply, and the very low cost of its electronics. Similar logic applies to the badge reader (number 5); marketing, packaging, and similar costs become dominant as electronics cost becomes insignificant.

The voice input device (number 6) is novel; only a few exist today in limited applications. Limitations on the recognition capability of the devices are expected to remain severe, but gradual improvement should permit the devices to see more use in controlled applications. Costs are not expected to decline much between 1977 and 1985, because complexity is expected to increase as recognition limitations are reduced. The voice response device (number 7) which might complement a voice input device is a central subsystem rather than a terminal; the need to handle multiple lines at high speed will keep its costs relatively high. In this area, too, there will be a tendency to trade off lower electronics cost for greater flexibility.

The purpose of this article is to forecast the capability of future software as perceived by the user, and as it

SOFTWARE

affects his system development and operating resource needs. Coverage of such matters as scheduling algorithms of operating systems, evolution of specific language features, and data base structure is therefore relatively light.

Operating Systems

As was indicated in the discussion of computers, many of the functions now performed by operating system software are likely by 1985 to be performed by computer microcode. The major functions that remain, such as job scheduling, non-shareable device allocation, error monitoring, and recovery, will be performed by relatively simple monitors dedicated to specific modes of operation (e.g., batch, time-sharing) operating in some form of virtual machine environment. Evolution to this functional pattern will be slow and will still be in its early stages in 1977, but the trend is already visible.

Operating systems today also perform a set of functions designed to help the user manage the flow of work fed to the computer, its effective overall utilization, and the events surrounding it. These system management software functions are expected to increase steadily in importance and sophistication, but are also expected to become more clearly separated from the operating system proper. They are therefore considered separately in the article.

System Management Software

By 1985, computer systems should automatically log and report the data needed to control related external activities including tape and disc library control, external job scheduling, and user accounting and billing. Logging will also be automatic for references to protected files: the file management system will control access codes symbolically, and the logging system (inaccessible to any user) will record all references. This capability, a subset of the automatic recovery logging process, should provide adequate file access control for many users.

System performance measurement facilities will be needed in addition to basic logging facilities, so that users can observe the performance of programs, the balancing of system resources, and the like. These measurement facilities will probably interface with the diagnostic and error-detection software. System manufacturers and specialized software firms have already developed very competent per-

formance measurement software; little further evolution is needed for adequacy of measurement at an overall level. System simulation software, to help users predict the behavior of changed systems and configurations, will be based on the results of the measurement software and is similarly well advanced.

Data Management

The structure of data base management systems will evolve toward that shown in Fig. 1 (page 67). The major elements of such systems will be a unified data management supervisor (roughly corresponding to current host language processors), an inquiry/report module which will become a front end to the DMS, a data definition processor, a reorganization/backup module, and a performance statistics analyzer. The evolution and function of each of these modules is described below.

The data management supervisor (DMS) is the heart of the data management system. Its main function is to manage inputs to and outputs from the data base that originate from on-line or batch application programs or from the inquiry report module. To do this, it makes use of the separately stored data base definition, which is output from the data definition processor. The DMS may call upon standard I/O service programs or special ones built to support itself. One of the reasons for this will be the trend toward modularity in system level software; this will enable users to select certain options which the DMS provides and to omit other options, thereby reducing overhead for features which are not desired.

Specific functions which will be provided by the data management supervisor are as follows:

- *Access Control.* One function of the DMS will be to control access from programs to the data base. Users accessing the system via the inquiry/report module or interfacing directly from application programs will have to supply passwords or equivalent identification means. The DMS will ascertain whether a particular user or class of users is entitled to access the data base in a variety of ways. This includes read-only and read-and-write capabilities.

- *Record Performance Statistics.* Another function of the DMS will be to record access and usage statistics in a variety of ways. These statistics will be utilized for several purposes: (1) they will enable the data base administrator to determine who is accessing the data base and how; (2) they will enable him to tune or reconfigure the data base

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structure for optimal performance by the application programs; and (3) they will help him to reorganize the data base at appropriate points for performance or backup purposes.

- **Handle Concurrent Updates.** Partially through improved software, but possibly including additional hardware facilities such as test and set instructions, the ability to handle and resolve conflicts in multiple concurrent update situations will be greatly enhanced. Lockout mechanisms at the individual record level will be provided. Deadlock resolution capabilities will be provided which will enable the system to hold one particular requestor in a suspended state and allow another transaction to be processed to completion before the first transaction gains control of any record. Improved performance in handling multiple requests of all types will be provided through reentrant coding of the DMS.

- **Backup/Recovery.** The DMS will record on an independent device all activities which have affected the data base. This will entail the writing on a data base journal log file of before-and-after images of data base records, which are time stamped and linked to the source that caused the change. Using this file, the DMS will be able to restore the data base to its condition prior to a failure, either by applying after-images to a backup copy, or by applying before-images to the present copy if the failure was not physical in nature.

- **Integrity Checking.** Future data management supervisors will pay increased attention to insuring the integrity of the data base. This will include the ability to code into the data base definition certain relationships and consistency checks which must exist between individual records or fields. Each time a record or field is altered, these consistency checks will be invoked and the transaction rejected if the prescribed conditions are not met.

The functions of the inquiry/report module will evolve into a front-end general purpose routine for the unified data management supervisor. From the user's point of view, it will provide many of the same features that current inquiry/report systems provide, such as the ability to specify a variety of searching criteria, to locate records which satisfy these criteria, to perform elementary calculations on appropriate data, and to format specialized or one time output reports from the data base. In addition, provided authorized access permission has been obtained, the user will be able to write simple programs that, in effect, update the data base. These can be used for data entry operations or can be utilized to process simple transactions.

As greater numbers of systems are built with a data base system in mind, normal output report requirements will be met through the inquiry report module. This will permit easy modification of report formats and contents

as desired by user departments. The reporting function will be carried out by application programs only in the case where reports are a direct by-product of application program update functions, or where complex computations or high volumes are involved that require high efficiency.

The data definition processor is utilized to define the structure of the data base and other characteristics such as access limitations. Two evolutions can be seen in data definitions for future data management systems. These are:

- A greater degree of data independence. Data independence refers to the separation of the data definition and processing from the application program. This is provided by the independently stored data base definition, which is output from the data definition and processing application program. The individual programmer will need to know less about the structure of the data base, and additional degrees of freedom in reorganizing or altering the data base structure will be possible without affecting the operation of individual programs. Specifically, it will provide for independence from physical media, the ability to add new record types to the data base, the ability to add new fields to existing records, and the ability to alter relationships among elements and records.

- Additional flexibility in data structuring and access methods. Currently, most data management systems impose a primary data structuring scheme, usually a variant of an inverted index or chained organization. Future systems will allow the user more flexibility in selecting data structures and access methods, and will make it easier to accommodate different and more complex data structures. This will be done in such a way as to optimize the data structure for the given application and thereby improve the performance of the system.

The functions of the reorganization and backup module include selectively copying the data base and reorganizing it for improved efficiency. These functions are included in the same module because they can be done concurrently. Backup copies of the data base need to be kept on a volume basis so that recovery from an individual volume failure is possible.

The performance statistics analyzer module is responsible for analyzing the statistics which are output by the DMS and reporting them to the data base administrator. This is one way that the administrator will monitor the activity against the data base. He may either choose to reorganize the data base or restructure it on the basis of the ana-

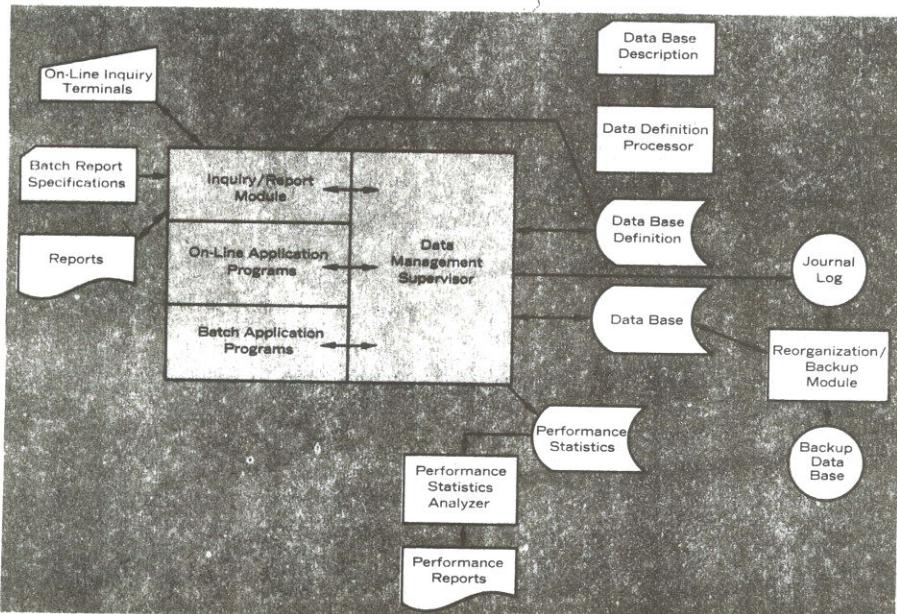


Fig. 1. Data base management systems will evolve toward the structure shown here, with the unified data management supervisor as the heart of the system. The inquiry/report module acts as a front-end to the supervisor, while the reorganization/backup module helps to constantly improve efficiency. A greater degree of independence between the data definitions and the applications programs can be expected, as well as more flexible data structures.

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lyzer output.

Languages

Job control or command languages will become simpler, partly because the greater degree of automation within computer systems will mean that the user is required to provide less detailed instructions, and partly because of specific efforts to make them so. Simplifications will include higher level symbols closer to natural language and interactive command language facilities to help users specify their wants. In the inquiry/report module of the data management system, command language and programming language will have combined, in a sense; the user will not be conscious of providing one or the other but addresses the machines in a combination of both. Command languages with these features have already appeared in some systems; they can be expected to become general early in the forecast period.

The functional capabilities of API, PL/I, COBOL, and FORTRAN will not have changed dramatically by the early 1980s. Dialects for these languages will have been developed to accommodate structured programming techniques and to help with testing and event synchronization problems. They will also have better capabilities for dealing with data bases.

For the smaller machines, cross-compilers will be available, and subset dialects of the full-scale languages will be used for these machines. For the medium- and large-scale monoprocessor or multiprocessor machines, compiling will be done on the target machine, and complete sets of the languages will be available. Special versions of these common languages will be utilized on machines which have special architectures, such as array processors.

The development of very high level languages (problem-oriented languages) will continue, perhaps to the point where users can more easily develop standard applications such as payroll, accounts receivable, billing, materials control, accounts payable, and similar systems. These will be implemented most widely on minicomputer-class systems so that the user can be his own programmer; several software offerings approaching this ideal have already appeared. Problem-oriented languages will not, however, become the standard way of developing an application system. Most systems that require heavy production use will probably be developed using procedure-oriented languages. An "end-user language" may become available

for the nonprogrammer, evolved from COBOL, BASIC and inquiry languages.

Program Development Aids

While programming languages are not expected to change much, facilities for supporting programmers will evolve considerably. Concepts of structured programming will have evolved enough by the early 1980s to be incorporated in interactive syntax and logic checking software that automatically accumulates code into modules for subsequent batch linking and initiation; a combination of interactive and batch debugging processes will be used. Listings prepared as a result will probably be useful as part of the documentation for programs. System testing, where numerous programs are involved, will be facilitated by automatic generation of test data (a by-product of the data base management system), and by automatic linking and generation of tables including data names, and symbolic identifications of system resources used, and the like. These, too, will be available to form part of program documentation; these program development aids will make the programming process partly self-documenting. These programming aids should have a substantial effect on programmer productivity; on the average, the time required to write and test a program should be reduced by half or better. This assumes, however, that the programmer is working in the structured form which the software is designed to accept.

Software Cost

The trend toward separate pricing of software should continue. The operating system is not expected to be software priced, largely because (as discussed above) it will have fewer functions and be less visible to the user. The other varieties of software discussed above will be separately priced, however. The prices will vary by function and by level of computer system for

which they are designed, but for the large multiprocessor system, 1985 software prices are forecast to be as follows:

Data Management System	\$60,000
Language Processor (each)	\$12,000
System Management Complex	\$60,000
Message Control Program	\$50,000

These are generally higher than prices for equivalent products today, because of their greater value and complexity (the data management and system management software will often dominate the user's interaction with his computer). Separate prices for program development aids are not shown, because they will probably be bundled with the compilers.

COMMUNICATIONS

Controllers

Small computers and terminals will usually be provided with a limited degree of communications control capability, since the great majority will be connected to communication lines at least part of the time, and the cost of incorporating an extra level 1 component processor for the purpose will be insignificant. With the larger monoprocessors and multiprocessors, and perhaps in some cases with miniprocessors used in networks, stand-alone communications controllers or front-end processors will be generally used. The host dependent communications controllers that are now widely used will, in general, be superseded by them. These stand-alone controllers will receive, route, sequence, and account for streams of message traffic of varied kinds independently of the connected host processors. They will have their own disc storage, I/O equipment, and software. Their functions will be essentially the same as those now performed by comparable devices, but their costs are expected to drop dramatically because of the decreased costs of their

COST FORECASTS FOR COMMUNICATIONS CONTROLLERS

A. Large systems			
2 CPU's* + 128K memory	\$ 80,000	\$30,000	\$15,000
100-megabyte disc	55,000	22,000	10,000
Line adapters (100)	45,000	25,000	10,000
Host interface	12,000	8,000	2,500
Total	\$192,000	\$85,000	\$37,500
B. Intermediate systems			
CPU* + 16K core	\$ 12,000	\$ 6,000	\$ 3,000
2-megabyte disc	5,000	1,000	100
Line adapters (20)	6,000	4,000	1,500
Host Interface	8,000	5,000	2,000
Total	\$ 31,000	\$16,000	\$ 6,600

*Processors include teleprinter control, power supply system, power fail/auto restart, memory protection, and similar features.

Table 10. Cost forecasts for communications controllers.

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processors and other components. Table 10 summarizes their expected costs by major component. Costs are shown only for large systems (incorporating redundant CPU's and fail-silence) designed to work primarily with multiprocessors, and for intermediate systems that will work primarily with monoprocessors.

Small systems are not expected to exist, because the small host computers should have a limited degree of intrinsic capability. Message control

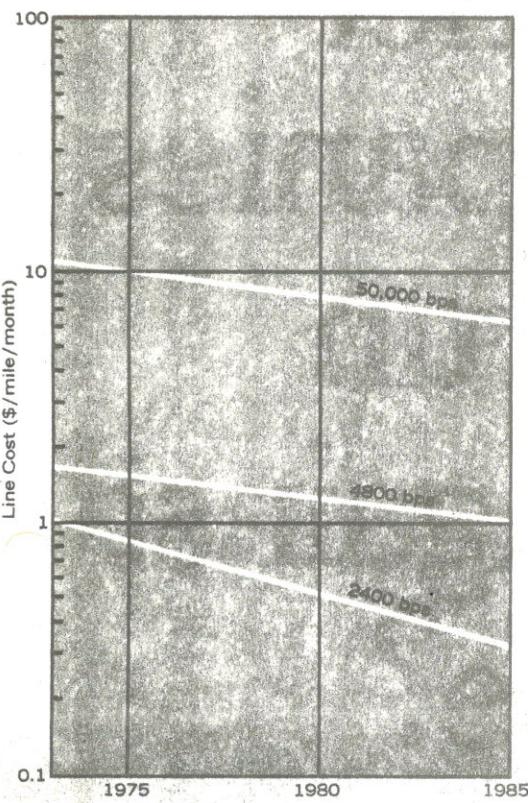


Fig. 2. The trend of data transmission line costs will be down through 1985, with an average cost reduction of 50% for transmission at each of three standard speeds.

software will be unbundled and priced separately; an estimated software purchase cost for a large system is shown above in the software cost section. It is conceivable that the cost of software for communications controllers will become greater than that of hardware.

Networks

Data traffic in the U.S. is expected to continue growing at its recent 35% annual rate continuously through 1985. A variety of new and expanded carrier services will evolve to meet this demand.

The Bell System expects to be serving about 100 major metropolitan areas in the United States with an in-

terconnected digital data service (DDS) by about 1978. We anticipate that the initial point-to-point networking of DDS will be followed by switching digital transmission service before 1985.

The first of several domestic satellite systems commenced operation in early 1974, offering new flexibility to data communications services in terms of routing, capacities, and pricing structure. Western Union's Westar network typifies one approach to domestic satellite systems, wherein large earth stations are looped to users via conventional terrestrial links. A more innovative approach, where small earth stations are placed at the user's operating location, should be implemented in this time period.

The emerging specialized common carriers, such as MCI and Datran, have entered a critical period of development. We expect that at least two of the MCI-type networks will achieve economic viability. However, it will be several years before the form of their unique service offerings is definite.

This expansion of common carrier services is likely to be accompanied by substantial reductions in charges, brought about both by technological improvement and increased competition. Fig. 2 forecasts the overall trend of line costs through 1985 for three standard speeds; the average reduction should be about 50% through 1985. (The actual reductions will of course be discontinuous because they will result from specific tariff changes; these are overall trends.)

In addition to acquiring leased or dial-up lines, users will increasingly have the alternative of using packet switching. Packet switching technology was developed specifically to improve data communications services and make possible network performance capabilities suited to the requirements of terminal-to-computer and computer-to-computer communications. Briefly, these capabilities are as follows:

- Rapid response time—packets are transmitted through the network with an average delay of less than a second. The network delay incurred in the establishment of a connection between a terminal and a host is on the order of a second.

- High reliability—multiple transmission paths between packet switching nodes protect against line failures. High reliability at each node can be insured with redundant packet switching equipment.

- Very low error rate—powerful error detection systems insure that transmission errors are detected and corrected before packets are delivered

to users, thus providing users with virtually error free data communications.

- Dynamic allocation of transmission capacity—the capacity of a packet switched network is dynamically shared among the nodes so that if any node is momentarily relatively inactive, more transmission capacity is available to all other nodes.

- Charges proportional to traffic volume—a user consumes significant network resources only when he is actually sending or receiving data. Thus, his charges can be based primarily on the quantity of data transmitted rather than on-line holding time, line capacity (bandwidth), or distance, as is the case in communications circuit tariffs.

- Improved transmission facilities—as new transmission facilities are introduced by the carriers, a packet switching network can quickly take advantage of these developments and pass the improvements in cost and/or performance on to the user without any effort on the user's part.

Because these advantages of packet switching will appeal to many users it is expected to become widely available and to grow steadily. However, since its growth involves the establishment of extensive networks requiring a great deal of capital, the rate of growth of packet switching services will be slower than demand would permit.

A final word

This article includes many generalizations and brief, overall forecasts of product areas that are in fact broad and complex. The data processing industry is heterogeneous, and many products will prosper that vary widely from those forecast here. Nevertheless, at an overall level this article may provide useful guidance to users concerned about tomorrow's products. □



Ted Withington, a senior staff member at Arthur D. Little, Inc., was the edp task leader of the study. He has published three books and numerous articles, and has been a contributing editor of DATAMATION for five years.