USER MANUAL

ICs for Digital Audio

SAA7705H

Car Radio Digital Signal Processor

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2.1	July 14, 1997	chapter 8.3.3 : functional description and adjustment procedure Level IAC and Dynamic IAC functions added. pages 33, 56 and 60 : optimal setting IAC control register for ICE-tuner changed from $0AED to $0BB5 table 9.13 (page 65) : startaddress mode (X:modpntr) for speech mode corrected (the two values were swapped incidently). appendix 11.1, application diagram SAA7705H : Value R17 changed from 1kW into 100W Value C17 changed from 10mF into 100mF Component C50 (22mF muratal) added for LW interference suppression.
3.0	February 16, 1998	chapter 8.1.2.3 : Value R17 changed from 1kΩ into 100Ω Value C17 changed from 10µF into 100µF chapter 8.3.3 : description FM IAC improved, default register contents for TEA6811/6824 added, IIC_IAC and IIC_LEVEL_IAC definition tables added. chapter 8.6 : resistor and capacitor values analog CD input changed in order to optimise CMRR characteristics. chapter 9.0.2 : default register contents for IIC_IAC and IIC_LEVEL_IAC added page 68 : procedure for starting up modes changed for mode switch digital input mode -> analog input mode chapter 9.1 , fig. 9.1 : audio monitor points added chapter 9.1.2. : Loudness coefficient tables split in high/low part coefficients chapter 9.1.4.4 : rmx values for QPD pointers added chapter 9.1.5 : second order peaking low pass filter for Bass tone control added chapter 9.1.6 : description equalizer improved chapter 9.1.7 : Subwoofer coefficient tables split in high/low part coefficients chapter 9.1.8 : Subwoofer coefficient tables split in high/low part coefficients chapter 9.2 : Coefficients for Level response time with TEA6840 tuner added chapter 9.3.4. : Coefficient table FM audio filter corrected chapter 9.3.6 : Coefficients for Noise filter response time with TEA6840 tuner added chapter 9.3.7 : Interface with TEA6840 tuner added

Summary.

The purpose of this manual is to give all hardware and software application information on the SAA7705H, being a Car Radio Digital Signal Processor (CDSP), needed to write control software and to make a hardware application.

Before reading this report it is necessary to read first the data sheet of the SAA7705H.

In this manual all the pins are described with additional information on the input- and output circuits. The blockdiagram is given and all functions are explained. All necessary coefficient settings and tables for several selections are given. The application diagram is explained in detail.
Furthermore a general outline is given for the layout of a PCB with special attention to the diminishing of EMI.
Information concerning the evaluation board and the demo software is treated in the separate usermanual "evaluation board and demo software SAA7705H".

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1 Introduction.

Digital techniques have been widely accepted in the audio world including in the Car Radio.
The CD was the first example, nowadays the digitisation of the Car Radio is a logical continuation of this trend.
Furthermore, in the Car Radio world there is a growing demand not only for a good radio perception but also for a better sound quality. People want the sound of their living room in their vehicle.
This led not only to the digitisation of analogue designs of the Car Radio, but also to the incorporation of a customized DSP on board of a Car Radio I.C., delivering many possibilities for sound quality improvement.

2 General description.

The CDSP I.C. can perform all the signal functions in front of the power amplifier and behind the AM and FM demodulation and tape/auxiliary inputs. These functions are: interference absorption, stereo decoding, RDS decoding, weak signal processing (soft mute, sliding stereo etc.), Dolby-B tape noise reduction, audio signal control (volume, balance, fader) and audio signal improvement (tone control, 10 bands equalisation, dynamic range compression, deemphasis). Some functions have been implemented in hardware (stereo decoder, RDS decoder and FM-IAC) and are not freely programmable. Digital audio signals from 2 external sources with I2S and LSB-justified format are accepted.
There are four independent analog output channels and two stereo digital output channels.

The DSP contains a basic program which enables a set with AM/FM reception, sophisticated AM/FM weak signal functions, Music Search, Dolby-B tape noise reduction, CD play with compressor function, separate bass and treble tone control and fader/balance control. For high end sets with special and more sophisticated features, an additional DSP (e.g. SAA7740H) can be connected (see literature list for the data sheet). Examples of such features are room and acoustic effects.

3 Hardware/software features.

3.1 Hardware features

. 3 Bit stream 3rd order Sigma-Delta A/D convertors with anti aliasing broadband input filters

. 1 Bit stream 1st order Sigma-Delta A/D convertor with anti aliasing broadband input filter

. 4 Sign-magnitude D/A convertors with four fold oversampling digital filters and noise shaping

. Digital stereo decoder

. Improved digital IAC for FM

. RDS processing with optional 16 bits buffer via separate channel (two tuners possible)

. Auxiliary high CMMR analog CD input (CD-walkman, speech, economic CD-changer etc.)

. 4 channel 5 band I2C controlled parametric equalizer

. Analog single ended tape input

. Separate AM left and right inputs

. Two separate full I2S and LSB-justified formats high performance in/out interfaces

. Expandable with additional DSP's for sophisticated features through an I2S gateway

. Internal Phase Lock Loop for generating the high frequency DSP clock from common fundamental oscillator crystal

. Audio short circuit protected

. I2C bus controlled (fast mode)

. -40 to 85 degr C operating temperature range

. Easy applicable

3.2 Software features

. Enhanced FM dynamic signal processing

. Integrated 19 KHz MPX filter and de-emphasis

. Electronic adjustment of AM/FM level, FM channel separation, Dolby level

. AM dynamic signal processing

. AM IAC

. Baseband Audio processing (treble/bass/balance/fader/volume)

. Soft Audio Mute

. Dynamic bass boost or loudness

. Quasi peak detector for audio output monitoring

. Tape equalisation (Tape analogue playback)

. Music search detection for Tape (MSS)

. Pause detection for RDS updates

. Hard mute during RDS updates

. Hold function for level, noise and multipath during RDS updates

. Dolby-B tape noise reduction

. Dynamics compressor for CD

. CD De-emphasis processing

. Signal level, noise and multipath detection for AM/FM signal quality information

. Improved AM reception

. 6th order low-pass filter for AM and mono input modes

. General purpose tone generator

4 Quick reference specification.

Important: This overview shows the best specification which can be obtained with an 'ideal' receiver in combination with the SAA7705H. However the specification points 4.1 and 4.2 will be limited by the front-end receiver and not by the SAA7705H.

4.1 FM reception

Frequency response(+/-1 dB)	20 Hz - 15 KHz
S/N (mono, 1KHz, 22.5 KHz dev.) (deemphasis 50 us)	> 69 dB ; typical 72 dB
S/N (stereo, 1 KHz, 22.5 KHz dev.) (deemphasis 50 us)	> 60 dB ; typical 63 dB
Max. deviation (at THD < 1%) at 1 KHz	> 120 KHz
Mono distortion, 1 KHz	
at 75 KHz deviation	< 0.2 %
at 22.5 KHz deviation	< 0.1 %
Stereo distortion, 1KHz, 1 channel	
at 22.5 KHz deviation	< 0.2 %
Stereo channel separation, 1 KHz	> 40 dB ; typical 45 dB

4.2 AM reception

Frequency response with tuner	20 Hz - 2 KHz
Frequency response (+/-1 dB) with DSP software brickwall filter (without tuner)	20 Hz - 4.5 KHz
Frequency response (+/-1 dB) without brickwall filter (without tuner)	20 Hz - 15 KHz
S/N at 1 KHz, 30 % AM	> 70 dB ; typical 75 dB
Distortion, 400 Hz, BW 5 KHz	
80 % AM	< 0.2 %
30 % AM	< 0.1 %

4.3 Analog tape input

Frequency response (+/-3 dB)	20 Hz - 18 KHz
Typ. S/N at 1 KHz, 0 dB (without Dolby-B)	85 dB
Typ. THD+N, 1 KHz (0.5 Vrms)	-80 dB
Typ. channel separation, 1 KHz	50 dB

RDS traffic information reception from radio signals in this mode is possible; the decoder is still operating

4.4 Analog CD input

Frequency response (+/-3 dB)	20 Hz - 18 KHz
Typ. S/N at 1 KHz, 0 dB	86 dB
Typ. THD+N, 1 KHz (0.5 Vrms, opamp gain = 1)	-85 dB
Typ. channel separation, 1 KHz	50 dB

RDS traffic information reception from radio signals in this mode is possible; the decoder is still operating

4.5 RDS reception

Min. nearby selectivity (neighbour ch at 200 KHz)	61 dB
Min. pilot attenuation	50 dB

4.6 CD I2S input

The performance of these input signals is actually limited by the DAC output, as described in chapter 4.7

The analog CD input can be used as an alternative input for the analog CD.

RDS traffic information reception from radio signals in this mode is possible; the decoder is still operating

4.7 Audio output performance

Typ. output level	0.72 Vrms
Bandwidth (fs=44.1 KHz, -3 dB)	20 Hz - 22 KHz
Typ. S/N	110 dBA
Typ. output noise	3 μV
Typ. THD+N, 1 KHz, 0 dB	-70 dBA
Typ. Dynamic Range, 1 KHz (-60 dB)	102 dBA
Max. crosstalk, 10KHz	-69 dB

4.8 Audio processing

4.8.1 Volume/balance/fader/tone/loudness/dynamic bass boost control

(figures count for default coefficient set)

Volume control range	-66 dB --> +20 dB
Balance attenuation range (Left/Right)	0 dB --> -30 dB
Fader attenuation range (Front/Rear)	0 dB --> -30 dB
Tone control range	
Bass control	-12 dB --> +15 dB
Treble control	-12 dB --> +15 dB
Dynamic loudness control range (level and offset)	
level	0 dB --> +14 dB
offset	0 dB --> +24 dB
Dynamic bass boost control range	
level	0 dB --> +14 dB
offset	0 dB --> +24 dB

4.8.2 Equalisation

Number of channels	4 channels
Number of bands	5 bands
Filter order	2nd order BP
Centre frequency	50 Hz --> 18 KHz
Gain control range	-30 dB --> +12 dB
Quality factor	0.001 --> 100

4.8.3 Compression

Attenuation at 0 dB input	-9 dB
Threshold level	-54 dB
Compression ratio	1:2
Amplitude shift below threshold level	+18 dB

4.8.4 Music Search (MSS)

Detection level	-35 dB
Detection time	70 msec

5 Block diagrams.

5.1 Total block diagram

The total block diagram indicates a possible application in which the CDSP can be used.
The SAA7740H must be considered as a high end application addition.

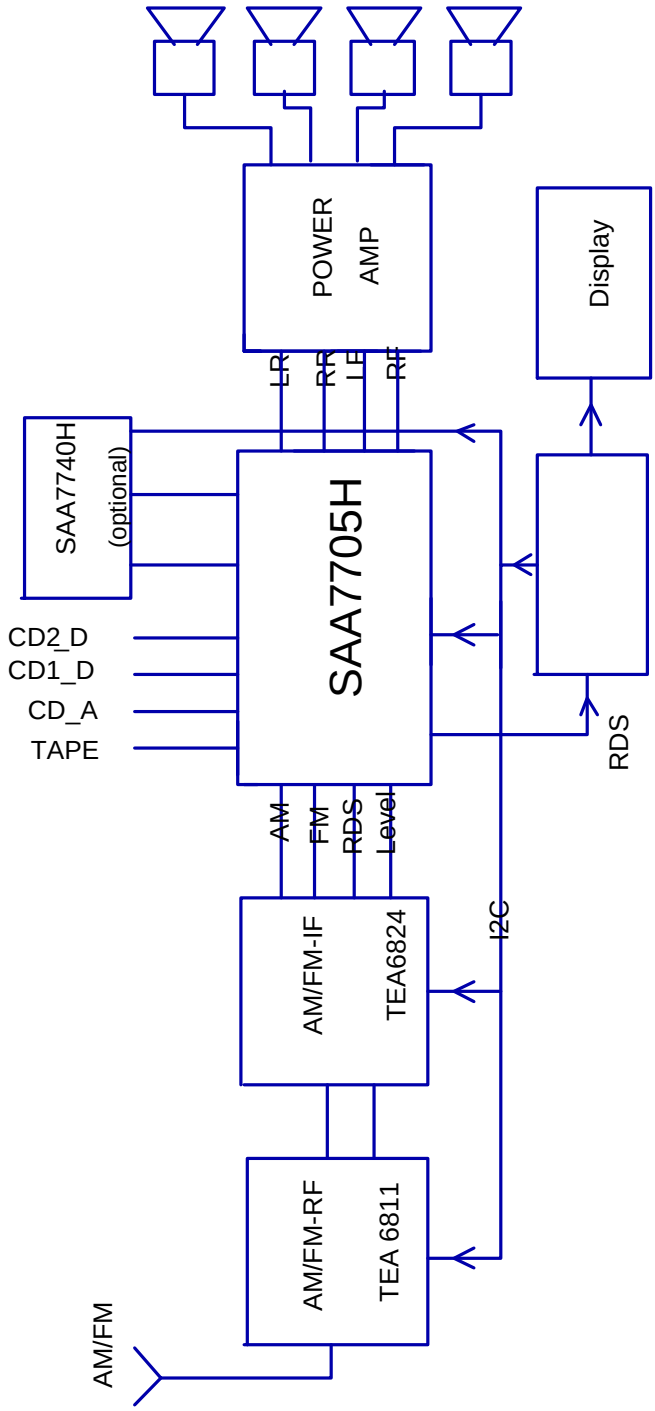


Fig 5.1 Total block diagram

5.2 CDSP Block diagram.

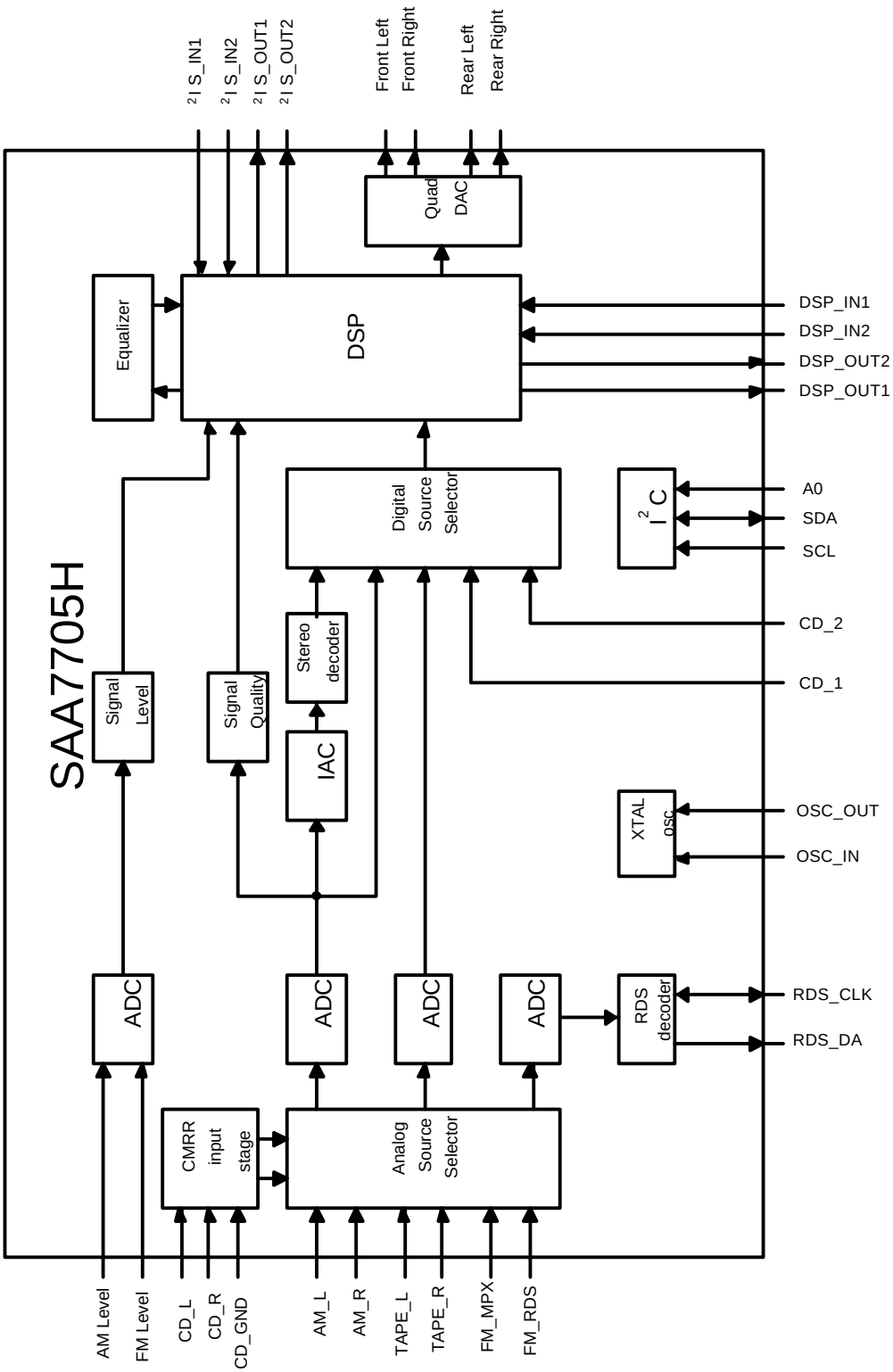


Fig 5.2 Block diagram CDSP

6 Pinning diagram.

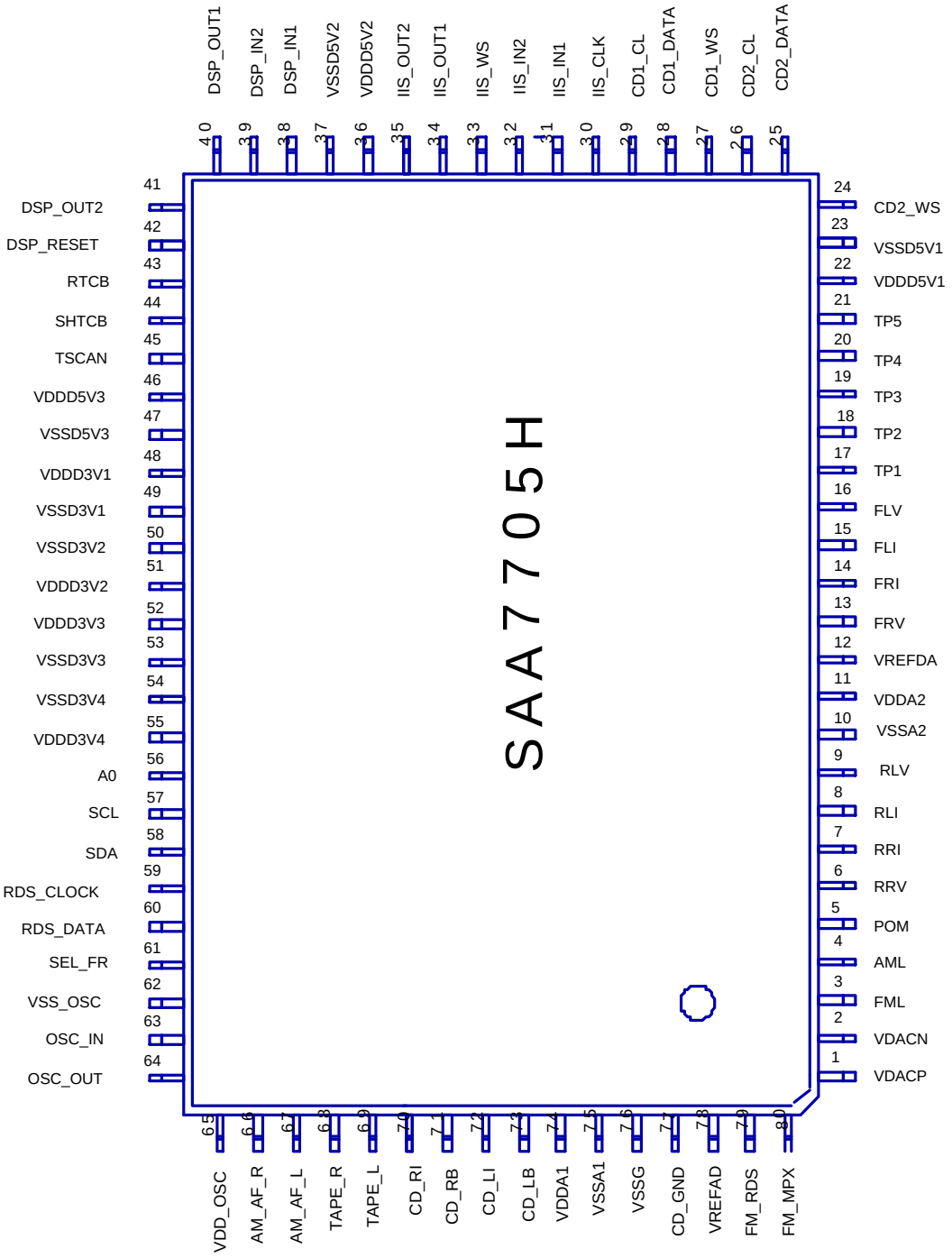


Fig 6.1 Pinning diagram

6.1 Pin description.

SYMBOL	PIN	DESCRIPTION
VDACP	1	Positive reference voltage SCAD1, SCAD2, SCAD3 and Level AD
VDACN	2	Ground reference voltage SCAD1, SCAD2, SCAD3 and Level AD
FML	3	FM-level input. FM-level information is needed for FM dynamic signal processing and search tuning in the DSP. The input goes to a 2 input multiplexer (other input is AML). Input is selected by SEL-LEV-AM/FM bit of IIC_selection register (see data sheet).
AML	4	AM-level input. AM-level information is fed to the DSP for search tuning. The input goes to the multiplexer described under pin 3.
POM	5	Input for the power on mute circuit of the DAC's which limits the maximum output current of the DAC's during power-up (active low). The timing is determined by an external capacitor.
RRV	6	Voltage output of the DAC op-amp for the Rear-right speaker. The DC output voltage is typ. VDDA2/2. These figures count also for pin 9, 13 and 16.
RRI	7	Current output of the DAC for the Rear-right speaker. The typical peak output current is 500 μA. The voltage on this pin is VDDA2/2 (typical 1.65V). These figures count also for pin 8, 14 and 15.
RLI	8	Current output of the DAC for the Rear-left speaker. For a description see pin 7.
RLV	9	Voltage output of the DAC op-amp for the Rear-left speaker. For a description see pin 6.
VSSA2	10	Ground supply of the analog part of the QDAC.
VDDA2	11	3.3V positive supply for the analog part of the QDAC.
VREFDA	12	Voltage input for the internal buffer of the DAC reference current source. This voltage is made by an internal resistance divider. In order to obtain the best ripple rejection, a filter capacitor has to be added between this pin and ground.
FRV	13	Voltage output of the DAC op-amp for the Front-right speaker. For a description see pin 6.
FRI	14	Current output of the DAC for the Front-right speaker. For a description see pin 7.
FLI	15	Current output of the DAC for the Front-left speaker. For a description see pin 7.
FLV	16	Voltage output of the DAC op-amp for the Front-left speaker. For a description see pin 6.
TP1	17	Testpin 1. This pin is used as output in factory testmode, must be unconnected.
TP2	18	Testpin 2. This pin is used as output in factory testmode, must be unconnected.

SYMBOL	PIN	DESCRIPTION
TP3	19	Testpin 3. This pin is used as output in factory testmode, must be unconnected.
TP4	20	Testpin 4. This pin is used as output in factory testmode, must be unconnected.
TP5	21	Testpin 5. This pin has an internal pull-down resistor and is used in factory test mode, must be connected to +5V.
VDDD5V1	22	5V positive supply 1 for the digital peripheral circuitry.
VSSD5V1	23	Ground supply 1 for the digital peripheral circuitry.
CD2_WS	24	I2S or LSB-justified format Word select input from digital audio source 2. This input synchronises the DSP program.
CD2_DATA	25	I2S or LSB-justified format Left-Right data input from digital audio source 2.
CD2_CL	26	I2S or LSB-justified format clock input from digital audio source 2. External source is master and delivers the clock.
CD1_WS	27	I2S or LSB-justified format Word select input from digital audio source 1. This input synchronises the DSP program.
CD1_DATA	28	I2S or LSB-justified format Left-Right data input from digital audio source 1.
CD1_CL	29	I2S or LSB-justified format clock input from digital audio source 1. External source is master and delivers the clock.
IIS_CLK	30	I2S external output clock for extra DSP chip; controlled by the ENA-HOST_IO bit of the IIC_HOST register.
IIS_IN1	31	I2S external input data channel 1 (front) from extra DSP chip.
IIS_IN2	32	I2S external input data channel 2 (rear) from extra DSP chip.
IIS_WS	33	I2S external input/output word select signal for extra DSP chip. The external device has to be synchronised by this word select signal because the CDSP chip acts as master transmitter. Controlled by the ENA-HOST_IO bit of the IIC_HOST register.
IIS_OUT1	34	I2S external output data for extra DSP chip; controlled by the ENA-HOST_IO bit of the IIC_HOST register.
IIS_OUT2	35	I2S or LSB-justified subwoofer output; controlled by the EN_HOST_IO bit of the IIC_HOST register.
VDDD5V2	36	5V positive supply 2 for the digital peripheral circuitry.
VSSD5V2	37	Ground supply 2 for the digital peripheral circuitry.
DSP-IN1	38	Digital input 1 of the DSP-core ; FM mute input (active low).
DSP-IN2	39	Digital input 2 of the DSP-core ; De-emphasis input in case a CD-D input is used (active high). Activates Freeze function for RDS updates (active low).

SYMBOL	PIN	DESCRIPTION
DSP-OUT1	40	Digital output 1 of the DSP-core ; gives indication of FM stereo (active high)
DSP-OUT2	41	Digital output 2 of the DSP-core ; FM pause detector/MSS detector (active high). Acts also as IAC trigger output. Is controlled by the IAC_trigger bit of the IIC_IAC control register.
DSP-RESET	42	This reset pin is active low and has an internal pull-up resistor. A capacitor between this pin and VSSD determines the switch-on time during power-up. As long as the power supply is not stabilised this pin should remain low (if controlled by μP), that means that a fixed timing relationship between the DSP reset (pin 42) and the POM (pin 5) is obligatory. For further explanation see chapter 8.1.4.
RTCB	43	This pin has an internal pull-down resistor and is used in factory test mode. May be connected to ground.
SHTCB	44	This pin has an internal pull-down resistor and is used in factory test mode. May be connected to ground.
TSCAN	45	This pin puts the chip in factory test mode if pulled high. This pin has an internal pull-down resistor and may be connected to ground.
VDDD5V3	46	5V positive supply 3 for the digital peripheral circuitry.
VSSD5V3	47	Ground supply 3 for the digital peripheral circuitry.
VDDD3V1	48	3.3V positive supply 1 for the DSP-core.
VSSD3V1	49	Ground supply 1 for the DSP-core.
VSSD3V2	50	Ground supply 2 for the DSP-core.
VDDD3V2	51	3.3V positive supply 2 for the DSP-core.
VDDD3V3	52	3.3V positive supply 3 for the DSP-core.
VSSD3V3	53	Ground supply 3 for the DSP-core.
VSSD3V4	54	Ground supply 4 for the DSP-core.
VDDD3V4	55	3.3V positive supply 4 for the DSP-core.
A0	56	This pin corresponds to the slave sub-address of the I2C selection. This allows the device to have 2 different addresses. May be connected to ground if A0=0
SCL	57	Serial clock input (I2C-bus).
SDA	58	Serial data input/output (I2C-bus).
RDS_CLOCK	59	Radio Data System bit clock output. Clock recovered from inaudible RDS information which is transmitted by FM broadcasting. Also RDS external clock input to clock out the buffered RDS data; controlled by the RDS_CLKIN bit of the IIC_RDS control register.
RDS_DATA	60	Radio Data System data output; to be used for further processing in a suitable decoder.

SYMBOL	PIN	DESCRIPTION
SEL_FR	61	Selects in FM mode between FM-MPX and FM-RDS inputs: low or open for FM-MPX, high for FM-RDS. The selected signal goes to the SCAD3.
VSS_OSC	62	Ground supply for the X-tal circuitry.
OSC_IN	63	Crystal oscillator input. This pin can also be used as forced input in slave mode.
OSC_OUT	64	Crystal oscillator output. The crystal used is a fundamental mode crystal (11.2896 MHz).
VDD_OSC	65	3.3V positive supply for the X-tal circuitry. The supply connections of the crystal oscillator circuit are separated from the other 3.3V supplies. This to minimise the feedback from the ground bounce of the chip to the crystal oscillator circuit. This supply voltage may not have any spikes on it.
AM_AF_R	66	Analog input pin for AM audio frequency Right channel.
AM_AF_L	67	Analog input pin for AM audio frequency Left channel.
TAPE_R	68	Analog input for Tape Right signal.
TAPE_L	69	Analog input for Tape Left signal.
CD_RI	70	Analog input for CD Right signal.
CD_RB	71	Feedback input for analog CD Right signal.
CD_LI	72	Analog input for CD Left signal.
CD_LB	73	Feedback input for analog CD Left signal.
VDDA1	74	3.3V positive supply for analog part of the ADC's. The analog part of the ADC's have a separate supply to allow maximum filtering (see the application diagram in chapter 12.1).
VSSA1	75	Ground supply for analog part of the ADC's.
VSSG	76	This pin is connected to a guard ring which isolates the analog input part from the digital circuitry. This pin has to be connected to VSSA1.
CD_GND	77	Analog input for ground shielding of analog CD cable. A very high ohmic resistor (1 MΩ) should be connected between this pin and VREFAD (pin 78).
VREFAD	78	Common mode Midref voltage for SCAD1, SCAD2, SCAD3 and Level AD. In order to prevent crosstalk between the AD inputs and to obtain the best PSSR, a filter capacitor has to be added between this pin and VSSA1.
FM_RDS	79	Analog FM-RDS input. The signal should contain the inaudible RDS information which is transmitted by FM radio broadcasting.
FM_MPX	80	Analog input pin for FM multiplex signal. Selection between FM signal and aux/AM/tape signals is controlled by the SEL_AUX_FM bit of the IIC_selection register.

7 Functional description of the CDSP modes and functions.

Introduction.

The CDSP block diagram is depicted in figure 5.2. For a thorough description of the CDSP block diagram see the data sheet of the SAA7705H. In this chapter a general overview is given of all modes and functions.

The CDSP can be set in several operation modes. Each mode executes functions which are required for that particular mode.
The selection of a particular mode is software controlled (via the I²C bus) and described in chapter 9.
The required inputs for each mode can be selected by a analog or digital source selector which is software controlled (via the I²C bus). The source selection is also described in chapter 9.

7.1 Audio processing

All basic audio processing in the CDSP chip is performed by the integrated digital signal processor, except the parametric equalizer that is realized in hardware.

The signal flow is fixed and the functions are controlled by sending coefficient values to the appropriate places in the processor coefficient memory via the I²C bus.

The functions of the Audio processing block are always executed **independent of the mode**.

The following functions for the two independent a.f. channels have been implemented:

- Volume control

The volume control function determines the output voltage of the CDSP. The volume control is split into a gain and a attenuation section which acts equal for both channels. The volume control contains also a prescaling which ensures that for the various input signals the same sound pressure level (for a fixed volume setting) can be obtained at the output of the CDSP.

- Tone control

The tone control function consists of a filter that controls the gain of the bass and treble section.
The cut-off frequency of both sections is selectable. To avoid clipping in the tone control filter the input signal is first attenuated and after processing amplified again (in the balance block).

- Loudness

The loudness function consists of a filter that boosts the high and low frequency part of the audio spectrum. It is not a part of the tone control filter.
The loudness filter can boost the high and low frequencies in the 3 following ways:

a) Static loudness, in this case the bass and treble boost is controlled by the volume setting.

b) Dynamic loudness, in this case the bass and treble setting is controlled by the instantaneous output level. The output level is measured by the quasi peak detector and the highest value of the two output channels is used to determine the loudness curve.

c) Dynamic bass boost, in this case only the low frequencies are boosted and is controlled by the instantaneous output level. The dynamic loudness and dynamic bass boost cannot be active at the same time because both functions use the same processing block.

- Balance

The balance function controls the attenuation of either the left or the right channel while the other channel is kept constant.

- Fader

The fader function controls the attenuation of either the front or rear channels while the other channels are kept constant.

- Soft audio mute

The soft audio mute function enables the user to generate a gradual mute or de-mute function without undesired clicks.

- Quasi Peak Detector

The purpose of the peak detector is to give an indication of the output level.
Two independent peak detectors are available.

- Parametric Equaliser

The 4 channel 5 band parametric equaliser can be used to optimize the sound reproduction in a car or tone control. The equalizer is controlled via the I²C bus.

7.2 AM/FM signal quality processing

The level signal of a tuner is used for detection of the quality of a received station, being fieldstrength (AM and FM level information) and multipath. This information is used for enhanced AM and FM dynamic signal processing (see AM and FM mode in chapter 9) and is also available for the controller (for search and for RDS strategy).

The level signal of the tuner is processed in the DSP and the output of the AM/FM signal quality processing block delivers normalized and filtered level and multipath information.

The DSP processing is always executed and so the signal quality signals are internally available in every mode. The selected inputs are AM-Level and/or FM-Level.

7.3 FM mode

This is the mode for FM reception. The selected input is FM-MPX or FM-RDS

The program in the FM mode offers the following functions:

Enhanced FM dynamic signal processing

The FM dynamic signal processing adapts the FM audio characteristics depending on the quality of the received station. As criterium to judge this quality the following parameters are used:

- the level signal as a measure for the fieldstrength
- the multipath detector output as a measure for the multipath distortion
- the noise above 60 KHz of the MPX signal as a measure for the adjacent channel interference

From the audio characteristics the output level (softmute), the stereo image (sliding stereo to mono) and the audio frequency response (high cut control) are adapted. The following functions are implemented:

- Softmute as a function of level and noise:
  - fast attack and recovery at level dips with a low repetition rate
  - fast attack with slow recovery at dips with a high repetition rate or with a long duration
  - fast attack and recovery at adjacent channel breakthrough

- Stereo control (sliding stereo) as a function of level, noise and multipath:
  - fast attack and recovery at level dips, noise or multipath bursts with a low repetition rate
  - fast attack with slow recovery at events with a high repetition rate or with a long duration

- Audio frequency response control as a function of level, noise and multipath:
  - fast attack and recovery at level dips, noise or multipath bursts with a low repetition rate
  - fast attack with slow recovery at events with a high repetition rate or with a long duration.

Adjustment of channel separation

The purpose of this function is to compensate for the non flat frequency response around 38 KHz of the FM tuner which causes extra cross-talk.

FM De-emphasis filter and 19 KHz MPX filter

The purpose of the de-emphasis filter is to compensate the pre-emphasized FM signal with a filter with a time constant of 50 µs or 75 µs. The notch filter at 19 KHz is used to protect tweeters in high power applications from overload by the stereo pilot.

FM audio filter

The purpose of the FM audio filter is to set the audio bandwidth in FM mode independent from the other modes.

Stereo detection

The purpose of the stereo detector is to indicate the presence of a pilot tone and that the stereo decoder is in lock. The output of the stereo detector is the DSP_OUT1 pin (pin 40). "High" indicates FM stereo and "low" FM mono.

Noise filter

The noise level is detected in a band from 60 KHz till 120 KHz with an envelope detector (see data sheet). The noise level is used as adjacent channel information for the controller and for the FM dynamic signal processing.

RDS updates

This function offers the following features:

- Pause detection
  The purpose of the pause detection is to search for a pause in the FM signal.
  A pause is detected when the FM signal is below a pre-defined level for a certain amount of time.
  The output of the pause detector is the DSP-OUT2 pin (pin 41). "High" indicates pause.

- Mute
  The purpose of the mute is to mute the FM signal that goes to the audio processing block.
  This mute is activated by the external control pin DSP-IN1 (pin 38). "Low" is mute.

- Hold function
  The purpose of the hold function is to prevent that the information retrieved during an RDS update can disturb the filters in the FM signal processing block.

- Freeze function
  The purpose of the freeze function is to freeze the level, noise and multipath values measured during an RDS update and to read them out after the update. The freeze function is activated by the external control pin DSP-IN2 (pin 39). "Low" indicates freeze.

Interference absorption circuit (IAC)

The Interference Absorption Circuit (IAC) detects and suppresses ignition interference.
The characteristics of the IAC can be adapted to the properties of different FM tuners by means of the predefined coefficients in the IAC control register. The values can be changed via the I²C bus.
On power on the nominal setting for a good performing IAC is selected (all IAC control bits are set to their default value, according the SAA7705 datasheet). For further information see chapter 8.3.

7.4 AM-mono mode

This is the mode for mono MW, LW or SW reception, the selected input is AM_AF_R.
The program in the AM-mono mode offers the following functions:

AM dynamic signal processing

The AM dynamic signal processing adapts the AM audio characteristics depending on the quality of the received station. As criterium to judge this quality the level signal as a measure for the fieldstrength is used.

From the audio characteristics the output level (softmute) and the audio frequency response (high cut control) are adapted. The following functions are implemented:

- Softmute as a function of level
- Audio frequency response control as a function of level

6th order Low-pass filter

The purpose of the low-pass filter is to suppress interference whistles from adjacent channels and noise.

AM IAC

The AM IAC (interference absorption circuitry) detects and eliminates audible clicks caused by impulsive interference, such as caused by engine ignition or van, on AM reception.
The characteristics of the AM IAC can be adapted to the properties of different AM tuners by means of coefficients in the YRAM of the CDSP. For further information see chapter 9.4.6.

7.5 Tape mode

This is the mode for processing the output of an analog tape deck. The selected inputs are Tape_L and Tape_R.
The program in the Tape mode offers the following functions:

- Standard Dolby-B decoder (on/off via I²C control)

- Adjustment of the Dolby level

7.6 CD-analog mode

This is the mode for processing the output of the analog output of a CD player. The selected inputs are CD_RI/RB and CD_LI/LB.
The program in the CD_A mode offers the following functions:

- Dynamics compressor (on/off via I²C control)
  The compressor attenuates high level input signals and boosts low level input signals according to a fixed compression curve.

7.7 CD-digital mode

This is the mode for processing the digital input signal from a CD player.
The selected input is either CD-1 I²S or CD-2 I²S.
The program in the CD_D mode offers the following functions:

- Dynamics compressor (on/off via I²C control)
  The compressor attenuates high level input signals and boosts low level input signals according to a fixed compression curve.

- De-emphasis (on/off via input DSP-IN2 (pin 39))
  The DSP-IN2 pin is activated by the CD player in case that player is playing back a recording with pre-emphasis.

7.8 General purpose tone generator

The tone generator generates a wide range of bleep sounds with selectable frequency and wave form. These bleep sounds can be used for audio feedback or for test purposes.

7.9 MSS mode

The purpose of the Music Search (MSS) mode is to search for the next pause on a cassette tape.
The selected input is Tape_L and Tape_R.
The output of the MSS mode is the DSP-OUT2 pin (pin 41). This pin is "High" when the level of the input signals remain below a pre-defined level for a certain amount of time.

7.10 Speech mode

The speech mode offers the function that a mono, e.g. a speech signal, can be applied at one channel and reproduced by all output channels. The preferred input is the AM_L input but it is also possible to use one of the analog CD or Tape inputs if desired.
In the speech mode a 6th order filter is available e.g. to optimise the audio response for speech.

7.11 Radio Data System (RDS) function

The selected input for this function is either FM-RDS or FM-MPX.
This function offers the following features:

- Decoding of the inaudible RDS information, which is transmitted by FM broadcasting and send it to a suitable external decoder

- two tuners concept. There are two different input pins from which the RDS information can be retrieved. The RDS information is available by each bit or buffered by 16 bits.

7.12 Second processor extension function

This function offers the possibility of the addition of second DSP (e.g. SAA7740H) which offers special, more sophisticated features such as acoustic and room effects.

7.13 Transparant mode

The transparant mode offers the possibility to connect any (stereo) input directly to the (stereo) audio processing block without any additional source processing.
This mode can be used for instance:

if an external AM stereo decoder is used	(AM_L and AM_R inputs)
if an external DOLBY C decoder is used	(TAPE-L and TAPE_R or with CD_L and CD_R inputs)
for handling external DAB signals	(CD-1 or CD-2 inputs)

7.14 Digital subwoofer and center output function

This function offers digital outputs for subwoofer and center output application.
With external D/A converters these signals can be made audible to the user.
The following functions are available :

- Subwoofer with 4th order low pass filter in combination with flat Center
- Subwoofer Left and Right, with a second order low pass for each

8 HW application of the CDSP

General

In this chapter the external components are discussed, sometimes in combination with the on chip input/output circuits.
The sequence in which the hardware aspects of the different modes are discussed is the same as in chapter 7.
How to select a mode is described in chapter 9 and how to select a specific input is described in the data sheet.

The external components are depicted in the CDSP application diagram which can be found in appendix 12.1. It must be stressed here that this application diagram is an example, not the ultimate application diagram. The PCB lay-out of the application diagram is depicted in appendix 12.4.

The value, maximum tolerance and material of all external components are indicated in the partslist which can be found in appendix 12.3.

There is also an application diagram of the evaluation board and that contains much more components in order to optimize the EMC. The evaluation board is treated in detail in the separate usermanual "evaluation board & software SAA7705H".

8.1 Audio processing

In this chapter the following hardware functions will be covered

- Analog outputs (D/A convertors)
- Voltage and current reference sources
- Power on/off mute
- DSP reset

8.1.1 Analog outputs (pin 6, 7, 8, 9, 13, 14, 15 and 16)

There are 8 analog outputs namely those which make the 4 outputs of the 4 D/A convertors (Front Left/Right and Rear Left/Right). The basic block diagram of one analog output is depicted in figure 8.1.

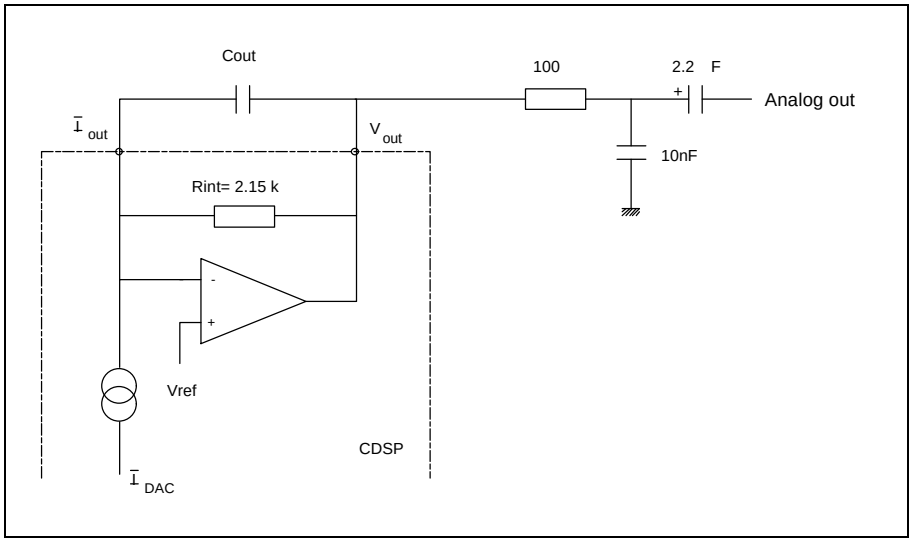


Fig. 8.1 Analog output block diagram

An analog output consists mainly of a current to voltage convertor.
A current to voltage convertor is constructed by using the internal CMOS op-amp and resistor as depicted in figure 8.1. The current from the DAC is converted into a voltage via Rint. The out of band noise and the audio band images around multiples of the sampling frequency can be further attenuated by adding a capacitor Cout and creating so a 1st order low pass filter. The audio band image around 4*sample frequency (4fs) is the strongest one because this audio band image is not filtered by the digital filter but only by the socalled sinx/x roll-off and by the analog postfilter. The effect of the sinx/x roll-off is shown in a plot of the overall frequency spectrum which can be found in the data sheet.

Application considerations:

a) VOUT_AC = 0.75 Vrms (full scale)
R_{int} = 2.15 KΩ ± 30%
C_{out} = 2.2 nF (C33, C34, C35, C36)

b) The RC value results in a cut-off frequency of 33.6 KHz (**fc=1/2πRC**). This cut-off frequency is chosen in order to fulfil the required stopband attenuation. The stopband attenuation is an addition of the roll-off of the RC filter, the sinx/x roll-off and the suppression of the digital filter.
A cut-off frequency of 33.6 KHz gives the following figures for the roll-off of the RC filter :

fs = 38 KHz :
Roll-off at 19 KHz : -1.20 dB (19 KHz is the edge of the pass band in case fs=38 KHz)
Roll-off at 133 KHz: -12.21 dB (133KHz = 4*38KHz -19 KHz)

fs = 44.1 KHz :
Roll-off at 22.05 KHz : -1.55 dB (22.05 KHz is the edge of the pass band in case fs=44.1 KHz)
Roll-off at 154.35 KHz: -13.43 dB (154.35 KHz = 4*44.1 KHz -22.05 KHz)

Because the tolerance of the cut-off frequency, the required tolerance for C_{out} is 5%.

c) The sinx/x roll-off can be calculated as follows: **A = 20log (sin πf/4fs)/(πf/4fs)**

Calculation example for fs=38 KHz:

Roll-off at 133 KHz --> A = 20 log (sin π133/152)/(π133/152)= -17 dB.
Roll-off at 19 KHz --> A = 20 log (sin π19/152)/(π19/152)= -0.22 dB.

Similar for fs=44.1 KHz:

Roll-off at 154.35 KHz = -17 dB.
Roll-off at 22.05 KHz = -0.22 dB.

d) Total typical roll-off:

fs = 38 KHz :
Total roll-off at 19 KHz is -0.22dB - 1.20 dB - 1 dB (dig. filter) = -2.42 dB
Total roll-off at 133 KHz is -17 dB - 12.21 dB = -29.21 dB (no extra digital filtering is this region)

fs = 44.1 KHz :
Total roll-off at 22.05 KHz is -0.22dB - 1.55 dB - 1 dB (dig. filter) = -2.77 dB
Total roll-off at 154.35 KHz is -17 dB - 13.43 dB = -30.43 dB (no extra digital filtering is this region)

e) Worst case roll-off figures:

The tolerance of components R_{int} and C_{out} influence the roll-off figures.
Table 8.1 give the worst case roll-off figures when taken into account a tolerance of 30% for R_{int} and 5% for C_{out}.

fs = 38 KHz	max. passband attenuation at 19 KHz	3.25 dB
	min. stopband attenuation at 133 KHz	26.0 dB
fs = 44.1 KHz	max. passband attenuation at 22.05 KHz	3.77 dB
	min. stopband attenuation at 154.35 KHz	27.1 dB

Table 8.1 Worst case roll-off figures analog postfilter

Remark: If the total roll-off in the pass band is considered to be too big then a smaller capacitor can be used resulting in a smaller roll-off in the pass band but also a smaller roll-off in the stopband. The final choice is up to the applicant.

f) The DC output voltage is the same as VREFDA (typ. 1.65V). This DC is removed by the electrolytic capacitors C41, C42, C43 and C44. The cut-off frequency (and phase non-linearity) of these high pass filters depends on the input impedance of the equipment behind the CDSP.
The extra 1st order RC filter is to suppress radiation from the analog output to the outside world (fc = 160 KHz) (R27, R28, R29, R30, C37, C38, C39, C40). The cut-off frequency is not critical (component tolerance of 20% is tolerable). These filters may be omitted if considered not necessary.

8.1.2 Internal reference sources

The CDSP contains an internal reference voltage source and an internal reference current source for the D/A convertors and two internal voltage reference sources for the A/D convertors.

8.1.2.1 Internal reference voltage source VREFDA (pin 12)

The block diagram of the reference voltage source VREFDA is depicted in figure 8.2.

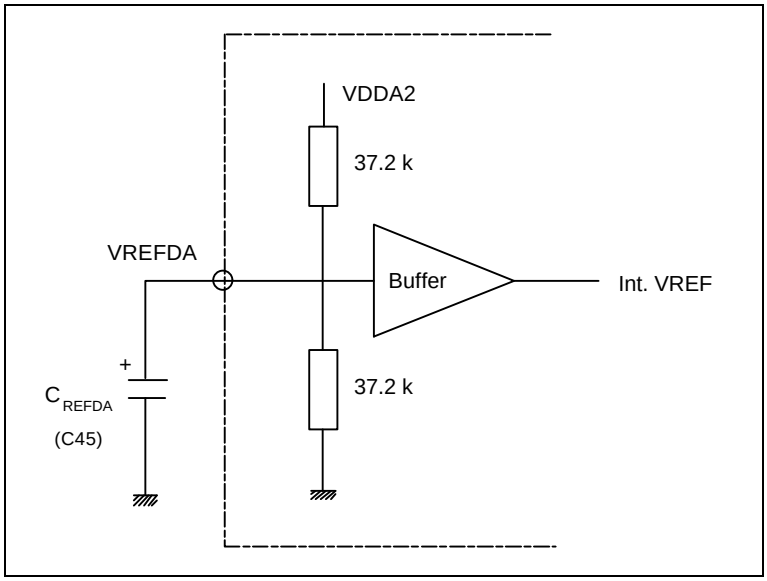


Fig. 8.2 Internal reference voltage source VREFDA block diagram

The supply voltage VDDA2 is divided by two internal 37.2 kΩ resisters and buffered. The output is called the internal Vref and is used as the reference voltage for the current source of the D/A convertors. As filtering for the internal reference voltage a capacitor is added at the VREFDA pin.

In the CDSP application we use:

f >= 1 KHz (Vripple=100 mV), ripple rejection (PSRR)= typ. 60 dB, C_{REFDA}=22µF (C45).

8.1.2.2 Internal reference current source

The internal reference current source delivers the current for the D/A convertors.
The block diagram of the internal current reference source is depicted in figure 8.3.

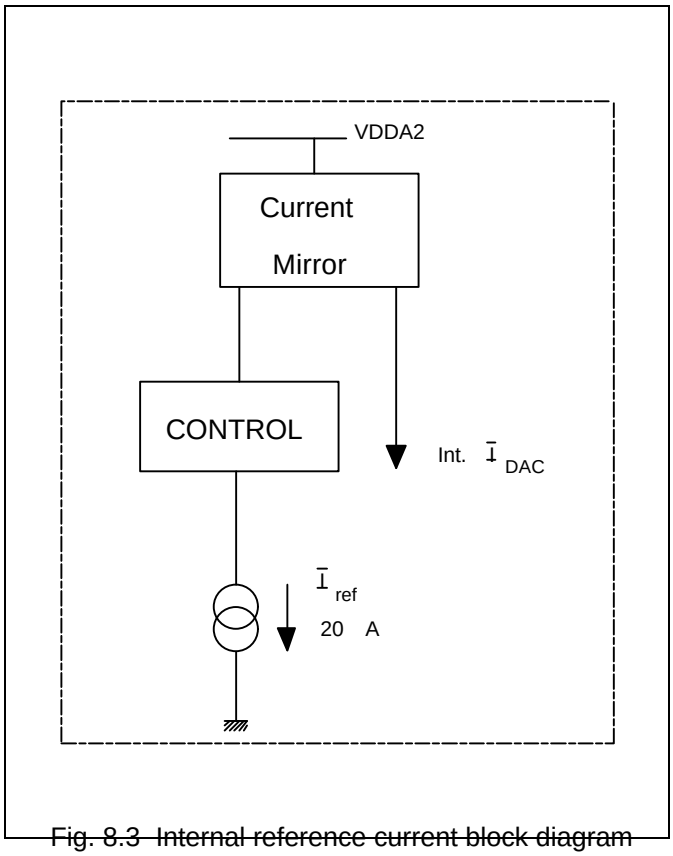


Fig. 8.3 Internal reference current block diagram

Fig. 8.3 Internal reference current block diagram.

The peak current of the D/A convertor current source equals 25 times the current drawn by the internal current source (I_{ref}) and is 500 μA. Note that this current is fixed and that it is not possible to change the current value.

8.1.2.3 Internal reference voltage source VREFAD (pin 78)

The block diagram of this internal voltage reference source is depicted in figure 8.4.

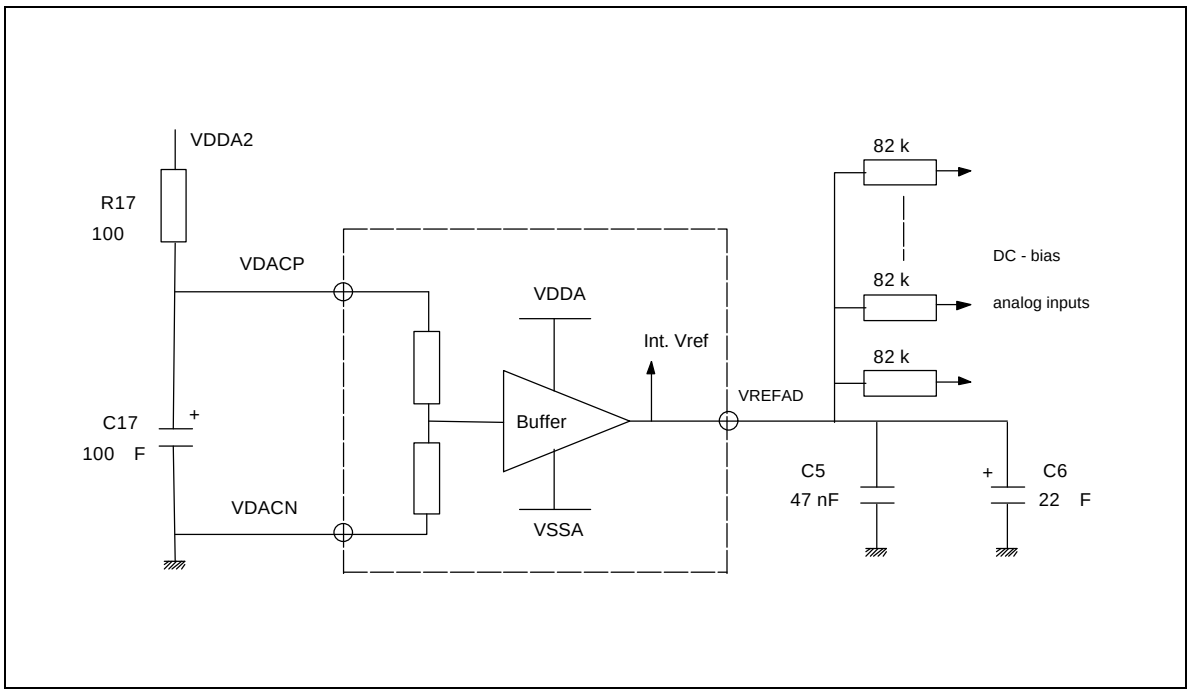


Fig. 8.4 Block diagram internal voltage reference source VREFAD.

VREFAD is the 1.65 V reference voltage of the switch capacitor D/A convertors (and buffers) of the level A/D convertor, SCAD1, SCAD2 and SCAD3.
The external 100 Ω resistor (R17) and 100 µF elco (C17) filter the analog supply voltage VDDA2 and are added to improve the power supply rejection ratio (PSRR).
In the CDSP application we use:

f >= 1 KHz (Vripple=100 mV), ripple rejection (PSRR)= typ. 36 dB, C_{REFDA}=100µF (C17).

The supply voltage VDDA2 is divided by two internal resistors and buffered. The output impedance of the buffer is about 20 Ω, the external 47 nF capacitor (C5) is added to remove high frequency noise on the reference voltage for the A/D convertors.

The VREFAD voltage is also used as a DC-bias for the analog AM, Tape and CD input via 82 kΩ resistors. Due to the low output impedance of the buffer, the crosstalk between the analog inputs is ≤ -74 dB at DC, the external 22 µF elco (C6) is added to further improve the crosstalk rejection to ≤ -80 dB at 1 KHz.

8.1.3 Power on/off mute

The block diagram of the power on mute (POM) circuit is depicted in figure 8.5.

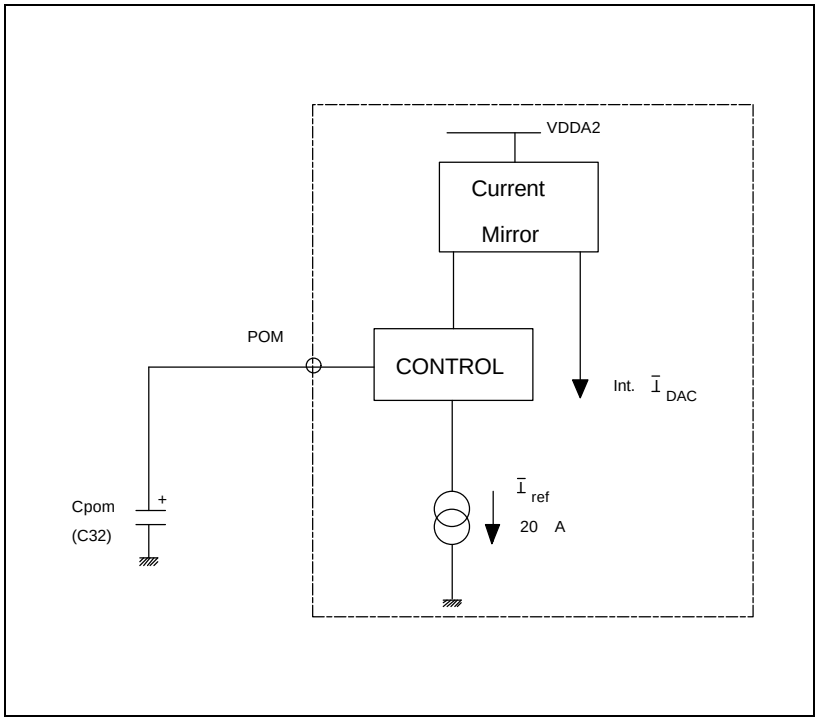


Fig. 8.5 Power on mute block diagram

Power on Mute (pin 5)

To avoid any uncontrolled noise at the audio outputs after power-on/off of the IC, the internal reference current source of the D/A converter is controlled. The capacitor on the POM pin (C32) determines the switch-on timing of this current. See figure 8.6

At power-on the current outputs are 0 µA and V_{POM} = 0 V. The CONTROL function generates a current through C_{pom} of 4 µA. V_{POM} increases linearly until V_{POM} = 0.7 V , at this point the POM current becomes about 85 µA and V_{POM} increases fast until it reaches VDDA.

As a result of this POM control the Vout-AC at the DAC outputs (in dB) increases almost linear from -100 dBFS till 0 dBFS.

Remark : There will always be a small DC plop of about 300 mV on the DAC outputs at power-on of the CDSP.

At time=t_{pom} the DAC output Vout-AC = -20 dBFS, before this output voltage is reached the chip must be resetted. After the reset the chip comes automatically in the idle mode via the DSP program (see also chapter 9). This DSP program sets the outputs of the digital upsampling filters to digital silence and therefore the AC output current of the DAC's to 0 µA (see also in the next chapter).

The time t_{pom} as function of C_{pom} is : $\mathbf{t_{pom} = 0.175 * C_{pom}}$ (C_{pom} in µF)

The time t_s during which the output voltage further increases from -20 dBFS to 0 dBFS is :

$\mathbf{t_s = 0.15 * t_{pom}}$

In the CDSP application we use:

Tpom = 820 msec (± 20%)
Cpom = 4.7µF (C32)

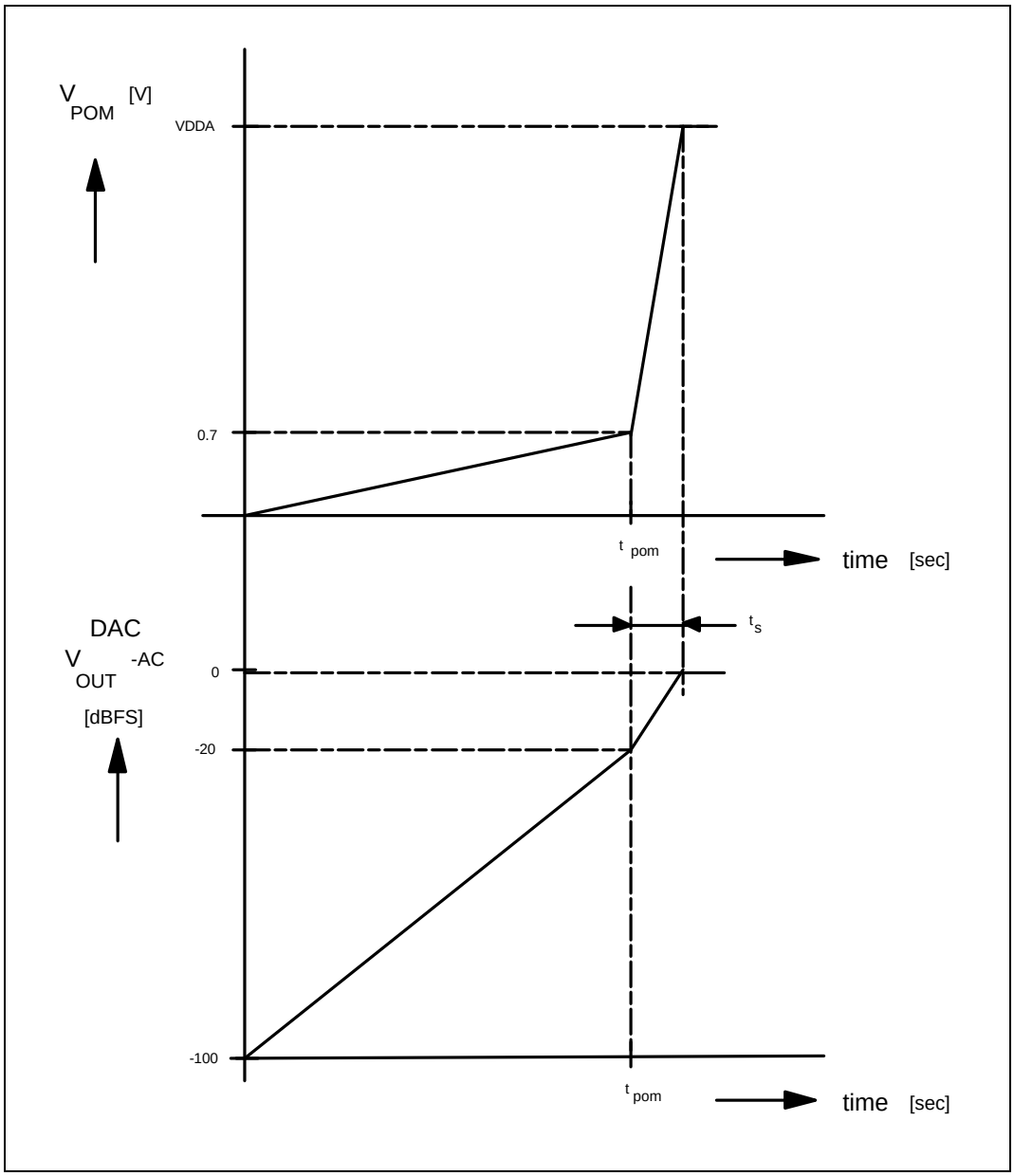


Fig. 8.6 Switch-on timing DAC

Hard mute

A hard mute via the software is only possible in the FM mode using the DSP_IN1 pin (pin 38).
In case a hard analog output mute is required in all other modes during normal use, the POM pin can be used as a hard output mute by de-charging C_{pom}.
Note that the reference currents of the A/D convertors are not affected by the POM circuit,
the DSP and the RDS demodulator remain getting data during a hard mute with the POM pin.

Power off plop suppression

To avoid plops in a power amplifier, the supply voltage of the analog part of the D/A converter and the op-amps are fed by an external voltage regulation circuit (R31, R32 and T1) and an extra capacitor (C30) as indicated in the application diagram. During power-off the output voltage will decrease gradually, allowing the power amplifier some extra time to switch off without audible plops.
In addition the POM should be pulled to zero by the µProcessor before the power supply of the digital circuitry (VDDD3V1, VDDD3V2, VDDD3V3 and VDDD3V4) is below 2.2V. Below this value the digital circuitry is undefined and can therefore cause extra undesirable clicks during power-off.

8.1.4 DSP Reset (pin 42)

The reset pin is active low and has an internal pull-up resistor of which ranges between 23 kΩ and 80 kΩ. Between this pin and the VDDD3V ground a capacitor (C25) should be connected to allow a proper switch-on of the supply voltage. The capacitor value is such that the chip is in reset as long as the power supply is not stabilised. A more or less fixed relationship between the DSP reset (pin 42) time constant and the POM (pin 5) time is obligatory. The voltage on the POM pin determines the current flowing in the DACs. At 0 V at the POM pin the DAC currents are zero and so are the DAC output voltages. At 3.3 V the DAC currents are at their nominal value. Long before the DAC outputs get to their nominal output voltages, the DSP must be in working mode to reset the output register of the digital filter, therefore the DSP reset time constant must be shorter than the POM time (t_{pom}).
The dsp reset input is a digital input (with hysteresis) and that means that the dsp reset circuit is enabled when Vc_{dspres}=80%Vdd.

In the CDSP application we use:

Tdspres	=	7.3-31.2 msec (tolerance is due to tolerance on the pull-up resistor (between 23 kΩ 80 kΩ) and the capacitor tolerance (10%))
Cdspres	=	220 nF (C25)

In calculating Tdspres it is assumed that Vc_{dspres}=80%Vddd and the formula to calculate Tdspres is:

$$\mathbf{Vc_{dspres} = Vddd(1 - e^{-Tdspres/RC})}$$

The reset has the following functions:

- the bits of the I^2C control register are set to their preset values
- the bits of the input selector control register are set to 0
- the program counter is set to address $0000
- pin 40 (DSP-OUT1) and pin 41 (DSP-OUT2) are resetted to 0

When the level on the reset pin is at logical high (Vc_{dspres}=80%Vddd), the DSP program starts to run from the idle mode, resets the output registers of the digital filters and the µProcessor can start sending commands.

General timing requirements are:	Tdspres	>	Tpower
	Tpom	>	Tdspres
	TµPcomm	>	Tdspres

Figure 8.7 gives an overview of the several time constants.

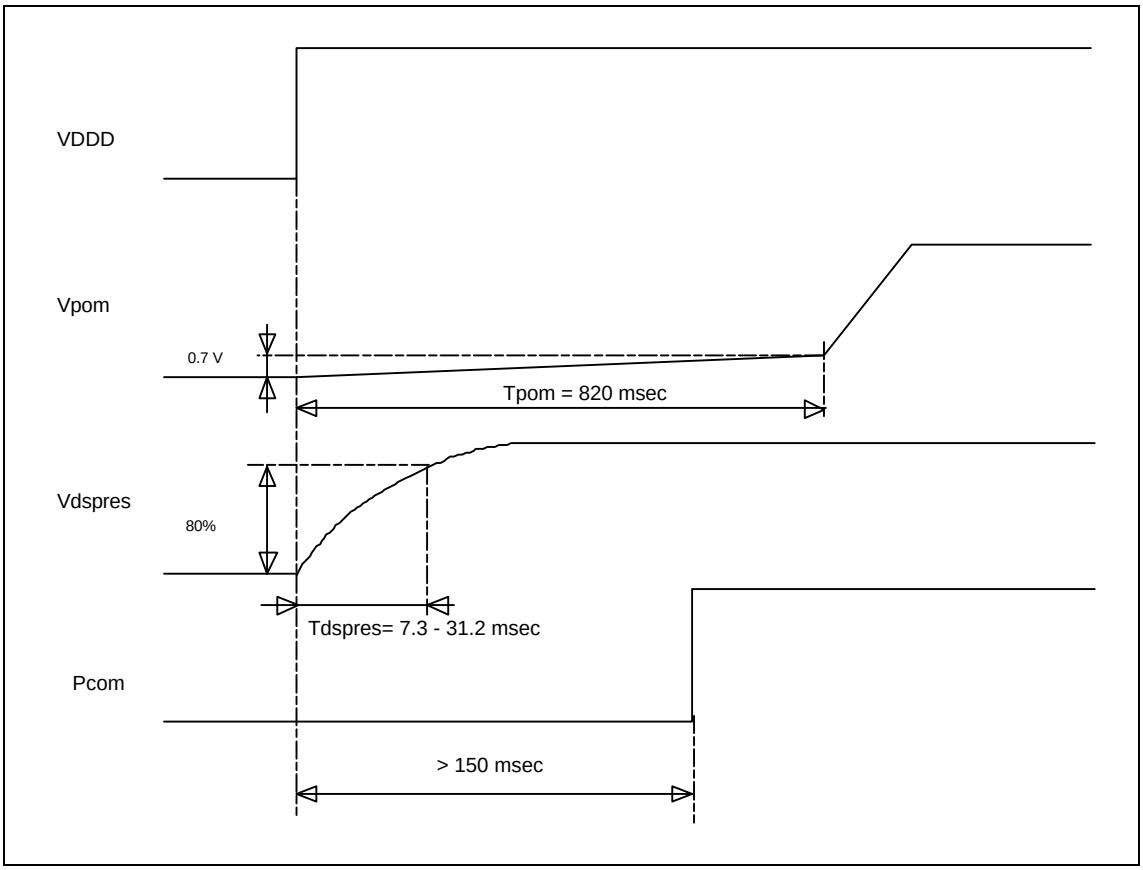


Fig. 8.7 Power-up timing diagram to avoid clicks

8.2 AM/FM signal quality processing

FM/AM level (pin 3 and pin 4)

The basic circuit diagram of the FM/AM level input is depicted in figure 8.8.

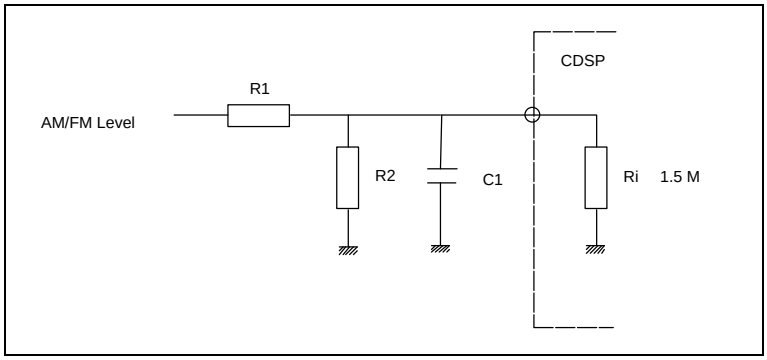


Fig. 8.8 FM/AM level input
Fig. 8.8 FM/AM level input

The level signal from the tuner is divided with resistors R1 and R2 in order to match the conversion range of the Level A/D convertor to the tuner properties.
With R1, R2 and C1 a first order low pass filter is realised at the level input.
The cut-off frequency of this filter is :

$$fc = \frac{1}{2.p.\frac{R1.R2}{R1+R2}.C1}$$

The low pass filter at the input of the FM level pin has two functions:

- to avoid aliasing in the level A/D convertor, that means that frequency components of $f > 1/2\ fs_{A/D}$ < 54 dB below the maximum input of the level A/D convertor (figure for S/N for level A/D convertor, mentioned in data sheet)

- to create a filter for the multipath detector with a cut-off frequency of 34 KHz (± 20%)

These functions are realised with R1=27 kΩ (± 10%), R2=27 kΩ (± 10%) and C1= 330 pF (± 10%). The capacitor is connected to the ground plane.

Remarks:
a) The source resistance is not taken into account because this R_{source} << (27 kΩ /2) otherwise the cut-off frequency is affected.
b) The input resistance of the CDSP is not taken into account because this Rin is big (1.5 MΩ min.).

The conversion range of the A/D convertor is from 0 V to VDDA1 (see spec in the data sheet).
The voltage range of the FM level information has to be within this range. The total voltage range of the level information has to be >= 1/2 VDDA1 to meet the minimum resolution.

8.3 FM mode

8.3.1 FM input pins

SEL_FR (pin 61)

The function of the SEL_FR pin is to select in FM mode between the FM-MPX and FM-RDS input (see chapter 9.3.8 for more information). This pin has an internal pull down resistor and needs no external components because the applied signal is static (0V or 5V). Note that this pin is not used in the application diagram (appendix 12.1) and therefor left open.

FM-MPX (pin 80)

The basic circuit diagram of the FM-MPX input is depicted in figure 8.9.

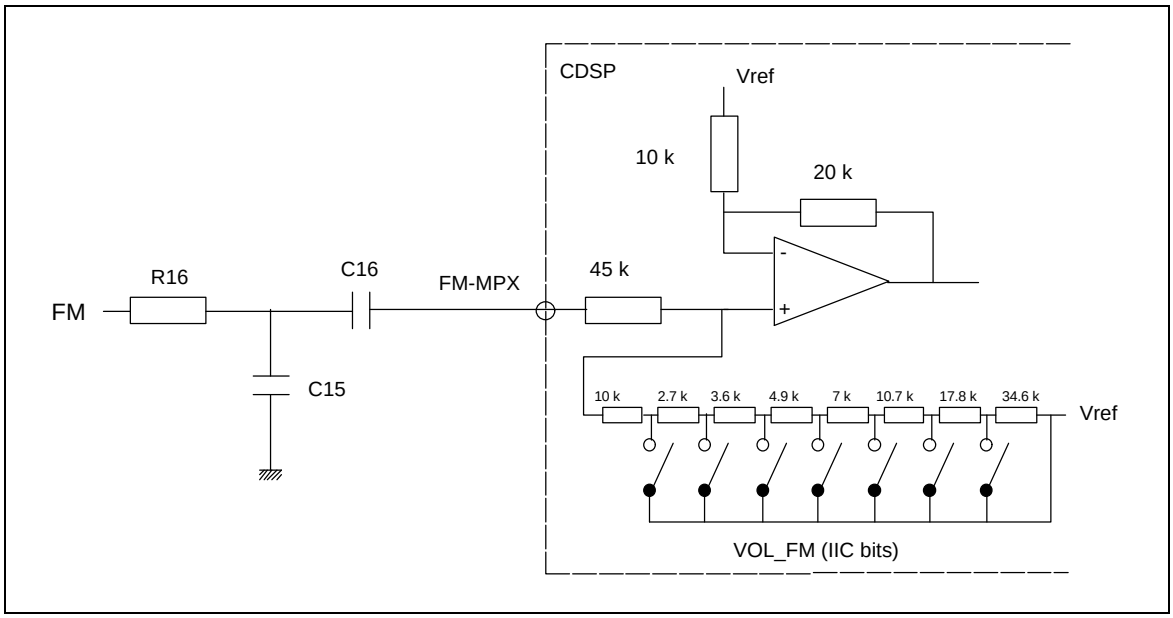


Fig. 8.9 FM-MPX input

The 1st order RC filter (R16 and C15) at the input of the FM-MPX pin has two functions:

- to avoid aliasing in the SCAD1 A/D convertor, that means that frequency components of $f > 1/2\ fs_{A/D}$ < 85 dB below the maximum input of the SCAD1 A/D convertor (figure for S/N for SCAD2 A/D convertor, mentioned in data sheet)

- to create a filter for the FM-MPX input with a cut-off frequency > 250 KHz

This filter is realised with R16=3.3 kΩ (± 10%) and C15=150 pF (± 10%) resulting in a cut-off frequency of 320 KHz (± 20%).

Remarks:
a) The source resistance is not taken into account because this R_{source} << 3K3 otherwise the cut-off frequency is affected.
b) The input resistance of the CDSP is not taken into account because this Rin is big (> 55 kΩ).
c) Concerning C15, X7R SMD capacitors are not allowed because they show some voltage dependency which causes extra distortion, therefore NP0 SMD capacitors are recommended.

8.3.2 FM input sensitivity selection

The FM input sensitivity is designed for tuner front ends which deliver an output voltage in the range 65 mV to 225 mV (af = 1 KHz, 22.5 KHz deviation). The input sensitivity can be changed in steps of 1.5 dB by means of 3 bits of the IIC_AD register ($0FFD) as also described in the datasheet.
The input impedance of the FM-MPX pin is also a function of the sensitivity setting.
The input sensitivity of the FM input with the required IIC settings and corresponding input impedance is listed in table 8.2

TUNER OUTPUT VOLTAGE (mV) at _f = 22.5 KHz	VOL_FM_2	VOL_FM_1	VOL_FM_0	FM INPUT IMPEDANCE
65	0	0	0	137 kΩ
78	0	0	1	103 kΩ
93	0	1	0	84.8 kΩ
111	0	1	1	74 kΩ
132	1	0	0	67 kΩ
158	1	0	1	62 kΩ
188 (default)	1	1	0	58.4 kΩ
225	1	1	1	56 kΩ

Table 8.2 FM input sensitivity and impedance

The capacitor C16 is applied to block any DC content of the incoming signal. The capacitor C16 forms with the Rin of the CDSP a high pass filter which must fulfil the following requirements:

- maximum leakage current < 0.5 µA, otherwise the specified dynamic range of the SCAD2 A/D convertor is limited by an offset voltage (I_{leak} * Rin_{max}=V_{offset}); 0.5 µA * 136K = 68 mV offset, compared to 0.66 Vrms input voltage this results in a loss of dynamic range of 0.85 dB.
- the cut-off frequency <= 5 Hz, a higher fc limits the maximum channel separation of FM due to phase shift at 19 KHz. In the CDSP application we use C16 = 680 nF (MKT).

8.3.3 IAC

The Interference Absorption Circuit (IAC) detects and eliminates audible clicks caused by impulsive interference on FM reception.The block diagram of the IAC is depicted in figure 8.10.

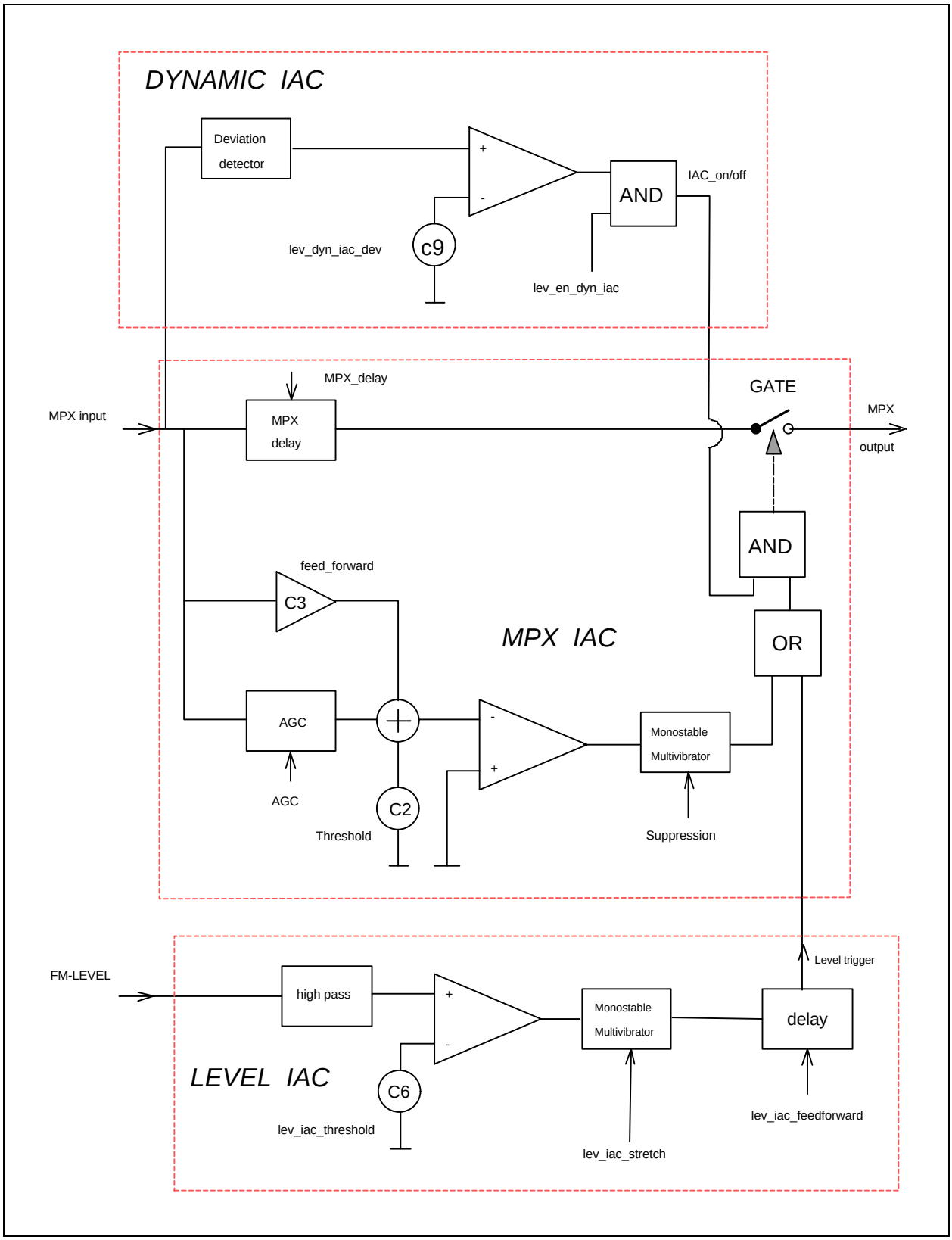


Fig. 8.10 Block diagram of IAC

The IAC consists of three circuits :

- MPX IAC
- Level IAC
- Dynamic IAC

The input signal of the MPX-IAC circuit is the MPX signal derived from the decimated output signal of the A/D convertor. The MPX signal is fed to a delay circuit followed a gate switch. This gate is activated by the interference detector which consists of a feed forward path, an AGC circuit, a comparator and a monostable multivibrator. The interference detector analyses the high frequency content of the MPX signal and discriminates between interference pulses and other signals. The mute switch interrupts the normal signal flow, during mute switch activation the output is held at a constant level which is obtained from a LPF. The MPX-IAC circuit performs optimally in higher antenna voltage circumstances.

The input signal of the Level IAC circuit is the FM level signal. This detector is added to the IAC circuit in order to further optimise the IAC performance at lower antenna voltage circumstances. This detection circuit is complementary to the MPX-IAC detection circuit.

The third IAC function is the Dynamic IAC circuit. This function is intended to switch OFF the IAC completely at the moment that the MPX signal has a too high frequency deviation. In case the frontend tuner has narrow IF filters a too high frequency deviation will result in AM modulation that could be interpreted by the IAC circuitry as interference caused by the car's engine. By enabling the Dynamic IAC function this false triggering will be avoided.

The characteristics of the IAC can be adapted to the properties of different FM tuners by means of the predefined coefficients in the hardware I2C registers **IIC_IAC** (address $0FFB) and **IIC_LEVEL_IAC** (address $0FFC), see tables 8.3 .. 8.12. The values can be changed via the I2C bus. On power on the nominal setting for a good performing IAC is selected (all IAC control bits set to there prefix value). Note that the Level IAC and the Dynamic IAC functions are switched off after power on.
There are in total 9 different coefficients which will be described in short.

AGC (bit 11 of IIC_IAC register)

In case the sensitivity and feed forward factor are out of range in a certain application, the set point of the AGC can be shifted.

Threshold (sensitivity offset) (bit 2,1,0 of IIC_IAC register)

Sets the threshold sensitivity of the comparator in the interference detector.
It also influences the amount of unwanted triggering.

feed_forward (bit 5,4,3 of IIC_IAC register)

Determines the reduction of the detector sensitivity. This mechanism prevents the detector from unwanted triggering at noise with modulation peaks.

Suppression (bit 8,7,6 of IIC_IAC register)

Sets the duration of the pulse suppression after the detector has stopped sending trigger pulses.

MPX_delay (bit 10,9 of IIC_IAC register)

Sets the delay time (between 2 and 5 samples of Fs=304 KHz) depending on the used front end of the car radio.

lev_iac_threshold (bit 3,2,1,0 of IIC_LEVEL_IAC register)

> Sets the sensitivity of the comparator in the ignition interference pulse detector.
> It also influences the amount of unwanted triggering. With the prefix value '0000' the Level IAC function is switched OFF.

lev_iac_feedforward (bit 5,4 of IIC_LEVEL_IAC register)

> This parameter allows to adjust for delay differences in the signal paths from the FM antenna to the MPX mute, namely via the FM level ADC and Level IAC detection and via the FM demodulator and MPX conversion and filtering. These differences depend on the used frontend tuner in the car radio.

lev_iac_stretch (bit 7,6 of IIC_LEVEL_IAC register)

> Sets the duration of the pulse suppression after the FM level input has stopped exceeding the threshold level.

lev_dyn_iac_dev (bit 14,13 of IIC_LEVEL_IAC register)

> If enabled by the lev_en_dyn_iac bit (bit 15 of the IIC_LEVEL_IAC register), this block will disable temporarily all IAC action in case the MPX signal exceeds a threshold deviation for a certain period of time.

A higher MPX IAC threshold means a lower overall trigger sensitivity, a higher deviation feed forward factor causes a lower trigger sensitivity at a non zero FM deviation. When the MPX IAC suppression stretch time is increased, the suppression of the MPX signal will last longer after the last pulse detection. Increasing the MPX delay causes that the suppression of the MPX signal begins and ends earlier, relative to the MPX signal itself. In case the sensitivity and feed forward factor are out of range in a certain application, the set point of the AGC can be shifted with parameter AGC set point; this decreases the overall sensitivity of the IAC circuit.

The more often and the longer the MPX signal is suppressed, the more distortion of the audio signal will be the result. In practice, the best setting of the parameters is obtained when the annoying interference pulses are eliminated and when the IAC reacts only little at noise and audio signals.
For the TEA6811/6824 tuner, the value codes **$0AED** for IIC_IAC register (address $0FFB) and **$E086** for IIC_LEVEL_IAC register (address $0FFC) showed a good performance, also on the road.

IAC testing

The internal trigger is visible on DSP-OUT2 (pin 41) if the IAC_trigger bit of the IIC_IAC control register is set (bit 15). In this mode the parameter settings on the IAC performance can be verified.

The IAC can be tested with the setup given in figure 8.11. The schematics of the interference simulation network (ISN) and the dummy antenna are given in figure 8.12 and 8.13 respectively.
The rise time of the pulse generator has to be faster than 5 nanoseconds. The loaded voltage amplitude must be circa 10 Volts. Note that the ISN attenuates the FM signal by circa 20 dB, so the RF signal output of the generator should be compensated for this.

Ignition interference of a four cylinder engine running at 6000 rev/min can be simulated by setting the frequency of the pulse generator at 100 Hz and the duty cycle at 50%. Note that the rising edge as well as the falling edge of the square wave causes a pulse in the RF signal to the receiver. When IAC is switched off, each 5 milliseconds a pulse can be expected in the audio signal. However, because of the random phase relation between the square wave and the FM signal, the amplitude of the pulses in the audio signal varies and can even be zero.

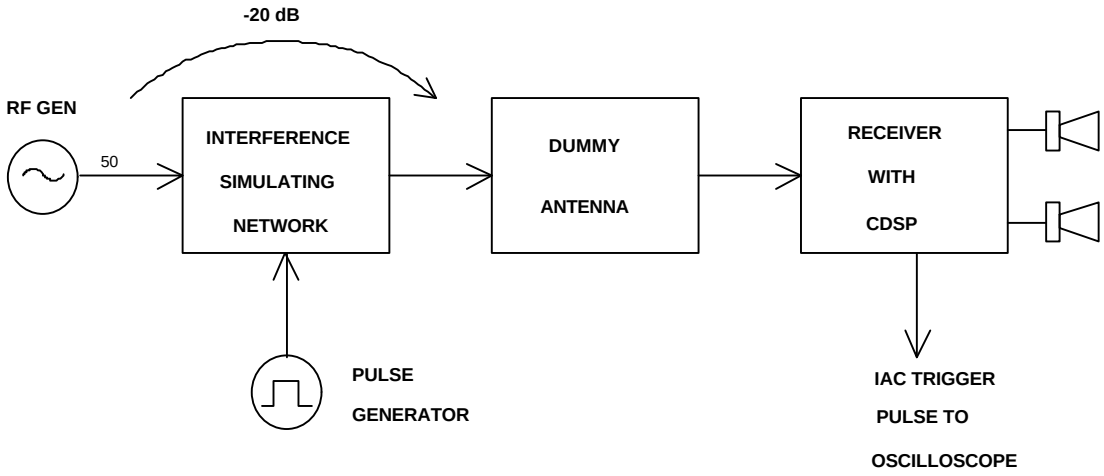


Fig. 8.11 IAC test setup

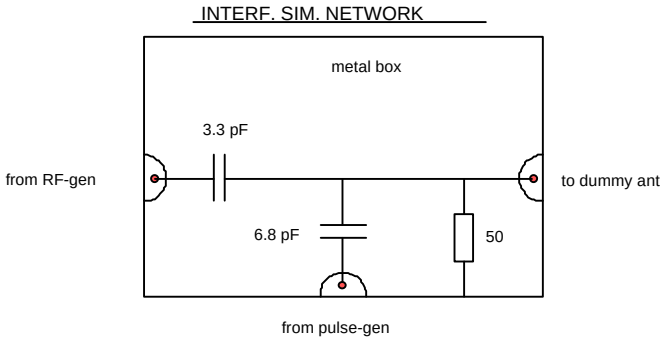


Fig. 8.12 ISN schematics

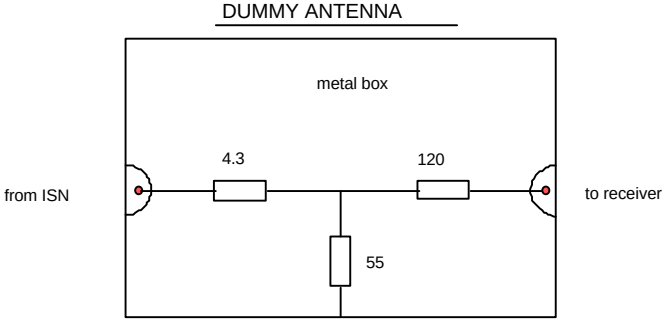


Fig. 8.13 Dummy antenna schematics

Optimisation procedure IAC parameters

Using the measurement set-up in figure 8.11, the parameters of the IAC can be optimized.
(all RF-voltages measured at the input of the dummy antenna. Signal to noise is relative to 22,5 KHz deviation).

The IAC characteristics can be adapted by means of the IAC control registers. These registers (IIC_IAC and IIC_LEVEL_IAC) contain the control bits that define the IAC parameters.
Tables with relation bit value <-> IAC parameter value are given in tables 8.3 .. 8.12.
For monitoring the IAC trigger pulse at pin DSP-OUT2 (pin 41), bit IAC_trigger of the IIC_IAC register ($0FFB) should be set to 1. See also the datasheet of the SAA7705H.

The complete IAC function can be optimised in three steps :

1) Optimise the MPX IAC
2) Optimise the Dynamic IAC
3) Optimise the Level IAC

1. Optimisation of the MPX IAC

Figure 8.14 gives a graphical presentation of the effect that the MPX IAC parameters have on the interference noise and MPX signal. The procedure to optimise the MPX IAC parameters is described below.

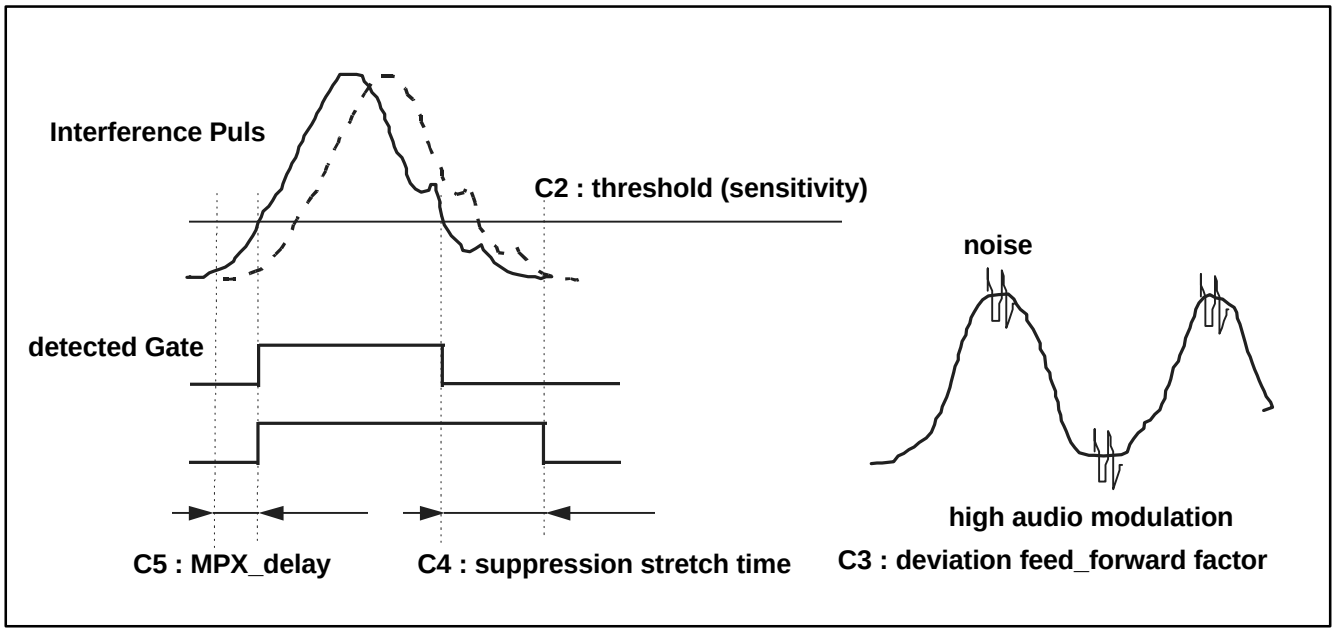


Fig. 8.14 Graphical presentation MPX IAC parameters

Switch OFF the Level IAC and Dynamic IAC functions (set bits 0,1,2,3 and 15 of the LEVEL_IAC control register $0FFC to '0').
The optimisation of the MPX IAC can be done by listening, optimise the parameters in the order as given below. Note that the optimisation procedure is iterative, in some circumstances it is needed to re-adjust an already optimised parameter in order to get the overall optimal results.

adjustment of IAC parameter : ***Threshold*** (sensitivity)
Use no ISN. No modulation. Set ***feed_forward*** to minimum (0.00000). By decreasing the RF voltage, the SNR decreases (some sputtering noise can be heard now). Changing ***Threshold*** causes unwanted trigger pulses. After increasing the RF voltage (which causes also SNR to increase), the unwanted trigger pulses should disappear. Increase of SNR due to unwanted trigger pulses has to be less than 1 dB, this requirement has to be met for any fieldstrength, this can be verified by comparing the audible noise in case of MPX IAC switched ON with the audible noise in case of MPX IAC switched OFF. The audible noise in case of switching ON the MPX IAC should not increase significantly.

adjustment of IAC parameter : ***feed_forward***
Use no ISN. Modulation: fmod=1 KHz, deviation=75 KHz. Choose the RF voltage amplitude so that some trigger pulses occur around the zero crossings of the audio signal. Adjust ***feed_forward*** to the value at which the number of unwanted trigger pulses around the peaks of the audio signal is about the same as the number around the zero crossings.

adjustment of IAC parameters ***Suppression*** and ***MPX_delay***
Use the ISN and create interfering pulses. Make the RF voltage so low that the IAC is still sensitive for pulses. (At lower voltages the IAC will be too sensitive for pulses because of the noise). At this RF voltage,the suppression time is shortest, so the timing of the beginning and the end of the suppression period is most critical. Set ***Suppression*** and ***MPX_delay*** to maximum. The beginning of an interference pulse or maybe the whole pulse is suppressed now. Reduce ***MPX_delay*** to the value at which the beginning of the pulse is still just eliminated. Then, reduce ***Suppression*** so much that the tail of the pulse is just suppressed well. The adjustment of ***Suppression*** and ***MPX_delay*** can be done by listening.

2. Optimisation of the Dynamic IAC

The Level IAC function should remain switched OFF; MPX IAC adjusted and switched ON.

adjustment of IAC parameter : ***lev_dyn_iac_dev***

Use no ISN. Set the RF voltage to 200 µV. Modulation: fmod=10 KHz, deviation= 22.5 KHz.
First switch OFF the Dynamic IAC. Increase the deviation until the MPX IAC starts (unwanted) triggering.
Now switch ON the dynamic IAC and set ***lev_dyn_iac_dev*** to maximum deviation (65 kHz).
Adjust (decrease) ***lev_dyn_iac_dev*** to the value at which the unwanted trigger pulses just disappear, now the highest deviation at which no unwanted triggering occurs is achieved.

3. Optimisation of the Level IAC

Switch OFF the Dynamic IAC.
MPX IAC adjusted and switched ON.

adjustment of IAC parameter : ***lev_iac_threshold***

Use ISN and create interfering pulses. NO modulation. Set ***lev_iac_threshold*** to maximum (0.5), ***lev_iac_feedforward*** to minimum (-2) and ***lev_iac_stretch*** to maximum (15). Apply a low RF voltage amplitude such that the MPX IAC stops triggering.
Decrease ***lev_iac_threshold*** until the Level IAC starts triggering. The sensitivity can be increased by further decreasing ***lev_iac_threshold*** but then also false triggering on audio can occur; this can be verified by removing the interfering pulses. Choose ***lev_iac_threshold*** such that there is no false triggering and that the Level IAC sensitivity is sufficient at a lower fieldstrength.

adjustment of IAC parameter ***lev_iac_feedforward*** and ***lev_iac_stretch***

Create interfering pulses and verify the audio output signal. Increase ***lev_iac_feedforward*** to the value at which the beginning of the interfering pulse is still just eliminated. Then, reduce ***lev_iac_stretch*** so much that the tail of the pulse is just suppressed well. The adjustment of ***lev_iac_feedforward*** and ***lev_iac_stretch*** can be done by listening.

IIC_IAC and IIC_LEVEL_IAC register definition

Table 8.3 **IIC_IAC register ($0FFB)**

NAME	BITS	DESCRIPTION	DEFAULT	BIT POS
Threshold	3	Threshold sensitivity (see table 8.5)	0.031	2,1,0
feed_forward	3	Deviation feed forward factor (see table 8.6)	0.0078	5,4,3
Suppression	3	Stretch time suppression (see table 8.7)	2 samples	8,7,6
MPX_delay	2	Delay settings MPX (see table 8.8)	5 periods	10,9
AGC	1	AGC set point 1/256 (1) or 1/128 (0)	1/256	11
Not used	3			14,13,12
IAC_trigger	1	IAC output (1) or DSP_OUT2 output selection (0)	DSP	15

Table 8.4 **IIC_LEVEL_IAC register ($0FFC)**

NAME	BITS	DESCRIPTION	DEFAULT	BIT POS
lev_iac_threshold	4	IAC level threshold setting (see table 8.9). At '0000' Level IAC is switched OFF	Level IAC off	3,2,1,0
lev_iac_feedforward	2	IAC level deviation feed forward factor (see table 8.10)	-2 periods	5,4
lev_iac_stretch	2	IAC level stretch time (see table 8.11)	13 periods	7,6
Not used				12-8
lev_dyn_iac_dev	2	the deviation threshold frequency setting of the dynamic IAC (see table 8.12)	00	14,13
lev_en_dyn_iac	1	enables FM frequency deviation dependent IAC (1)	0	15

Table 8.5 **MPX IAC threshold settings**

VALUE			THRESHOLD (DECIMAL VALUE)
Bit 2	**Bit 1**	**Bit 0**	
1	0	0	0.027
1	0	1	0.031 (prefix value)
1	1	0	0.038
1	1	1	0.047
0	0	0	0.055
0	0	1	0.063
0	1	0	0.074
0	1	1	0.085

Table 8.6 **MPX IAC Feed forward factor settings**

VALUE			FACTOR (DECIMAL VALUE)
Bit 5	**Bit 4**	**Bit 3**	
0	0	0	0.00146
0	0	1	0.00195
0	1	0	0.00293
0	1	1	0.00391
1	0	0	0.00586
1	0	1	0.00781 (prefix value)
1	1	0	0.01172
1	1	1	0.00000

Table 8.7 **MPX IAC Suppression stretch time**

VALUE			PULSE LENGTH ON SINGLE TRIGGER	STRETCH (# SAMPLES)
Bit 8	**Bit 7**	**Bit 6**		
0	0	0	0	N.A.
0	0	1	1	0
0	1	0	2	1
0	1	1	3	2 (prefix)
1	0	0	4	3
1	0	1	5	4
1	1	0	6	5
1	1	1	7	6

Table 8.8 **MPX IAC Delay settings**

VALUE		DELAY (DECIMAL VALUE) PERIODS OF 304 KHZ
Bit 10	Bit 9	
1	0	2
1	1	3
0	0	4
0	1	5 (prefix)

Table 8.9 **Level IAC threshold settings**

IIC VALUE				THRESHOLD (DECIMAL VALUE)
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	Level IAC off (prefix)
0	0	0	1	0.02
0	0	1	0	0.025
0	0	1	1	0.0316
0	1	0	0	0.04
0	1	0	1	0.05
0	1	1	0	0.063
0	1	1	1	0.08
1	0	0	0	0.1
1	0	0	1	0.126
1	0	1	0	0.16
1	0	1	1	0.2
1	1	0	0	0.25
1	1	0	1	0.316
1	1	1	0	0.4
1	1	1	1	0.5

Table 8.10 **Level IAC deviation feed forward factor**

IIC VALUE		DELAY (DECIMAL VALUE) IN PERIODS OF 304 KHZ
Bit 5	Bit 4	
0	0	-2 (prefix value)
0	1	-1
1	0	0
1	1	1

Table 8.11 **Level IAC stretch time**

IIC VALUE		PULSE LENGTH ON SINGLE TRIGGER IN PERIODS OF 304 KHZ
Bit 7	Bit 6	
0	0	9
0	1	11 (prefix value)
1	0	13
1	1	15

Table 8.12 **Dynamic IAC deviation threshold**

VALUE		DEVIATION [KHZ]
Bit 14	Bit 13	
0	0	42
0	1	48
1	0	58
1	1	65

8.4 AM-mono mode

AM-AF Left/Right (pin 66 and pin 67)

The basic circuit diagram of the AM-AF-L and AM-AF-R input is depicted in figure 8.15.

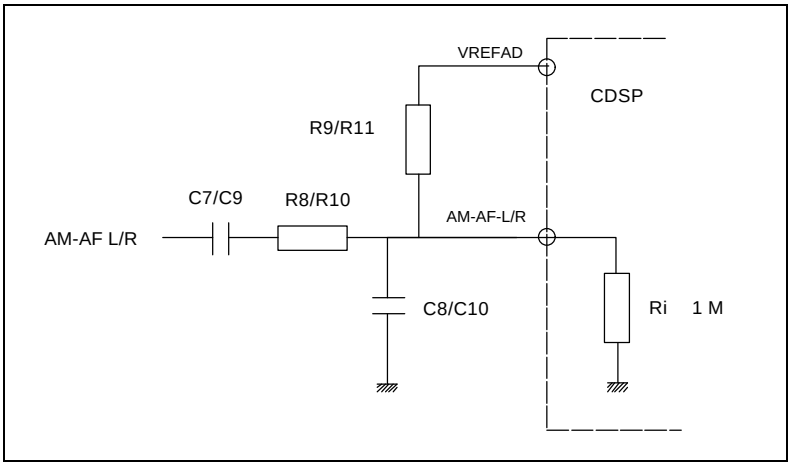


Fig. 8.15 AM-AF Left/Right input

The AM-AF Left/Right input pin requires a DC bias (VDDA/2), for this reason the AM-AF Left/Right input pin is connected with VREFAD via a 82 kΩ resistor (R9 and R11 respectively).
The resistor combinations R8, R9 and R10, R11 attenuates the input signal in order to match the AM output voltage of the tuner to the input range of the A/D convertor.
For the CDSP application the AM output voltage of the tuner is assumed to be about 1 Vrms max, R8 and R10 are 68 kΩ, this results in a voltage of 550 mV rms at the AF-AM Left/Right pins of the CDSP.

With R8, R9, C8 and R10, R11, C10 a first order low pass filter is realised at the Left and Right inputs respectively.
The cut-off frequency of this filter (Left channel example) is :

$$fc = \frac{1}{2.p.\frac{R8.R9}{R8+R9}.C8}$$

The 1st order filter at the input of the AM-AF Left/Right pins is to avoid aliasing in the SCAD1 and SCAD2 A/D convertors, that means that frequency components of f > 1/2 $fs_{A/D}$ < 90 dB below the maximum input of the A/D convertor (figure for S/N for AM-inputs mentioned in the data sheet).
The requirements are not critical though.
If R8/R10 = 68 KΩ (+/-10%) and C8/C10 = 100 pF (+/-10%), then the cut-off frequency fc = 42.8 kHz.

Remarks:
a) The source resistance is not taken into account because this R_{source}<< 150 KΩ otherwise the cut-off frequency is affected.
b) The input resistance of the CDSP is not taken into account because this Rin ≥ 1 MΩ.
c) Concerning C8/C10, X7R SMD capacitors are not allowed because they show some voltage dependency which causes extra distortion, therefore NP0 SMD capacitors are recommended.

The capacitor C7/C9 is applied to block any DC content of the incoming signal. The capacitor C7/C9 forms with R8+R9 / R10+R11 a high pass filter but there are no critical requirements.
For the CDSP application we use :
C7/C9 = 220nF (+/-10%) and Rin = 150 KΩ (+/-10%), resulting in a fc = 4.8Hz (+/-20%).

8.5 Tape mode

TAPE Left/Right (pin 68 and pin 69)

The tape input is for connecting a cassette deck.
The basic circuit diagram of the TAPE-L and TAPE-R input is depicted in figure 8.16.

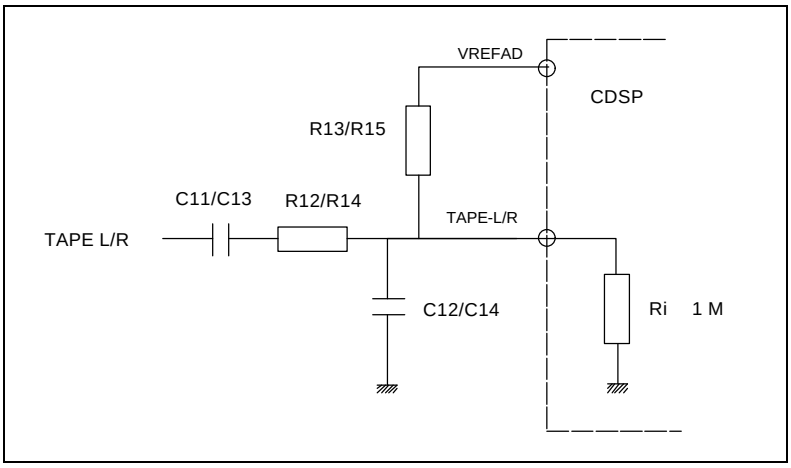


Fig. 8.16 Tape Left/Right input

The TAPE L/R inputs uses also SCAD1 and SCAD2 A/D convertors as can be seen in the block diagram of the input selection which is depicted in the data sheet. That means that these signals follow the same path as the AM Left/Right signals.

The input filtering for the Tape input is the same as for the AM input (see chapter 8.4),
with R12/R14 = 68 kΩ (± 10%) and C12/C14 = 100 pF (± 10%) a low pass input filter with cut-off frequency fc = 42.8 kHz is realised.

The capacitor C11/C13 is applied to block any DC content of the incoming signal. The capacitor C11/C13 forms with R12+R13 / R14+R15 a high pass filter but there are no critical requirements.
For the CDSP application we use :
C11/C13 = 220nF (± 10%) and Rin = 150 KΩ (± 10%), resulting in a fc = 4.8Hz (± 20%).

Remarks:
a) The source resistance is not taken into account because this R_{source}<< 150 KΩ otherwise the cut-off frequency is affected.
b) The input resistance of the CDSP is not taken into account because this Rin ≥ 1 MΩ.
c) Concerning C12/C14, X7R SMD capacitors are not allowed because they show some voltage dependency which causes extra distortion, therefore NP0 SMD capacitors are recommended.
d) In case the tape input signal is processed with Dolby-B the DSP program part Dolby-B has to be aligned which is also described in chapter 9.5.

8.6 CD-analog mode

CD Left/Right and Ground (pin 70, 71, 72, 73 and 77)

The analog CD input is for connecting the analog output signal of a CD player or CD-changer.
The input has a high level of common-mode rejection and thus eliminates ground noise.
The ground wire of the CD-cable has a separate input at the CDSP in order to realize the required level of Common Mode Rejection Ratio.
The basic circuit diagram of the analog CD-input is depicted in figure 8.17.

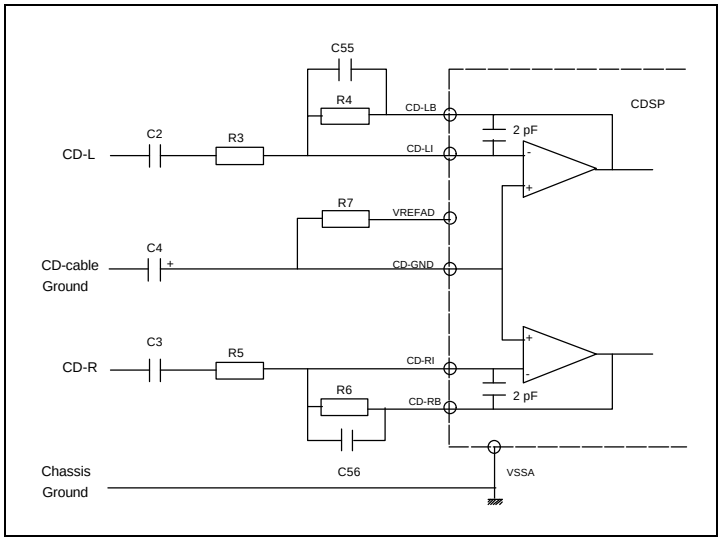


Fig. 8.17 Analog CD input

Low pass filter
The input stage of the analog Left/Right CD input consists of an opamp. The filtering of the incoming signal is a first order RC low pass filter realized with the external feedback resistors R4 and the feedback capacitor C55 for the Left channel input and with R6 and the feedback capacitor C56 for the Right channel input. The cut-off frequency (fc) of this filter (Left channel) is :

$$fc = \frac{1}{2.p.R4.C55}$$

In the CDSP application we use R4 = R6 = 8.2 kΩ (± 10%), in combination with the feedback capacitor C55 = C56 = 330 pF (± 10%), this results in a cut-off frequency fc = 58.8 KHz (± 20%).

Remarks:
The fixed internal feedback capacitor (2 pF) is small compared with the external feedback capacitor of 330 pF; the effect on the cut-off frequency can be neglected.
Note that pin CD_LI and CD_RI are virtual ground points, resistors R3 and R5 do not affect the cut-off frequency for this reason.

Variable gain
The gain of the Left- and Right input stages is adjustable and equals R4/R3 and R6/R5 respectively. The 0 dB output level of the input stage opamps is 0.55 Vrms. In the CDSP application we assume a level of 1 Vrms at the CD-L and CD-R input, the gain is adjusted by using R3 = R5 = 15 KΩ.
It is recommended only to change the resistor value R3 and R5 if a different input gain is required, R4 and R6 should remain about 8.2 KΩ for optimal CMRR characteristics.

CMRR

The chassis ground connection between the CD changer and the CDSP radio is not an ideal (zero impedance) signal return path, the common return path impedance Z_R is a source of interference coupling. Any currents flowing in the Chassis ground return path will produce potential differences between the chassis ground points at CD changer and CDSP radio. This voltage source V_{CM} is the common mode voltage, V_{CM} is present on all wires of the CD-cable. The CD input stage of the CDSP is designed for a high level of Common Mode Rejection. The CD-cable shield is connected with the signal ground in the CD-changer and via a high ohmic resistor to signal ground in the CDSP radio ;
the Common Mode voltage on the radio inputs CD_L, CD_R and CD-ground will be the same now and will be rejected by the input stage, see figure 8.18.

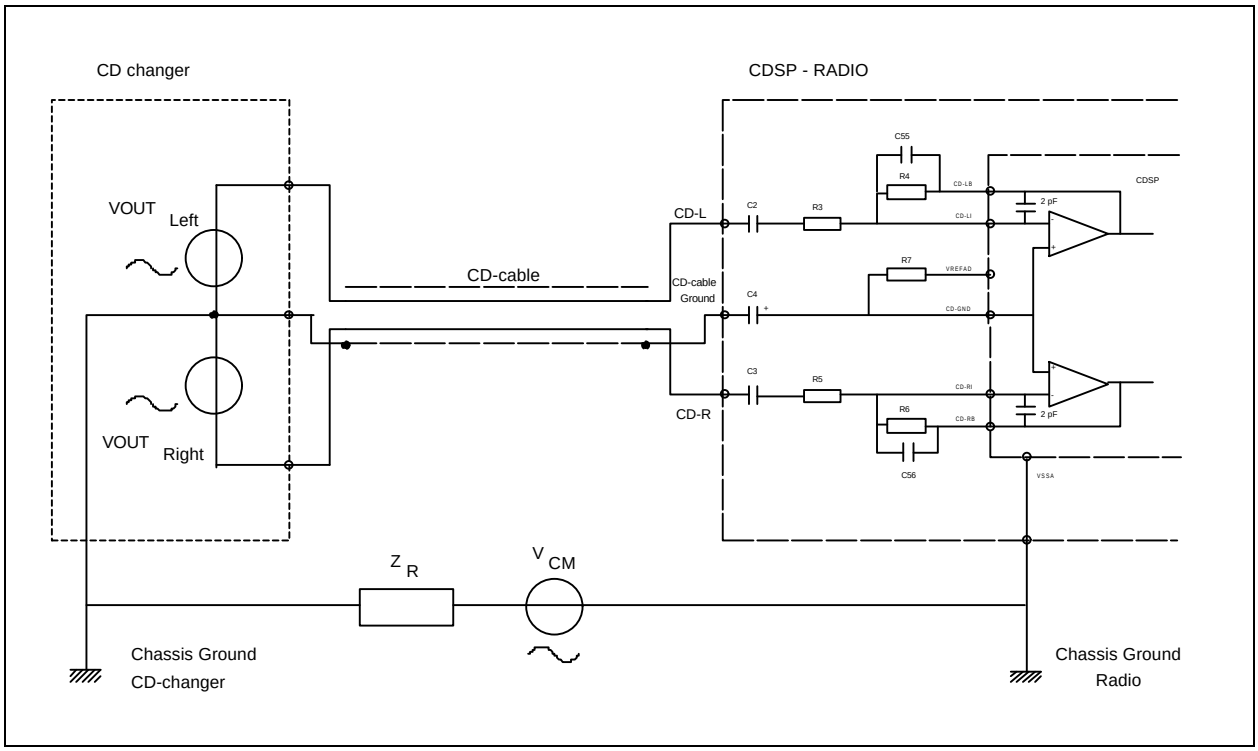


Fig. 8.18 Common Mode Rejection diagram

The input stage opamps get a DC-bias (VDDA2/2) via resistor R7 that is connected between pin CREFAD and pin CD_GND of the CDSP. Resistor R7 should be a very high ohmic because the CMMR of the circuit is determined by the ratio of R7 and the series impedance Z_R of the ground return path. In the CDSD application we use : R7 = 1 MΩ (± 10%).

If the return ground impedance in the connection to the CD changer is < 1 KΩ and R7 = 1 MΩ, then the Common Mode Rejection Ratio will be > 60 dB.

Remarks:

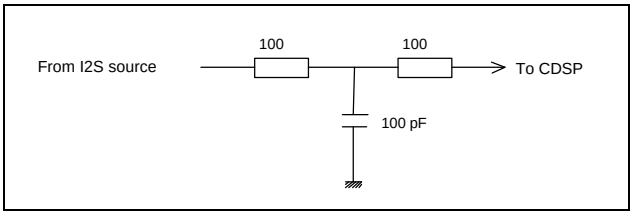
- The capacitors C2 and C3 are applied to block any DC content of the incoming signal. The capacitors C2/C3 forms with the R3/R5 a high pass filter. The cut-off frequency of this filter must be ≤ 15 Hz. With R3 = R5 = 15 KΩ this means C2/C3 ≥ 700 nF, in the CDSP application we use C2/C3 = 1 µF (± 10%).

- Capacitor C4 is applied to block the DC-bias voltage at the CD-GND pin, in the CDSP application we use C4 = 1 µF (± 10%).

8.7 CD-digital mode

I2S inputs **CD1-CL (pin 29), CD1-WS (pin 27), CD1-DATA (pin 28) and CD2-CL (pin 26), CD2-WS (pin 24), CD2-DATA (pin 25)**

The digital inputs CD-1 and CD-2 are capable of handling multiple input formats (I^2S and LSB-justified). If these inputs are not used they must be connected to ground as is indicated in the application diagram. If they are used then in every input line a T-filter must be used, see figure below.



The T-filter is used to avoid incoming and outgoing radiation (component tolerance of the T-filter is ± 20%). In case the I2S signals come from a device with slew rate controlled outputs, this T-filter might be unnecessary. Please note that this filter is optimised for a bitrate of 64*fs ; the rise- and fall times of the I2S signals will be too high when a higher bitrate is used, in this case the component values of the filter should be adapted in order to compensate for this.

If the I²S driver outputs of the external digital source IC's have Tri-state outputs, they can all be connected on one single I²S input. (not used outputs must be put in the high impedance mode).

Deemphasis input

The digital output signals from a CD player can be processed by activating the DSP programmed digital de-emphasis filter (see chapter 9.7).
The DSP-IN2 pin (pin 39) must be activated by a signal coming from a CD decoder circuit.
If this pin is used it needs an RC input filter as indicated in the application diagram (component tolerance is 20%).

8.8 General purpose tone generator mode

Not applicable.

8.9 MSS mode

Not applicable.

8.10 Speech mode

In the speech mode any Left- or Right input pin can be used to connect the speech source.
(for example AM-AF L, AM-AF R, CD-L or CD-R).
From a hardware point of view the inputs are the same as those described in the previous sections.

8.11 Radio Data System (RDS) function

RDS-clock and RDS Data (pin 59, 60)

These two pins needs for EMC reasons a RC filter in the input/output lines as is indicated in the application diagram. The components are not critical so a tolerance of 20% is tolerable.

FM-RDS (pin 79)

At this pin the FM signal of a second tuner can be applied but this possibility is not used in the current application.

8.12 Second processor extension function

For communication with external processors, delay lines or other I²S controllable devices a complete dual channel 18 bit output bus is implemented. The CDSP is acting as the master transmitter and the external device has to be synchronised with the word select line. As input for the processed data two data input lines have been implemented which are processed synchronously with the data output to the external processor. This enables in total a feedback of two stereo audio channels.

To the external processor, the DSP program should move data to the two Ext IIS DATA output registers, and read it back from the two or four Ext IIS DATA 1/2 input registers. The hardware of the bus can be enabled by setting the EN_HOST_IO bit of the IIC_HOST register. To minimise EMC, the output has to be disabled in case the output is not used.

I2S input/outputs: IIS_IN1 (pin 31), IIS_IN2 (pin 32), IIS_OUT1 pin(34), IIS_CLK (pin 30), IIS_WS (pin33)

When used, in the output lines of pin 30, 33 and 34 a T-filter must be applied (for EMC reasons) similar as for the digital CD input (chapter 8.7). The input lines of pin 31 and 32 don't need filtering.
The T-filter is not critical so a component tolerance of 20% is tolerable. Please note that this filter is optimised for a bitrate of 64*fs ; the rise- and fall times of the I2S signals will be too high when a higher bitrate is used, in this case the component values of the filter should be adapted in order to compensate for this.

8.13 Digital subwoofer and center output

The CDSP offers an additional dual channel 18 bit digital output for the use of a subwoofer and center output. Similar as the second processor extension function, the digital subwoofer output is capable of generating multiple output formats (I2S and LSB justified data formats). It is however not possible to select different data formats for the second processor and the subwoofer output.

The hardware of the bus can be enabled by setting the EN_HOST_IO bit of the IIC_HOST register.
To minimise EMC, the output has to be disabled in case the output is not used.

I2S outputs: IIS_OUT2 pin(35), IIS_CLK (pin 30) and IIS_WS (pin33)

When used, in the output lines of pin 30, 33 and 35 a T-filter must be applied (for EMC reasons) similar as for the digital CD input (chapter 8.7).
The T-filter is not critical so a component tolerance of 20% is tolerable.
Please note that this filter is optimised for a bitrate of 64*fs ; the rise- and fall times of the I2S signals will be too high when a higher bitrate is used, in this case the component values of the filter should be adapted in order to compensate for this.

External DAC
An external DAC should be applied to convert the digital subwoofer/center signal to an audible signal. Note that the output I2S bitclock (IIS_CLK) does have some out of the audio band noise-shaped jitter in the FM mode and the analog input modes with fs = 38 KHz ; in these modes the DCS is generating the 38 KHz based clock signals by a special dividing mechanism. The external DAC should be capable of handling this jittering I2S bitclock.

The TDA1387T (Stereo Continuous Calibrating DAC) can be applied to convert the digital subwoofer and center signal. Please note that due to the concept of this device an analog postfilter is required.
This postfilter can be a basic first order filter for the subwoofer output, for the center output however a higher order postfilter might be required in order to sufficiently attenuate the out of band output noise.

8.14 X-tal oscillator circuit

OSC_IN and OSC_OUT (pin 63 and pin 64)

The on chip crystal oscillator is a Pierce oscillator and is described in the data sheet.
The crystal is running in fundamental mode on 11.2896 MHz. Although a multiple of the crystal frequency falls within the FM reception band, this will not influence the reception because the crystal is driven in a controlled way.
The crystal oscillator circuit can operate both in master mode and in slave mode.
The blockdiagram of the X-tal oscillator circuit in master mode is depicted in figure 8.19.
The active element Gm compensates for the loss resistance of the crystal. The AGC circuit controls the gain of the oscillator and prevents clipping of the generated sine-wave and therefor minimises the higher harmonics.
The blockdiagram of the X-tal oscillator circuit in slave mode is depicted in figure 8.20.

In order to minimize feedback due to ground bounce the power supply connections of the crystal oscillator circuit are separated from the other power supply lines. It is absolutely necessary that the power supply line doesn't contain any spikes on it.

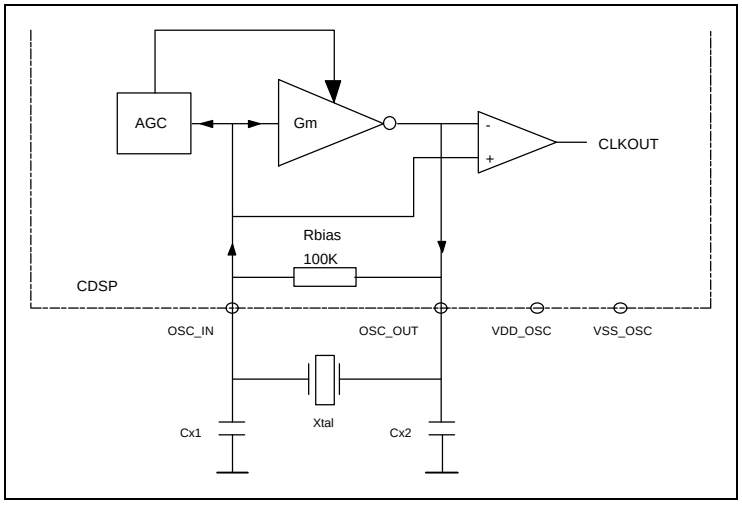


Fig. 8.19 Block diagram oscillator in master mode

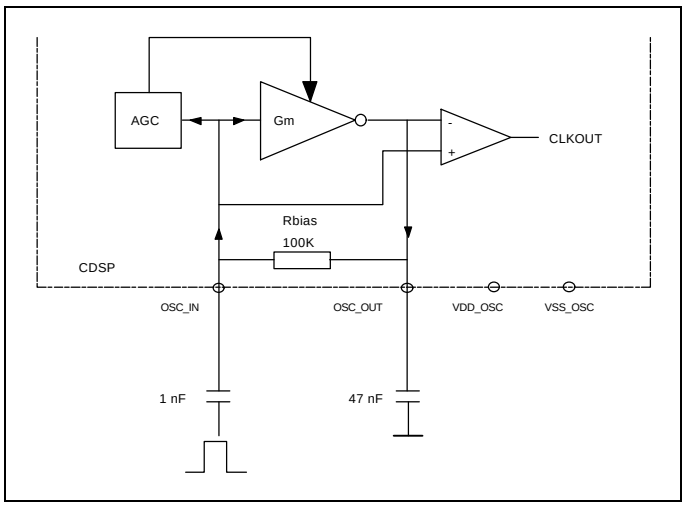


Fig. 8.20 Block diagram oscillator in slave mode

X-tal calculations

It can be shown that in order to start-up the transconductance of the active element must have a certain value $g_{m,A}$

$$g_{m,A} = 4\omega^2 RC^2_L$$

Where R is the loss resistance of the crystal and C_L is the load capacitance:

$$C_L = \frac{C_x1.C_x2}{C_x1 + C_x2} + C_p$$

C_{x1} and C_{x2} are the capacitors connected to either side of the crystal and C_p is the parasitic shunt capacitance of the crystal.

In the CDSP the minimum transconductance is 4 mA/V. In order to ensure start-up, the following inequality must hold:

$$w^2.R.C_L^2 < \frac{g_{m,\min}}{4}$$

Filling in the oscillation frequency of the CDSP (f_0 = 11.2896MHz) and $g_{m,min}$ one obtains:

$$RC^2_L < 1.99\ 10^{-19}$$

For example, if $C_{x1} = C_{x2}$ = 18pF and C_p = 5pF so that C_L = 14pF, the loss resistance R of the crystal must be smaller than 1000 Ω. However it is wise to take a safety margin of 30% because the above equations are approximations. In this example that would mean that the maximum loss resistance of the crystal (which is specified by the manufacturer) should not exceed 700 Ω.

The internal bias resistor R_{bias} is chosen high enough (100 kΩ) in order to prevent start-up problems.
A safe value for R_{bias} is

$$R_{bias} \ll \frac{1}{w_0^2 . R_s . C_p^2}$$

where ω_0 is the oscillation frequency, R_s is the resonator series resistance and C_p its parallel capacitance.

This means : R_{bias} >> 8 kΩ ; the value of 100 kΩ is sufficiently large.

8.15 External control pins

For external control two input pins have been implemented. The status of these pins can be changed by applying a logical level. The status of these pins is recorded in the internal status register of the DSP. The function of each pin is as follows:

DSP-IN1 (pin 38) Hard mute input and Hold FM filters (0 = mute) (only active in FM mode)

DSP-IN2 (pin 39) This pin activates the de-emphasis filter for CD (1 = de-emphasis on)
Also used to freeze level, noise and multipath information during RDS updates (0 = freeze).

To control external devices two output pins are implemented. The status of these pins is controlled by the DSP program. The functions of these pins are the following :

DSP-OUT1 (pin 40)	Indicates if an FM broadcasting is in stereo (1 = stereo) indication
DSP-OUT2 (pin 41)	Indication of a pause in FM or tape search mode (1 = pause). Also IAC trigger output for IAC alignment if the corresponding I²C bit is set.

All these input/output pins need an RC filter in the input/output lines for EMC reasons. In the application diagram such a filter is added for pin 38,39,40 and 41. This filter is not critical so a component tolerance of 20% is tolerable.

SCL (pin 57), SDA (pin 58)

These two pins needs a RC filter in the input/output lines for EMC reasons, as is indicated in the application diagram. The components are not critical so a tolerance of 20% is tolerable.

8.16 EMC measures

In order to optimise the EMC behaviour of the SAA7705H device, some measures are taken in the SAA7705H design :

1. On-chip decoupling capacitor ; this reduces the high frequency components of the supply currents.

2. Distributed clock ; the switching moments of the digital circuitry is spread in time.

3. Adjustable PLL frequency; this enables to change core frequency under microprocessor control in case FM receiption is interfered by the SAA7705H emission.

To further optimise the EMC behaviour of the SAA7705H in a CDSP application, some additional measures are required. The application diagram as given in appendix 11.1 complies with the recommended EMC measures described below.

It is important to realize that the required EMC measures strongly depend on the EMC characteristics of the total application of which the SAA7705H is part. Some EMC measures might not be required for a specific application. For example in an application in which the physical distance between the SAA7705H chip and the tuner circuitry is relatively small, the filtering of I/O pins might be more important in order to minimise self-pollution, whereas in an application in which the physical distance between the SAA7705H chip and the tuner circuitry is relatively high, I/O filtering might be unnecessary. An other point of concern is the radiated emission of the radio set with SAA7705H, the use of I/O filtering might be necessary if the shielding effectiveness of the radio housing is poor or when the SAA7705H chip is positioned close to a physical opening in the housing.

The given application diagram and the PCB layout in appendix 12.1 and 12.3 should therefore be seen as an example. The EMC measures taken into account in the application diagram, in order of importance, are :

1. <u>Supply filtering digital circuitry</u>
   The EMC most critical supply pins are VDDD3V1, VDDD3V2, VDDD3V3 and VDDD3V4. Via these pins the core is supplied, so the bulk of the digital current is flowing through these pins. To suppress interferences with the LW reception, a 22 μF capacitor (C53) is added.

2. Main ground plane
   The pinning of the CDSP chip has been chosen in such a way that the lay-out is possible with a double sided PCB. It is recommended to create a ground plane on the non-SMD side of the PCB. This main ground plane provides a low inductance ground return for the power supply and signal currents. This plane act as an equipotential point for the digital as well as for the analog parts of the CDSP circuitry. The EMC critical peripheral components should be above the plane.

3. Ground plane under the CDSP chip
   It is recommended to provide a ground plane under the CDSP chip at the SMD side of the PCB. The seven ground pins (VSSD) of the digital related signals and the oscillator ground pin (VSS-OSC) have to be connected directly to this plane in order to reduce the loop area of the digital supply, this reduces the EMC emission and ground bounce. This small ground plane has to be connected to the main ground plane with sufficient vias. Do not use the small ground plane under the chip for the other ground pins, these have to be directly connected to the main ground plane.

4. Oscillator circuit
   Mount the oscillator peripheral components (X1, C21 and C22) as close as possible to the CDSP chip.
   The oscillator supply is very susceptible for RF signals. For this reason the VDD-OSC pin must not be directly connected with the VDDD5V pins. The oscillator supply is separately filtered with components C20 and L1.

5. I/O filtering
   Each interconnection wire from the CDSP chip area to the environment is a possible EMC source. In order of importance filtering might be required for :
   - digital output signals
   - digital input signals
   - analog output signals

   In the application diagram the following measures have been taken :

   - first order RC-filtering of the digital signals RDS-Clock (R19 and C19), RDS-Data (R18 and C18), SCL (R20 and C23), SDA (R21 and C24), DSP-IN1 (R23 and C26), DSP-IN2 (R24 and C27), DSP-OUT1 (R25 and C28) and DSP-OUT2 (R26 and C29).

   - first order RC-filtering of the analog output signals Front-Left (R27 and C37), Front-Right (R28 and C38), Rear-Left (R29 and C39) and Rear-Right (R30 and C40).

The I2S input signals for CD1 and CD2 (CD1-CL, CD1-WS, CD1-DATA, CD2-CL, CD2-WS and CD1-DATA) and the I2S signals (IIS-OUT1, IIS-OUT2, IIS-IN1, IIS-IN2. IIS-CLK and IIS-WS) are not used in the application diagram.
If these signals are used in the application, a T-filter is recommended (as indicated in section 8.8).
The incoming I2S signals should be filtered in the external transmitter (f.i. the CD-changer) ; the outgoing I2S signals should be filtered in de radio set with SAA7705H.

note: it is important to place the capacitors of the I/O filters at the edge of the main ground plane and their connection to the ground plane should be as short as possible.

Furthermore it is important to separate the supply of the digital circuitry from the supply of the analog circuitry. For this reason the filter components L2 and L3 are added.
For sufficient bulk capacity, C51 and C53 are added.

9 Software application of the CDSP

9.0 General

9.0.1 Notations and definitions

a) This chapter contains several formula's and it is important to know that the calculation results are fractions. These fractions have to be converted in 12 bit or 18 bit 2's complement hexadecimal values in the following way:
HEX number = HEX[Fraction*2048]⌊ (12 bit representation in 2's complement notation)
HEX number = HEX[Fraction*131072]⌊ (18 bit representation in 2's complement notation)
HEX values are truncated to 12 or 18 bits. Negative HEX numbers are truncated to the relevant digits e.g. $FFFF12 = $F12.

Throughout this user manual a 12 bit value is indicated by a "$" and an 18 bit value is indicated by a "#".

Examples:	0.45*2048 =	921.6 =	$399
	-0.45*2048 =	-921.6 =	$C67
	0.82*131072 =	107479.04 =	#1A3D7
	-0.82*131072 =	-107479.04 =	#E5C29

b) The standard representation for names and default values of coefficients and data throughout this usermanual is:

Label	**Default value**	**; comment**
Y:SMTC	$7FF	; coefficient in YRAM with max. 12 bit HEX value, fraction = 0.999511
Y:STRC	$800	; max. 12 bit HEX negative, fraction = -1.0
X:LEVA	#1FFFF	; data value in XRAM with max. 18 bit HEX value, fraction = 0.99999237
X:MLTFLIM	#20000	; max. 18 bit HEX negative, fraction = -1.0

c) Sometimes a number has to be represented in double precision (especially in the audio processing). The procedure is as follows:

HEX number = HEX[Fraction*8388608]⌊ (24 bit representation in 2's complement notation)
HEX number = HEX[Fraction*34359738368]⌊ (36 bit representation in 2's complement notation)

Example for 24 bits representation:
$0.9815162 = 7DA252_H$
Storing this value in memory as two 12 bits numbers is done by splitting the hex number into two 12 bits words: high_part:$7DA and low_part:$252
The low_part must be shifted by one bit (MSB bit always zero). Low_part becomes then $129.
So $7DA252_H$ is stored as $7DA and $129 in memory.

$-0.48549039 = C1DB73_H$ is represented as $C1D and $5B9 in memory.

The 36 bit representation for Data is seldom used.
The procedure is similar as the one described for 24 bits representation. Splitting the 36 bits word into two 18 bits words, followed by shifting the low_part by one bit.

d) Full scale or F.S. is the maximum positive value for XRAM and YRAM.
The fractional value for F.S. is 1

e) Fs means audio sample frequency. For all analog inputs fs=38 KHz or 44.1 KHz and for digital inputs fs=32, 44.1 or 48 KHz. The DSP is synchronized with the WS signal of the selected source.

f) The address registers and modulo registers are treated as register pairs, and the contents of these register pairs can be saved and restored to and from memory. In order to save instruction cycles, the contents of these register pairs are transferred to/from memory in a concatenated way.
As a consequence, a save or a restore operation just requires a single instruction cycle.

The address value RX (RY) ranges from $00 till $FF (8 bits R7..R0) (lower bank)
and from $100 till $17F (9 bits R8..R0) (upper bank).

The modulo value MX (MY) ranges from $00 till $7F (7 bits M6..M0),
so only an address range RX (RY) from maximum $00 till $7F, from maximum $80 till $FF or from $100..$17F can be selected.
Please take note that bit R8 - deciding between lower or upper bank can't be stored.

The value of RMX (RMY) pointer is stored as an XMEM value (18 bits) (bits P17..P0) as follows:

```
P P P P  P P P P P P P P  P P P P P P
17  15   13  11  9   7    5   3   1
  16  14   12  10  8   6  5 4   2   0

0 0 0 x  x x x x x x x x  x x x x x x   <- RMX pointer 18 bits

       M  R R R R R R R R  M M M M M M
       6  7 6 5 4 3 2 1 0  5 4 3 2 1 0

                           ----------    6 LSB bits modulo value
          ---------------                8 bits address value
       -                                 (1) MSB bit modulo value
```

Example:
RX= $A2, MX= $44 => 000 1 10100010 000100= 00 0110 1000 1000 0100= #06884
RX= $135, MX= $4 => 000 0 00110101 000100= 00 0000 1101 0100 0100= #00D44

So the XMEM containing this RMX pointer must be loaded with above calculated value.

9.0.2 Hardware configuration of the SAA7705H

Some hardware functions of the SAA7705H are configurable under microprocessor control via the I2C interface; this makes the SAA7705H a flexible device that can be adapted to the properties of the radio set. The following hardware functions are configurable :

Analog inputs :
- input sensitivity FM-MPX and FM-RDS tuner inputs
- one/two tuner configuration
- sample frequency CD/Tape/AM inputs : 38 KHz or 44.1 KHz

Digital (I2S) inputs :
- data format selection : Standard I2S or LSB justified

Digital (I2S) outputs :
- data format selection (independent from digital input format) : Standard I2S or LSB justified
- output bitrate : 256 fs, 128 fs or 64 fs
- enable/disable digital outputs

Equalizer :
- two channel / four channel configuration

Phase Locked Loop :
- selectable DSP-core frequency

RDS demodulator :
- buffered / unbuffered configuration

IAC :
- AGC setting
- threshold
- deviation feed forward factor
- suppression stretch time
- MPX delay

All the hardware functions above are controlled by one or more bits of IIC control registers.
The SAA7705H has 8 IIC-Control registers, in general all registers should be set when putting the device in on of the operating modes. After setting of the IIC control registers the mode can be activated conform the procedure as given in section 9.0.2.3.
See the SAA7705H datasheet for a detailed overview of the I2C register contents.
After reset the I2C register contents will be the default value as specified in the datasheet.
The IIC-Control registers of the SAA7705H are given in table 9.1.

IIC-register	address
DCS_ConTRol	$0FFF (absolute)
DCS_DIVide	$0FFE (absolute)
AD	$0FFD (absolute)
LEVEL_IAC	$0FFC (absolute)
IAC	$0FFB (absolute)
SELection	$0FFA (absolute)
HOST	$0FF9 (absolute)
RDS_ConTRol	$0FF3 (absolute)

Table 9.1 Location IIC Control Registers SAA7705H

RDS_ConTrol register ($0FF3) settings

Selected defaults :

RDS-AD for RDS decoder input (bit 9 = 0)

RDS_ConTrol ($0FF3)	
RDS-output mode	
Buffered	Unbuffered
$0100	$0000

Table 9.2 RDS_ConTrol register settings

DCS & PLL settings

The divide factor of the PLL determines the frequency of the DSP clock and other derived clocks. One (default) divide factor is recommended to use for the SAA7705H, resulting in a DSP clock frequency of 27.1656 MHz.
The clock for DCS is also derived from the PLL block, the DCS parameters are therefore a function of the PLL frequency. The PLL divide factor and the corresponding DCS parameters are given in table 9.3. The parameter fx is the PLL frequency, the DSP clock frequency is equal to fx/2.

fx [MHz]	F0	F1	DCS_COEF	gain_h_l	PLL_DIV (3,2,1,0)
54.3312	$3	$2	$28ED	1	1010

Table 9.3 DCS & PLL settings

Other DCS settings :

- locked_preset : locked in FM-mode, preset in all other modes
- ISN clock on/off : On in FM-mode, Off in all other modes
- Loopo : switched off (no external ceramic DCS filter applied)

DCS_ConTRol and DCS_DIV register settings

The PLL divide factor and the DCS parameters in table 9.3 are used to determine the contents of the DCS_ConTRol and DCS_DIVide registers for the functional operating modes. See table 9.4.

Note that the DCS parameters for the analog input modes running at asf=44.1 Khz are set to the parameter values required for asf=38 Khz; this means that for asf=44.1 KHz the DCS keeps running at 38 KHz, this enables RDS demodulation. The clock signals for the Audio A/D and decimation path based on 44.1 KHz processing are directly derived from the Xtal-oscillator and not from the DCS.
In the digital input modes the DCS is also running at 38 KHz (preset mode, free running), this enables RDS demodulation in the digital input modes as well.

fx = 54.3312 MHz (f_{clock} = 27.1656 MHz)

Mode	asf [KHz]	DCS_ConTROl $0FFF	DCS_DIV $0FFE
FM	38	$5323	$28ED
Speech (via AM_L input)	38	$D223	$28ED
AM/Tape/CD_A	38 44.1	$D223 $D223	$28ED $28ED
CD_D/DCC_D	32 38 44.1 48	$D223 $D223 $D223 $D223	$28ED $28ED $28ED $28ED

Table 9.4 DCS_ConTROl & DCS_DIV register settings for fx = 54.3312 MHz

AD register ($0FFD) settings

With the AD register a configuration with one or two tuners can be selected, assumed is a one tuner configuration. Furthermore the input sensitivity of the FM-AD and RDS-AD can be set with this register. The input sensitivity is set to 200 mV (@ 22.5 KHz deviation) for both the FM-AD and RDS-AD, this is the TEA6811/6824 tuner compatible setting.
Bit 11 of the AD register is reserved for future applications and will be used to double the PLL output frequency. For the current SAA7705H application this bit must be set to 0 (no doubling).

The AD register contents now only depends on the equalizer configuration, and is not a direct function of the selected operating mode. See table 9.5.

Equalizer configuration	Two channel	$106C
	Four channel	$006C

Table 9.5 AD register settings

LEVEL IAC register ($0FFC) settings

The LEVEL IAC register contains the settings for the Level IAC and the Dynamic IAC functions, both are new functions for SAA7705H. The optimal setting for these functions has to be adjusted to the applied front-end tuner, see chapter 8.3.3 of this manual for detailed information about the IAC functions and adjustment procedures. The LEVEL IAC function is switched OFF when the register contents is $0000. The LEVEL IAC and Dynamic IAC are switched ON and set to their optimal values in combination with the TEA6811/6824 tunermodule with register contents **$E086**.

IAC register ($0FFB) settings

For the FM-mode the setting for a good performing IAC in combination with the TEA6811/6824 tuner the IAC register should be set to **$0AED** (this is the optimal setting of the IAC register for SAA7705H in combination with the TEA6811/6824 tuner).

For all other modes the contents of the IAC register is don't care because the ISN path is not used and switched off in this case. So the IAC register has be to initialized only once and the register contents can remain unchanged for all modes.

SELection register ($0FFA) settings

Except the input selector, the SELection register also controls other functions like the hardware DC-filter on/off switch and the decimation filter bandwidth setting.

Other assumed defaults are :

* bit 13 (inv_host_ws) : set to 0 (non-invert) for all modes.
* bit 12 (sel_nsdec) : set to 1 (1:8 wide band noise filter).
* bit 11 (adc_src) : set to 0 (audio-AD compensation) for all modes.
* bit 9 (DC-offset) : set to 0 (DC-offset ON) for all modes.
* bit 8 (bypass_pll) : set to 0 (PLL active) for all modes.
* bit 7 (sel_def) : set to 0 (29 KHz) for all modes (SELLEV mode not used anymore).
* bit 6 (wide_narrow) : set to 1 (audio; narrow) for all modes.
* bit 5 (sel_lev_am/fm) : set to to 0 for other modes (combined AM/FM level output from tuner assumed).

SEL-register settings for functional operating modes :

Mode	**asf** [KHz]	**SEL ($0FFA)**
FM	38	$1048
AM	38	$1044
Tape	38	$1040
CD-Analog	38 44.1	$104A $904A
SPEECH (via AM_L)	38	$1044
CD1_D	38,44.1,48	$1048
CD2_D	38,44.1,48	$1048

Table 9.6 SEL register settings

HOST register ($0FF9) settings

The HOST-register configures the AUDIO register selection and data format, and configures the CLOOP block (data format digital data outputs). The audio source- format selection is a function of active input mode, the Host_IO format and CLOOP_mode is a function of required digital output data format (if external I2S is enabled).
The following tables show the HOST-register settings per group of operating modes, as a function of digital output data format.
For the Digital input modes (CD1 and CD-2) CLOOP is set to Bypass WS in order to prevent any delay between WS input and WS output. In all other modes the CLOOP-mode is set to output WordSelect duty-cycle of 50% in order to transformate the non 50% duty cycle of the ISN Wordselect signal form stereo decoder and Audio AD into a 50% output WS dutycycle.

HOST ($0FF9) for FM mode				
External I2S / I2S output line driver				
Disabled	Enabled			
	output bitclock			
	64*fs	128*fs	256*fs	Output format
$0020	$D020	$B020	$9020	Standard I2S
	$D420	$B420	$9420	Japanese, LSB justified, 16 bits
	$D820	$B820	$9820	Japanese, LSB justified, 18 bits
	$DC20	$BC20	$9C20	Japanese, LSB justified, 20 bits

Table 9.7 HOST register settings for FM-mode

HOST ($0FF9) for AM, Tape, CD_A, SPEECH VIA AM_L				
External I2S / I2S output line driver				
Disabled	Enabled			
	output bitclock			
	64*fs	128*fs	256*fs	Output format
$0000	$D000	$B000	$9000	Standard I2S
	$D400	$B400	$9400	Japanese, LSB justified, 16 bits
	$D800	$B800	$9800	Japanese, LSB justified, 18 bits
	$DC00	$BC00	$9C00	Japanese, LSB justified, 20 bits

Table 9.8 HOST register settings for AM/Tape/CD_A/Speech modes

	HOST ($0FF9) for CD_1 mode				
	External I2S / I2S output line driver				
	Disabled	Enabled			
		output bitclock = input bitclock/N			
Input format		N = 1	N = 2	N = 4	Output format
Standard I2S	$0240	$1240	$3240	$5240	Standard I2S
		$1640	$3640	$5640	LSB just, 16 bits
		$1A40	$3A40	$5A40	LSB just, 18 bits
		$1E40	$3E40	$5E40	LSB just, 20 bits
Japanese, LSB justified, 16 bits	$00C0	$10C0	$30C0	$50C0	Standard I2S
		$14C0	$34C0	$54C0	LSB just, 16 bits
		$18C0	$38C0	$58C0	LSB just, 18 bits
		$1CC0	$3CC0	$5CC0	LSB just, 20 bits
Japanese, LSB justified, 18 bits	$0140	$1140	$3140	$5140	Standard I2S
		$1540	$3540	$5540	LSB just, 16 bits
		$1940	$3940	$5940	LSB just, 18 bits
		$1D40	$3D40	$5D40	LSB just, 20 bits
Japanese, LSB justified, 20 bits	$01C0	$11C0	$31C0	$51C0	Standard I2S
		$15C0	$35C0	$55C0	LSB just, 16 bits
		$19C0	$39C0	$59C0	LSB just, 18 bits
		$1DC0	$3DC0	$5DC0	LSB just, 20 bits

Table 9.9 HOST register settings for CD_1 mode

	HOST ($0FF9) for CD_2 mode				
	External I2S / I2S output line driver				
	Disabled	Enabled			
		output bitclock = input bitclock/N			
Input format		N = 1	N = 2	N = 4	Output format
Standard I2S	$0260	$1260	$3260	$5260	Standard I2S
		$1660	$3660	$5660	LSB just, 16 bits
		$1A60	$3A60	$5A60	LSB just, 18 bits
		$1E60	$3E60	$5E60	LSB just, 20 bits
Japanese, LSB justified, 16 bits	$00E0	$10E0	$30E0	$50E0	Standard I2S
		$14E0	$34E0	$54E0	LSB just, 16 bits
		$18E0	$38E0	$58E0	LSB just, 18 bits
		$1CE0	$3CE0	$5CE0	LSB just, 20 bits
Japanese, LSB justified, 18 bits	$0160	$1160	$3160	$5160	Standard I2S
		$1560	$3560	$5560	LSB just, 16 bits
		$1960	$3960	$5960	LSB just, 18 bits
		$1D60	$3D60	$5D60	LSB just, 20 bits
Japanese, LSB justified, 20 bits	$01E0	$11E0	$31E0	$51E0	Standard I2S
		$15E0	$35E0	$55E0	LSB just, 16 bits
		$19E0	$39E0	$59E0	LSB just, 18 bits
		$1DE0	$3DE0	$5DE0	LSB just, 20 bits

Table 9.10 HOST register settings for CD_2 mode

Combined mode table SAA7705H

Mode	**asf** [KHz]	**DCS_ConTRol** $0FFF	**DCS_DIVide** $0FFE	**AD** $0FFD	**LEVEL_IAC** $0FFC	**IAC** $0FFB	**SEL** $0FFA	**HOST** $0FF9	**RDS_ConTRol** $0FF3
FM	38	$5323	$28ED	$006C [1)]	$E086	$0AED	$1048	table 9.7	$0000 [2)]
AM	38	$D223	$28ED	$006C [1)]	$E086	$0AED	$1044	table 9.8	$0000 [2)]
Tape	38	$D223	$28ED	$006C [1)]	$E086	$0AED	$1040	table 9.8	$0000 [2)]
CD-A	38 44.1	$D223 $D223	$28ED $28ED	$006C [1)] $006C [1)]	$E086 $E086	$0AED $0AED	$104A $904A	table 9.8 table 9.8	$0000 [2)] $0000 [2)]
SPEECH (via AM_L)	38	$D223	$28ED	$006C [1)]	$E086	$0AED	$1044	table 9.8	$0000 [2)]
CD1_D	38 44.1 48	$D223	$28ED	$006C [1)]	$E086	$0AED	$1048	table 9.9	$0000 [2)]
CD2_D	38 44.1 48	$D223	$28ED	$006C [1)]	$E086	$0AED	$1048	table 9.9	$0000 [2)]

Table 9.11 Combined mode table SAA7705H for fx = 54.3312 MHz

Notes : 1) See table 9.5 for other settings 2) See table 9.2 for other settings

9.0.3 Operation modes and functions

This chapter gives a short functional description of the CDSP software program, the selection of the different operation modes and the downloading of the coefficient sets.

9.0.3.1 Functional description of the Main program

The CDSP main program can be set in 9 different operation modes. In each mode functions are executed which are common for **all modes** and functions which are required for that **particular mode** only.

The functions common for all modes are:

- Audio Processing block (not executed during waitloop after RESET):
    - Treble and bass control
    - Volume, balance and fader
    - Soft Audio Mute
    - (Hardware) parametric equalizer (4*5 or 2*10 bands)
    - Bass boost or loudness
    - Quasi peak detectors for (audio) output monitoring
    - General purpose tone generator
    - Subwoofer
- AM or FM Signal Quality information for the system controller and for AM and FM signal processing :
    - adjustment of the FM or AM level information to a normalized curve
    - normalized and filtered level information
    - fast multipath detection (not for AM)
    - average multipath information for the controller (not for AM)

Selectable modes and required functions

1 Idle_Audio mode:is automatically selected after leaving wait loop from RESET and has to be used during mode switching

- Performs all common audio functions.
  Sets all DAC outputs to zero except in the case that the Tone generator is selected

2 FM mode : mode for FM reception, selected inputs are FM-MPX and AM/FM level

- FM dynamic signal processing
- De-emphasis filter
- 19 kHz notch filter
- FM audio filter
- Stereo detection, stereo indication available at output pin 40 (DSP-OUT1 pin)
- Pause detection for RDS updates, output at pin 41 (DSP-OUT2 pin)
- Hold function for level, noise and multipath during RDS updates with input pin 38 (DSP-IN1 pin)
- Mute function during RDS updates with input pin 38 (DSP-IN1 pin)
- Adjustment for maximum channel separation
- Signal quality filter (noise information)
- Adjustment possibility for noise sensitivity

3 AM mono mode : mode for MW , LW or SW reception, selected input is AM-R

- 6th order LPF filter
- Softmute
- High cut control
- AM IAC (Interference Absorbtion Circuit)

4 Tape mode : selected inputs are Tape-L and Tape-R

- Dolby level adjust
- Dolby-B noise reduction

5 CD_A mode : mode for analog CD signals, selected inputs are CD_L,CD_R and CD_GND

- Compressor

6 CD_D mode : mode for processing the digital input from a CD player. The selected input is either
CD-1 or
CD-2 I²S

- De-emphasis
  selectable on/off via input pin 39 (DSP-IN2 pin)
  on/off via processing YRAM register via IIC
- Compressor

7 MSS mode : pause search, selected inputs are Tape-left and right

- pause indication at pin 41 (DSP-OUT2 pin)

8 Speech mode : This mode can be used to apply for instance a mono speech signal to one input pin and to get output over all channels.

- In the SPEECH mode normally the AM_L input is directed to both channels (Left and Right) of the Audio processor.
  It is also possible to use any other single input to process voice_in to both AUDIO channels, for instance the CD_A inputs with CMMR input stage.
- 6th order filter available, for optimization of speech audio response

9 Transparant mode : This mode directly couples any stereo source directly to the AUDIO block.

Can be used for instance of handling external Dolby C or external AM stereo signals

General purpose Tone Generator:

This is not a separate mode, but this function can be called in each of above mentioned modes.

- generates various waveforms with selectable frequencies
- possibility to superimpose various waveforms at the end of the 4 channel audio chain

9.0.3.2 Definition of the digital in- and output control pins

Pin	Function
DSP-IN1 (pin 38)	FM Mute and Hold FM filters, 0=Mute
DSP-IN2 (pin 39)	Freeze function for level, noise and multipath for RDS updates, 0= Freeze (see also chapter 9.3.8. RDS update function)
DSP-IN2 (pin 39)	De-emphasis at CD_D, 1=de-emphasis If a conflict occurs with the freeze function (using same pin), it is possible to control by IIC the de-emphasis function via setting/clearing a YMEM register
DSP-OUT1 (pin 40)	FM stereo indication, 1=stereo
DSP-OUT2 (pin 41)	Pause indication during FM mode, 1=pause
DSP-OUT2 (pin 41)	Pause indication during MSS mode, 1=pause

Table 9.12 Definition of the digital in- and output control pins

9.0.3.3 Mode selection and Easy Programming

After power up the contents of the XRAM and YRAM of the DSP is random. Before any operation mode is selected the contents of the XRAM and YRAM has to be initialized by calling an easy programming routine, see description below.
After power up the DSP program rests in a waitloop with all DAC outputs set to zero. Leaving this loop one starts loading the default AUDIO and Tone generator settings and automatically the Idle_Audio mode is entered.

An (new) operation mode can be selected by first entering its specific easy programming mode. This easy programming mode initiates XRAM and YRAM for the particular mode and forces the program in the Idle_Audio mode. It can than be followed by the value of the (new) mode pointer X:modpntr.
See table 9.13.

Memory map for XRAM and YRAM

The YRAM and XRAM memories are divided into a part common for all modes and into parts preserved for the various modes.

Memory space common for all modes:

XRAM address fields $00 - $0D, $58 - $7F and $C4 - $133
YRAM address fields $00 - $2B and $AC - $159
ROM version number is located in YRAM address $17F (Y:$17F= 2)

Memory space not common for all modes (Mode Field):
The XRAM address fields $0E - $57 and $80 - $C3 and the YRAM field $2C - $AB are preserved for the different modes (Mode Field).

The YRAM and the XRAM can not hold the coefficients and data required for all operation modes together. Therefor 5 different sets of easy programming routines are programmed:

set1 : a common set for ALL modes (including AUDIO and Tone generator)
(only accessed once)
set2 : an additional set for the FM mode
set3 : an additional set for the OTHER1 mode (MSS, TAPE)
set4 : an additional set for the OTHER2 mode (CD)
set5 : an additional set for the OTHER4 mode (AM, Speech)

The mentioned sets with addresses, values and label names are listed in appendix 13.5.

Download procedure and entering new mode

By initializing the XRAM and YRAM with set 1 (ALL) one leaves the waitloop after RESET and automatically enters the Idle_Audio mode.

Depending of the desired mode another specific Easy Programming set should be selected, (set2..set5) Downloading of the data and coefficients to the SAA7705H apart from this Easy Programming has to be done by the I^2C bus control. For detailed information see the data sheet SAA7705H, chapter "I^2C bus control and commands".

If the easy programming set together with specific data and/or coefficients are loaded, then that operation mode can be selected.
For selecting the different operating modes use table 9.13.

Easy Programming set 1 (ALL) need to be loaded ONCE after RESET. It leaves the waitloop after reset and enters the Idle_Audio mode.

start loading Easy Programming set1 (ALL) by loading Y:mod00= $4EC

Easy Programming set 2 .. set 5 can be loaded by loading X:modpntr with its specific value, after initiating these sets the current program is directly forced into Idle_Audio mode and allows setting specific parameters before starting up the selected mode.
(See par.: I²C settings for Mode selection)

start loading Easy Programming set 2	(FM)	X:modpntr= #00600
start loading Easy Programming set 3	(MSS,Tape)	X:modpntr= #00580
start loading Easy Programming set 4	(CD)	X:modpntr= #005C0
start loading Easy Programming set 5	(AM,Speech)	X:modpntr= #00640

Procedure for starting up selecting modes

1. enable SAM (audio becomes muted)
2. wait till SAM control time is passed
3. activate POM (pin 5) note 1)
4. initiate hardware I2C register settings (see table 9.11)
5. load specific Easy Programming mode (set2 .. set 5) (loading X:modpntr acc. table 9.13)
6. release POM note 1)
7. wait till POM control time is passed (800 ms in default application) note 1)
8. *****[initiate specific wanted parameters] note 2)
9. select mode (see table 9.13)
10. disable SAM

notes : 1) steps 3, 6 and 7 are only required when switching from a digital to an analog input mode in order to prevent a audible switching click.
2) commands between [...] brackets are optional

Digital modes CD_D

In case of CD_1 or CD_2 the external I²S input is selected. The synchronization flag for the DSP program is generated by the external WordSelect.

Warning : If no source is connected to the external I²S there is **no synchronization flag**. As a consequence the core is waiting for the flag and so **no program is executed** until the source is connected or another mode with an internal source is selected (f.i. Tape).

Table 9.13 Settings for each mode SAA7705H

Mode	start address Easy Programming X:modpntr a)	start address Mode X:modpntr	input selections
Idle AUDIO	Y:mod00=$4EC	a)	
FM	#00600	#00080	FM
AM_mono	#00640	#00100	AM_R
Tape	#00580	#00140	TAPE_L/R
CD_A	#005C0	#00200	CD_L/R
CD-D only compressor	#005C0	#00200	I2S CD-1 or 2 input
CD_D deemphasis via flag followed by compressor	#005C0	#00240	I2S CD-1 or 2 input
CD_D deemphasis via RAM followed by compressor	#005C0	#00280	I2S CD-1 or 2, deemphasis OFF: Y_dmfViaRAM = $000 ON : Y_dmfViaRAM <> $000
Tone generator (NOT a special mode, can be selected in EACH mode)	n.a.	n.a.	OFF: Y:sinusMode = $89A ON : Y:sinusMode = $897 Superposition : Y:sinusMode = $88D
MSS	#00580	#00500	Restart Y:mod20 = $12F
Speech	#00640	#00300 #002C0	AM_L or another Left input any other Right input
Transparant	n.a.	#00400	any stereo input

Remark: a) Loading all Easy Programming sets 1..5 enter the Idle_Audio mode

9.1 Audio processing

9.1.0 General Overview

This chapter describes the audio processing block. A diagram of this audio block is given in fig. 9.1. This block is implemented twice: for the left and for the right audio channel.

The different program parts, which occur in the audio processing block, are described.

The sections are:

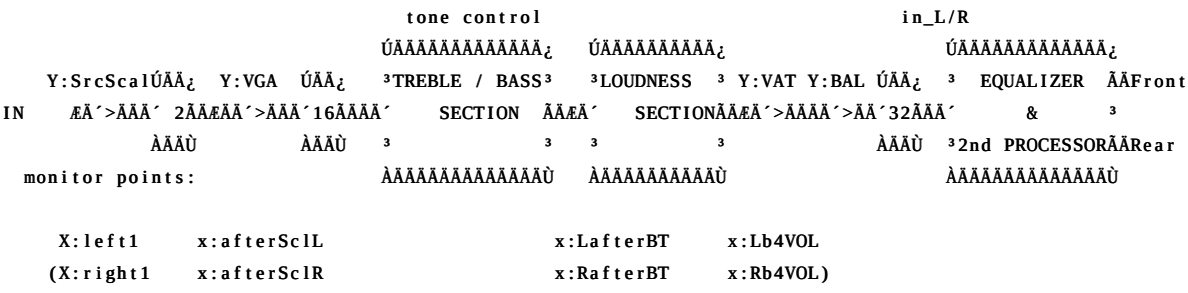


Fig. 9.1 audio path CDSP program (one channel)

9.1.0.1 RAM memory use, overview

The memory places related to the audio function of the CDSP chip are located at the end of the RAM range, as follows:

XRAM data memories X:LoudnXL .. X:S1QPD0 and X:samZh .. X:S1QPD1
YRAM coefficients Y:KML1h .. Y:Ctre

The following grouped YRAM coefficients are generally used. The names of the variables are given together with where these coefficients are explained.

A group of 20 coefficients, needed for the audio block, is located in a bank from Y:VGA .. ScrScal.

Coefficient	description section	remark
Y:VGA	9.1.1.2	
Y:KLCl	9.1.2	low part double precision value
Y:KLCh	9.1.2	high part double precision value
Y:KLBl	9.1.2	low part double precision value
Y:KLBh	9.1.2	high part double precision value
Y:KLA0l	9.1.2	low part double precision value
Y:KLA0h	9.1.2	high part double precision value
Y:KLA2l	9.1.2	low part double precision value
Y:KLA2h	9.1.2	high part double precision value
Y:KLtre	9.1.2	adaptive value
Y:KLbas	9.1.2	adaptive value

Coefficient	description section	remark
Y:KLmid	9.1.2	
Y:VAT	9.1.1.2	
Y:SAM	9.1.3	adaptive value
Y:OutSwi	9.13	
Y:FLcof	9.1.1.3 and 9.13	
Y:FRcof	9.1.1.3 and 9.13	
Y:RLcof	9.1.1.3 and 9.13	
Y:RRcof	9.1.1.3 and 9.13	
Y:SrcScal	9.1.1.0	

Bank switching principle.

Another group of YRAM coefficients are located in two 14 coefficients long audio banks.
This group of coefficients are twice present, once in bank0, and also in bank1.

Coefficients			
Bank0	Bank1	description section	remark
Y:Ctl0	Y:Ctl1	9.1.5	low part double precision value
Y:Cth0	Y:Cth1	9.1.5	high part double precision value
Y:Btl0	Y:Btl1	9.1.5	low part double precision value
Y:Bth0	Y:Bth1	9.1.5	high part double precision value
Y:At00	Y:At01	9.1.5	
Y:At10	Y:At11	9.1.5	
Y:At20	Y:At21	9.1.5	
Y:KTrt0	Y:KTrt1	9.1.5	
Y:KTft0	Y:KTft1	9.1.5	
Y:KTmid0	Y:KTmid1	9.1.5	
Y:KTbas0	Y:KTbas1	9.1.5	
Y:KTtre0	Y:KTtre1	9.1.5	
Y:BALL0	Y:BALL1	9.1.1.1 and 9.1.5	(combination balance with TCC)
Y:BALR0	Y:BALR1	9.1.1.1 and 9.1.5	(combination balance with TCC)

Together with these separated YRAM banks a pointer, holding the current startaddress is needed:
X:audioc.

To prevent clicks during a change of bass, treble settings a bank_switch system is implemented.
The filter coefficients are located in two banks. One is the working (active) bank (used by the DSP algorithms), the other is the (passive) bank gathering new coefficients via I2C interface.
When the loading process of the passive bank is finished, a bank switch command (loading a new pointer in X:audioc) must be issued to activate this new group of coefficients. (See section 9.1.5.4). After generating the bank switch command, the function of passive and active bank interchange.

At initialization, be sure that the active bank is loaded with valid data, before the mute is deactivated.
Also be sure that all data in the passive bank is valid before giving the bankswitch command.

9.1.1 Source Scaling, Volume, Balance and Fader

9.1.1.0 Source Scaling

The various audio sources which can be connected to the DSP have different mean values and dynamic ranges. Therefore a scaling of the input signal is necessary to give the same sound pressure level for a fixed volume setting. Input scaling is realized via coefficient Y:SrcScal. (see fig. 9.1)

Maximum possible gain 6 dB (one bit shifter)

Input variable: SF:Input Scaling [dB] Output coefficient: Y:SrcScal

$$Y:\ SrcScal\ =\ \frac{10^{\frac{SF}{20}}}{2}$$

Example:

SF= 2 dB Y:SrcScal= (10^(2/20))/2= (10^0.1)/2)= 1.258925/2= 0.629463 ($509)

9.1.1.1 Volume

The volume control is split into two sections:

- Gain setting and input scaling by coefficient VGA and a four bit shifter. (Maximum gain possible 24 dB)
- Attenuation setting by coefficient VAT.

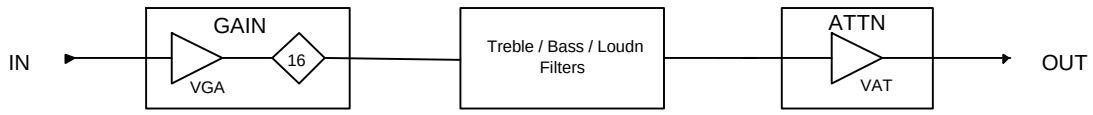


Fig. 9.2 Volume Control

The gain or attenuation setting is equal for both channels. The practical control range is between +20 dB and -66 dB. Some volume settings and corresponding coefficient values are summarized in table 9.14. Because of the limited coefficient word length, the steps are larger than 1 dB for volume settings less than -40 dB. (see Y:VGA at end of table 9.14)

9.1.1.1.0 RAM memory use for Volume

Y:VGA
Y:VAT

These two volume coefficients are located in a group of 19 audio coefficients.

9.1.1.1.1 Calculation of Volume Control

Input variables: Gdb: Volume [dB]

Output coefficients: Y:VGA, Y:VAT

$$Y:VAT = -1$$

$$Y:VGA = \frac{-10^{\frac{Gdb}{20}}}{16}$$

if Gdb ≥ 0 dB then

$$Y:VAT = -10^{\frac{Gdb}{20}}$$

$$Y:VGA = -\frac{1}{16}$$

else

Example:

GdB= 10 dB
Y:VAT= -1 ($800)
Y:VGA= -(10^(10/20))/16= -(10^0.5)/16)= -3.16/16= -0.198 ($E6C)

Gdb	Y:VAT	Y:VGA
10 dB	$800	$E6C
0 dB	$800	$F80
-35 dB	$FDC	$F80
-39 dB	$FEA	$F80
-40.2 dB	$FEC	$F80
-41.1 dB	$FEE	$F80
-42.1 dB	$FF0	$F80
-43.3 dB	$FF2	$F80
-44.6 dB	$FF4	$F80
-46.2 dB	$FF6	$F80
-48.2 dB	$FF8	$F80
-50.7 dB	$FFA	$F80
-54.2 dB	$FFC	$F80
-60.2 dB	$FFE	$F80
-66.2 dB	$FFF	$F80

Table 9.14 Volume coefficients VGA and VAT

9.1.1.2 Balance

The balance control function is performed by one coefficient per audio channel: Y:BALLn and Y:BALRn. The value of these coefficients is determined by the balance setting and the tone control setting : if a positive gain of the treble and/or bass section of the tone control filter is desired then this gain will NOT be realized in the tone control function but in the balance function ; the variable TCC is used for this purpose (TCC in section 9.1.5).

9.1.1.2.0 RAM memory use, balance

bank0	bank1
Y:BALL0	Y:BALL1
Y:BALR0	Y:BALR1

These values for balance are 2 coefficients out of a group of 14 general audio coefficients in banks used for bankswitching.

9.1.1.2.1 Calculation of Balance

Input variables:	BL:	Left channel attenuation (attenuation range 0.. ∞ dB)	[dB]	Output coefficients:	Y:BALLn Y:BALRn
	BR:	Right channel attenuation	[dB]		
	TCC:	Tone control compensation			

$$Y:BALLn = 10^{-\frac{BL}{20}} * TCC$$

$$Y:BALRn = 10^{-\frac{BR}{20}} * TCC$$

Example:

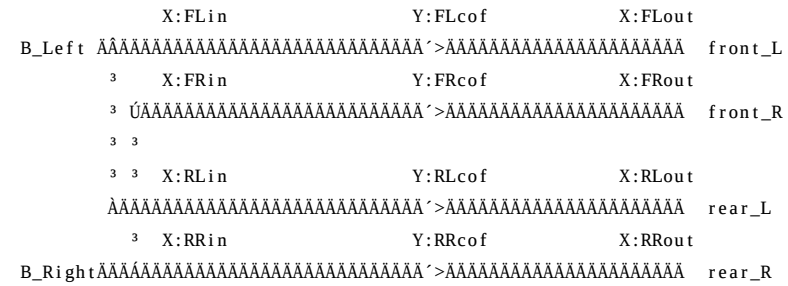
Table 9.15 gives a few examples for the channel attenuation and coefficient values as a function of the balance setting, note that TCC=1 in these examples.

Channel attenuation [dB] BL	BR	Y:BALLn	Y:BALRn
30	0	$040	$7FF
10	0	$287	$7FF
0	0	$7FF	$7FF
0	30	$7FF	$040

Table 9.15 Coefficient values Balance

9.1.1.3 Fader

In the situation with no second processor the input signal to the fader is the output signal from the audio processing block. (Signal B_Left and B_Right just after the Equalizer function)



All front and rear output channels use a separate coefficient: Y:FLcof.. Y:RRcof.
(Information about the fader function in the case of a second processor can be found in section 9.12)

9.1.1.3.1 Calculation of Fader

Input variables:		Output coefficients:
FR_att: front attenuation (attenuation range 0.. ∞ dB)	[dB]	Y:FLcof, Y:FRcof
RE_att: rear attenuation. (attenuation range 0.. ∞ dB)	[dB]	Y:RLcof, Y:RRcof

$$Y:FLcof = Y:FRcof = -10^{-\frac{FR\_att}{20}}$$

$$Y:RLcof = Y:RRcof = -10^{-\frac{RE\_att}{20}}$$

Examples:

Table 9.16 gives some attenuation and coefficient values as a function of the fader setting.

Attenuation [dB] FR_att	RE_att	Y:FLcof	Y:RLcof
30	0	$FC0	$800
6	0	$BFE	$800
0	0	$800	$800
0	30	$800	$FC0
0	99	$800	$000 (rear channel muted)

Table 9.16 Coefficient values Fader

9.1.2 Loudness

9.1.2.1 General function description

Function of the loudness filter is to boost the high and low frequency part of the audio spectrum. The filter is implemented separate from the tone control filter. In this way the frequency response curves of both filters have been made independent.

The treble section offers a practical control range from 0 dB to +14 dB in selectable step values. The cutoff frequency is fixed and depends on the sample frequency. The bass stage offers a practical control range from 0 dB to +14 dB in selectable step values. The cutoff frequency is adjustable.

With the chosen separate loudness implementation it is possible to realize:
-static loudness
bass boost and treble boost are directly coupled to the volume setting. External controller transmits a control value (Y:statLou) to the Attack/ Release filter.
-dynamic loudness (bass and treble boost)
coefficients for bass and treble depending of current audio level, and generated by the DSP itself
-dynamic bass boost
coefficient for bass depending of current audio level, and generated by the DSP itself. Treble control is switched off.

Fig. 9.3 Loudness coefficient generation function

With the coefficient Y:OFFS it is possible to limit the active region of the bass and treble coefficient generator (only in case of dynamic loudness). With Y:OFFS= $080 the dynamic loudness (or bass boost) function is active for the full input level range, for Y:OFFS= $100 the dynamic loudness (or bass boost) function is active only for input signals less then 6 dB from full scale. The ultimate level of the control signals are determined by Y:Cllev and Y:Ctre. In case bass boost Y:Ctre= 0.

9.1.2.2 RAM memory use for Loudness function

Y:KLCl	Y:louSwi
Y:KLCh	Y:statLou
Y:KLBl	Y:OFFS
Y:KLBh	Y:KPDL
Y:KLA0l	Y:KMDL
Y:KLA0	Y:Cllev
Y:KLA2l	Y:Ctre
Y:KLA2	
Y:KLmid	

The coefficients Y:KLCl..Y:KLmid determine the desired loudness curve.

9.1.2.3 Calculations of loudness Filter

9.1.2.3.0 First order highpass

The cutoff frequency fkt of the high pass branch is determined by the sample frequency fs and **cannot** be changed:

$$fkt = \frac{fs}{4}$$

9.1.2.3.1 First order lowpass.

Input variables:	fkb: Cutoff frequency bass fs: Sample frequency	[Hz] [Hz]	Output coefficients:	Y:KLA0h, Y:KLA0l Y:KLCh, Y:KLCl Y:KLA2h=0,Y:KLA2l=0 Y:KLBh=0, Y:KLBl=0 Y:KLmid= $200

$$t0 = \cos(\frac{2p \bullet fkb}{fs})$$

$$CL = 1 - \frac{t0 + \sqrt{(t0 - 2)^2 - 1}}{2}$$

If the value |CL|> 1 then a new value according next formula must be calculated.

$$CL = 1 - \frac{t0 - \sqrt{(t0 - 1)^2 - 1}}{2}$$

$$AL = 0.5 - CL$$

$$Y:KLA0h,Y:KLA0l = AL$$
$$Y:KLCh,Y:KLCl = CL$$

Example: fkb= 80 Hz, fs=38 kHz:

t0 = 0.999913			
CL= 0.493448	=3F294D	Y:KLCh = $3F2	Y:KLCl = $4A6
AL= 0.006552	=00D6B3	Y:KLA0h= $00D	Y:KLA0l= $359

9.1.2.3.2 Second order shelving low pass.

Input variables:	fkb: Cutoff frequency bass fs: Sample frequency	[Hz] [Hz]	Output coefficients:	Y:KLA0h, Y:KLA0l Y:KLCh, Y:KLCl Y:KLBh, Y:KLBl Y:KLA2h=0, Y:KLA2l=0 Y:KLmid= $200

$$Y:KLA0h,Y:KLA0l = AL0$$
$$Y:KLCh,Y:KLCl = CL$$
$$Y:KLBh,Y:KLBl = BL$$

The results for coefficients AL0, CL and BL for several sample frequencies fs and a cutoff frequencies fkb are shown in tables 9.17 through 9.20.

Loudness Filter for 2nd order shelving low pass (F_s= 32 kHz)						
fkb [Hz]	AL0		CL		BL	
	Y:KLA0l	Y:KLA0h	Y:KLCl	Y:KLCh	Y:KLBl	Y:KLBh
70	$30D	$000	$546	$7DD	$7AB	$C21
80	$3FA	$000	$648	$7D8	$5BD	$C26
90	$506	$000	$75A	$7D3	$39F	$C2B
100	$630	$000	$07C	$7CF	$153	$C30
110	$778	$000	$1AE	$7CA	$6D8	$C34
120	$0DE	$001	$2F1	$7C5	$430	$C39
130	$261	$001	$444	$7C0	$159	$C3E
140	$403	$001	$5A7	$7BB	$655	$C42
150	$5C1	$001	$71B	$7B6	$323	$C47

Table 9.17 Loudness Filter for 2nd order shelving low pass (fs = 32 kHz)

Loudness Filter for 2nd order shelving low pass (fs = 38 kHz)						
fkb [Hz]	AL0		CL		BL	
	Y:KLA0l	Y:KLA0h	Y:KLCl	Y:KLCh	Y:KLBl	Y:KLBh
70	$22B	$000	$072	$7E3	$561	$C1C
80	$2D4	$000	$78B	$7DE	$59F	$C20
90	$393	$000	$6B1	$7DA	$5BB	$C24
100	$467	$000	$5E2	$7D6	$5B6	$C28
110	$551	$000	$51E	$7D2	$590	$C2C
120	$651	$000	$466	$7CE	$548	$C30
130	$766	$000	$3B9	$7CA	$4E0	$C34
140	$090	$001	$318	$7C6	$457	$C38
150	$1CF	$001	$282	$7C2	$3AD	$C3C

Table 9.18 Loudness Filter for 2nd order shelving low pass (fs = 38 kHz)

Loudness Filter for 2nd order shelving low pass (fs = 44.1 kHz)						
fkb [Hz]	AL0		CL		BL	
	Y:KLA0l	Y:KLA0h	Y:KLCl	Y:KLCh	Y:KLBl	Y:KLBh
70	$19D	$000	$058	$7E7	$60A	$C18
80	$21B	$000	$3F4	$7E3	$1F0	$C1C
90	$2A9	$000	$799	$7DF	$5BD	$C1F
100	$347	$000	$347	$7DC	$171	$C23
110	$3F6	$000	$6FD	$7D8	$50C	$C26
120	$4B4	$000	$2BB	$7D5	$08F	$C2A
130	$583	$000	$682	$7D1	$3F9	$C2D
140	$662	$000	$252	$7CE	$74B	$C30
150	$750	$000	$62A	$7CA	$284	$C34

Table 9.19 Loudness Filter for 2nd order shelving low pass (fs = 44.1 kHz)

Loudness Filter for 2nd order shelving low pass (fs = 48 kHz)						
fkb [Hz]	AL0		CL		BL	
	Y:KLA0l	Y:KLA0h	Y:KLCl	Y:KLCh	Y:KLBl	Y:KLBh
70	$15D	$000	$081	$7E9	$621	$C16
80	$1C7	$000	$667	$7E5	$7D0	$C19
90	$23F	$000	$454	$7E2	$16B	$C1D
100	$2C5	$000	$249	$7DF	$2F0	$C20
110	$359	$000	$045	$7DC	$461	$C23
120	$3FA	$000	$648	$7D8	$5BD	$C26
130	$4A9	$000	$452	$7D5	$703	$C29
140	$056	$000	$263	$7D2	$036	$C2D
150	$630	$000	$07C	$7CF	$153	$C30

Table 9.20 Loudness Filter for 2nd order shelving low pass (fs = 48 kHz)

9.1.2.3.3 Second order peaking low pass.

Input:	f_c:	centre frequency	[Hz]	Output	Y:KLA0h, Y:KLA0l
	fs:	sample frequency	[Hz]	coefficients:	Y:KLCh, Y:KLCl
	Q:	shape factor	[-]		Y:KLA2h, Y:KLA2l
					Y:KLBh, Y:KLBl
					Y:KLmid= $200

The shape factor is defined by:
(with f_1 and f_2 being the -3 dB turn-over frequencies)

$$Q = \frac{f_c}{f_2 - f_1}$$

$$t0 = \frac{2p \bullet f_c}{fs}$$

$$BL = -0.5 \bullet \frac{1 - \tan(t\frac{0}{2Q})}{1 + \tan(t\frac{0}{2Q})}$$

$$CL = (0.5 - BL)\cos(t0)$$

$$AL = (0.5 + BL) / 2$$

$$Y{:}\,KLBh, Y{:}\,KLBl = BL$$
$$Y{:}\,KLCh, Y{:}\,KLCl = CL$$
$$Y{:}\,KLA0h, Y{:}\,KLA0l = AL$$
$$Y{:}\,KLA2h, Y{:}\,KLA2l = AL$$

Example: f_c= 100 Hz, fs=38 kHz, Q= 1.65:

t0 = 0.0165347			
BL = -0.495015	=C0A359	Y:KLBh = $C0A	Y:KLBl = $1AC
AL = 0.0024925	=0051AC	Y:KLA0h= $005	Y:KLA0l= $0D6
CL = 0.994879	=7F5831	Y:KLA2h= $005	Y:KLA2l= $0D6
		Y:KLCh = $7F5	Y:KLCl = $418

9.1.2.3.4 Calculations for static loudness

Input variable:	gbb: bass boost [dB] (range 0..14 dB)	Output coefficient:	Y:statLou Y:Cllev= $400 (0.5) Y:Ctre= $0CD (0.1)

$$statLou = 1 - 0.5 * \sqrt{10^{\frac{gbb}{20}} - 1}$$

The actual value of the generated gain coefficients may be controlled with Y:Cllev and Y:Ctre. (See fig. 9.3).
The default values are given in the output coefficient block.
With Ctre it is possible to reduce the treble boost compared to the bass boost.

9.1.2.3.5 Calculation for loudness offset control (dynamic loudness only)

Note that the offset control with coefficient Y:OFFS is only active in case of dynamic loudness (see also fig. 9.3) , in case of static loudness the required offset is implicitly realized in the (user) design of the static loudness curve ; see section 9.1.2.4.1. for further explanation.

Input Ulo: Level loudness off [dB] (range 0..24 dB) Output: Y:OFFS

$$Y:OFFS = \frac{10^{\frac{Ulo}{20}}}{16}$$

Example: Ulo= 6 loudness not active for signals ≥ -6 dBFS)

Y:OFFS= (10^(6/20))/16= 2/ 16= 0.125 $100

9.1.2.4 General control action for Loudness

The loudness filter coefficients are 'fixed' by choosing the desired loudness filter type and characteristics for the loudness bass- and treble section.
The attack/release filter coefficients are 'fixed' to get a soft switch on and switch off behaviour.
These coefficients (Y:KPDL= $819 and Y:KMDL= $023) are loaded by Easy Programming set1; it is strongly recommended to use these default values because they are the result of listening tests that were done to determine the optimum attack/release time.

Select the offset value Y:OFFS (only in case of dynamic loudness, Y:OFFS is not used in case of static loudness). For Y:OFFS= $100 the dynamic loudness is only active for signals less than 6 dB full scale

9.1.2.4.1 Control actions for Static Loudness

For static loudness the bass and treble boost has to be controlled by the micro controller and needs to made a function of the volume setting. The loudness curve (loudness boost as function of volume) has to defined by the user. The loudness boost is set with coefficient Y:statLou. Every time the volume setting changes the micro controller should also send a new Y:statLou value in order to change the loudness boost for the new volume setting.

Use the following procedure to program the static loudness function :

1. Draw a desired loudness curve (loudness boost as function of volume setting).
   Make sure that the curve starts with 0 dB boost and ends with 14 dB boost (examples of such curves are curve 1. and 2. in fig 9.4). Note that loudness offset is implicitly realized in the design of the loudness curve, the coefficient Y:OFFS has no function in case of static loudness.

2. Make a table with loudness boost and Y:statLou as function of the volume setting,
   see the example table 9.21 that corresponds with curve 1 in fig. 9.4.
   The Y:statLou values can be calculated with the formula given in 9.1.2.3.4, the input variable 'gbb' corresponds with the loudness boost in the user table.

3. The maximum loudness boost of both the bass section and treble section can be scaled if desired with coefficients Y:Cllev and Y:Ctre respectively, according next formulas :

Input gdbb: maximum bass boost — Output: Y:Cllev
gdtb: maximum treble boost — Y:Ctre

$$Y{:}Cllev = \frac{10^{\frac{gdbb}{20}} - 1}{8}$$

$$Y{:}Ctre = \frac{10^{\frac{gdtb}{40}} - 1}{4}$$

When the volume setting is decreased with Y:Cllev= $400 and Y:Ctre= $0FE the bass boost gradually increases to a maximum of 14 dB and the maximum treble boost will be 7 dB.

Examples of the maximum boost as a function of the volume setting is shown in fig. 9.4. for three different situations (offset = volumesetting where bassboost does start, gain ≈ 0.5 dB). The loudness function needs to be fully controlled by the micro controller by loading the Y:statLou value together with volume settings. The Y:statLou value is the input to an attack/ release filter. In this way audible clicks during on/off switching and updates are prevented.

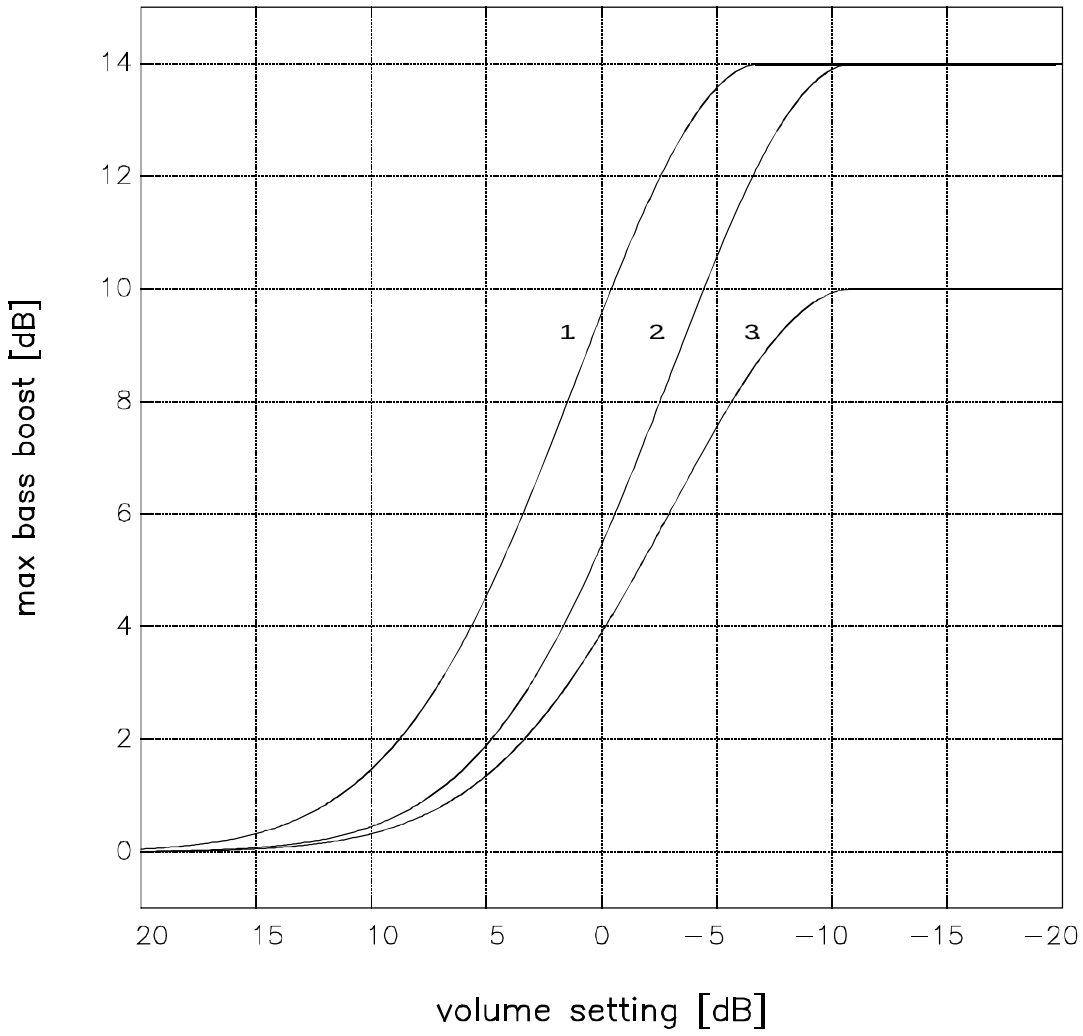


Fig. 9.4 Bass boost as a function of volume setting.

curve	offset [dB]	max gain [dB]
1.	14	14
2.	10	14
3.	10	10

- Loudness **off**

  Set loudness switch Y:louSwi= $90D, and Y:statLou= $7FF.

- Static loudness **on**

  After loading the loudness curve coefficients Y:KLCl till Y:KLmid, together with the scaling factor Y:Cllev for bass boost and Y:Ctre for treble boost, the loudness switch should be set to Y:louSwi= $90D. (Same value as for loudness function off).

(For Y:Cllev= $400 max. bass boost : 14 dB, for Y:Ctre = $0FE max. treble boost: 7 dB. formulas for Y:Cllev and Y:Ctre see par. 9.1.2.4.1)

Example: (curve 1 of fig. 9.4)

Table 9.21 gives the value Y:statLou= f(Volume), together with the chosen bass boost value, in the case maximum bass boost = 14 dB. (Y:Cllev= $400)

Volume [dB]	Bass Boost [dB]	Y:statLou
20	0.00	$7FF
19	0.001250	$7B8
18	0.106059	$78E
17	0.155526	$776
16	0.224528	$75A
15	0.319119	$73A
14	0.446527	$715
13	0.615117	$6EB
12	0.834222	$6BB
11	1.11383	$685
10	1.46411	$649
9	1.89469	$606
8	2.4139	$5BC
7	3.02771	$56B
6	3.73873	$511
5	4.54513	$4AF
4	5.43981	$445
3	6.40967	$3D2
2	7.43534	$359
1	8.49143	$2D9
0	9.54717	$257
-1	10.5678	$1D6
-2	11.5161	$159
-3	12.355	$0E7
-4	13.0494	$086
-5	13.5693	$03C
-6	13.8911	$00D
-7	14	$000

Table 9.21 Coefficient values Static Loudness as function of Volume setting.

9.1.2.4.2 Control actions for Dynamic Loudness

- Loudness **off**
  Set loudness switch Y:louSwi= $90D, and Y:statLou= $7FF.

- Dynamic loudness **on**
  After loading the loudness curve coefficients Y:KLCl till Y:KLmid, together with the scaling factor Y:Cllev for bass boost and Y:Ctre for treble boost, the dynamic loudness function can be switched on by Y:louSwi= $910.
  (For Y:Cllev= $400 max. bass boost : 14 dB, for Y:Ctre = $0FE max. treble boost: 7 dB.
  formulas for Y:Cllev and Y:Ctre see section 9.1.2.4.1)

  Set the desired loudness offset with Y:OFFS (see formula in section 9.1.2.3.5).

  The attack/release filter with coefficient generator processes bass control and treble control.

9.1.2.4.3 Control actions for Dynamic BassBoost

- Loudness **off**
  Set loudness switch Y:louSwi= $90D, and Y:statLou= $7FF.

- Dynamic bassboost **on**
  After loading the loudness curve coefficients Y:KLCl till Y:KLmid, together with the scaling factor Y:Cllev for bass boost and Y:Ctre= 0 (no treble boost), the dynamic bassboost function can be switched on by Y:louSwi= $910.
  (For Y:Cllev= $400 max. bass boost : 14 dB, formula for Y:Cllev see section 9.1.2.4.1)

  Set the desired loudness offset with Y:OFFS (see formula in section 9.1.2.3.5).

  The attack/release filter with coefficient generator processes bass control.

9.1.3 Soft Audio Mute. (SAM)

The Soft Audio Mute circuit is implemented to switch the audio signal on and off without undesired click noise. Besides that it is possible to perform fade-in and fade-out actions.

The Soft Audio Mute circuit enables the user to generate an output signal Y:SAM. This signal controls the audio level of both audio channels. (see graphs in section 9.1.1.3)
The circuit is triggered by writing the required values into three places in coefficient-memory: Y:delta, Y:switch and double precision coefficient Y:samCh, Y:samCl. These values determine the steepness and direction of the slope (exponential ramp) of output signal Y:SAM.

9.1.3.0 RAM memory use for Soft Audio Mute function

Next YRAM coefficients are in use with the ramp calculation part:

Y:samCl
Y:samCh
Y:delta
Y:switch
Y:SAM (one (adaptive) coefficient out of 20 in group 'fixed' audio coefficients)

9.1.3.1 Calculations of Soft Audio Mute

The definition of rise time (Ta) and fall time (Tr) is pictured in fig. 9.5. The maximum rise time is determined by the double precision coefficient Y:samCh,Y:samCl. For normal use Ta= Tr.

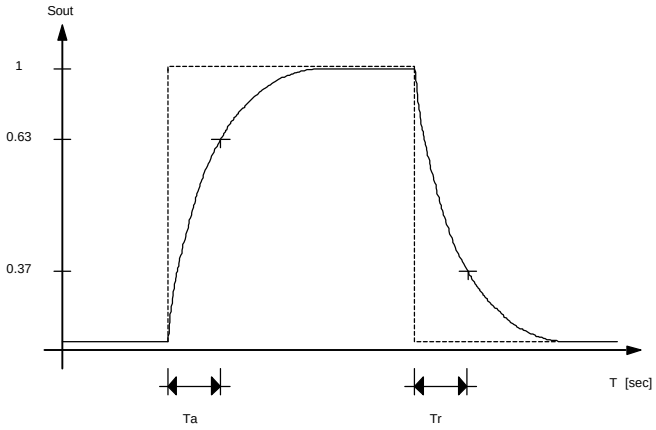


Fig. 9.5 Rise time definition exponential SAM

Fig. 9.5 Rise time definition exponential SAM

Input variables:	Tr:	rise/fall time	[sec]	Output coefficients:	Y:delta
	fs	sample frequency.	[Hz]		Y:switch
					Y:samCh, samCl

$$a = e^{\frac{-8}{Tr \bullet fs}}$$

$$Y:samCh,samCl = a$$

$$(Y:delta) * (Y:switch) = (1-a)$$

Choose the coefficient values Y:delta and Y:switch in such a way that the product is (1-a)
A solution is: Y:delta = Y:switch = $\sqrt{(1-a)}$

Example: Tr= 10 ms fs= 38 kHz

a=0.979167 $7D5558_H$ Y:samCh=$7D5 Y:samCl=$2AC
1-a=0.020833
$\sqrt{(1-a)}$=0.144336 Y:delta=$128 Y:switch=$128

9.1.3.2 Control Actions for Soft Audio Mute

Table 9.22 gives possible values for the coefficients for equal rise/fall time.
For a wide range of rise/fall times it is not necessary to change Y:delta.

Enable SAM: Y:switch= 0,
Disable SAM: (enable audio) Y:switch according table 9.22

For practical values Tr= 4.6 .. 1000 ms, one can work with Y:delta fixed, and only varying Y:switch according following table.

Soft Audio Mute coefficients for fs =38 kHz				
Tr (msec)	Y:samCl	Y:samCh	Y:delta	Y:switch
4.6	$189	$7A5	$07D	$5D4
6.8	$580	$7C1	$07D	$401
10.0	$2B5	$7D5	$07D	$2BC
14.7	$6B4	$7E2	$07D	$1E0
21.5	$0B1	$7EC	$07D	$146
31.6	$34C	$7F2	$07D	$0DF
46.4	$5DD	$7F6	$07D	$098
68.1	$574	$7F9	$07D	$067
100.0	$58C	$7FB	$07D	$046
146.8	$085	$7FD	$07D	$030
215.5	$7FF	$7FD	$07D	$021
316.3	$518	$7FE	$07D	$016
464.2	$092	$7FF	$07D	$00F
681.4	$2F0	$7FF	$07D	$00A
1000.1	$48D	$7FF	$07D	$007

Table 9.22 Practical values for Soft Audio Mute coefficients

9.1.4 Quasi Peak Detectors

9.1.4.1 Functional description.

In the Audio program two independent Quasi Peak Detectors are available:

QPD_0 Inputs free selectable. Response time selectable.
QPD_1 Inputs free selectable. Response time selectable.

9.1.4.1 Functional description.

Purpose of a Quasi Peak Detector is to give an indication of the absolute input level. This input level is measured at 2 independent points in X_data memory of the lower XMEM region. (XMEM[0..$FF])

General use is to fetch the data sample out of the left audio channel together with its corresponding right channel signal.
Possible pair of input signals can be found in fig. 9.1 (f.i. X:left1 and X:right1), in fig. 9.9 (X:Center and X:SubWoof) or in par. 9.1.1.3 (f.i. X:FLout and X:FRout). See also appendix 11.4 for the complete audio blockdiagram, the possible QPD input signals are highlighted in this diagram.

The maximum (absolute) value of these two signals is fed to an attack/release filter.
This attack/release filter has been implemented to provide a reliable peak output value.

Fig. 9.6 shows the response of the attack / release filter on a block signal as input.
Attack time Ta and release time Tr are determined by the value of both double precision coefficients KML and KPL. (Y:KMLh.. Y:KPLl and Y:KML1h.. Y:KPL1l) The circuit allows the user to set different attack and release times.

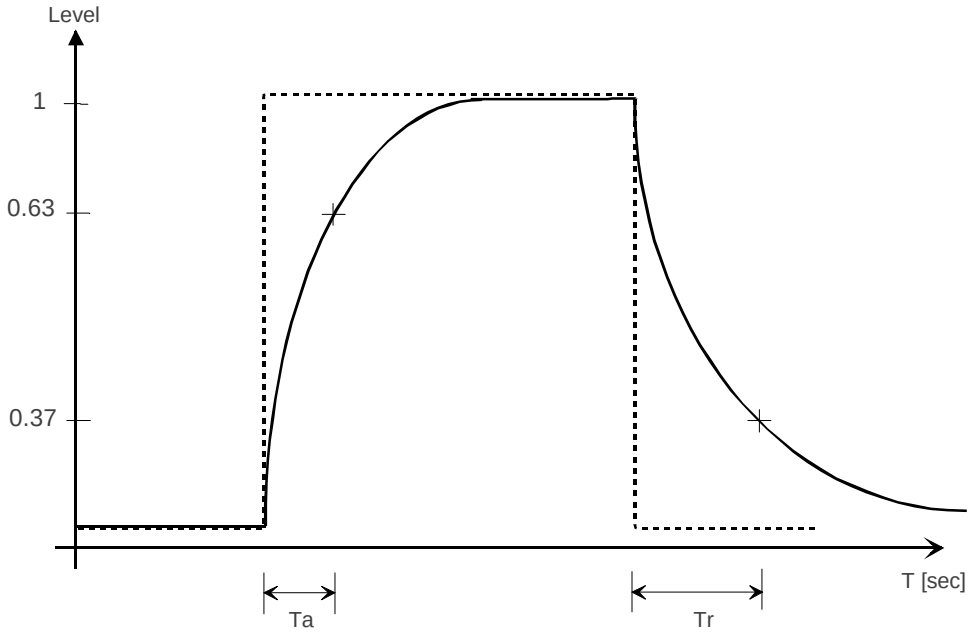


Fig. 9.6 Level filter response QPD

9.1.4.1 RAM memory use

Quasi Peak Detector QPD_0
X:S0QPD0
X:S1QPD0
X:maxDAT ;input to level detector 0, delivered by pointers X:S0QPD0 & X:S1QPD0
X:DATh
X:DATl

Y:KMLh
Y:KMLl
Y:KPLh
Y:KPLl

This function uses 1 XRAM data input memory (X:maxDAT) and one double precision data word (X:DATh, X:DATl), together with two double precision YRAM coefficients (Y:KMLh, Y:KMLl and Y:KPLh, Y:KPLl).

Quasi Peak Detector QPD_1
X:S0QPD1
X:S1QPD1
X:maxDAT1 ;input to level detector 1, delivered by pointers X:S0QPD1 & X:S1QPD1
X:DAT1h
X:DAT1l

Y:KML1h
Y:KML1l
Y:KPL1h
Y:KPL1l

This function uses 1 XRAM data input memory (X:maxDAT1), one double precision data word (X:DAT1h, X:DAT1l), together with two double precision YRAM coefficients (Y:KML1h, Y:KML1l and Y:KPL1h, Y:KPL1l).

9.1.4.3 Calculations of Quasi Peak Detector

Input variables:	Ta:	attack time	[sec]	Output coefficients:	Y:KMLh,KMLl
	Tr:	release time	[sec]		Y:KPLh,KPLl
	fs:	samplefreq.	[Hz]		

$$ca = e^{\frac{-8}{fs \bullet Ta}} \quad cr = e^{\frac{-8}{fs \bullet Tr}}$$

$$Y: KPLh, KPLl = -(cr + ca) / 2$$
$$Y: KMLh,KMLl = -(ca - cr)$$

Example: Ta= 10ms, Tr=459ms, fs=38 kHz

Y:KML=0.020374	Y:KMLh= $029	Y:KMLl= $5CE
Y:KPL=-0.989354	Y:KPLh= $815	Y:KPLl= $66B

9.1.4.4 Required controller actions for Quasi Peak Detector

Quasi Peak Detector QPD_0

```
X:S0QPD0    ;pointer that defines the Left input signal of QPD_0
X:S1QPD0    ;pointer that defines the Right input signal of QPD_0
X:maxDAT    ;input to level detector 0, delivered by pointers X:S0QPD0 & X:S1QPD0
X:DATh      ;QPD_0 output signal

Y:KMLh ;sets the attack- and release time of QPD_0
Y:KMLl      ;  "     "     "       "
Y:KPLh      ;  "     "     "       "
Y:KPLl      ;  "     "     "       "
```

Quasi Peak Detector QPD_1

```
X:S0QPD1    ;pointer that defines the Left input signal of QPD_1
X:S1QPD1    ;pointer that defines the Right input signal of QPD_1
X:maxDAT1   ;input to level detector 1, delivered by pointers X:S0QPD1 & X:S1QPD1
X:DAT1h     ;QPD_1 output signal

Y:KML1h     ;sets the attack- and release time of QPD_1
Y:KML1l     ;  "     "     "       "
Y:KPL1h     ;  "     "     "       "
Y:KPL1l     ;  "     "     "       "
```

Example for QPD_1 :

First select the wanted attack/ release times and load Y:KML1h.. Y:KPL1l.
The pointers S0QPD1 (signal0 to QPD_1) and S1QPD1 (signal1 to QPD_1) contain each a rmx value that make the pointers point to a XMEM address. The program determines the value of the rectified signal of both XMEMs, and stores the maximum one in X:maxDAT1, which is the input to the Quasi Peak Detector. The QPD_1 output can be read out of X:DAT1h (the most significant part of the double precision outputsignal, the least significant part of the output signal, X:DAT1l can be ignored).

The same approach is valid for QPD_0. Timing constants: Y:KMLh.. Y:KPLl, pointers X:S0QPD0.. X:S1QPD0 and output available in X:DATh.

The pointer rmx values of the possible QPD input signals and the corresponding XMEM locations where they are pointing to are listed in the following table :

QPD input signal	XMEM address	RMX pointer
X:left1 X:right1	$E8 $EC	#03A00 #03B00
X:afterSclL X:afterSclR	$E3 $E4	#038C0 #03900
X:LafterBT X:RafterBT	$E1 $E2	#03840 #03880
X:Lb4VOL X:Rb4VOL	$EB $EF	#03AC0 #03BC0
X:FLin X:FRin X:RLin X:RRin	$C8 $C9 $CA $CB	#03200 #03240 #03280 #032C0
X:FLout X:FRout X:RLout X:RRout	$CC $CD $CE $CF	#03300 #03340 #03380 #033C0
X:SubWoof X:Center	$D8 $D9	#03600 #03640

Example: Use QPD0 to measure the peak of the Left/Right signal directly after source scaling :

```
X:S0QPD0 = #038C0
X:S1QPD0 = #039C0
```

9.1.5 Tone Control.

9.1.5.1 Functional description.

The tone control section processes the bass and treble section.
To prevent clicks at changing bass and/or treble settings, the bank switching principle is used.
In next section the calculations for first order high pass with first order low pass are described.
To prevent overflow in the case of bass and/or treble gain, a compensation factor TCC is combined with balance coefficients Y:BALLn and Y:BALRn. (see section 9.1.1.2.1)

9.1.5.2 RAM memory use for Tone control

X:audioc

Bank0	Bank1
Y:Ctl0	Y:Ctl1
Y:Cth0	Y:Cth1
Y:Btl0	Y:Btl1
Y:Bth0	Y:Bth1
Y:At00	Y:At01
Y:At10	Y:At11
Y:At20	Y:At21
Y:KTrt0	Y:KTrt1
Y:KTft0	Y:KTft1
Y:KTmid0	Y:KTmid1
Y:KTbas0	Y:KTbas1
Y:KTtre0	Y:KTtre1
Y:BALL0	Y:BALL1
Y:BALR0	Y:BALR1

The pointer X:audioc hold the startaddress of the selected bank. Each of this bank contains 10 single precision and 2 double precision YRAM coefficients.

9.1.5.3 Calculation of Tone Control

First Order Bass

Input variables:	gb:	Gain	[dB]	Output coefficients:	Y:At0n, Y:At1n, Y:Cthn, Y:Ctln Y:At2n=0 Y:Bthn=0,Y:Btln=0
	fgb:	Cutoff frequency	[Hz]		
	fs:	Sample frequency	[Hz]		
				Output variable:	KTbas'

$$if\ gb \geq 0\ then\ \ f\ =\ fgb\ -\ 3*|gb|$$

$$else\ \ f\ =\ \frac{fgb\ -\ 3*|gb|}{10^{\frac{gb}{20}}}$$

$$t0\ =\ \cos(2p*\frac{f}{fs})$$

$$CT\ =\ 0.5*\{\ \frac{1}{t}0\ +\ \sqrt{\frac{1}{t0^2}-1}\ \}$$

$$if\ |CT|\ >\ 1/2\ then$$

$$CT\ =\ 0.5*\{\ \frac{1}{t}0\ -\ \sqrt{\frac{1}{t0^2}-1}\ \}$$

$$Y:\ Cthn,Ctln\ =\ CT$$

$$Y:\ At0n\ =\ Y:\ At1n\ =\ \frac{1-2*CT}{4}$$

$$KTb\ =\ 10^{\frac{gb}{20}}-1$$

Due to the implementation of the coefficients Y:At0n and Y:At1n in single precision a modification of KTb is required to obtain the correct gain at centre frequency:

$$KTbas'\ =\ \frac{KTb}{Y:At0n}\bullet\frac{1-2*CT}{4}$$

where Y:At0n is the 12 bits truncated value of (1-2*CT)/4

Example: fgb=125 Hz, fs=44100 Hz, gb=-12 dB

f= 356 Hz, t0= 0.998714, CT= 0.475263 $3CD56B_H$ Y:Cthn= $3CD Y:Ctln= $265
(1- 2*CT)/4= 0.0123685 Y:At0n= Y:At1n= $019 (=0.0122070) KTbas'= -0.758718

Second order peaking low pass filter for Bass

Input variables:	f_c:	center frequency	[Hz]	Output coefficients:	Y:At0n, Y:At2n
	fs:	sample frequency	[Hz]		Y:Cthn, Y:Ctln
	Q:	shape factor	[-]		Y:Bthn, Y:Btln
	gb:	Gain	[dB]		Y:At1n=0
				Output variable:	KTbas'

The shape factor is defined by:
(with f_1 and f_2 being the -3 dB turn-over frequencies)

$$Q = \frac{f_c}{f_2 - f_1}$$

$$t0 = \frac{2p \bullet f_c}{fs}$$

$$B'T = -0.5 \bullet \frac{1 - \tan(t\frac{0}{2Q})}{1 + \tan(t\frac{0}{2Q})}$$

$$C'T = (0.5 - B'T)\cos(t0)$$

$$A'T = (0.5 + B'T) / 2$$

$$KTb = 10^{\frac{|gb|}{20}} - 1$$

$$Y:Bthn, Y:Btln = BT = B'T$$
$$Y:Cthn, Y:Ctln = CT = C'T$$
$$Y:At0n = Y:At2n = AT = A'T$$

Due to the implementation of the coefficients Y:At0n and Y:At2n in single precision a modification of KTbas is required to obtain the correct gain at centre frequency:

$$KTbas' = \frac{KTb}{Y:At0n} \bullet AT$$

where Y:At0n is the 12 bits truncated value of AT

If gb ≤ 0 then a modification of AT, BT and CT is required :

$$BT = \frac{B'T + (A'T \bullet KTb)}{1 + (2 \bullet A'T \bullet KTb)}$$

$$CT = \frac{C'T}{1 + (2 \bullet A'T \bullet KTb)}$$

$$AT = \frac{-A'T}{1 + (2 \bullet A'T \bullet KTb)}$$

Example 1 : f_c= 100 Hz, fs=44100 Hz, Q=1.65, gb= 6 dB :

t0 = 0.0142476

BT = BT' = -0.495701 = $C08CDE_H$	Y:Bthn = $C08	Y:Btln = $66F
AT = AT' = 0.0021495	Y:At0n = $004(= 0.0019531)	
	Y:At2n = $004	
CT = CT' = 0.9956 = $7F6FD2_H$	Y:CThn = $7F6	Y:CTln = $7E9

KTb = 0.995262

KTbas'= 0.995262* 0.0021495/ 0.0019531 = 1.0953

Example 2 : f_c= 100 Hz, fs=44100 Hz, Q=1.65, gb= -6 dB :

t0 = 0.0142476

BT` = -0.495701

AT` = 0.0021495

CT` = 0.9956

KTb = 0.995262

KTbas'= 0.995262* 0.0021495/ 0.0019531 = 1.0953

BT = -0.491459 = $C117DF_H$	Y:Bthn = $C11	Y:Btln = $3EF
CT = 0.9913584 = $7EE4D5_H$	Y:CThn = $7EE	Y:CTln = $26A
AT = -0.0021403	Y:At0n = $FFC	
	Y:At2n = $FFC	

First order Treble

Input variables:	gt:	Gain	[dB]	Output coefficients:	Y:KTftn
	fgt:	Cutoff frequency	[Hz]		Y:KTrtn
	fs:	Sample frequency	[Hz]	Output variable:	KTtre'

$$if\ gt < 0\ then\ \ t0 = \cos(2p * \frac{fgt}{fs} * 10^{\frac{gt}{20}})$$

$$else\ \ t0 = \cos(2p * \frac{fgt}{fs})$$

$$KTrt = \frac{1}{t}0 + \sqrt{\frac{1}{t0^2} - 1}$$

$$if\ |KTrt| > 1\ \ then$$

$$KTrt = \frac{1}{t}0 - \sqrt{\frac{1}{t0^2} - 1}$$

$$Y: KTftn = \frac{1 + KTrt}{2}$$

$$Y: KTrtn = KTrt$$

$$KTtre' = 10^{\frac{gt}{20}} - 1$$

Example: gt= 12 dB, fgt= 5 kHz, fs= 44100 Hz:

t0= 0.756809 KTrt= 0.457666 Y:KTrtn= $3A9
KTft= 1.457666/2 Y:KTftn= $5D5
KTtre'= 2.981

Scaling Tone Control

Input variables:	Bass Gain	gb	[dB]	Output coefficients:	Y:KTbasn
	Treble Gain	gt	[dB]		Y:KTtren
	KTbas'				Y:KTmidn
	KTtre'			Output variable: TCC (Y:BALLn,Y:BALRn)	

To prevent overflow, the maximum gain of the tone filter is limited to 0 dB, independent on the setting. The +15 dB gain is realized afterwards with coefficient TCC and a 3 bit shifter. TCC is combined with the Y:BALLn, Y:BALRn coefficient in the Balance function. See section 9.1.1.2.
Depending on the filter gain coefficients Y:KTbasn, Y:KTtren, Y:KTmidn and TCC need to be scaled.

The scaling factor Cscal is the maximum of glb, glt and 1:

glb =	10^(gb/20)	{in case of first order bass filter}
glb =	10^(|gb|/20)	{in case of second order peaking low pass bass filter}
glt =	10^(gt/20)	

Cscal =	max(glb, glt, 1)
KTbas =	KTbas'/Cscal
KTtre =	KTtre'/Cscal
KTmid =	1/Cscal

TCC = Cscal/8

$$Y: KTmidn = KTmid$$
$$Y: KTbasn = KTbas$$
$$Y: KTtren = KTtre$$

The filter gain coefficients Y:KTbasn, Y:KTtren, Y:KTmidn are 3 coefficients out of a group of 14 general audio coefficients in banks used for bankswitching.

In case of **first order bass filter** the attenuation at 1 kHz increases if low and high frequencies are both cutoff. In that case the effective attenuation is less then expected.
If the attenuation of frequency components around 1 kHz is not desired an additional modification of the coefficients calculated above is required :

If gb<0 and gt<0 then

$$TCC = TCC*(1+0.35*(\frac{KTtre+KTbas}{2})^2)$$

$$Y:KTbasn = KTbas*(1.2+0.2*KTbas)$$

$$Y:KTtren = KTtre*(1.2+0.2*KTtre)$$

Example: gb= -12 dB, gt= 12 dB, KTbas'= -0.758718, KTtre'= 2.981

glb= 0.251, glt= 3.981	Cscal= 3.981
KTbas= -0.190585	Y:KTbasn= $E7A
KTtre= 0.748807	Y:KTtren= $5FE
KTmid= 0.251189	Y:KTmidn= $202
TCC= 0.497634	Y:BALLn, Y:BALRn= $3FB (balance = 1.0)

Note : this additional modification of coefficients is NOT applicable in case of the second order peaking low pass filter for Bass.

9.1.5.4 Required controller actions for Tone Control

The calculated coefficients starting Y:Ctln till Y:BALRn are loaded in the (passive) coefficient bank. After all prepared coefficients are loaded in this passive bank, then a bank switching command must be issued to activate this new group:

To activate bank0: X:audioc= #02C00
bank1: X:audioc= #02F80

9.1.6 Equalizer

To optimize sound reproduction in the car, a hardware parametric equalizer is incorporated in the CDSP chip. Its processing is included in the audio processing block.
Applications of the equalizer are:

- compensation for the vehicle's acoustic limitations.
- predefined, mode dependent frequency response.
- extension of the tone control.

9.1.6.1 Functional description

The equalizer consists of 20 second order sections .
These 20 sections can be grouped as 4*5 (each DAC channel) or 2*10 (Left and Right channel)

Of all 20 sections the centre frequency, gain and Q-factor can be set independently from each other. Every section is followed by a variable attenuation by 0 or 6 dB. Two 16 bits words per section are needed to store these settings.

The Equalizer & 2nd Processor block in fig. 9.1 can be used as shown in next graphs.
In case Equalizer without 2nd Processor:

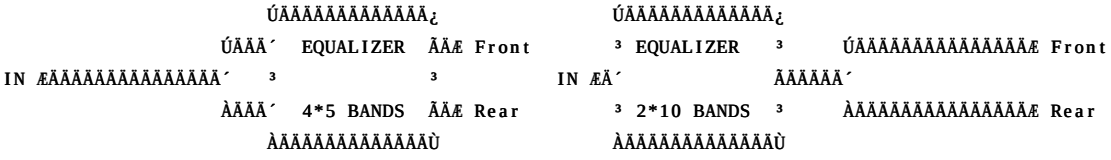


Fig. 9.7.0.1 Equalizer possibilities without 2nd Processor

In case Equalizer together with 2nd Processor: (see also paragraph 9.12)

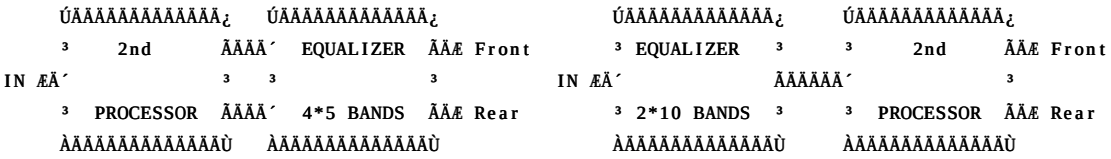


Fig. 9.7.0.2 Equalizer possibilities together with 2nd Processor

Equalizer configurations

4-channel configuration

In the 4-channel configuration there are 5 equalizer sections available for each DAC channel.
The equalizer sections are grouped as depicted in figure 9.7.0.3. The numbers in the equalizer sections are equal to the section-id numbers as used by the equalizer software tool.
To select the 4-channel configuration : set bit 12 (TWO-FOUR) of the IIC_AD register
(address $0FFD) = 0

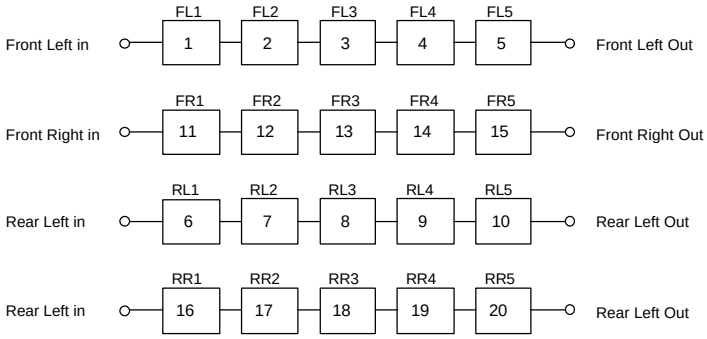


Fig. 9.7.0.3 4-channel equalizer configuration

2-channel configuration

In the 2-channel configuration there are 10 equalizer sections available for the Left- and Right channels.
The equalizer sections are grouped as depicted figure 9.7.0.4. The numbers in the equalizer sections are equal to the section-id numbers as used by the equalizer software tool.
To select the 2-channel configuration : set bit 12 (TWO-FOUR) of the IIC_AD register
(address $0FFD) = 1

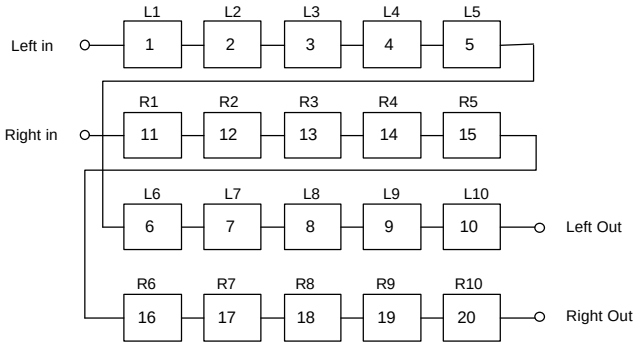


Fig. 9.7.0.4 2-channel equalizer configuration

9.1.6.2 Calculations of Equalizer

The equalizer is controlled by coefficient words that are stored in hardware I2C registers.
Each equalizer section uses 2 coefficient words, "word1" and "word2".
A software tool for PC is available to compute the 2 coefficient words for the given center frequency, gain and shape factor.

If the center frequency and shape factor of the equalizer sections can remain unchanged, the gains can be changed by writing new "Word2" coefficients only. Therefor, the "Word2" coefficients are stored in consecutive coefficient memory locations and the equalizer memory consists of a "Word1" segment and a "Word2" segment, each 20 positions long. See par. 9.1.6.3 for detailed information about the equalizer memory map.

Note that all 20 equalizer sections are always active; it is not possible to disable one or more sections. For this reason all sections must be initialized with their coefficients words. Equalizer sections can be set to a flat response by setting their gain to 0 dB.

Equalizer software tool

The equalizer software tool calculates the coefficient words for the equalizer sections.
The program uses the following input variables :

Variables that are valid for all sections :

fs:	sample frequency	[kHz]
configuration:	4-channel or 2-channel	[-]

Equalizer section specific variables :

f_c:	centre frequency	[Hz]
G_{dB}:	gain at centre freq.	[dB]
Q:	shape factor	[-]
output scaling:	0 or -6	[dB]
bandfilter_id:	1 ... 20 (see figures 9.7.0.3 and 9.7.0.4)	

Equalizer software tool program files

The equalizer software tools consists of the following files:

EQU.EXE	(the executable file)
COEFINP.DAT	(sample input file)
COEFOUTP.LOG	(output file with calculated coefficient words)

To run the executable :

1) Edit the input file coefinp.dat and enter the general equalizer settings :
   - sample frequency
   - 2x10 or 4x5 channel configuration

   Enter the required equalizer settings per section :
   bandfilter_id, gain, shape factor, center frequency and optional scaling

   Note that the bandfilter_id corresponds with the section numbers in figures 9.7.0.3 and 9.7.0.4 of this document.

   Since the equalizer program processes line per line of the inputfile it is possible to make the program calculate more then one setting of the same equalizer section or to change the sample frequency and equalizer configuration (2-channel/4-channel) at some point.
   See the next page for a inputfile example.

2) Run the program with command EQU

   Note that there is no response on the screen from the program, syntax errors in the input file will be reported in the output logfile.

3) The calculated coefficient words with their coefficient memory address and the (re-calculated) realized equalizer characteristics are written to the output file "coefoutp.log".

   Notes :

   1. If the optional -6dB output scaling is set for a section then the output signal of the equalizer section is attenuated 6dB. The gain at the center frequency is 6 dB lower then the calculated realized gain as reported in the output logfile. In normal applications there is no need to use the additional output scaling since the gain range without output scaling is -30dB .... +12dB.

   2. The output file will be overwritten by the program when running equ.exe again.

```
# Sample equalizer input file
# for SAA7705H equalizer
# Equalizer command lines should start with "$"
#
# Command syntax :
# ----------------
# 1) Set sample frequency [Hz] : the next 2 lines set fs=38 KHz
# $s
# $38000.
#
# 2) Set equalizer configuration, 0 = 4-channel ; 1 = 2-channel
#    the next 2 lines set configuration = 4-channel
# $c
# $ 0
#
# 3) Enter the equalizer section variables :
#      bandfilt_id (1 ... 20)  [-]
#      f_center                [Hz]
#      Q-factor                [-]
#      Gain (-30 ... +12)      [dB]
#      Output scaling 0 = NO scaling ; 1 = -6 dB scaling
#
#      Each equalizer section definition line should be preceded with the calculation execution
#      command "x".
#
$c
$ 0
$s
$ 38000.
$x
$ 1 100 1 10 0
$x
$ 2 500 0.5 -4 0
$x
$ 3 1000 1.1 3 0
$x
$ 4 5000 0.5 0 0
$x
$ 5 10000 0.85 -4 0
$x
$ 6 100 2.3 12 0
$x
$ 7 500 0.7 -6 0
$x
$ 8 1000 0.5 -10 0
$x
$ 9 5000 1 12 0
$x
$ 10 10000 2 -3.2 0
$x
$ 11 100 1.2 3 0
$x
$ 12 500 0.5 0 0
$x
$ 13 1000 1.5 3 0
$x
$ 14 5000 1.2 -9 0
$x
$ 15 10000 0.5 0 0
$x
$ 16 100 2.5 -3 0
$x
$ 17 500 1.4 2 0
$x
$ 18 1000 0.5 4 0
$x
$ 19 5000 0.7 -5 0
$x
$ 20 10000 1.2 8.5 0
```

9.1.6.3 RAM memory use for Equalizer

The 20 equalizer sections require a total of 40 coefficients. These are stored in a specific order in the coefficient memory. The order is chosen in such a way, that it is possible to update *word1* or *word2* of the sections with the same execution order within each channel by using incremental addressing. The coefficient addresses are defined in the table below, the filter sections are labeled with the section id's of figure 9.7.0.3 and figure 9.7.0.4.

Equalizer coefficient memory map

Section id#	section function		Word1 address	Word2 address
	2-chan config	4-chan config		
1	FL1	L1	$0F80	$0F94
11	FR1	R1	$0F81	$0F95
6	RL1	L6	$0F82	$0F96
16	RR1	R6	$0F83	$0F97
2	FL2	L2	$0F84	$0F98
12	FR2	R2	$0F85	$0F99
7	RL2	L7	$0F86	$0F9A
17	RR2	R7	$0F87	$0F9B
3	FL3	L3	$0F88	$0F9C
13	FR3	R3	$0F89	$0F9D
8	RL3	L8	$0F8A	$0F9E
18	RR3	R8	$0F8B	$0F9F
4	FL4	L4	$0F8C	$0FA0
14	FR4	R4	$0F8D	$0FA1
9	RL4	L9	$0F8E	$0FA2
19	RR4	R9	$0F8F	$0FA3
5	FL5	L5	$0F90	$0FA4
15	FR5	R5	$0F91	$0FA5
10	RL5	L10	$0F92	$0FA6
20	RR5	R10	$0F93	$0FA7

9.1.6.4 Required controller actions for Equalizer

Initialisation at power up

At power up the equalizer coefficient words are NOT automatically initialized.
Before the equalizer is used in an application mode of the SAA7705H, the equalizer should be loaded with valid coefficients to its RAM. Since all equalizer sections are active it is required to load the coefficient words of ALL 20 sections. It is advised to set all sections to a flat response (gain = 0 dB) after power up.

Setting of the equalizer configuration

To select the 4-channel configuration bit 12 (TWO-FOUR) of the IIC_AD register must be set "0".

To select the 2-channel configuration bit 12 (TWO-FOUR) of the IIC_AD register must be set "1".

The IIC_AD register is one of the hardware I2C registers in SAA7705H that should be set at power on or during mode switching. See the SAA7705H usermanual for further information about hardware I2C register settings.

Gain setting of the equalizer sections

The equalizer gain must be changed in steps of maximum 1 dB to prevent switching noise. If the change in equalizer shape is big, an additional audio muting is preferred to prevent clicking noise.

9.1.6.4.1 Digital line out mode

In this mode no subwoofer processing (for subwoofer see par 9.1.7) is possible because IISout2 channel is in use for digital line out and no second processor interaction is available (for second processor see par 9.12) because the signal IISout1 to this second processor is needed for digital line out.

- equalizer **off**

After using equalizer change EqualizerGain in steps of max. 1 dB towards EqualizerGain= 0. (flat response)

To start next configuration <No 2nd Processor,IIS and no equalizer>:
- load Y:OutSwi = $A45
- bit TWO-FOUR of IIC_AD register= don't care

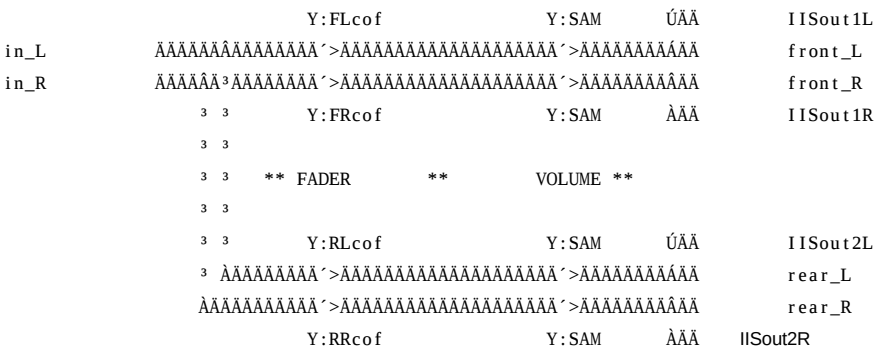


Fig. 9.7.1 Possible interconnections for Digital line out mode

- equalizer 4*5 bands **on**

To start next configuration <No 2nd Processor,IIS and 4*5 bands equalizer>:
- load Y:OutSwi = $A50
- bit TWO-FOUR of IIC_AD register= 0

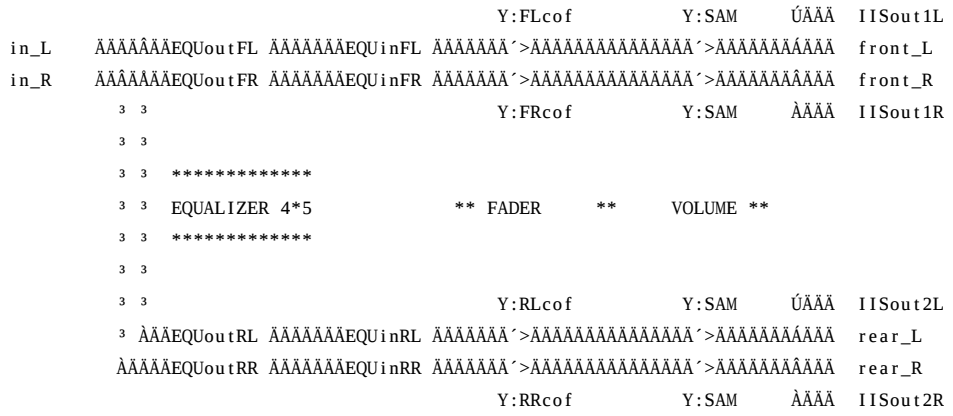


Fig. 9.7.2 Possible interconnections for Digital line out mode

****

- equalizer 2*10 bands **on**

To start next configuration <No 2nd Processor,IIS and 2* 10 bands equalizer>:
- load Y:OutSwi = $A49
- bit TWO-FOUR of IIC_AD register= 1

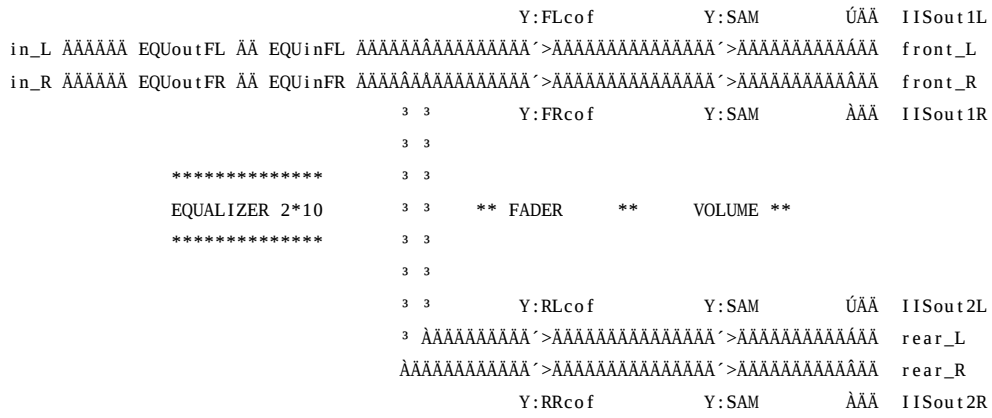


Fig. 9.7.3 Possible interconnections for Digital line out mode

9.1.6.4.2 Equalizer with separate Subwoofer function

The digital output IISout1 is primarily meant for interfacing with equalizer or second processor. Digital port IISout2 is used as the subwoofer channel. (see section 9.1.7)

Next 6 blockdiagrams (fig. 9.8.1 and 9.8.2) gives the 6 different choices for possible interconnections between equalizer and/or 2nd processor.

First 3 groups don't use the possibilities of a second processor.

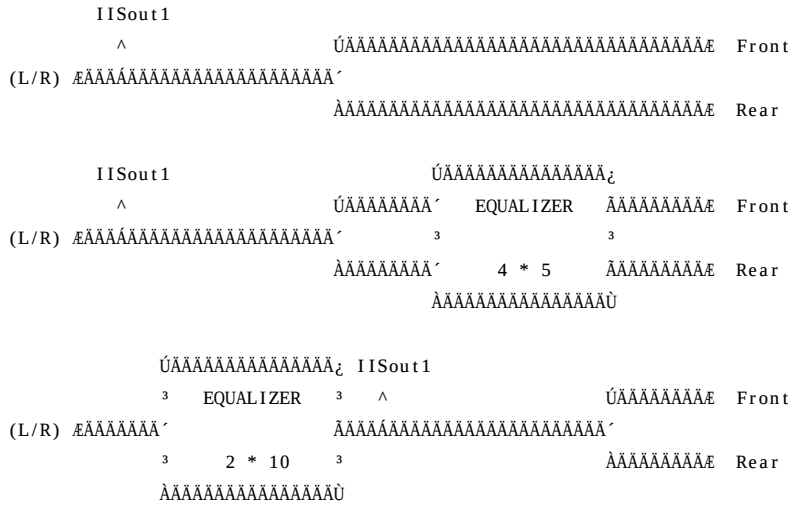


Fig. 9.8.1 Possible interconnections of Equalizer only

Next 3 groups make use of a second processor (see section chapter 9.12 for additional information about the second processor).

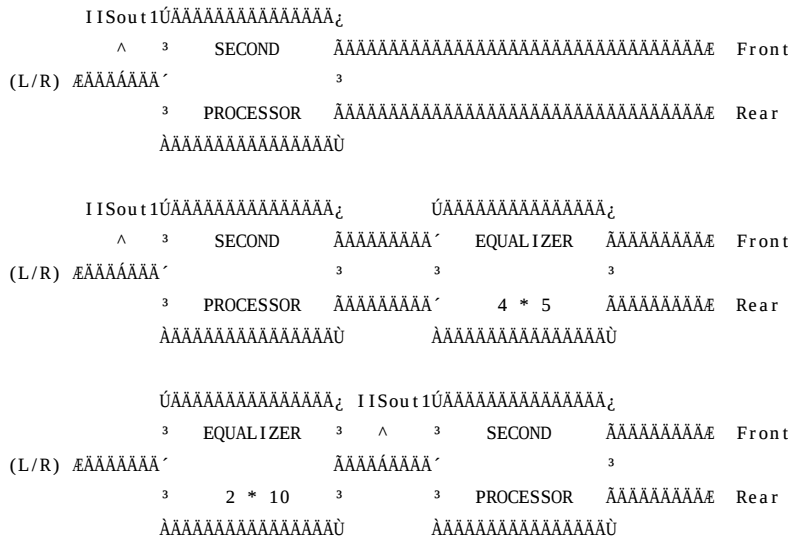


Fig. 9.8.2 Possible interconnections of Equalizer together with 2nd Processor

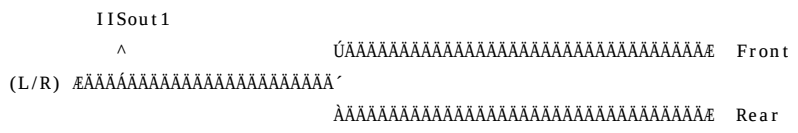
The required actions to select all above mentioned possibilities are specified on next pages.

9.1.6.4.3 Required action controls Equalizer (second processor off)

- equalizer **off**

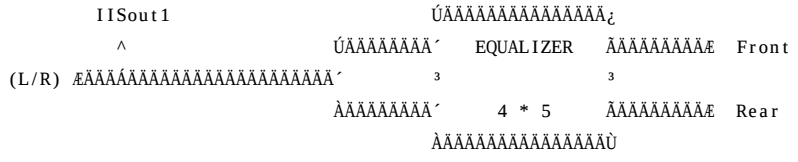
After using equalizer change EqualizerGain in steps of max. 1 dB towards EqualizerGain= 0. (flat response)

To start next configuration <No 2nd Processor,DAC and no equalizer>:
- load Y:OutSwi = $A76
- bit TWO-FOUR of IIC_AD register = don't care.



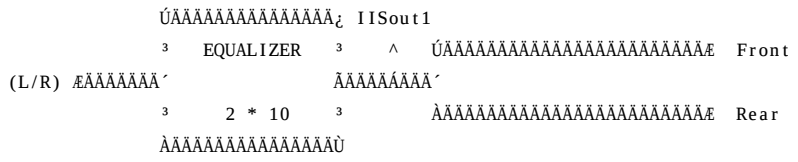
- equalizer 4*5 bands **on**

To start next configuration <No 2nd Processor,DAC and 4*5 bands equalizer>:
- load Y:OutSwi = $A85
- bit TWO-FOUR of IIC_AD register= 0



- equalizer 2*10 bands **on**

To start next configuration <No 2nd Processor,DAC and 2*10 bands equalizer>:
- load Y:OutSwi = $A7C
- bit TWO-FOUR of IIC_AD register= 1



Second processor **on**.

A) no Equalizer (Subwoofer enabled)	See second processor section 9.12.4
B) 4*5 bands Equalizer (Subwoofer enabled)	See second processor section 9.12.4
C) 2*10 bands Equalizer (Subwoofer enabled)	See second processor section 9.12.4

9.1.7 Subwoofer

The second digital IIS output port is primarily used to offer the user Subwoofer functions
These functions are NOT available during 4 channel Digital Line Out mode. (section 9.1.6.4.1)
Next paragraphs describe the two implemented Subwoofer functions, being:

- Subwoofer with 4th order low pass together with flat Center
- Subwoofer Left and Right, with a second order low pass for each

With external D/A converters these signals can be made audible to the user.

9.1.7.1 Subwoofer and Center.

9.1.7.1.1 Functional description.

The Center function is derived from the sum signals of the Front channels just in front of the Soft Audio Mute coefficient (Y:SAM). (see fig. 9.9). This signal can have an additional gain of 24 dB maximum before it is multiplied with Y:SAM. The result is stored in X:Center and is sent to IISout2R.

The Subwoofer function is derived from the sum signals of all 4 audio channels just in front of the fader coefficients and passes a fourth order low pass filter with additional 24 dB possible gain before it is multiplied with Y:SAM. The signal just in front of Y:SAM is stored in X:Subwoofer. The Subwoofer output is sent to IISout2L.

Fig. 9.9 Subwoofer and Center function.

9.1.7.2 RAM Memory use for Subwoofer and Center.

The 4th order subwoofer low pass filter is initialized by coefficients

Y:ca11l	Y:pa11l	Y:outSwi
Y:ca11h	Y:pa11h	Y:IISout2
Y:ca12l	Y:pa12l	Y:volSubw
Y:ca12h	Y:pa12h	Y:scalCenter
Y:cb10l	Y:pb10l	
Y:cb10h	Y:pb10h	
Y:cb11l	Y:pb11l	
Y:cb11h	Y:pb11h	
Y:cb12l	Y:pb12l	
Y:cb12h	Y:pb12h	

Depending of value Y:OutSwi it can be decided to select output IISout2 to be used for Digital Line Out or Subwoofer/Center function.
Subwoofer gain is located in Y:volSubW. Possible gain 24 dB.
Center gain is located in Y:scalCenter. Possible gain 24 dB.

9.1.7.3 Control actions for Subwoofer and Center.

With easy programming (cold start directly after leaving waitloop after reset) the coefficients for the 4th order Butterworth low pass filter are loaded for with cut off frequency fkb= 100 Hz and sample frequency fs= 38 kHz.

Y:ca11l	=$6BA	Y:pa11l	=$684
Y:ca11h	=$7E0	Y:pa11h	=$7F2
Y:ca12l	=$70E	Y:pa12l	=$73F
Y:ca12h	=$c1E	Y:pa12h	=$C0C
Y:cb10l	=$08D	Y:pb10l	=$08F
Y:cb10h	=$000	Y:pb10h	=$000
Y:cb11l	=$11B	Y:pb11l	=$11E
Y:cb11h	=$000	Y:pb11h	=$000
Y:cb12l	=$08D	Y:pb12l	=$08F
Y:cb12h	=$000	Y:pb12h	=$000

The default values of next coefficients (easy programming ALL set) are:

Subwoofer & flat Center selected	Y:IIS2outs	= $AC5
Volume Subwoofer 0 dB	Y:volSubw	= $F80
Volume Center 0 dB	Y:scalCenter	= $80
Output :no 2nd Processor no Equalizer	Y:Outswi	= $A76

Subwoofer Gain default (easy programming ALL set) 0dB Y:volSubw= $F80
For processing the Subwoofer Gain apply next equation:

Input variable: SG: Subwoofer Gain [dB] (max 24 dB) Output coefficient: Y:volSubW

$$Y: volSubW = -\frac{10^{\frac{SG}{20}}}{16}$$

Example: SG= 2 dB
Y:volSubw= (-10^(2/20))/16= (-10^0.1)/16)= -1.258925/16= -0.078683 ($F5F)

Center Gain default (easy programming ALL set) 0dB Y:scalCenter= $80
For processing the Center Gain apply next equation:

Input variable: CG: Center Gain [dB] (max 24 dB) Output coefficient: Y:scalCenter

$$Y: scalCenter = \frac{10^{\frac{CG}{20}}}{16}$$

Example: CG= 2 dB
Y:scalCenter= (10^(2/20))/16= (10^0.1)/16)= 1.258925/16= 0.078683 ($0A1)

To apply different cut off frequencies and/or samplefrequencies use lookup tables (9.23.1, 9.23.2 and 9.23.3). Here the coefficient values are given for 2nd order Butterworth low pass filter.

First low pass Filter (F_s= 38 kHz)										
fkb [Hz]	ca11		ca12		cb10		cb11		cb12	
	Y:ca11l	Y:ca11h	Y:ca12l	Y:ca12h	Y:cb10l	Y:cb10h	Y:cb11l	Y:cb11h	Y:cb12l	Y:cb12h
40	$19C	$7F3	$604	$C0C	$016	$000	$02F	$000	$019	$000
60	$246	$7ED	$4EC	$C12	$031	$000	$066	$000	$034	$000
80	$07E	$7E7	$616	$C18	$05A	$000	$0B5	$000	$05A	$000
100	$6BA	$7E0	$70E	$C1E	$08D	$000	$11B	$000	$08D	$000
120	$4F4	$7DA	$7DC	$C24	$0CB	$000	$198	$000	$0CB	$000
Second low pass filter (F_s= 38 kHz)										
fkb [Hz]	pa11		pa12		pb10		pb11		pb12	
	Y:pa11l	Y:pa11h	Y:pa12l	Y:pa12h	Y:pb10l	Y:pb10h	Y:pb11l	Y:pb11h	Y:pb12l	Y:pb12h
40	$536	$7FA	$269	$C05	$019	$000	$02F	$000	$016	$000
60	$12D	$7F8	$604	$C07	$034	$000	$066	$000	$032	$000
80	$3EF	$7F5	$2A3	$C0A	$05B	$000	$0B6	$000	$05B	$000
100	$684	$7F2	$73F	$C0C	$08F	$000	$11E	$000	$08F	$000
120	$0EB	$7F0	$3DC	$C0F	$0CE	$000	$19C	$000	$0CB	$000

Table 9.23.1 Subwoofer filter with 4th order low pass (fs = 38 kHz)

First low pass Filter (F_s= 44.1 kHz)										
fkb [Hz]	ca11		ca12		cb10		cb11		cb12	
	Y:ca11l	Y:ca11h	Y:ca12l	Y:ca12h	Y:cb10l	Y:cb10h	Y:cb11l	Y:cb11h	Y:cb12l	Y:cb12h
40	$7C0	$7F4	$7F9	$C0A	$010	$000	$023	$000	$010	$000
60	$6F2	$7EF	$076	$C10	$024	$000	$04C	$000	$028	$000
80	$408	$7EA	$2E9	$C15	$041	$000	$087	$000	$045	$000
100	$125	$7E5	$535	$C1A	$069	$000	$0D2	$000	$069	$000
120	$643	$7DF	$75E	$C1F	$097	$000	$12F	$000	$097	$000
Second low pass filter (F_s= 44.1 kHz)										
fkb [Hz]	pa11		pa12		pb10		pb11		pb12	
	Y:pa11l	Y:pa11h	Y:pa12l	Y:pa12h	Y:pb10l	Y:pb10h	Y:pb11l	Y:pb11h	Y:pb12l	Y:pb12h
40	$32A	$7FB	$48E	$C04	$013	$000	$023	$000	$010	$000
60	$1F2	$7F9	$575	$C06	$028	$000	$04C	$000	$024	$000
80	$7B5	$7F6	$73B	$C08	$045	$000	$087	$000	$042	$000
100	$559	$7F4	$0FE	$C0B	$06A	$000	$0D4	$000	$06A	$000
120	$2DB	$7F2	$2C0	$C0D	$099	$000	$131	$000	$099	$000

Table 9.23.2 Subwoofer filter with 4th order low pass (fs = 44.1 kHz)

First low pass Filter (F_s= 48 kHz)										
fkb [Hz]	ca11		ca12		cb10		cb11		cb12	
	Y:ca11l	Y:ca11h	Y:ca12l	Y:ca12h	Y:cb10l	Y:cb10h	Y:cb11l	Y:cb11h	Y:cb12l	Y:cb12h
40	$04A	$7F6	$77B	$C09	$00D	$000	$01C	$000	$010	$000
60	$0D1	$7F1	$6AC	$C0E	$020	$000	$041	$000	$020	$000
80	$1FA	$7EC	$522	$C13	$037	$000	$072	$000	$03A	$000
100	$291	$7E7	$40B	$C18	$056	$000	$0B1	$000	$05B	$000
120	$32B	$7E2	$2D4	$C1D	$07D	$000	$0FF	$000	$082	$000
Second low pass filter (F_s= 48 kHz)										
fkb [Hz]	pa11		pa12		pb10		pb11		pb12	
	Y:pa11l	Y:pa11h	Y:pa12l	Y:pa12h	Y:pb10l	Y:pb10h	Y:pb11l	Y:pb11h	Y:pb12l	Y:pb12h
40	$6C1	$7FB	$104	$C04	$010	$000	$01C	$000	$00D	$000
60	$620	$7F9	$15E	$C06	$020	$000	$041	$000	$020	$000
80	$5A6	$7F7	$174	$C08	$03B	$000	$072	$000	$037	$000
100	$4D2	$7F5	$1C7	$C0A	$05C	$000	$0B3	$000	$056	$000
120	$3E3	$7F3	$218	$C0C	$083	$000	$102	$000	$07E	$000

Table 9.23.3 Subwoofer filter with 4th order low pass (fs = 48 kHz)

9.1.8 Subwoofer Left and Right.

9.1.8.1 Functional description.

These functions are NOT available during 4 channel Digital Line Out mode. (section 9.1.6.4.1)
The Subwoofer Left function is derived from the signals of the Left channels Front and Rear in front of the fader coefficients. This signal passes a second order low pass filter and can have an additional 24 dB gain before it is stored in X:Center. This last signal is multiplied with Y:SAM and sent to IISout2L.
The Subwoofer Right function is derived from the sum signals of the two Right audio channels. This signal passes a second order low pass filter and can have an additional 24 dB gain before it is multiplied with Y:SAM. (see fig. 9.10). The signal in front of Y:SAM is stored in X:SubWoof. The Subwoofer output is sent to IISout2R.
Note that these 2 subwoofer signals share the same volume setting coefficient Y:volSubw.

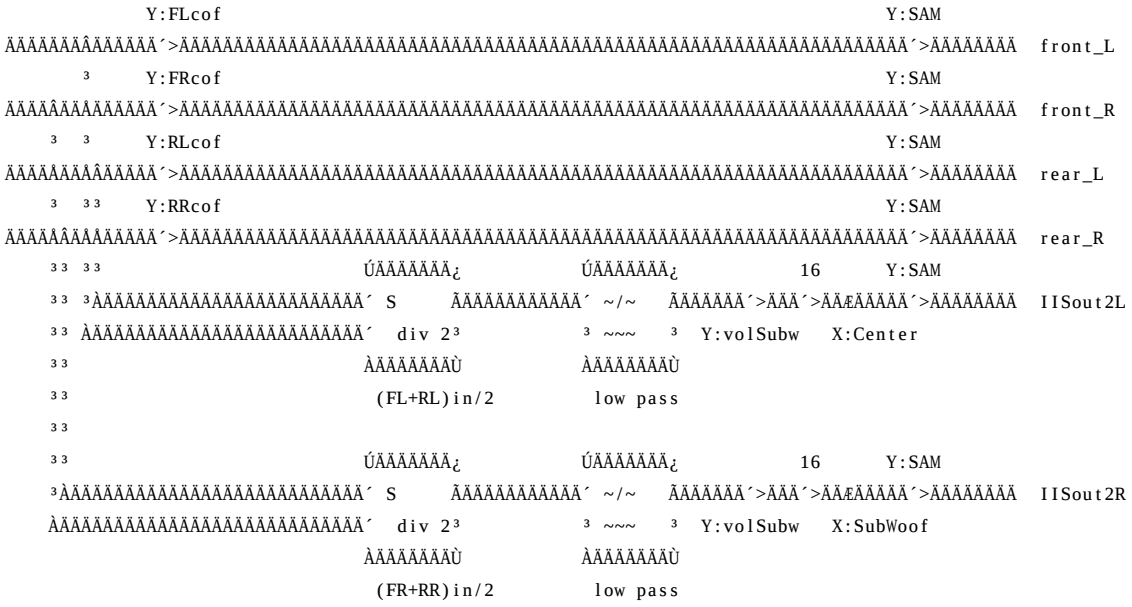


Fig. 9.10 Subwoofer Left and Right function.

9.1.8.2 RAM Memory use for Subwoofer Left and Right.

The 2nd order subwoofer low pass filter is initialized by coefficients

Y:ca11l	Y:cb10l	Y:OutSwi
Y:ca11h	Y:cb10h	Y:IISout2
Y:ca12l	Y:cb11l	Y:volSubW
Y:ca12h	Y:cb11h	
	Y:cb12l	
	Y:cb12h	

Subwoofer gain located in Y:volSubW. The maximum gain that can be realized is 24 dB.

9.1.8.3 Control actions for Subwoofer Left and Right.

With easy programming (cold start directly after reset) the coefficients for the 4th order elliptic low pass filter are loaded for cut off frequency fkb= 100 Hz and sample frequency fs= 38 kHz.
Only the coefficients of its first filtersection are used. The coefficients might be used as 'default' values, but it is better to refer to values mentioned in tables 9.24.1, 9.24.2 and 9.24.3

Y:ca11l = $306	Y:cb10l = $1CC
Y:ca11h = $7ED	Y:cb10h = $00A
Y:ca12l = $284	Y:cb11l = $699
Y:ca12h = $C12	Y:cb11h = $FEB
	Y:cb12l = $1CC
	Y:cb12h = $00A

For selecting Subwoofer Left and Right function load Y:IIS2outs= $B06

Subwoofer Gain default (easy programming ALL set) 0dB Y:volSubw= $F80
For processing the Subwoofer Gain apply next equation:

Input variable: SG: Subwoofer Gain [dB] (max 24 dB) Output coefficient: Y:volSubW

$$Y:\ volSubW\ =\ -\frac{10^{\frac{SG}{20}}}{16}$$

Example: SG= 2 dB
Y:volSubw= (-10^(2/20))/16= (-10^0.1)/16)= -1.258925/16= -0.078683 ($F5F)

To apply different cut off frequencies and/or samplefrequencies use next lookup tables. Here the coefficient values are given for 2nd order Butterworth low pass filter.

Filter for 2nd order low pass (F_s= 38 kHz)										
fkb [Hz]	ca11		ca12		cb10		cb11		cb12	
	Y:ca11l	Y:ca11h	Y:ca12l	Y:ca12h	Y:cb10l	Y:cb10h	Y:cb11l	Y:cb11h	Y:cb12l	Y:cb12h
40	$358	$7F6	$44C	$C09	$016	$000	$02D	$000	$016	$000
60	$4F8	$7F1	$23A	$C0E	$033	$000	$066	$000	$033	$000
80	$688	$7EC	$00B	$C13	$05B	$000	$0B6	$000	$05B	$000
100	$003	$7E8	$5C4	$C17	$08E	$000	$11C	$000	$08E	$000
120	$163	$7E3	$369	$C1C	$0CC	$000	$199	$000	$0CC	$000

Table 9.24.1 Subwoofer filter with 2nd order low pass (fs = 38 kHz)

Filter for 2nd order low pass (F_s= 44.1 kHz)										
fkb [Hz]	ca11		ca12		cb10		cb11		cb12	
	Y:ca11l	Y:ca11h	Y:ca12l	Y:ca12h	Y:cb10l	Y:cb10h	Y:cb11l	Y:cb11h	Y:cb12l	Y:cb12h
40	$5F4	$7F7	$1C7	$C08	$010	$000	$021	$000	$010	$000
60	$4E6	$7F3	$281	$C0C	$026	$000	$04C	$000	$026	$000
80	$3CE	$7EF	$322	$C10	$043	$000	$087	$000	$043	$000
100	$2A9	$7EB	$3AF	$C14	$069	$000	$0D3	$000	$069	$000
120	$173	$7E7	$42C	$C18	$098	$000	$130	$000	$098	$000

Table 9.24.2 Subwoofer filter with 2nd order low pass (fs = 44.1 kHz)

Filter for 2nd order low pass (F_s= 48 kHz)										
fkb [Hz]	ca11		ca12		cb10		cb11		cb12	
	Y:ca11l	Y:ca11h	Y:ca12l	Y:ca12h	Y:cb10l	Y:cb10h	Y:cb11l	Y:cb11h	Y:cb12l	Y:cb12h
40	$32C	$7F8	$49A	$C07	$00E	$000	$01C	$000	$00E	$000
60	$4CF	$7F4	$2AF	$C0B	$020	$000	$040	$000	$020	$000
80	$66A	$7F0	$0B0	$C0F	$039	$000	$072	$000	$039	$000
100	$022	$7ED	$678	$C12	$059	$000	$0B2	$000	$059	$000
120	$1A6	$7E9	$457	$C16	$080	$000	$100	$000	$080	$000

Table 9.24.3 Subwoofer filter with 2nd order low pass (fs = 48 kHz)

9.2 AM/FM Signal Quality processing

9.2.1 Functional description

The level signal of the tuner is used for detection of the quality of a received station, being fieldstrength (AM and FM level information) and multipath. This information is used for FM dynamic signal processing (see the FM mode in chapter 9.3), AM signal processing (see the AM mode in chapter 9.4) and is also available for the controller (for search purposes and for RDS strategy).

The level signal of the tuner is processed and the following functions are performed:

- Adjustment of the FM or AM level information to a normalized level curve
- Fast normalized level information for the controller with a resolution of 8 bits, output at **X:LEVN**
- Filtered level information for the controller and FM dynamic signal processing, output at **X:LEVA**
- Fast multipath information for the controller and FM dynamic signal processing, output at **X:MLTFLIM**
- Average multipath information for the controller, output at **X:MLTA**

AM/FM signal quality processing is always executed and so the above mentioned signals are available in every mode.

Input and outputs

There is one DIO input register used: D:level, this contains the incoming level signal of the tuner with a resolution of 8 bits.
The memory places of the outputs are:

X:LEVN
X:LEVA
X:MLTFLIM
X:MLTA

X:LEVN and adjustment of FM and AM level

The level signal from the tuner has to be adjusted to a normalized level curve X:LEVN in the DSP. This to eliminate the spread on the level signal. The use of the normalized level minimizes the spread in the FM dynamic signal processing functions like softmute and stereo- and response control.
X:LEVN is not filtered and therefore suitable for fast fieldstrength information for the controller (e.g. during RDS updates). The response time is 100µs.
X:LEVN delivers a between 0 and 1 (Full Scale) normalized level value for the fieldstrength of the received station with a resolution of 8 bits. Fig. 9.11 shows the normalized level curve. LEVN-lin is the ideal normalized level curve. LEVN is the level curve after adjustment of the linear part of the level curve from the tuner to the LEVN-lin curve . The spread in non linearity of the level curve from the tuner, at low and at high fieldstrength, is not compensated in the DSP.

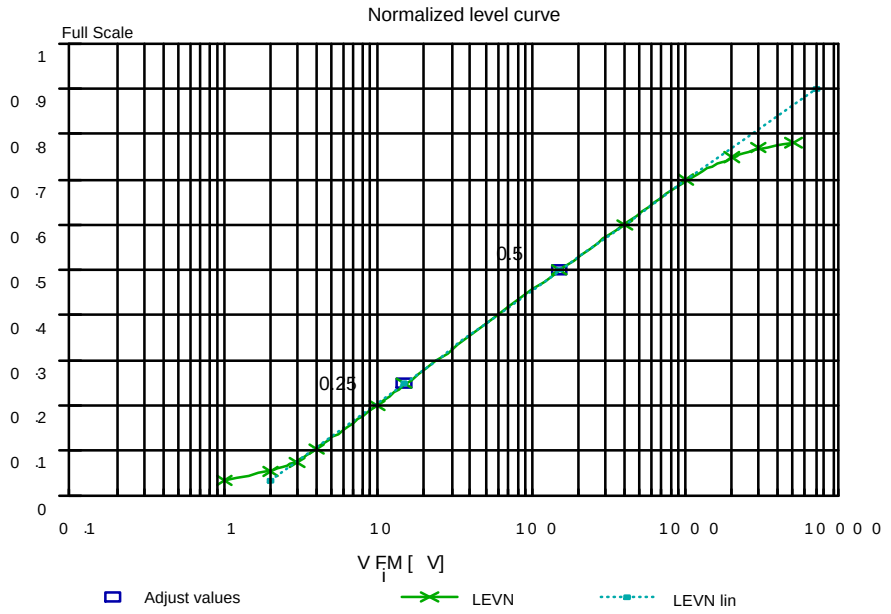


Fig. 9.11 Normalized and ideal level curve

X:LEVA

X:LEVA is a filtered level output of X:LEVN. The average amplitudes are equal. The aim of this filter is to attenuate the FM/AM conversion components. The response time of X:LEVA is 1 ms in FM mode, this is the optimal setting in combination with the TEA6811/6824 tuner. In case the SAA7705H is used with the TEA6840 tuner then the optimal response time of X:LEVA is 0.7 ms in FM mode. The response time of X:LEVA is 5 ms in AM mode, this is the optimal setting for both TEA6811/6824 and TEA6840 tuner.
The FM dynamic signal processing uses X:LEVA as level information.
If the response time of X:LEVA is fast enough for level measurements by the controller, this output is preferred above X:LEVN. Default the coefficients for the level filter are set to the values for the FM mode in combination with TEA6811/6824 tuner (loaded with Easy Programming set 'ALL'). For AM and FM in combination with the TEA6840 tuner they are according the following table.

Coefficient	FM mode with TEA6811/6824 (response time = 1 ms)	FM mode with TEA6840 (response time = 0.7 ms)	AM mode (response time = 5 ms)
Y:C21	$7CD	$7B4	$7F5
Y:C20	$066	$098	$016

9.2.2 Alignment level

X:LEVN and X:LEVA alignment for FM

The linear part of the incoming level curve has to be adjusted to the curve LEVN-lin to get the normalized level curve (see fig. 9.11). This adjustment is performed by the following formula:

X:LEVN= X:LEVA = 4(D:level*Y:p1+Y:q1)

D:level is the incoming level signal on the DIO register of the DSP and has a resolution of 8 bits.
With coefficient Y:p1 the gain (slope) and with Y:q1 the offset of the incoming level curve can be adapted.

Requirement for the normalized level curve:
Coefficients Y:p1 and Y:q1 have to be aligned such that X:LEVA becomes a 1/2 of Full scale for a fieldstrength value of 158 μV (-63 dBm) and 1/4 of Full scale for 15.8 μV (-83 dBm).

Alignment procedure:

- first initialize coefficients with Y:p1 = $200 and Y:q1 = $000
- then apply an RF FM carrier modulated with 1 kHz Δ f = 22.5 kHz to the Tuner via a Dummy antenna as given in fig. 8.13. of chapter 8.3.3.
- apply 158 μV and measure X:LEVA and convert to a fraction: value X:LEVA1
- then apply 15.8 μV and measure X:LEVA and convert to a fraction: value X:LEVA2
- calculate the new coefficient values with the formula's below:

$$Y{:}\,p1 = \frac{1}{16(X{:}\,LEVA1 - X{:}\,LEVA2)}$$

$$Y{:}\,q1 = \frac{1}{16} - (X{:}\,LEVA2 * p1)$$

- with the calculated values for Y:p1 and Y:q1 the normalized level curve X:LEVA should fulfil the above mentioned requirement.

Alignment for AM level

It is possible to align the level signal separately for FM and for AM. In case of a separate alignment for AM a second set Y:p1, Y:q1 for AM has to be defined.
A separate alignment can be required if AM signal processing for softmute and/or high cut control is activated and the applicated tuner has too much tolerance between the FM and AM level signal.
Alignment can be performed in a similar way as for FM.
In case of no AM signal processing the AM level information X:LEVA has only the purpose of AM fieldstrength information for the controller and no additional set Y:p1, Y:q1 is required, then:

Y:p1 (AM_mode) = Y:p1 (FM_mode)
Y:q1 (AM_mode) = Y:q1 (FM_mode)

9.2.3 Multipath detection

The implemented multipath detector detects the AM modulation of the level signal input around 19kHz. This results in a fast multipath output X:MLTFLIM. The multipath information is used for the FM dynamic signal processing and is also available for the controller.

A peak detector performs the multipath envelope detection. The response times for attack and recovery have been optimized and the default values are τa = 100 μs and τr = 3 ms.
The sensitivity of the multipath detector has to be aligned to **X:MLTFLIM = 0.65 of full scale at 50% AM** modulation with an 18 kHz sinewave.
Adjustment is done with Y:c1. Y:c1 has to be determined once for a FM Tuner type. The default value is valid for the tuner module with TEA6811\TEA6824.

Alignment maximum multipath on X:MLTFLIM

Apply an RF carrier with 50 % AM modulation with 18 kHz and a fieldstrength of 100 µV to the Tuner. Determine coefficient Y:c1 such that X:MLTFLIM becomes 0.65 of Full Scale. For Y:c1 a negative value has to be taken.

Default value: (loaded with Easy Programming)
Y:c1 $C32 ;alignment multipath, 50% AM = 0.65 F.S. for tuner module with TEA6811/TEA6824

Multipath information for the controller X:MLTA

For multipath information for the controller, a separate multipath filter with independent attack and recovery times is implemented. These attack and recovery times can freely be chosen by the user. This enables average or quasi peak measurements with fast or slow response of the multipath strength.
The attack time is determined by coefficient ta01=Y:ta011*Y:tr11 and the release time by coefficient tr1=Y:tr12*tr11. In order to realize long time constants Y:ta011 and Y:tr12 are scaled with Y:tr11.

Attack (rising slope) and recovery times (falling slope) are defined as the time needed to reach 63% of the total slope between zero and full scale.

The formula's to calculate the coefficients are:

$$ta01 = Y{:}ta011 * Y{:}tr11 = \frac{0.63}{fs(Hz) * attacktime(s)}$$

$$tr1 = \quad Y{:}tr12 * Y{:}tr11 = \frac{0.63}{fs(Hz) * recoverytime(s)}$$

fs = audio sample frequency (38, 44.1 or 48 kHz)

The default values are:

Y:ta011	$210	;attack time = 12ms (fs=38kHz)
Y:tr12	$108	;recovery time = 25ms (fs=38 KHz)
Y:tr11	$00A	;scaling factor

9.2.4 Required control actions

All mentioned default coefficient values for the AM/FM signal quality processing are automatically loaded with Easy Programming. If different values are required they have to be loaded by the micro controller. The level alignment values for Y:p1 and Y:p2 have to be loaded always by the micro controller. In case of separate alignments for FM and AM level, Y:p1 and Y:q1 have to be loaded with the values for AM in the AM mode and with the values for FM in all other modes.

9.3 FM Mode

9.3.1 Overview of Functions / Features

The FM program offers the following functions:

- Enhanced FM dynamic signal processing:
  The FM dynamic signal processing adapts the FM audio characteristics depending of the quality of the received station. As criterium to judge this quality the following parameters are used:
  - the level signal as a measure for the fieldstrength
  - the multipath detector output as a measure for the multipath distortion
  - the noise above 60 kHz of the MPX signal as a measure for adjacent channel interference.

  From the audio characteristics are the output level (softmute), the stereo image (Sliding stereo to mono) and the audio frequency response (High Cut control) adapted.

  The following functions are implemented:

  - Softmute as a function of level and noise:
    - fast attack and recovery at level dips with a low repetition rate
    - fast attack with slow recovery at dips with a high repetition rate or with a long duration.

  - Stereo control as a function of level and noise and multipath:
    - fast attack and recovery at level dips or noise bursts with a low repetition rate
    - fast attack with slow recovery at events with a high repetition rate or with a long duration.

  - Audio frequency Response control as a function of level and noise and multipath:
    - fast attack and recovery at level dips or noise bursts with a low repetition rate
    - fast attack with slow recovery at events with a high repetition rate or with a long duration.

  - **All these functions can be enabled or disabled by the controller**
  - **All parameters of these functions can be changed by the controller**

- Features for RDS updates:

  - Pause detection, output at DSP-OUT2 pin
  - Hold function for level, noise and multipath during RDS updates, control with the DSP-IN1 pin
  - Mute during RDS updates, control with the DSP-IN1 pin
  - Freeze function for level, multipath and noise values measured on the alternative frequency during RDS updates. This allows readout after the update by the controller. Control with DSP-IN2 pin

  General features:
  - FM de-emphasis filter and 19 kHz MPX filter
  - FM audio filter, this allows to define the audio bandwidth for the audio in FM independent from the other modes
  - Stereo detection filter, output at pin DSP-OUT2
  - Adjustment for maximum channel separation
  - Signal quality information for the controller (noise information)

The FM program consists of the following functional parts :

9.3.2 FM control part

9.3.2.1 General

The FM control part determines the adaptive coefficients for the FM audio signal processing part.
The diagram of the FM control part is depicted in fig. 9.13. The functional parts are:

- **Softmute control**, to determine coefficient **Y:SMTC** for softmute attenuation
- **Stereo control**, to determine coefficient **Y:STRC** for sliding stereo
- Audio frequency **Response control** (High cut control), to determine the coefficients **Y:RSPC1, Y:RSPC2 and Y:RSPC3** for the bandwidth of the audio signals
- Hold function for the input signals level, noise and multipath during RDS updates
- Noise function for softmute control
- Multipath and noise functions for stereo and response control

Inputs and outputs

The inputs are:

X:LEVA	filtered level signal from AM/FM signal quality processing
X:MLTFLIM	multipath signal from AM/FM signal quality processing
X:NOISFLT	filtered noise input signal
X:PLTD	pilot I signal from the Stereo detection filter
Y:STRO	coefficient to select stereo or mono, this has to be set by the controller

The outputs are: Y:SMTC, Y:STRC, Y:RSPC1, Y:RSPC2 and Y:RSPC3

Control functions

The FM control functions are implemented in a modular way. They consists of a few building blocks :

- **a linear function** : The adjustable parameters of the control functions are realized by application of linear functions. These functions define the desired working area of an input signal, across which a function like, softmute, sliding stereo or adaptive frequency response, will be activated.
  All linear functions have a maximum control range from zero to 1 (full scale) at the output. Zero causes the maximum effect of a function and at full scale a function becomes just inactive.
  To adjust the desired working area, the input signal is multiplied by **Y:p** and shifted by **Y:q.**

- **Minimum Detector 2** : The response times, being the attack and recovery times, of all control functions are realized with a minimum detector 2 filter section.
  The output of this filter section reacts fast on events with a low repetition rate and a short duration and slow on events with a high repetition rate or a with a long duration. Fig. 9.12 shows the result on an input signal.

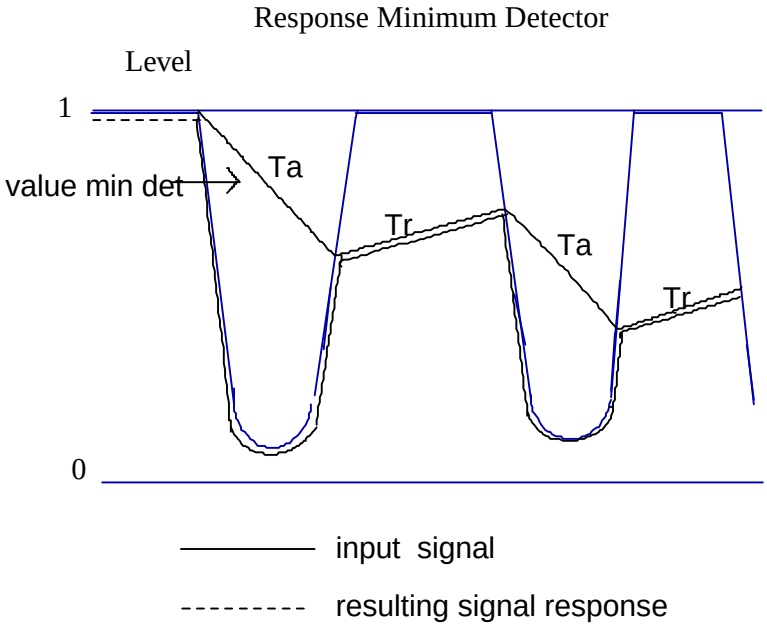


Fig. 9.12 Response minimum detector 2

This function comprises a minimum detector, with independent attack (Ta) and recovery (Tr) times. As long as the input signal is below the value of the minimum detector, the output signal follows the input signal (fast response). As soon as the input signal becomes higher than the value of the minimum detector, the output signal follows the response time of the minimum detector (slow response).

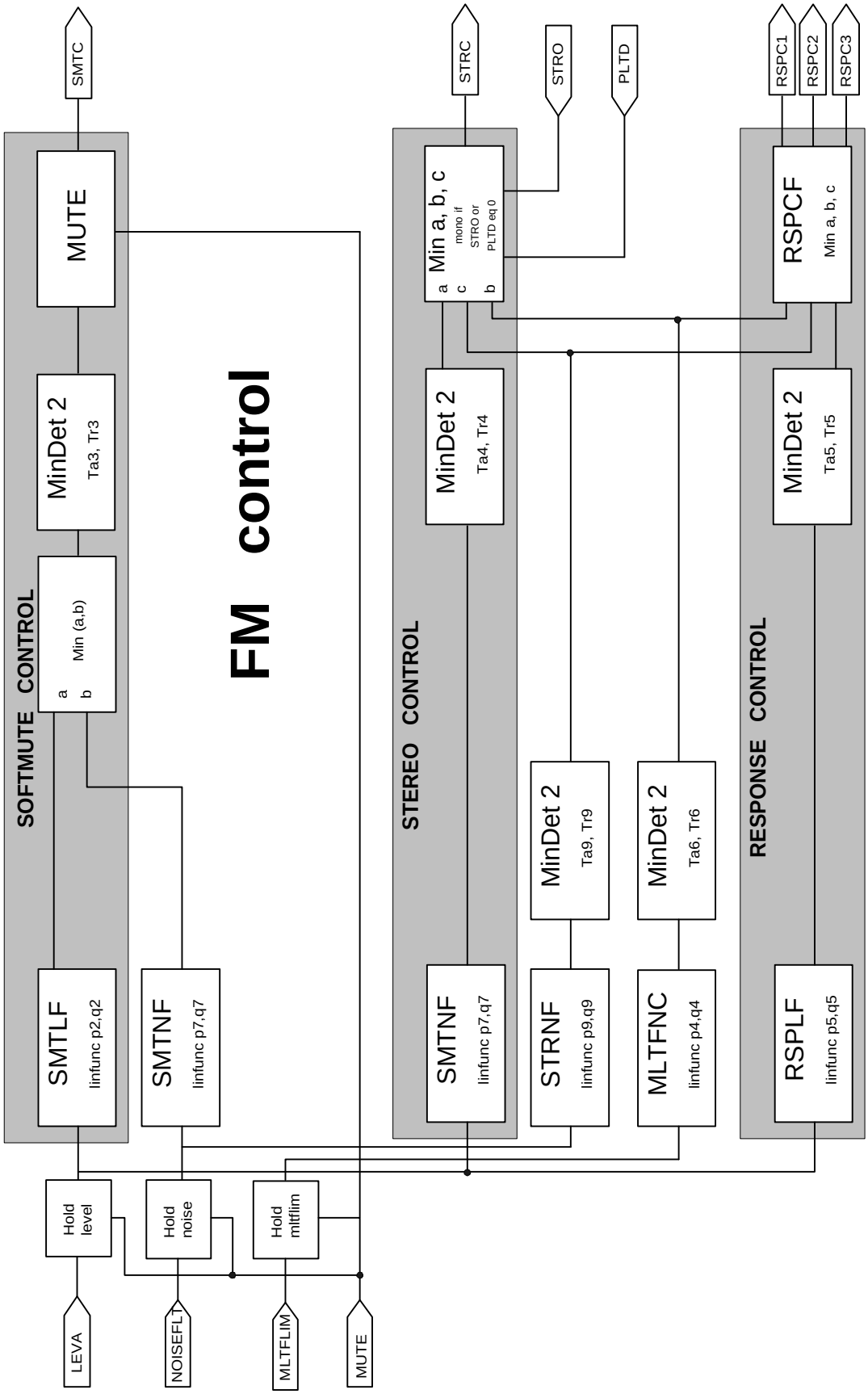
The attack and recovery times are defined as 63% of the total slope time between zero and full scale. Ta is determined by a single coefficient $Y:ta_n$. To enable long recovery times Tr is defined as double precision, by a multiplication of two coefficients $Y:tr_{n1} * Y:tr_{n2}$.

formula for Minimum detector 2 timing:

attack time	$Y:ta_n$ =	-(0.63*8)\(fs*attack time[s])	(5 ms < Ta ≤ 270 ms)
recovery time	$tr_n = Y:tr_{n1}*Y:tr_{n2}$ =	(0.63*8)\(fs*recovery time[s])	(0 ms < Tr ≤ 17 sec)

fs is the audio sample frequency, this is 38kHz for the FM mode.

Fig. 9.13 Diagram FM-control functions



9.3.2.2 Softmute control

Softmute control is a function of the input signals, level and noise. The working area's of these input signals are determined by the following linear functions :

SMTLF for level with parameters Y:p2, Y:q2 and Y:minsmtc
SMTNF for noise with parameters Y:p7, Y:q7 and Y:minsmtcn

For both functions the maximum softmute attenuation can be limited. For level with coefficient Y:minsmtc and for noise with Y:minsmtcn.
The strongest effect of these functions is calculated in Min(a,b) and fed to a Minimum detector 2 filter section with parameters :

Y:ta3 and Y:tr3 for the response times.

The resulting coefficient Y:SMTC determines the Softmute attenuation.
For RDS Mute purposes Y:SMTC can be forced to zero with the DSP-IN1 pin.
See chapter RDS update functions 9.3.8.

The level controlled softmute can cause some THD for audio signals with high modulation and low frequency. This effect can be limited by selecting a long recovery time for a fieldstrength below the softmute point.
Therefore the recovery time tr3 is switched to another value as long as the level signal X:LEVA is below the threshold value Y:trshTSW.

recovery time for X:LEVA > Y:trshTSW is tr3= Y:tr31*Y:tr33
and for X:LEVA < Y:trshTSW is tr3= Y:tr31*Y:tr34

All the response times are calculated according the formula for the minimum detector 2 timing.
The default values are : (loaded by Easy Programming, set2 FM)

```
Y:ta3     $FFB     ;Tattack softmute, 50ms
Y:tr31    $014
Y:tr33    $214     ;Trecovery softmute, tr3=tr31*tr33 = 50ms
Y:tr34    $07E     ;Trecovery softmute, tr3=tr31*tr34 =200ms
```

Calculation level control (Y:p2, Y:q2)

The softmute function for level control is :

SMTLF= 4(4*Y:p2 * X:LEVA + Y:q2)

Define for 2 fieldstrength values (ViFM) the desired softmute attenuation. Then calculate the corresponding SMTLF values for the attenuation according formula :

SMTLF = 10^(-Attenuation/20)

and look up the corresponding X:LEVA (equal to X:LEVN) values for the fieldstrength in fig. 9.11,
or apply the desired fieldstrength values to the tuner and readout the corresponding X:LEVA values from the XRAM.

example:

ViFM	X:LEVA	Attenuation softmute+tuner = total			SMTLF
7µV	0.1633	2	1	3dB	0.7943
2µV	0.0398	14	2	16dB	0.1995
maximum attenuation		24	8	30dB	Y:minsmtc = 0.079 = $0A3 (see calculation below)

make 2 equations with formula SMTLF and calculate Y:p2 and Y:q2 :

Y:p2= 1/16 (SMTLF1 - SMTLF2)/(X:LEVA1 - X:LEVA2) = 1/16 (0.7943-0.1995)/(0.1633-0.0398) = 0.301 = $269
Y:q2= 1/4 * SMTLF1 - (4*X:LEVA1 * Y:p2) = 1/4 * 0.7943 - (4 * 0.1633 * 0.301) = 0.002 = $004

The default implemented values for Softmute control are: (loaded by Easy Programming, set2 FM)

```
Y:p2    $269            ;3 dB softmute attenuation at 7µV
Y:q2    $004
```

calculation for the maximum softmute attenuation (Y:minsmtc and Y:minsmtcn)

The formula for the maximum attenuation is :
Y:minsmtc, Y:minsmtcn = 10^(-Attenuation/20)

Default values: (loaded by Easy Programming, set2 FM)

```
Y:minsmtc       $0A3        ;maximum softmute for level control is 22 dB (excl. tuner)
Y:minsmtcn      $2A4        ;maximum softmute for noise control is 9.6 dB
```

calculation for the threshold fieldstrength Y:trshTSW

Apply the desired fieldstrength for the threshold value to the tuner and readout X:LEVA. Then translate the 18 bit HEX value to fractional. Then translate this fraction to a 12 bit HEX value.

Default value: (loaded by Easy Programming, set2 FM)

```
Y:trshTSW       $147        ;threshold value for switching tr3, is about 7 µV
```

Calculation of the noise control range for Softmute activation (Y:p7, Y:q7)

For the calculation see chapter 9.3.2.3 "Calculation of the noise control for Stereo and Response control". The calculation for Y:p7 and Y:q7 is equal to the one for Y:p9 and Y:q9. The coefficients Y:p7 and Y:q7 may be chosen independently from Y:p9 and Y:q9.

The formula for the noise control range for Softmute is:

SMTNF = 16(Y:p7*X:NOISFLT+Y:q7)

The default values for the noise control for Softmute are: (loaded by Easy Programming, set2 FM)

```
Y:p7    $AF6            ;noise control range Δf= 50 - 75 kHz
Y:q7    $15C
```

9.3.2.3 Stereo control

Stereo control is a function of level, noise and multipath. The level function is determined by linear function:
STRLF with parameters Y:p3 and Y:q3

The noise and multipath functions for stereo and response control are combined :

STRNF for noise with parameters Y:p9 and Y:q9
MLTFNC for multipath with parameters Y:p4 and Y:q4

The response time for level control is determined by a Minimum detector 2 filter with parameters Y:ta4 and tr4=Y:tr41*Y:tr42
The response times for multipath and noise control are determined by separate Minimum detector 2 filters.
Response time parameters for noise Y:ta9 and tr9=Y:tr91*Y:tr92
Response time parameters for multipath Y:ta6 and tr6=Y:tr61*Y:tr62

The stereo control coefficient Y:STRC is the result of the filter outputs from level-, noise- and multipath control. Coefficient Y:STRC determines the stereo channel separation. Moreover, Y:STRC is forced to zero (mono) if no pilot is detected (X:PLTD=0) or when mono is selected by the controller (Y:STRO= 0).
With coefficient Y:STRO the FM mode can be set to mono or stereo reproduction, 0=mono and 1=stereo.

All mentioned response times, except Y:ta4, are calculated according the formula for the minimum detector 2 timing.
The formula for Y:ta4 = -(128*0.63)/(38000*attack time [sec]) (5 ms < Ta < 4 sec)
The default values are :

```
Y:ta4     $FF0   ;Tattack level control stereo is 271 ms
Y:tr41    $01D   ;Trecovery level control for stereo, tr4=Y:tr41*Y:tr42 = 959 ms
Y:tr42    $014
Y:ta6     $FFB   ;Tattack multipath control for stereo is 54 ms
Y:tr61    $01D   ;Trecovery multipath control stereo and response, tr6=Y:tr61*Y:tr62 = 959 ms
Y:tr62    $014
Y:ta9     $FFB   ;Tattack noise control stereo and response is 54 ms
Y:tr91    $01D   ;Trecovery noise control stereo and response, tr4=Y:tr41*Y:tr42 = 959 ms
Y:tr92    $014
```

Calculation level control (Y:p3, Y:q3)

The function for level control is :

STRLF= 8(Y:p3*X:LEVA+Y:q3)

Define at 2 fieldstrength values (ViFM) the desired channel separation. Then calculate the corresponding STRLF value for the channel separation according formula:

STRLF= -(1-10^(c/20)) / (1+10^(c/20))
c = channel separation [dB]

and look up the corresponding LEVA (equal to LEVN) values for the fieldstrength in fig. 9.11 or apply the desired fieldstrength values to the tuner and readout the corresponding X:LEVA values from the XRAM.

example:

ViFM	X:LEVA	CH.sep	STRLF
350µV	0.59	30dB	0.94
140µV	0.485	10dB	0.52

make 2 equations with formula STRLF and calculate Y:p3 and Y:q3 :
Y:p3= 1/8 (STRLF1 - STRLF2) / (X:LEVA1 - X:LEVA2) = 1/8 (0.94-0.52) / (0.59-0.485) = 0.50 = $400
Y:q3= 1/8 * STRLF2 - (X:LEVA2 * Y:p3) = 1/8 * 0.52 - (0.485 * 0.5) = - 0.1775 = $E95

The implemented default values for stereo control are: (loaded by Easy Programming, set 2, FM)

```
Y:p3      $348          ;10 dB channel separation at 180µV, mono to stereo 1 decade
Y:q3      $ECD
Y:STRO    $7FF          ;FM stereo, FM mono = $000
```

Calculation of the noise control range for Stereo and Response control (Y:p9, Y:q9)

The formula for the noise control range is:

STRNF = 16(Y:p9*X:NOISFLT+Y:q9)

The sensitivity of X:NOISFLT is defined as a FM deviation (∆F=[kHz]) with an AF frequency of 80 kHz.
For a ∆f = 75 kHz X:NOISFLT = 0.275 (see adjustment Noise filter chapter 9.3.6).

Then the formula for the sensitivity is: X:NOISFLT = (0.275 * ∆f[kHz]) / 75 kHz

Define the desired maximum ∆f for which no effect on the Stereo and the Response control functions is wanted (then STRNF=1). This means maximum stereo and a flat audio response. Then select the ∆f for which the maximum control effect is wanted (then STRNF=0). This means MONO and a maximum attenuation at 10 kHz of 4 dB (default value).
Then calculate the corresponding values for X:NOISFLT. Then make 2 equations with formula STRNF and calculate Y:p9 and Y:q9.

example:

∆f	X:NOISFLT	STRNF
50 kHz	0.1833	1 = no effect
75 kHz	0.275	0 = max effect

make 2 equations with formula STRNF and calculate Y:p9 and Y:q9 :
Y:p9= 1/16 (STRNF1 - STRNF2) / (X:NOISFLT1 - X:NOISFLT2) = 1/16(1-0) / (0.1833 - 0.275)=
-0.68 =$A8D

Y:q9= 1/16 (STRNF2) - (X:NOISFLT2 * Y:p9) = 1/16(0) - (0.275 * (-0.68)) = 0.187 = $17F

Note: Due to the non-linear behaviour of X:NOISFLT the default implemented coefficients differ slightly from the calculated ones.

The default values for the noise control range are: (loaded by Easy Programming, set 2, FM)

```
Y:p9    $AF6          ;noise control range ∆f= 50 - 75 kHz
Y:q9    $15C
```

Calculation of the multipath control range for Stereo and Response control (Y:p4, Y:q4)

The formula for the multipath control range is:

MLTFNC= 8(Y:p4 * X:MLTFLIM + Y:q4)

The sensitivity for X:MLTFLIM is defined as %AM modulation with 18 kHz at a fieldstrength of 100 μV.
For 50 %AM modulation X:MLTFLIM ≈ 0.65.

Then the formula for the sensitivity is: : X:MLTFLIM = (0.65 * %AM) / 50

Define the desired maximum %AM modulation for which no effect on the Stereo and the Response control functions is wanted (MLTFNC=1). This means maximum stereo and a flat audio response. Then define the %AM modulation for which the maximum control effect is wanted (MLTFNC=0). This means MONO and a maximum attenuation at 10 kHz of 4 dB (default value).
Then calculate the corresponding values for X:MLTFLIM. Then make 2 equations with formula MLTFNC and calculate Y:p4 and Y:q4.

example:

%AM	X:MLTFLIM	MLTFNC
30 %	0.39	1 = no effect
50 %	0.65	0 = max effect

make 2 equations with formula MLTFNC and calculate Y:p4 and Y:q4 :
Y:p4= 1/8 (MLTFNC1 - MLTFNC2) / (X:MLTFLIM1 - X:MLTFLIM2) = 1/8(1-0) / (0.39 - 0.65) = -0.48 = $C28

Y:q4= 1/8 (MLTFNC2) - (X:MLTFLIM2 * Y:p4) = 1/8(0) - (0.65 * (-0.48)) = 0.312 = $27E

Note: Due to the non-linear behaviour of X:MLTFLIM the default implemented coefficients differ slightly from the calculated ones.

The default values for the multipath control range are: (loaded by Easy Programming, set 2, FM)

```
Y:p4    $BC0        ;multipath control range %AM = 30 - 50 %
Y:q4    $2D8
```

9.3.2.4 Audio frequency Response control

The audio frequency Response control adapts the bandwidth of audio signal (High cut control) depending on the quality of the received station. Full bandwidth at good quality and attenuation of the high notes at decreasing quality.
The response control is a function of the input signals level, noise and multipath. The level function is determined by:

RSPLF with parameters Y:p5 and Y:q5.

The noise and multipath functions are combined with the stereo control ,see in chapter 9.3.2.3.

The response time for the level control is adjustable with a Minimum detector 2 filter section with parameters: Y:ta5 and tr5=Y:tr51*Y:tr52.

The response time for the noise control is equal to those defined under stereo control for noise.

The result of the filter outputs from level-, noise- and multipath control is fed to a function RSPCF. This function generates the appropriate adaptive coefficients Y:RSPC1, Y:RSPC2 and Y:RSPC3 for the audio bandwidth, according table 9.25 or 9.26. Function RSPCF controls the attenuation at 10 kHz, with the default coefficient setting, between 0 dB and 4 dB.

The maximum attenuation at 10 kHz is defined by the function:

RSPCF with parameters	Y:p6 and Y:q6	for the sdr_deem filter type
and with parameters	Y:p61 and Y:q61	for the sdr_corr filter type

Adaptive audio frequency response

Adaptation of the audio bandwidth (high cut control) is performed by changing the coefficients of the de-emphasis- and MPX filter parts. Two different ways of frequency response adaptation are implemented ; the sdr_deem- and sdr_corr adaptation.

The desired type of response adaption can be selected with coefficient Y:sdr_d_c. The sdr_deem type is selected by the value $000 and the sdr_corr is selected by the value $7FF. The default value is :

```
Y:sdr_d_c       $000            ;selected adaptive frequency response filter type is sdr_deem
```

Sdr_deem response adaptation

The sdr_deem type, is realized by adapting the coefficients of the de-emphasis part of the filter with Y:RSPC1 and Y:RSPC2. Fig. 9.14 shows the adaptation of the response with **sdr_deem** type on a MPX signal with 50 µs pre-emphasis. Coefficients Y:RSPC1 and Y:RSPC2 are adapted such, that τ-de-emphasis shifts between e.g. 50 - 100 µs. Adaptation of these coefficients is performed by the FM control part. This type of response adaptation is also implemented in the tuner TEA6811/6824.

The desired maximum attenuation at 10 kHz can be defined with coefficients Y:p6 and Y:q6 according table 9.25 for 50 µs and for 75 µs de-emphasis. Other attenuations are possible but keep always for 50 µs Y:p6=0.41-Y:q6 and for 75 µs Y:p6=0.297-Y:q6.

Max attenuation at 10 kHz [dB]	coefficients for 75 µs de-emphasis		coefficients for 50 µs de_emphasis	
	Y:p6	Y:q6	Y:p6	Y:q6
1	$039	$226	$04D	$2F9
2	$070	$1EF	$095	$2B2
3	$09F	$1C0	$0D7	$270
4	$0CB	$194	$112	$235
5	$0F3	$16C	$149	$1DF
6	$118	$147	$17A	$1CC
7	$139	$126	$1A7	$19F
8	$158	$108	$1D0	$176
9	$172	$0ED	$1F5	$151
10	$18B	$0D4	$21A	$12D

Table 9.25 coefficients for the sdr_deem filter type

Sdr_corr response adaptation

The **sdr_corr** is realized by adapting the correction- and notch part of the filter with Y:RSPC1 and Y:RSPC3. Fig. 9.15 shows the resulting response of sdr_corr type on a MPX signal with 50 µs pre-emphasis.

Sdr_corr offers a higher attenuation of the high notes (above 10 kHz) than sdr_deem, while the frequency band below 2 kHz is hardly affected. This avoids fluctuations of sound pressure. But default the sdr_deem type is selected.
Adaptation of these coefficients is performed by the FM control part.

The desired maximum attenuation at 10 kHz can be defined with coefficients Y:p61 and Y:q61 according table 9.26a for both 50 and 75 µs de-emphasis. Additional the de-emphasis coefficients Y:c61 and Y:c91 has to be set according table 9.26b.
Other attenuations are possible but keep always Y:p61=0.75-Y:q61.
The default values for 50 µs de-emphasis and attenuation 12 dB are loaded via Easy Programming set2 FM.

Attenuation at 10 kHz [dB]	coefficient Y:p61	coefficient Y:q61
0.5	$000	$600
3	$1D5	$42B
6	$30E	$2F2
8	$399	$266
10	$3F8	$208
12 (default)	$44D	$1B2

Table 9.26a coefficients for sdr_corr filter type

coefficients for 50 µs de-emphasis		coefficients for 75 µs de-emphasis	
Y:c61	Y:c91	Y:c61	Y:c91
$4B8	$347	$59E	$260

Table 9.26b coefficients for de-emphasis

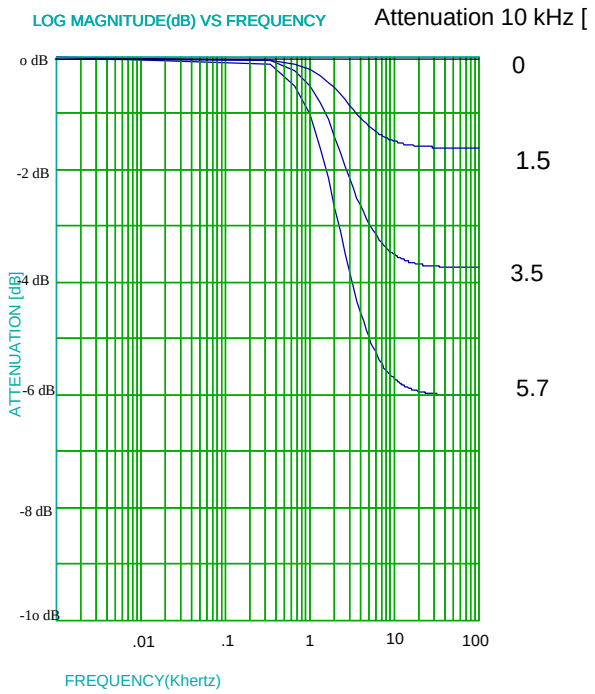


Fig. 9.14 sdr_deem response adaption

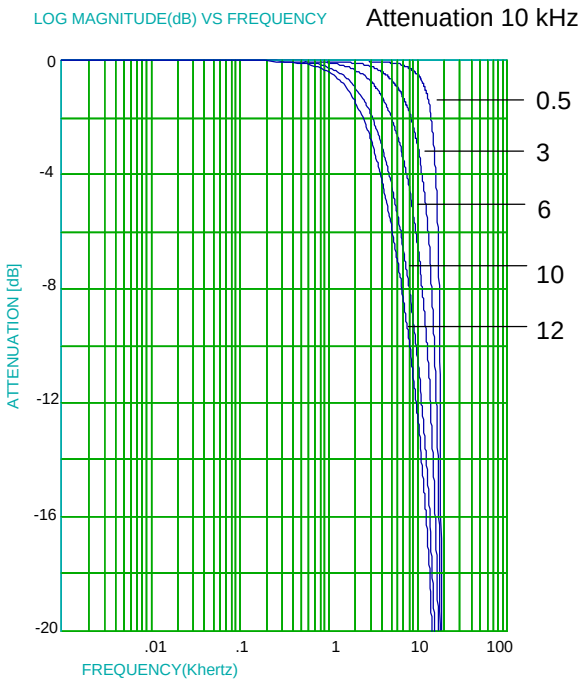


Fig. 9.15 sdr_corr response adaption

Calculation level control (Y:p5, Y:q5)

The frequency response function for level control is:

RSPLF= 8(Y:p5 * X:LEVA + Y:q5)

Select the desired fieldstrength value (ViFM) below which the response control should be activated (the point for 0dB attenuation at 10kHz) and the fieldstrength value for which the maximum attenuation at 10kHz should be reached. Then look up the corresponding X:LEVA (equal to X:LEVN) values for the fieldstrength in fig. 9.11, or apply the desired fieldstrength values to the tuner and readout the corresponding X:LEVA values from the XRAM.

RSPLF for 0dB attenuation at 10kHz = 1 and
RSPLF for the maximum attenuation at 10kHz = 0

example:

ViFM	X:LEVA	Attenuation at 10kHz	RSPLF
85µV	0.4475	0dB	1
6.3µV	0.1722	maximum attenuation	0

Y:p5= 1/8 (RSPLF1 - RSPLF2) / (X:LEVA1 - X:LEVA2) = 1/8 (1-0) / (0.4475-0.1722) = 0.4541 = $3A1
Y:q5= 1/8 * RSPLF1 - (X:LEVA1 * Y:p5) = 1/8 * 1 - (0.4475 * 0.4541) = - 0.0782 = $F60

default values for frequency response control: (loaded by Easy Programming, set 2, FM)

```
Y:p5      $3A1      ;1 dB attenuation for 10kHz at ViFM = 50µV
Y:q5      $F60      ;control range 1 decade for -0.5dB to max. attenuation
Y:ta5     $FFB      ;Tattack level control response, 50ms
Y:tr51    $014      ;Trecovery, 900ms
Y:tr52    $01D
```

9.3.3 Enable/disable of the control functions

All implemented control functions can be enabled (normal functionality) or disabled (switched off) independently by the controller.
The list below gives the coefficient values for the enabled and the disabled situation. Default all functions are enabled :

Function	enabled	disabled
Softmute f(level)	Y:p2, Yq2 set to default values	Y:p2=$000, Y:q2=$7FF
Softmute f(noise)	Y:p7, Yq7 set to default values	Y:p7=$000, Y:q7=$7FF
Stereo f(level)	Y:p3, Yq3 set to default values	Y:p3=$000, Y:q3=$7FF
Stereo f(noise)	Y:E_strnf_str = $000	Y:E_strnf_str = $7FF
Stereo f(multipath)	Y:E_mltp_str = $000	Y:E_mltp_str = $7FF
Response f(level)	Y:p5, Yq5 set to default values	Y:p5=$000, Y:q5=$7FF
Response f(noise)	Y:E_strnf_rsp = $000	Y:E_strnf_rsp = $7FF
Response f(multipath)	Y:E_mltp_rsp = $000	Y:E_mltp_rsp = $7FF

9.3.4 FM audio signal processing

9.3.4.1 General

The FM audio signal processing consists of the following parts:

- a coefficient Y:SCOR for adjustment of the maximum channel separation
- adaptive coefficient Y:SMTC for softmute attenuation
- adaptive coefficient Y:STRC for sliding stereo
- de-matrix to retrieve left and right audio signals
- de-emphasis and 19 kHz MPX filter with adaptive coefficients Y:RSPC1, Y:RSPC2 and Y:RSPC3, for audio frequency response control (High Cut Control)
- FM audio filter

Inputs and outputs

In the FM mode the stereo decoder delivers to the input registers of the DSP the signals :

left channel, D:in_L = 1/2(R-L)
right channel, D:in_R = R + L

After de-matrix- and FM audio signal processing the Left and Right channel signals are delivered to the AUDIO processing block.

output left channel: X:left1 = L
output right channel: X:right1 = R

9.3.4.2 Adjustment of the channel separation

In case of a flat frequency response of the MPX signal, the channel separation is typically 50 dB at 1 kHz. Cross-talk caused by a non flat frequency response of the MPX signal from the tuner can be compensated with coefficient Y:SCOR. Y:SCOR adapts the ratio between (R-L) and (R+L).

Alignment procedure:
Apply an RF carrier to the tuner with FM modulation on the Left channel (1kHz with Δf=22.5kHz). Adapt Y:SCOR such that the cross-talk on the right channel becomes minimal.

Default value for tuner module TEA6811/TEA6824: (loaded by Easy Programming, set 2, FM)

```
Y:SCOR      $490        ;alignment coefficient for FM channel separation
```

9.3.4.3 De-emphasis and 19 kHz MPX filter

The FM mode offers a filter section with a 50 μs or a 75 μs de-emphasis and a notch at 19kHz. The coefficient values for both corrections are given in table 9.27. Default the values for 50 μs de-emphasis are implemented. (loaded by Easy Programming, set 2, FM)

	τ de-emphasis 50 μs	τ de-emphasis 75 μs
Y:p6	$11E	$0E5
Y:q6	$228	$17B

Table 9.27 coefficients values for selection FM de-emphasis

9.3.4.4. FM audio filter

The audio bandwidth in FM can be defined with a first order Low-Pass filter. The table below gives the coefficients for several attenuations at 10kHz.

Attenuation at 10 kHz [dB]	coefficients		
	Y:FM_b0	Y:FM_b1	Y:FMa0
0	$7FF	$000	$000
2	$698	$000	$175
3	$5F2	$000	$20D
4	$56C	$000	$293
6	$47E	$000	$381
8	$3B9	$000	$446

Table 9.28 Coefficient values for FM audio bandwidth

9.3.5 Stereo detection

The stereo detection indicates the presence of a pilot tone and that the stereo decoder is locked to this pilot. The output of the stereo detection is the DSP-OUT1 pin. "High" indicates FM stereo and "Low" FM mono. Stereo is indicated for a pilot frequency deviation > 4 kHz.

9.3.6 Noise filter

The noise level is detected in a band from 60 kHz to 120 kHz of the MPX signal with an envelope detector and decimated to 38 kHz (see data sheet). The noise level is used as adjacent channel information for the controller and for the FM dynamic signal processing.
The response time of the incoming noise information D:NOISE = 100µs. To provide smooth noise information to the FM control part and to the controller, a first order low-pass filter is implemented. The default response time is 1ms (loaded with Easy Programming set 2, FM); this is the optimal setting in combination with the TEA6811/6824 tuner module. In case the SAA7705H is used in combination with the TEA6840 tuner module then the optimal response time is 0.7 ms. The output of the noise filter is X:NOISFLT. The coefficient for the response time of the noise filter is according the following table.

Coefficient	FM mode with TEA6811/6824 (response time = 1 ms)	FM mode with TEA6840 (response time = 0.7 ms)
Y:c_nf2	$68E	$5E8

Alignment noise detector on X:NOISFLT

The sensitivity of the noise detector has to be aligned once for a certain tuner, this to meet the specified control range for the noise controlled functions.

Apply an RF signal with a fieldstrength of 1mV to the tuner.
Modulate FM with two frequencies:
1) AF = 80 kHz and deviation = 75 kHz (simulation adjacent channel)
2) AF = 1 kHz and deviation = 22.5 kHz (audio signal)

Then adjust with coefficient Y:c_nf1 such, that X:NOISFLT = 0.275 for an average tuner.

```
X:NOISFLT                ;output noise filter
Y:c_nf1     $1C2         ;default value for the ICE-tuner module TEA6811/TEA6824
                         ;(loaded by Easy Programming, set 2, FM)
            $28E         ;value for the NICE tuner module TEA6840
```

Remark: For tuners with 3*M4 filters align AF=80 kHz and deviation= 85 kHz to X:NOISFLT = 0.275

9.3.7 RDS update functions

For RDS updates the following functions have been implemented:

- Pause detection, with output at pin DSP-OUT2
- Hold function to freeze the input signals for the FM control part (level, multipath and noise) during RDS updates, control with pin DSP-IN1.
- Freeze function for the sensor signals (level, multipath and noise for the micro controller) measured on the alternative frequency during RDS updates. Control via pin DSP-IN2.
- Mute of the audio signal during RDS updates, control with pin DSP-IN1 or DSP-IN2.

9.3.7.1 Pause detection

The purpose of the pause detection is to search a pause in the FM signal. This can be used for RDS updates. A pause is detected when the FM audio signal is below a pre-defined level for a certain amount of time. The output of the pause detector is on pin DSP-OUT2. "High" indicates Pause.

The detection threshold X:PMinLev, below which a pause will be detected is set to -44 dB below full scale in the CDSP. This results in a detection threshold for an average signal of -41 dB below full scale of the A/D converter (-44 dB peak + 3 dB, due to averaging of the input signal).
A pause is detected, after the input signal has remained below this threshold for a certain time. This time is determined by X:PCountMax. Default X:PCountMax is set to 21ms. For a sample frequency of 38/8 kHz, this corresponds to 99 samples. Since the decay time of the input filter (about 2 ms) has to be subtracted from 21ms, the value 90 is implemented (see calculations below). Further the detection time until a pause is detected depends slightly upon the input level. The constant X:PAttack is used to reduce the sensitivity of the pause detection if a distortion occurs during pause (music attack time). It is set to 10 (about 2 ms) for the current implementation.

calculation of X:PCountMax, X:PAttack and X:PMinlev

X:PCountMax = (minimum pause time(s) **-** 0.002) **x** 4750

X:PAttack = X:PCountMax / (4750 **x** music attack time(sec))

X:PMinLev = exp10 (1/20((detection threshold A/D in dB below full scale) **-** (3 dB)))

Default values: (loaded by Easy Programming, set 2, FM)

```
X:PCountMax     #0005A ;minimum pause time before a pause will be detected is about 21ms
X:PMinLev       #0033A ;threshold for pause detection is -41dB below Full scale of the A/D
X:PAttack       #0000A ;minimum music time before the pin DSP-OUT2 becomes low is 2 ms
```

9.3.7.2 Hold and Mute functions for RDS updates

The input signals of the FM control part can be frozen by a hold function with the DSP_IN1 pin. This avoids that various filters in the FM control part are loaded with erroneous samples during an RDS update sequence. It is possible to enable a Hard Mute, then also the audio output signals X:left1 and X:right1 are muted with pin DSP_IN1 by forcing the softmute coefficient Y:SMTC to zero. The Hard Mute can be enabled or disabled with Y:E_MUTE.
With a second hold function the sensor signals for level, noise and multipath can be frozen with pin DSP_IN2. The purpose of this hold is to freeze the values measured during an RDS update and to read them out after the update. This saves I²C communication time.

The XMEM lables of the various sensor signals are given in the table 9.29.

Input signals	**Holded signals** for FM signal processing Hold at DSP-IN1=low	**Frozen sensor signals** from update for the micro controller, Hold at DSP-IN2=low
X:LEVA	X:LEVH	X:LEVA_U
X:NOISFLT	X:NOISH	X:NOISFLT_U
X:MLTFLIM	X:MLTFLIMH	X:MLTFLIM_U

Table 9.29 Overview sensor signal lables

Timing RDS update

The timing diagram for RDS updates is given in fig. 9.16.

DSP_IN1 pin: This mute pin should be low as long as the tuner is de-tuned. During this time the hold and - if enabled -the mute are activated.

DSP_IN2 pin: This pin has to change from high to low as soon as the sensor values of X:LEVA, X:NOISFLT and X:MLTFLIM are stabilised after tuning to the RDS update frequency. Pin DSP_IN2 should become high after the values X:LEVA_U, X:NOISFLT_U and X:MLTFLIM_U are read out.

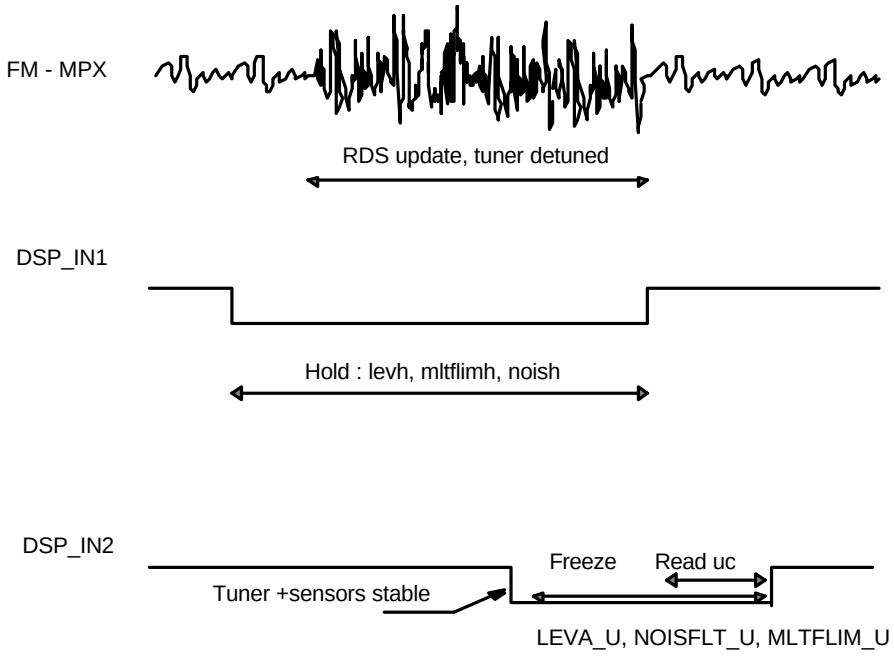


Fig. 9.16 Timing RDS updates

9.3.7.3 Interface with Tuner TEA6840 (NICE)

The tuner IC TEA6840 allows for a fast RDS update sequence of about 7ms. The IC has an RDS update timing sequencer on board which performs the following tasks:

- Mute of the FM-MPX signal with a slope of 1 ms for fade out and fade in of the MPX signal
- Tuning to the alternative frequency and back to the main frequency
- generating of two timing signals AFHold and AFSample to control the CDSP

Figure 9.17 shows the interface diagram between Tuner and CDSP and figure 9.18 the timing diagram. The TEA6840 delivers two MPX signals to the CDSP, one with Mute, the FMMPX and one without Mute, the RDSMPX. The RDSMPX signal enables the possibility to take also a Noise sample X:NOISFLT_U from the alternative frequency. This is realised by switching the input of the A/D converter from FMMPX to RDSMPX during the RDS update with SEL_FR. An internal mute in the CDSP is initiated with AFSample to suppress the modulation from the RDSMPX signal.

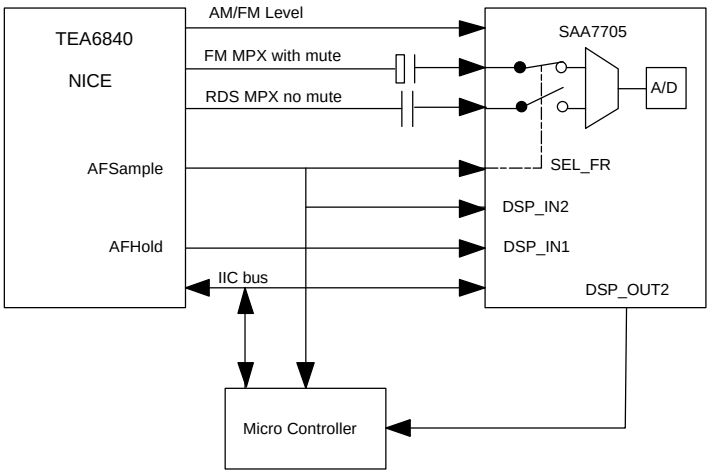


Fig. 9.17 Interface diagram between Tuner TEA6840 and CDSP

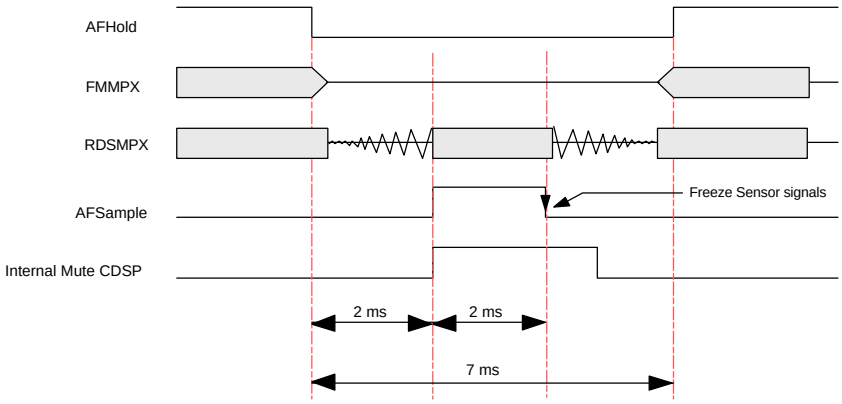


Fig. 9.18 Timing diagram RDS update with TEA6840

9.3.7.3 Control actions for RDS updates

Table 9.30 shows the coefficient settings for various application requirements.

Mute Type	Application	Coefficient setting	
		Y:E_Mute	Y:E_MuteF1
Hard Mute	Mute in CDSP	$7FF	$000
External Mute without internal Mute	TEA6840 without Noise sample during update	$000	$000
External Mute with internal Mute at DSP_IN2	TEA6840 with Noise sample during update	$000	$7FF

Table 9.30 RDS Mute type selection

Table 9.31 shows the functionality of the digital input signals for the various applications.

Mute Type	Application	Control		
		Mute activation	Hold sensors Main frequency	Freeze sensors Alternative frequency
Hard Mute	Mute in CDSP	DSP_IN1=low	DSP_IN1=low	DSP_IN2=low
External Mute	Mute in TEA6840	DSP_IN2=high	DSP_IN1=low	DSP_IN2=low

Table 9.31 RDS Mute type selection

The default coefficient setting (as loaded with easy programming) is set for a Hard mute in the CDSP, e.g. for application with Tuner TEA6811/6824:

```
Y:E_Mute      $7FF   ;Hard Mute via DSP_IN1 enabled
Y:E_MuteF1    $000   ;Mute via DSP_IN2 disabled
```

9.4 AM mono mode

For AM stereo the transparent mode (see chapter 9.13) has to be selected. In that case the AM signal processing functions as described in this chapter are not available.
The AM mono input signal has to be fed to the AM_R input.

9.4.1 Functions AM mono mode

The AM mono mode offers the following functions:

- 6th order low pass filter
- Softmute as a function of the fieldstrength (level x:LEVA)
- High Cut Control as a function of the fieldstrength
- AM Interference Absorption Circuit (IAC), also called a noise blanker

9.4.2 6th order low pass filter

9.4.2.1 Functional description

The 6th order low pass filter offers 40 dB additional attenuation above 4.5 kHz for MW and LW, and 40 dB additional attenuation above 4 kHz for SW. See frequency curves below.

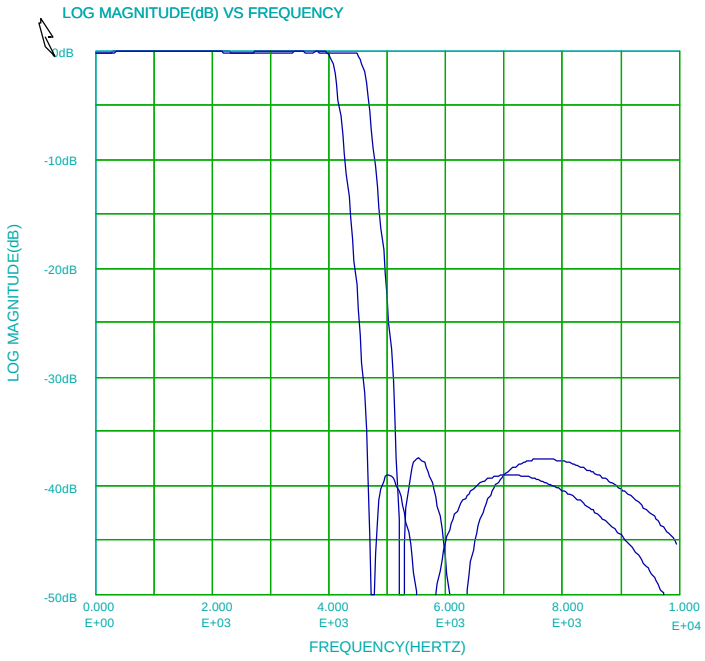


Fig. 9.19 response AM filter with cutoff frequencies at 4kHz and 4.5kHz

The benefits of this filter are an improved suppression of interference whistles, interstation noise and engine interference, resulting in clearer audio.

The default selected cut-off frequencies are as mentioned above, but if desired it is possible to program any other cut-off frequency between 1 kHz and 15 kHz.

9.4.2.2 Control actions and calculations 6th order filter

The default coefficients for the 6th order Low Pass Filter for MW and LW are given in the first column of table 9.32. They become automatically loaded with easy programming when the AM mode is chosen. For SW the values of the second column have to be loaded via I^2C. The third column gives the values for a flat response.

	Default values for MW 4.5 kHz, Attenuation = 38 dB ripple = 0.2dB	Values to be loaded for SW 4 kHz, Attenuation = 40dB ripple = 0.2db	Flat response
Y:AMb02	$051	$045	$000
Y:AMb01	$02F	$01B	$400
Y:AMb00	$051	$045	$000
Y:AMa02	$E4D	$E1B	$000
Y:AMa01	$4E1	$540	$000
Y:AMb12	$1B4	$19A	$000
Y:AMb11	$E3F	$E1D	$400
Y:AMb10	$1B4	$19A	$000
Y:AMa12	$D15	$D03	$000
Y:AMa11	$543	$5AB	$000
Y:AMb22	$307	$2FA	$000
Y:AMb21	$C1D	$BCF	$400
Y:AMb20	$307	$2FA	$000
Y:AMa22	$C44	$C41	$000
Y:AMa21	$592	$602	$000

Table 9.32 Coefficients AM- filter for MW/LW and SW and flat response

9.4.3. AM fieldstrength controlled softmute

9.4.3.1. functional description

The AM softmute attenuates the audio output as a function of the fieldstrength.
The benefit is an improved audio behaviour at weak signals, under bridges and in tunnels.
It is possible to define the fieldstrength for 10 dB attenuation (figure of merit), the steepness and the maximum attenuation of the softmute curve to customer demands. The softmute effect is shown in figure 9.20.

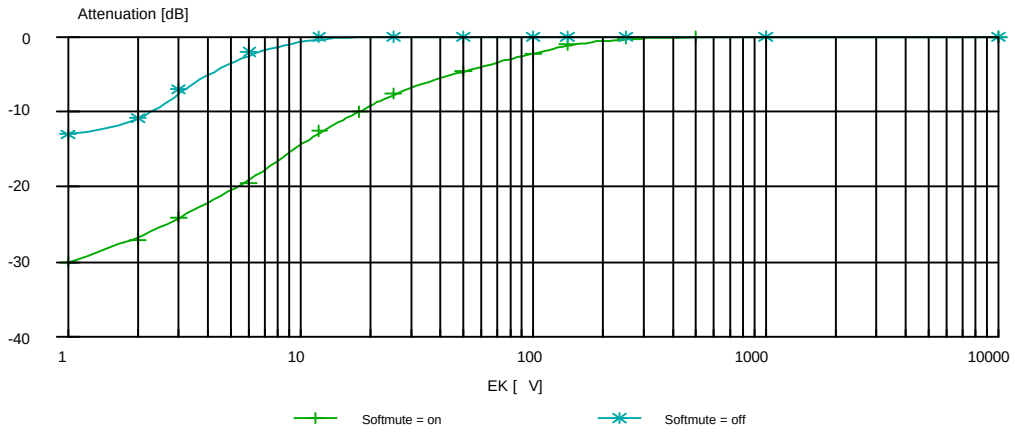


Fig. 9.20 AM softmute

9.4.3.2. parameter definition and calculations AM softmute

The table below shows which parameters can be defined and gives also the practical control range.

AM softmute as a function of :	control parameters with practical range		
fieldstrength (in μV E_k) range	figure of merit: fieldstrength for 10 dB attenuation	steepness curve: fieldstrength for x dB attenuation	maximum attenuation
	E_k = 4 - 30 μV	e.g. 2μV for 30 dB	10 .. 40 dB

As a measure for the fieldstrength the level signal X:LEVA is used. The softmute behaviour as function of the level signal is determined by the coefficients Y:p12, Y:q12 and Y:AMminsmtc.

- Y:p12 and Y:q12 determine the attenuation as function of X:LEVA
- Y:AMminsmtc limits the maximum softmute attenuation

The dynamic behaviour of the softmute is characterized by a attack time at a decreasing level signal and a recovery time at an increasing level. Coefficient AMta11 = Y:AMta11*Y:AMts determines the attack time and AMtr11 = Y:AMtr11*Y:AMts the recovery time. Y:AMts is a scaling factor in order to realize long time constants.
Attack and recovery times are defined as the time needed to reach 63% of the slope between minimum and maximum attenuation.

Calculation of the coefficients

The attenuation of the CDSP softmute control adds to the output attenuation of the tuner at low fieldstrength, the original figure of merit of the tuner.
The attenuation of the softmute control is defined as:

AMSMTLF=10^(-Attenuation/20) = 8*Y:p12 * X:LEVA + 2*Y:q12

The coefficient for the maximum attenuation is:

Y:AMminsmtc = 10^(-max_Attenuation/20)

calculation example:
Define for 2 fieldstrength values (Ek AM) the desired softmute attenuation (excl. attenuation tuner).
Specification for this example:
Attenuation at 22μV = 9.2dB and at 7μV = 17dB and the maximum attenuation = 17dB
Calculate now the AMSMTLF values, and then apply the desired fieldstrength values to the tuner and readout the corresponding X:LEVA values from XRAM.

Ek AM	X:LEVA	Attenuation [dB] softmute+tuner=total			AMSMTLF
22μV	0.017	9.2	.8	10	0.346
7μV	-0.059	17	3	20	0.14
maximum attenuation		17	17	34	0.14

make 2 equations with formula AMSMTLF and calculate Y:p12 and Y:q12 :

Y:p12= 1/8 (AMSMTLF1 - AMSMTLF2)/(X:LEVA1 - X:LEVA2) = 1/8*(0.346-0.14)/(0.017+0.059) = 0.34 = $2B8
Y:q12= 1/2 * AMSMTLF1 - (4*X:LEVA1 * Y:p12) = 1/2 * 0.346 - (4 * 0.017 * 0.34) = 0.15 = $133
Y:AMminsmtc = 0.14 = $11F

With the default coefficients (as loaded with easy programming) the Softmute is switched "off", then the coefficients are:

```
Y:p12          $000          ;Softmute is switched "off"
Y:q12          $7FF          ;          "          "
Y:AMminsmtc    $11F          ;max softmute is 17 dB (excl. attenuation tuner)
```

The attack and recovery timing coefficients can be calculated according the formula's:

$$AMta11 = Y{:}\,AMta11 * Y{:}\,AMts = \frac{0.63}{38000 * attack\ time(s)}$$

$$AMtr11 = \quad Y{:}\,AMtr11 * Y{:}\,AMts = \frac{0.63}{38000 * recovery\ time(s)}$$

The default values are :

```
Y:AMta11       $15B          ;Tattack softmute = 20ms
Y:AMtr11       $022          ;Trecovery softmute = 200ms
Y:AMts         $00A          ;scaling factor
```

9.4.4. AM High cut control

9.4.4.1. functional description

The AM High cut control adapts the audio bandwidth as a function of the fieldstrength.

The benefits are:
- improved AM sensitivity, due to a narrow bandwidth at low fieldstrength
- broader audio bandwidth can be offered at good receiving conditions (higher fieldstrength), resulting in clearer audio.

Fig. 9.21 shows the attenuation at 3 and 4 kHz as function of the fieldstrength EK and fig. 9.22 shows the minimum and maximum bandwidth with the default coefficient settings.

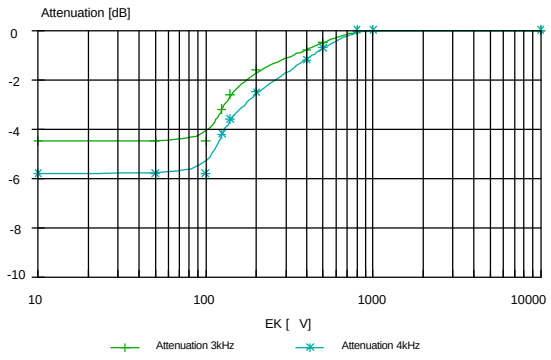


Fig. 9.21 minimum and maximum bandwidth

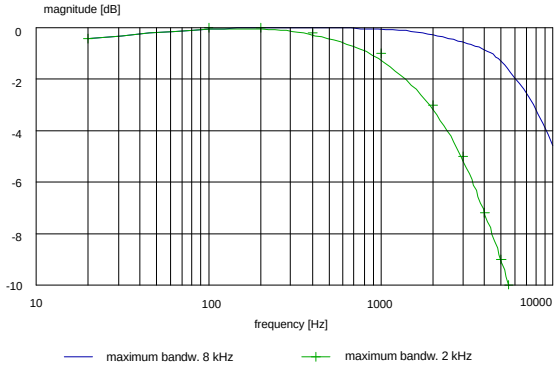


Fig. 9.22 attenuation as f(fieldstrength)

9.4.4.2. definition parameters and calculations AM High cut control

The table below shows which parameters can be defined and gives also a practical control range.

High Cut Control parameters	control parameters with practical range	
fieldstrength (in µV E_k)	fieldstrength for full audio bandwidth Ek > .. µV	fieldstrength for minimum bandwidth Ek < .. µV
range	300 .. 1000 µV	100 .. 300 µV
audio bandwidth	minimum bandwidth	maximum bandwidth
range	1.5 .. 2.5 kHz	2 .. 8 kHz

Remark: the maximum audio bandwidth is limited by the filters in the tuner.

The audio bandwidth is adapted gradually between the maximum and minimum bandwidth by the fieldstrength. As a measure for the fieldstrength the level signal X:LEVA is used. The High cut control behaviour as function of the level signal, between maximum and minimum bandwidth, is determined by the coefficients Y:p13 and Y:q13. The minimum and maximum bandwidth of the High cut filter section is determined by the coefficients Y:p14 and Y:q14.

The dynamic behaviour of the high cut control is characterized by a attack time at decreasing level signal and a recovery time at increasing level. Coefficient AMta12 = Y:AMta12*Y:AMts determines the attack time and AMtr12 = Y:AMtr12*Y:AMts the recovery time. Scaling factor Y:AMts is shared with the softmute section. Attack and recovery times are defined as the time needed to reach 63% of the slope between minimum and maximum bandwidth.

Calculation of the coefficients

The formula for the high cut control function as function of level is:

AMRSPLF= 8(Y:p13 * X:LEVA + Y:q13)

The bandwidth is maximal for AMRSPLF = 0 and minimal for AMRSPLF =1.

Example:
Define a fieldstrength value (Ek AM) below which the reduction of bandwidth should start and also a value for which the maximum bandwidth reduction should be reached.

Specification of this example:M
maximum bandwidth for Ek > 1000µV and minimum bandwidth for Ek < 100µV
Apply the desired fieldstrength values to the tuner and readout the corresponding X:LEVA values from the XRAM.

Ek AM	X:LEVA	Audio bandwidth	AMRSPLF
1000µV	0.398	maximal	1
100µV	0.176	minimal	0

make 2 equations with formula AMRSPLF and calculate Y:p13 and Y:q13:

Y:p13 = 1/8*(AMRSPLF1 - AMRSPLF2) / (X:LEVA1 - X:LEVA2) = 1/8 (1-0) / (0.398-0.176) = 0.563 = $481
Y:q13= 1/8 * AMRSPLF1 - (X:LEVA1 * Y:p13) = 1/8 * 1 - (0.398 * 0.563) = - 0.099 = $F35

With the default coefficients (as loaded with easy programming) the High Cut control is switched "off", then the coefficients are:

```
Y:p13    $000    ;High Cut Control is switched "off"
Y:q13    $7FF    ;          "          "
```

Determining the minimum and maximum bandwidth

The AM high cut control is realized using a first order low-pass filter. The transfer function is:

$$H(z) = \frac{Y{:}\,AMb0 + Y{:}\,AMb1 \bullet z^{-1}}{1 - Y{:}\,AMa1 \bullet z^{-1}}$$

Coefficients Y:AMb0, Y:AMb1 and Y:AMa1 are adapted by the DSP program as a function of AMRSPLF. The relation of AMRSPLF and coefficient Y:AMb0 is:

Y:AMb0 = Y:p14 * AMRSPLF + Y:q14

Calculation example:
Define the minimum and maximum desired bandwidth, choose Y:AMb1 = Y:AMb0 and calculate the corresponding values for Y:AMb0 (e.g. with IIR filterdesign program for 1st order and invariant type).

bandwidth	Y:AMb0	AMRSPLF
max= 8kHz	0.4379	1
min= 2kHz	0.143	0

$Y:q14 = Y:AMb0_{min} - Y:p14 * AMRSPLF_{min} = 0.143 - Y:p14 * 0 = 0.143 = \$124$
$Y:p14 = (Y:AMb0_{max} - Y:q14)/AMRSPLF_{max} = (0.4379 - 0.143)/1 = 0.2949 = \$25B$

The default values are:

```
Y:p14     $124      ;maximum bandwidth is 8 kHz and
Y:q14     $25B      ;minimum is 2kHz
```

For calculation of the attack and release timing coefficients use the formula from the softmute timing section. The default values are:

```
Y:AMta12  $045      ;Tattack response high cut control = 100ms
Y:AMtr12  $007      ;Trecovery = 1000ms
```

9.4.5 Enable/disable of the AM control functions

It is possible to enable (normal functionality) or to disable (switch off) the implemented control functions independently by the controller.
The coefficient values for the enabled and the disabled situation are listed below:

Function	enabled	disabled
AM Softmute	Y:p12, Yq12 set to default values	Y:p12=$000, Y:q12=$7FF
AM high cut	Y:p13, Yq13 set to default values	Y:p13=$000, Y:q13=$7FF

Default these functions are switched off.

9.4.6 AM IAC

9.4.6.1. functional description

The AM processing incorporates an AM IAC (interference absorption circuitry) or a so called AM noise blanker function. This function detects and eliminates audible clicks caused by impulsive interference, such as caused by engine ignition or van, on AM reception. The interference detection is performed behind the AM detection in a bandwidth up to 19kHz.

The block diagram is depicted in the figure 9.23.

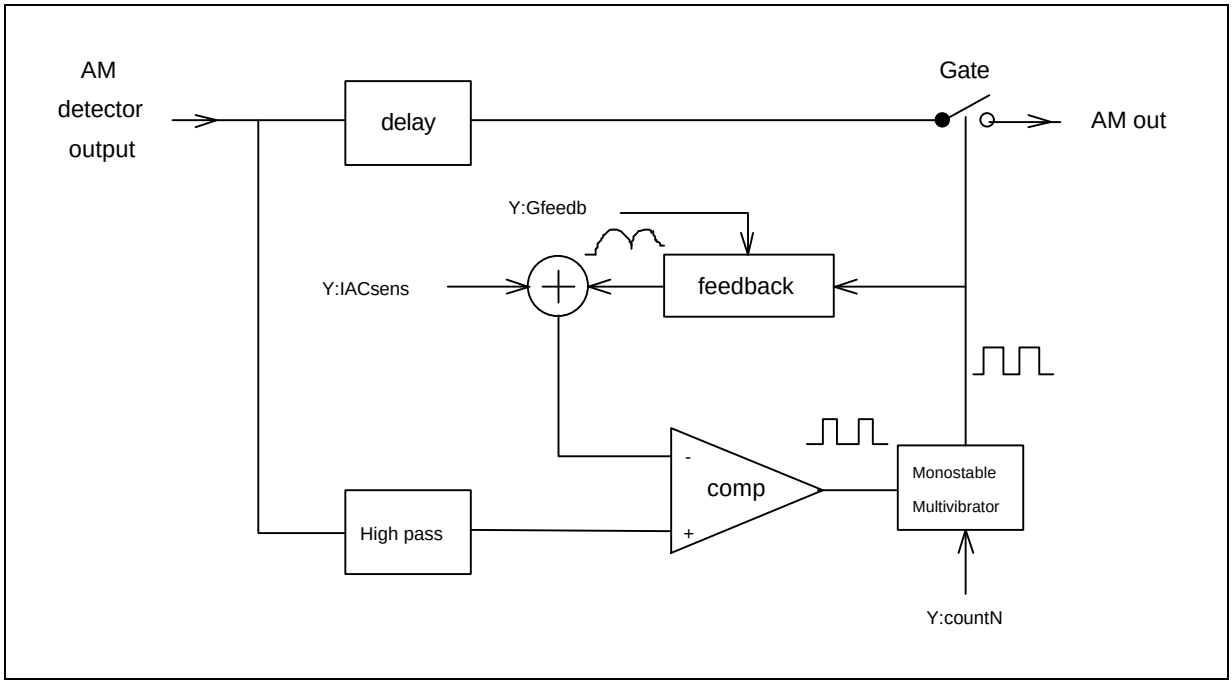


Fig. 9.23 Block diagram of AM IAC

The input signal of the IAC circuit is the AM detector output of the tuner derived from the decimated output signal of the A/D converter. This signal is fed to a delay circuit followed by a gate switch.
This gate is activated by an interference detector which consists of a high pass filtering, a comparator, a monostable multivibrator and a feedback loop. The interference detector analyses the AM audio frequency contents and discriminates between interference pulses and audio signals.

At interference the gate is activated for a minimum time determined by the monostable multivibrator.

9.4.6.2. IAC control and parameter settings

There are 3 parameters which can be defined by the user in order to optimise the IAC function for a certain tuner type. These parameters are implemented as coefficients in the YRAM of the DSP.
With easy programming default values for these coefficients are loaded, these values are optimised for application with tuner TEA6811/TEA6824.

Threshold sensitivity and switching on/off the AM IAC, Y:IACsens

Y:IACsens determines the threshold sensitivity of the comparator from the interference detector.
The optimal setting is a compromise between sensitivity for interference and protection against unwanted triggering.
With this coefficient the AM IAC can be switched on and off. With Y:IACsens = $600 the IAC is switched OFF. The value for ON is the desired sensitivity, the default “on” value is

Y:IACsens = $080.
Practical control range is $010 - $200

Suppression stretch time, Y:countN

Y:countN determines the minimum suppression time at interference detection. During this time the gate switch will be activated in case of interference detection. The suppression stretch time is

Ts = Y:countN * 26 µs

Default value is Y:countN = $036 thus the stretch time Ts = 54 * 26 µs = 1.4 ms.
Practical control range is 800 - 2000 µs.

Feedback factor, Y:Gfeedb

This factor is a protection against continues mute at interference pulses with a high repetition rate.

The default value is Y:Gfeedb = $150.
Practical control range is $050 - $300.

9.4.6.3. AM IAC postdetection filter

Interference detection is performed after the AM detector on the AM audio signal. For a good detection it is important to maintain the full AM bandwidth after AM IF selectivity. Therefore any postdetection filtering between AM detection and the AM input application of the SAA7705 chip should be removed, except the low pass filter as given in the application diagram with f_c= 50kHz. The AM processing incorporates a postdetection filter behind the IAC function. This is a 2nd order Butterworth filter.
With this filter the AM audio bandwidth can be limited to the desired cut-off frequency.
The overall AM bandwidth will be the result of the cascade of this filter and the AM IF filter within the AM tuner.

The coefficients for several cut-off frequencies are given in the table below.

	coefficients				
Cut-off frequency (-3dB)	Y:BWb2 address $6A	Y:BWa2 address $6B	Y:BWb0 address $6C	Y:BWb1 address $6D	Y:BWa1 address $6E
Flat response	$000	$000	$400	$000	$000
4 kHz (default set)	$04B	$E6E	$04B	$097	$464
3.5 kHz	$03F	$E46	$03F	$07E	$4BE
3 kHz	$02F	$E0A	$02F	$05F	$537
2.5 kHz	$023	$DD0	$023	$047	$5A1
2 kHz	$017	$D88	$017	$02F	$618

The graph in figure 9.24 shows the frequency curves for 2, 2.5, 3, 3.5 and 4 kHz

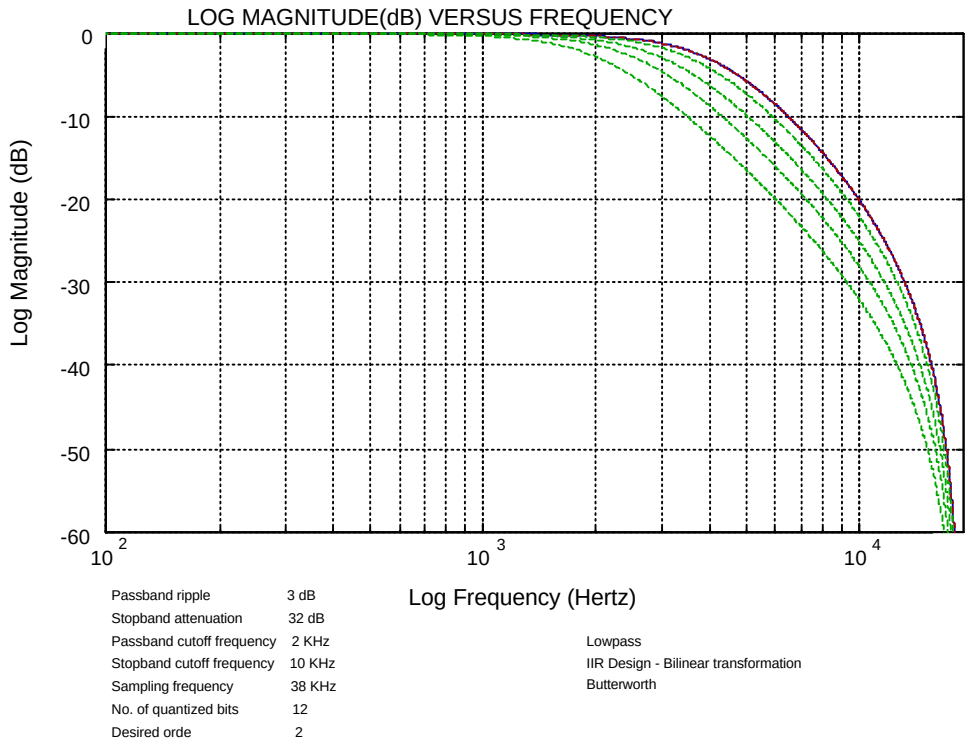


Fig. 9.24 frequency curves AM IAC postdetection filter

9.5 Tape mode

Overview of functions:
- Adjustment of dolby level
- Dolby-B

9.5.1 Adjustment of Dolby level

For the Tape mode the Dolby level for the program part Dolby-B has to be adjusted with coefficients **Y:DLBY_L and Y:DLBY_R** to compensate for the spread in sensitivity of the play-back head, the head amplifier and the A/D convertor.

The headroom for Dolby-B should be -12 dB (minimum) and for the tape head a tolerance of ± 3 dB is assumed. The head amplifier should deliver at Dolby level a nominal value of **1.1 Vrms - 15 dB = 200 mV** to the Tape (or CD_A) input circuit. (fig. 8.16)

The spread on this value has to be adjusted as follows:
Insert a cassette with Dolby level in the tape deck (200nW/m and 400 Hz).
Switch ON Dolby (set Y:cl4 = $26C).
For the left channel scale coefficient Y:DLBY_L with a factor α* LdefaultDolby until the value at X:DOLBY_LEV_L in XMEM meets the required value according table 9.33 with a certain tolerance. For the right channel scale the coefficient Y:DLBY_R with a factor α*RdefaultDolby until the value at X:DO-LBY_LEV_R in XMEM meets the required value according table 9.33 with a certain tolerance.

The required values (equal for left and right channel) are:

	Tolerance	Tolerance	Required value	Tolerance	Tolerance
	-1 dBr	-0.5 dBr	0 dBr	0.5 dBr	1 dBr
HEX value	#05F8A	#05EC3	#05DC5	#05CF3	#05C4E

Table 9.33 Required values for the Dolby-B decoder

Y:DLBY_L = α* LdefaultDolby
Y:DLBY_R = α* RdefaultDolby

LdefaultDolby= RdefaultDolby= 0.45 (= $399)

Note that Y:DLBY_L and Y:DLBY_R are set to $400 by Easy Programming Tape/MSS mode (set 3), these values should be set to $399 by the controller prior to the Dolby adjustment.

Remark: the scaling of the initial coefficients has to be within +/- 3 dB.
thus α= 1 +/- 3 dB α= 0.71.. 1.41

or Y:DLBY_L = α* LdefaultDolby= 0.32.. 0.64.
Y:DLBY_R = α* RdefaultDolby= 0.32.. 0.64.

9.5.2 Dolby-B

The Dolby-B noise reduction subroutine is designed for a sampling frequency of fs= 38 KHz. It realises the complete function of an analog Dolby-B decoder.
To switch on/off the Dolby function one has to set the following coefficient:

```
Y:cl4    $000    ; Default Dolby off
         $26C    ; Dolby on
```

9.6 CD_A mode

Overview of functions:
- Compressor

9.6.1 Compressor

The compressor curve (see fig. 9.25) is divided into two segments: There is a 1:1 ratio in the non-compression range below -54 dB Full Scale (FS), however with an amplitude shift of +18 dB, and there is a 1:2 ratio in the range above -54 dBFS. The 'point of no effect' is at (-18 dBFS/-18 dBFS) input/output level. To switch on/off the compressor function one has to set the following coefficient:

```
Y:(COMPRY0START+28)     $05A  ; Default Compressor off
                        $7AB  ;         compressor on
```

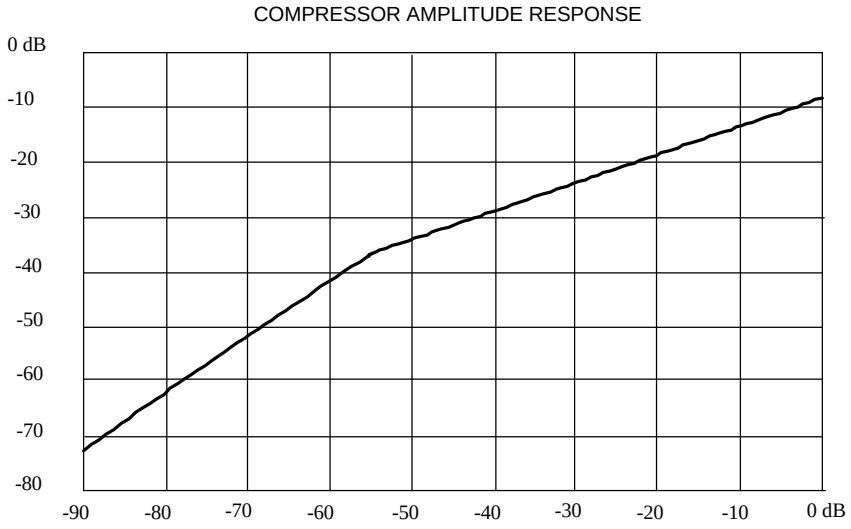


Fig. 9.25 Compressor curve

9.7 CD_D mode

Overview of functions:
- De-emphasis
  via flag
  via RAM
- Compressor

9.7.1 De-emphasis via flag

The frequency characteristic of the de-emphasis filter is according the CD standard (time constants are 50 µs and 15 µs and the sampling frequency is 44.1 KHz). These coefficients are automatically loaded via Easy Programming (set 4, CD)
The de-emphasis function via flag is automatically selected when pin DSP-IN2 = 1. This pin must be controlled by the de-emphasis control line coming from either a CD-1 or CD-2 player.

9.7.2 De-emphasis via RAM

The frequency characteristic of the de-emphasis filter is according the CD standard (time constants are 50 µs and 15 µs and the sampling frequency is 44.1 KHz). These coefficients are automatically loaded via Easy Programming (set 4, CD)
The de-emphasis function via RAM can be switched On/Off by sending an IIC message. The controller to SAA7705H must translate the polarity of the de-emphasis control line coming from either a CD-1 or CD-2 player into a value to Y:dmfViaRAM.

9.7.3 Compressor

The CD_D mode can use the compressor (see chapter 9.6) standalone or combined with one of the two above mentioned de-emphasis approaches.

9.7.4 Required control actions

After loading the easy programming set 4 (CD, X:modpntr= #005C0) one directly can select one of the three modes explained above:

de-emphasis via flag followed by compressor	X:modpntr= #00240
de-emphasis via RAM followed by compressor	X:modpntr= #00280
de_emphasis OFF	Y:dmfViaRAM= 0
de_emphasis ON	Y:dmfViaRAM= 1 (or another value not equal 0)
Compressor without any de-emphasis	X:modpntr= #00200 (same as for CD_A)

9.8 General purpose tone generator

9.8.1 Functional description

The purpose of the tone generator is twofold.

1. Generation of (sinewave) testsignals that may be used for measuring the performance of DA converters audio amplifiers.
   The signals may also be used for burn-in tests.
2. Production of a wide range of bleep sounds for audible feedback.

The tone generator continuously runs in all modes. Its output signal can be used in two ways:
- direct coupled to the input of the audio block, and skipping the selected source
- superposition at the output of the audio block without effecting the audio from the selected source (see section 9.8.5)

9.8.1.1 Tone generator

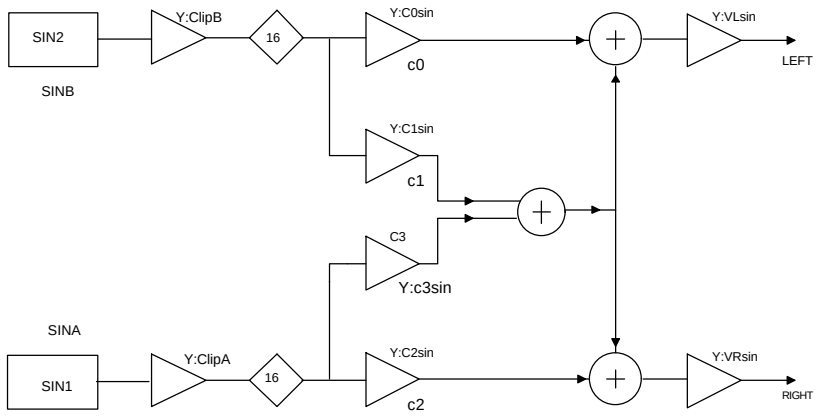


Fig. 9.26 Block diagram General Purpose Tone Generator

A block diagram of the generator is depicted in fig. 9.26. Sinewaves with adjustable frequency and full scale amplitude are produced by two independent generators: sin1 and sin2.
The signals are optionally amplified in a clipper that consists of a coefficient and a 4 bit shifter. So the clip level is determined by coefficients Y:ClipA and Y:ClipB. If Y:Clip.= 1/16 then a full scale pure sinewave signal is available.
By giving coefficients C0 to C3 (Y:c0sin.. c3sin) the appropriate value the Left and Right audio paths are connected with a sinewave generator or with a block, adding the generator outputs.

To initiate each generator - with output amplitude always full scale - the hostprocessor needs to update a separate double precision YRAM coefficient which determines the output frequency. Coefficients Y:VLsin and Y:VRsin determine the ultimate output level.
To start the oscillator we must select one out of next three initialization modes:
1: (re)start Sin1 and Sin2 synchronously
2: (re)start Sin1 only
3: (re)start Sin2 only

The frequency range runs from 20 to 17000 Hz. Measurements performed in the digital domain show that the inherent distortion is better then 96 dB (S/N + THD).

9.8.1.2 Timing generator

To simplify the actions of the host processor to control all types of beep signals, a timing generator has been added. The block diagram is shown in fig. 9.27.
This timing generator is always active.
The full scale output of a square wave generator with adjustable frequency and duty cycle is fed into an attack/release filter of the kind described in section 9.1.3.
The filter delivers an output 'a' which can be scaled (attenuation att in section 9.8.3.2) by coefficient Y:scalS1 and another output '1-a' which can be scaled by coefficient Y:scalS1~.

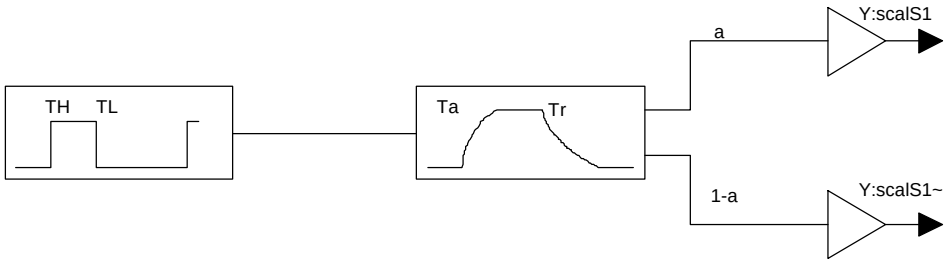


Fig. 9.27 Block diagram Timing Generator

Each filter output 'a' and '1-a' may be fed into one of the control coefficients C0, C1, C2, C3, (Y:c0sin..c3sin), Y:VLsin, Y:VRsin. The mutually inverted outputs 'a' and '1-a' are used to produce fade-in/out actions of both sinewave signals.

Fig. 9.28 shows the parameters which determine the square wave oscillator timing.

The output of a counter (X:counterX) is increased every sample period with a stepvalue X:stepSize. (default stepSize= 1). After reset the counter starts with a negative value determined by X:MinMax, the output of the square wave generator is then one. When the counter is positive, the square wave becomes zero. The counter is reset when it exceeds the X:PlusMax limit, then the process starts again.

The maximum periodtime T is 27.9 s. (MinMax=-131072 and PlusMax=131071 @ Fs= 38 kHz)

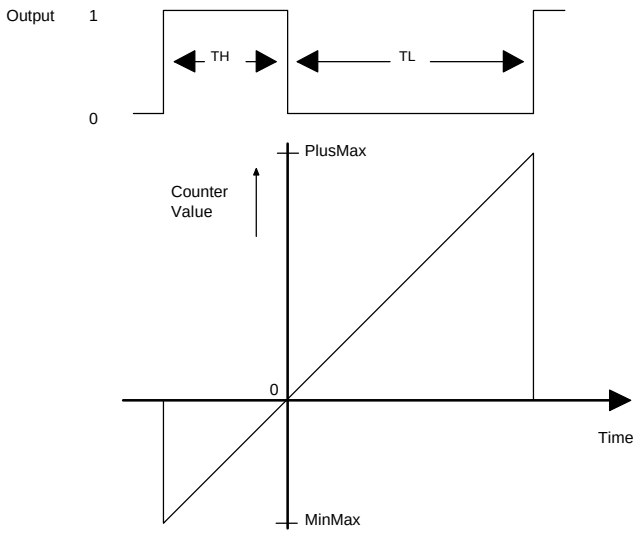


Fig. 9.28 CounterX and Output value as function of time.

9.8.2 RAM memory use for Sine Wave Generator

The next programmable XRAM places control the Timing generator.

X:counterX
X:PlusMax
X:MinMax

The YRAM places can be split up in three groups:
- The first group (Y:scalS1_ .. Y:c2sin) contains the values that control the Tone generator
- The second group (Y:VLsin .. Y:IcoefBH) contains the initialization values that determine the Volume and Frequency of each generator.
- The third group (Y:samDecl .. Y:switchA) contains the values that determine the attack and release (decay) times of the transitions in the Timing generator (Ta and Tr).

Y:scalS1_	Y:VLsin	Y:samDecl
Y:scalS1	Y:VRsin	Y:samDech
Y:cpyS1	Y:IclipAmax	Y:deltaD
Y:cpyS1_	Y:IclipAmin	Y:switchD
Y:c3sin	Y:IcoefAl	Y:samAttl
Y:c1sin	Y:IcoefAh	Y:samAtth
Y:c0sin	Y:IclipBmax	Y:deltaA
Y:c2sin	Y:IclipBmin	Y:switchA
	Y:IcoefBL	
	Y:IcoefBH	

YRAM Y:cpyS1_ holds a parameter where the scaled coefficient (1-a) must be copied to.
YRAM Y:cpyS1 holds a parameter where the scaled coefficient a must be copied to.
Each scaled coefficient can only be copied to one another coefficient out of next list.

The valid parameters for YRAM Y:cpyS1_ and Y:cpyS1 are:
VRsin ($8F5), VLsin ($8F6) and no_Action ($8FB), c0sin ($8F8), c1sin ($8F9), c2sin ($8F7) and c3sin ($8FA).

Example: If Y:cpyS1= $8F9 then Y:C1sin= a.

9.8.3 Calculations

9.8.3.0. sinewave generator:

Input variables:	f	Output frequency	[Hz]	Output coefficient: Csin (double precision)
	fs	Sample frequency	[Hz]	

$$q = \frac{2pf}{fs} \quad [rad]$$

$$Csin = \cos q$$

Example: f= 1000 Hz, fs= 38000 Hz

Θ= 0.165347
Csin= 0.986361 $7E4113_H$ (Y:IcoefAh = $7E4 Y:IcoefAl = $089)
(Y:IcoefBh = $7E4 Y:IcoefBl = $089)

9.8.3.1. generator clipping:

Input variable:	Gclip: Clip gain	[dB]	Output coefficient: Y:Clipn

for Gclip= 0 dB a full scale sine wave is generated, for values Gclip > 0 dB clipping occurs.

$$Y:Clipn = \frac{10^{\frac{Gclip}{20}}}{16}$$

Memory Y:Clipn is copied from the initialisation coefficients Y:IclipNmax and Y:IclipNmin.
Note that Y:IclipNmax and Y:IclipNmin should be set equal in all tone generator modes.

9.8.3.2. timing generator:

Input variables:	TH: High-out time	[sec]	Output coefficients:	X:PlusMax
	TL: Low-out time	[sec]		X:MinMax
	fs: Sample frequency	[Hz]		X:stepSize (default n=1)
	ps: Sample period (ps= 4/fs)	[sec]		
	ST: Step time (n* ps)	[sec]		Y:scalS1
	att: attenuation	[dB]		Y:scalS1~

$$X:stepSize = \frac{ST}{ps}$$

$$X:PlusMax = \frac{TL}{ST}$$

$$X:MinMax = \frac{TH}{ST}$$

$$Y:scalSx = 10^{\frac{att}{20}}$$

9.8.3.3. attack/release filter timing:

The implemented attack/ release filter has independent attack and release times, by using two separate filter coefficient sets. One for attack and the other for release time.

The rise/fall time definition is given in fig. 9.29. After 5* Tr (or 5* Ta) the transient is generally regarded as terminated.

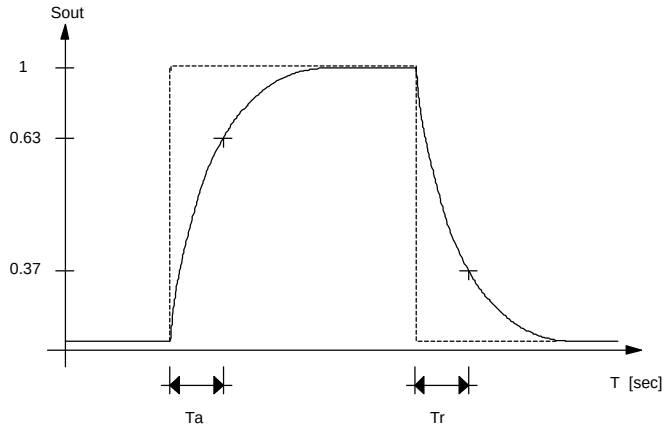


Fig. 9.29 Rise time definition

Input variables:	T:	rise/fall time	[sec]	Output coefficients:	Y:delta' Y:switch' Y:samH, samL
	fs:	sample frequency.	[Hz]		

$$a = e^{\frac{-4}{T \bullet fs}}$$

$$Y:samH,samL = a$$

$$(Y:deltaA) * (Y:switchA) = (1-a) \qquad (risetime)$$

$$(Y:deltaD) * (Y:switchD) = (0) \qquad (falltime)$$

Choose the coefficient values Y:deltaA and Y:switchA in such a way that the product is (1-a)
Choose the coefficient values Y:deltaD and Y:switchD in such a way that the product is 0

Approach 1:
A solution is: Y:deltaA= Y:switchA= $\sqrt{(1-a)}$

Example 1: fs= 38 kHz	Ta = 10 ms		Td= 10 ms	
a=0.989529 $7EA8E2_H$	Y:samAttl =	$471	Y:samDecl =	$471
1-a=0.0104711	Y:samAtth =	$7EA	Y:samDech =	$7EA
$\sqrt{(1-a)}$=0.102328	Y:deltaA =	$0D2	Y:deltaD =	$0D2
	Y:switchA =	$0D2	Y:switchD =	$000

Approach 2:
For a wide range of rise/fall times it is not necessary to change Y:deltaA and Y:deltaD.
For practical rise time values Ta= 3.2 .. 1000 ms, one can work with Y:deltaA= $059 fixed, and only varying Y:switchA and Y:samAtth,samAttl according following table.
For practical fall time values Td= 3.2 .. 1000 ms, one can work with fixed values Y:deltaD= $059 and Y:switchD=0 and Y:samDech,samDecl according following table (with Y:switchD=0 coefficient Y:deltaD is in fact don't care).

fs =38000 Hz	Ta/ Td (milli seconds)			
Ta/ Td	Y:sam.l	Y:sam.h	Y:delta.	Y:switch.
3.2	$7A4	$7BC	$059	$618
4.6	$0A6	$7D2	$059	$42C
6.8	$4D3	$7E0	$059	$2DA
10.0	$471	$7EA	$059	$1F3
14.7	$2EF	$7F1	$059	$154
21.5	$027	$7F6	$059	$0E8
31.6	$18F	$7F9	$059	$09E
46.4	$2E3	$7FB	$059	$06B
68.1	$6B5	$7FC	$059	$049
100.0	$6C3	$7FD	$059	$032
146.8	$441	$7FE	$059	$022
215.5	$7FF	$7FE	$059	$017
316.3	$28C	$7FF	$059	$00F
464.2	$449	$7FF	$059	$00A
681.4	$578	$7FF	$059	$007
1000.1	$646	$7FF	$059	$005

Example 2:

Input variables:	Ta: attack time Tr: release time (decay time)	[sec] [sec]	Output coefficients:	Y:switchA Y:deltaA Y:samAtth Y:samAttl	Y:switchD=0 Y:deltaD Y:samDech Y:samDecl

attack values for ta= 10 ms

Y:samAttl $471 double precision coefficient, low part
Y:samAtth $7EA double precision coefficient, high part
Y:deltaA $059
Y:switchA $1F3

release values for tr= 100 ms

Y:samDecl $6C3 double precision coefficient, low part
Y:samDech $7FD double precision coefficient, high part
Y:deltaD $059 Note that this value is in fact don't care
Y:switchD $000

9.8.4 Required process control

Loading Easy Programming set1 (ALL) automatically loads all default settings.
After this initialization one has to set volume, frequency and tone function according next selections.

9.8.4.1 Single tone (mono and stereo)

If a single tone on both outputs is needed, the following memories must be initialized:
(no local Soft Audio Mute function)

Y:scalS1_	= $7FF	Coefficient 1-a not scaled
Y:scalS1	= $7FF	Coefficient a not scaled
Y:cpyS1	= $8FB	(no action)
Y:cpyS1_	= $8FB	(no action)
Y:c3sin	= $000	
Y:c1sin	= $000	
Y:c0sin	= $7FF	
Y:c2sin	= $7FF	

Example: f= 1000 Hz, fs=38 kHz Full scale

Y:VLsin	= $7FF	Full scale output
Y:VRsin	= $7FF	Full scale output
Y:IClipAmax	= $080	Linear output (no clipping)
Y:IClipAmin	= $080	Linear output (no clipping)
Y:IcoefAl	= $089	low part coefficient A
Y:IcoefAh	= $7E4	high part coefficient A
Y:IClipBmax	= $080	Linear output (no clipping)
Y:IClipBmin	= $080	Linear output (no clipping)
Y:IcoefBL	= $089	low part coefficient B
Y:IcoefBH	= $7E4	high part coefficient B

The registers Y:Icoef.l and Y:Icoef.h must be loaded with the calculated (double precision) value Csin.
(see example in section 9.8.3.0)

To (re)start a single tone signal, first the amplitude (Y:V.sin), the frequency (Y:Icoef.h, Y:Icoef.l) and the clipping factor (IClip.max, Y:IClip.min) must be loaded, followed by selecting the wanted wave generator initialization mode:

Y:iSinusWant= $82A sinusA = sinusB

After initializing the oscillator mode can be selected:

Y:sinusMode= $89A OFF (default set by easy programming ALL) (set 1)
Y:sinusMode= $897 ON
Y:sinusMode= $88D Superposition (see section 9.8.5)

If a different tone on left or right is needed (stereo), without restarting the other one, then:

a) If new parameters for SIN1 (sinusA, right signal) are needed, the amplitude (Y:VRsin), the frequency (Y:IcoefAh, Y:IcoefAl) and the clipping factor (Y:IClipAmax, Y:IClipAmin) must be loaded, followed by selecting the wanted initialization:

Y:iSinusWant= $835 sinusA

After initializing the oscillator the ON mode can be selected by: Y:sinusMode= $897.

b) If new parameters for SIN2 (sinusB, left signal) are needed, the amplitude (Y:VLsin), the frequency (Y:IcoefBh, Y:IcoefBl) and the clipping factor (Y:IClipBmax, Y:IClipBmin) must be loaded, followed by selecting the wanted initialization:

Y:iSinusWant= $82D sinusB

After initializing the oscillator the ON mode can be selected by: Y:sinusMode= $897.

9.8.4.2 Single tone burst (mono), with local Soft Audio Mute function

If a single tone burst with different attack and release time is needed on both outputs, the following memories must be initialized:

Y:scalS1_	= $7FF	Coefficient 1-a not scaled
Y:scalS1	= $7FF	Coefficient a not scaled
Y:cpyS1	= $8F9	Copy a to C1
Y:cpyS1_	= $8FB	(no action)
Y:c3sin	= $000	
Y:c1sin	= $000	
Y:c0sin	= $000	
Y:c2sin	= $000	

Example: f= 400 Hz, fs=38 kHz Full scale

Y:VLsin	= $7FF	Full scale output
Y:VRsin	= $7FF	Full scale output
Y:IClipAmax	= $080	Linear output (no clipping)
Y:IClipAmin	= $080	Linear output (no clipping)
Y:IcoefAl	= $42D	low part coefficient A
Y:IcoefAh	= $7FB	high part coefficient A
Y:IClipBmax	= $080	Linear output (no clipping)
Y:IClipBmin	= $080	Linear output (no clipping)
Y:IcoefBL	= $42D	low part coefficient B
Y:IcoefBH	= $7FB	high part coefficient B

Setting: T_a= 4.6 ms, T_r= 21.5 ms
Y:samDecl = $027
Y:samDech = $7F6
Y:deltaD = $059
Y:switchD = $000

Y:samAttl = $0A6
Y:samAtth = $7D2
Y:deltaA = $059
Y:switchA = $42C

Initializing Timing generator: TH= 108 ms, TL= 500 ms,
X:counterX = #00000
X:plusmax = #01290
X:minmax = #3FBFE

The tone burst restarts after T= T_H+ T_L. If only one burst is wanted, this waveform generator program must be left just before the next period starts. If for example 3 bursts are needed, the main program must stay for a time of just less 3T in the waveform generator mode.

To start a burst signal, first load the YRAM coefficients, then start the timing generator XRAM coefficients, followed by initializing the tone generator:

Y:iSinusWant = $82A sinusA = sinusB

After this initialization the oscillator can be started by: Y:sinusMode= $897.
(For superposition see section 9.8.5)

9.8.4.3 Alternating tone (mono)

Switch over in frequency with Soft Audio Mute function (soft fade_out f1 and soft fade_in f2)
For next example equal attack and release time is chosen, and the following memories must be initialized:

Y:scalS1_	= $7FF	Coefficient 1-a not scaled
Y:scalS1	= $7FF	Coefficient a not scaled
Y:cpyS1	= $8FA	Copy a to C3 (during TH sinusA selected)
Y:cpyS1_	= $8F9	Copy 1-a to C1 (during TL sinusB selected)
Y:c3sin	= $000	
Y:c1sin	= $000	
Y:c0sin	= $000	
Y:c2sin	= $000	

Example: f1= 1350 Hz (sinusA, full scale) f2= 1050 Hz (sinusB, full scale) ; fs=38 kHz

Y:VLsin	= $7FF	Full scale output
Y:VRsin	= $7FF	Full scale output
Y:IClipAmax	= $080	Linear output (no clipping)
Y:IClipAmin	= $080	Linear output (no clipping)
Y:IcoefAl	= $183	low part coefficient A
Y:IcoefAh	= $7CD	high part coefficient A
Y:IClipBmax	= $080	Linear output (no clipping)
Y:IClipBmin	= $080	Linear output (no clipping)
Y:IcoefBL	= $1B2	low part coefficient B
Y:IcoefBH	= $7E1	high part coefficient B

Setting: $T_a = T_r = 4.6$ ms

Y:samDecl	= $0A6	Y:samAttl	= $0A6
Y:samDech	= $7D2	Y:samAtth	= $7D2
Y:deltaD	= $059	Y:deltaA	= $059
Y:switchD	= $000	Y:switchA	= $42C

Initializing Timing generator: TH= 50 ms, TL= 80 ms,

X:counterX	= #00000
X:plusmax	= #002F8
X:minmax	= #3FE25

The tone burst restarts after $T = T_H + T_L$. If only one burst is wanted, this waveform generator program must be left just before the next period starts. If for example 3 bursts are needed, the main program must stay for a time of just less 3T in the waveform generator mode.

To start an alternating tone signal, with local Soft Audio Mute function, first load the YRAM coefficients for frequency f1 and frequency f2, then start the timing generator by setting the relevant XRAM coefficients, followed by initializing the tone generator:

Y:iSinusWant= $82A sinusA= sinusB

After this initialization the oscillator can be started by: Y:sinusMode= $897.
(For superposition see section 9.8.5)

With the settings above, the start is in such a way that f1 is faded out, together with starting f2. To avoid this 'starting problem' one should set Y:cpyS1_ =$8FB (no action), and after t_a is passed SIN2 must be enabled by setting Y:cpyS1_= $8F9. (coupling 1-a to C1).
If a soft fade_out after the alternating tone is wanted, the timing of the main processor must be in such a way, that if the last wanted tone is active, the other one must be coupled off by either setting Y:cpyS1 or Y:cpyS1_ to no_action ($8FB).

9.8.5 Superposition of Tone generator with current Audio

9.8.5.1 Functional description

The superposition of a tone_generator_signal with the current audio signal is possible in all operation modes. The tone_generator_signal (note: left and right can be different, and have their own volume setting with coefficients Y:VLsin and Y:VRsin) can be added to each DAC signal (FL..RR) just after the SoftAudioMute coefficient. (see diagram in fig. 9.30)
Each superposition can be regulated by its coefficient Y:tfnFL..tfnRR. One should avoid the combination of too high Audio signals together with high amplitude tone_generator_signals, because of the possibility for clipping.
If the superposition is not used (coefficient 'switch' Y:sinusmode in drawn position) then automatically zero is added to the DAC outputs.
The paragraphs of chapter 9.8 handling the tone generator do apply also for this superposition. One should keep in mind that the generator frequency is dependent of the used sample frequency fs.

Fig. 9.30 Diagram Superposition tone generator signal to Audio

9.8.5.2 RAM memory use for Superposition

Next coefficients are used by the superposition function:
Y:tfnFL Y:sinusMode
Y:tfnFR
Y:tfnRL
Y:tfnRR

Coefficients Y:tfnFL..tfnRR determine the amplitude setting of the superimposed tone_generator_signal.
Initialized value by Easy Programming (set 1 ALL) Y:tfnFL..tfnRR= 0
The coefficient Y:sinusMode has 3 possible values. (Tone generator ON/ OFF or Superposition)
Initialized value by Easy Programming (set 1 ALL) Y:sinusMode= $89A (Tone generator OFF)

9.8.5.3 Calculation of attenuation for Superposition

Input variables:
SR: superposition attenuation [dB]
(attenuation range 0.. ∞ dB)

Output coefficients:
Y:tfnFL, Y:tfnFR
Y:tfnRL, Y:tfnRR

$$Y{:}tfnXX = -10^{-\frac{SR}{20}}$$

Examples:
Next table gives some example attenuation and coefficient values for the superposition coefficient setting.

attenuation SR [dB]	coefficient Y:tfnXX
6	$BFE channel -6B
99	$000 channel muted

9.8.5.4 Required control actions for Superposition of Tone generator

First select the wanted superposition level for each signal. (Coefficients Y:tfnFL..tfnRR according section 9.8.5.3).

Set frequency and timing generator for the actual sample frequency. (section 9.8.1.. 9.8.4), together with the amplitude of the generator. (Coefficients Y:VLsin and Y:VRsin)

After initializing these levels one can switch on the superposition mode by setting:
Y:sinusMode= $88D

9.9 Music Search Mode (MSS)

9.9.1 Functional description

The function of the MSS mode is, to search for the next pause on e.g. a cassette tape. A pause is detected when the tape audio signal is below a pre-defined level for a certain amount of time. The output of the pause detector is pin DSP-OUT2. If a Pause is detected, the DSP-OUT2 pin becomes "High", else "Low". The audio outputs are muted in the MSS mode.

9.9.2 Variable parameters MSS

The detection threshold X:MinLevel, below which a pause will be detected is default set to -35 dB below full scale in the CDSP. This results in a detection threshold for the average signal of -32 dB below full scale of the A/D convertor (-35 dB peak + 3 dB due to averaging the input signal).
A pause is detected, after the input signal has remained below the threshold for a certain time. This time is determined by X:CountMax. Default X:CountMax is set to 70 ms. For a sample frequency of 38 kHz, this corresponds to 2660 samples. Since the decay time of the filter has to be subtracted from 70 ms, the value 2500 is implemented (see calculations below). Further the onset of the DSP-OUT2 pin is slightly depending upon the input level. The constant X:Attack is used to reduce the sensitivity of the pause detection if a distortion occurs during pause (music attack time). It is set to 70 (about 1 ms) for the current implementation.

calculations:

X:CountMax = (minimum pause time(s) - 0.004) * 38000
X:Attack = X:CountMax / (38000 * music attack time(sec))
X:MinLev = exp10 (1/20((detection threshold A/D in dB below full scale) - (3 dB)))

Default values XMEM:

```
X:CountMax      #009C4   ;minimum pause time before a pause will be detected is about 70 ms
X:MinLev        #0091A   ;threshold for pause detection is -32 dB below Full scale of the A/D
X:Attack        #00046   ;minimum music time before the DSP-OUT2 pin becomes low is about 1 ms
```

9.9.3 Process control

Select MSS as follows:

- download Easy Programming set 3
- set X:modpntr to #00500. MSS is now continuously active and the pause pin indicates each pause.
- To restart the pause detection send Y:mod20=$12F. After restart the minimum pause time has to be passed until a pause becomes indicated.
- To exit the MSS mode and return to Tape mode, simply start the Tape mode according table 9.13

9.10 SPEECH mode

This mode is intended to apply for instance a mono speech signal to **one input channel**, and to get output over **both audio channels**. In these modes a 6th order filter is available e.g. to optimise the audio response for speech.

9.10.1 SPEECH control

The preferred use of the SPEECH mode is (voice) input via the (free) AM_L input. This signal is directed via a 6th order filter to the left and right channel of the Audio processor.

For SPEECH via AM_L input:

Load easy programming set 5 (AM, Speech) with x:modpntr= #00640
Load IIC control registers for AM input
Start SPEECH function (from a left input to both audio channels) with x:modpntr= #00300

If we want to get speech signals from other inputs, for example via the CMRR inputs CD_L or CD_R one must proceed in the following way:
For SPEECH via CD inputs:

Load easy programming set 5 (AM, Speech) with x:modpntr= #00640
Load IIC control registers for CD analog input
Start SPEECH function (from the left input to both audio channels) with x:modpntr= #00300
Start SPEECH function (from the right input to both audio channels) with x:modpntr= #002C0

9.10.2 6th order filter

The implemented 6th order filter is shared with the AM mode.
For calculations and coefficient settings see chapter 9.4.

9.11 Radio Data System (RDS) function

For extended information on the RDS decoder see the data sheet of the SAA7705H.
The RDS decoder has three different functions:

- RDS clock and data recovery from the MPX signal
- Buffering of 16 bits if selected
- Interfacing with the micro controller

The RDS chain has a separate input. This enables RDS updates during tape play and also the use of a second receiver for monitoring the RDS information of signals from another transmitter (double tuner concept). It can as such be done without interruption of the audio program. The MPX signal from the main tuner of the car can be connected to this RDS input via the built in source selector. The input selection is controlled by the sel_two_tun bit of the IIC_SELection register (see data sheet of the SAA7705H).

Buffer interface

The RDS interface buffers 16 data bits. Every time 16 bits are received, the data line is pulled down and the buffer is overwritten. The control microprocessor has to monitor the data line in at least every 13.5 msec. This mode is selected by setting the rds_clkin bit of the IIC_RDS_ConTrol register (see data sheet of the SAA7705H).
When this mode is not selected then the RDS data and clock come directly from the CDSP.

9.12 Use of a second processor

The most common use of this second processor is for additional audio functions/ features.
Normally the audio signals processed by the CDSP directly go to the fader section in front of the DA convertor (see also section 9.1.1.3). If no second processor and NO subwoofer is used then the I2S data output should be disabled to minimise EMI.

If one wants to use this second processor the CDSP must be initialized to be a master I2S transmitter (it can be the standard IIS but also Japanese formats) and the external device has to be synchronised with the word select line. The I2S output signals (IISout1L and IISout1R) from the CDSP are the in_L and in_R (section 9.1.1.2) just after the BALance function with its 5 bit shifter and is used as input to the external processor, or in the case of a 2*10 bands equalizer the equalizer outputs are used. (see next graph)
The feedback signals of the external processor are two processed stereo audio channels on respectively IIS_IN1 and IIS_IN2. The IIS signals are split in the CDSP as follows:
IIS_IN1 is split in IISin1L and IISin1R and IIS_IN2 is split in IISin2L and IISin2R .

```
in_L  ÄÄÄ (EQUoutFL ÄÄ EQUinFL) ÄÄÄÄ IISout1L
in_R  ÄÄÄ (EQUoutFR ÄÄ EQUinFR) ÄÄÄÄ IISout1R

                     Y:FLcof          Y:SAM
IISin1L ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´>ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´>ÄÄÄÄÄÄÄÄÄÄ  front_L
IISin1R ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´>ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´>ÄÄÄÄÄÄÄÄÄÄ  front_R
                     Y:FRcof          Y:SAM
                     Y:RLcof          Y:SAM
IISin2L ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´>ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´>ÄÄÄÄÄÄÄÄÄÄ  rear_L
IISin2R ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´>ÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄÄ´>ÄÄÄÄÄÄÄÄÄÄ  rear_R
                     Y:RRcof          Y:SAM
```

These two independent stereo IIS sources are coupled to front and rear stereo channels. Each channel has its own 'level setting' coefficient. With the coefficients Y:FLcof, Y:FRcof and Y:RLcof, Y:RRcof one independently can control each signal, in both amplitude as in balance with each other.
(Mostly all coefficients will have full scale value ($800))

In the case one uses a 4*5 bands equalizer each IISin data line can have its own equalizer.

It is possible to make a fader function for these two stereo input signals.
For calculation of the multiplying coefficients Y:F.cof and Y:R.cof for the fader function the formulas out of section 9.12.2 can be applied.

9.12.1 RAM memory use for Second Processor

Y:FLcof Y:RLcof
Y:FRcof Y:RRcof

Y:OutSwi

With the coefficients Y:FLcof, Y:FRcof and Y:RLcof, Y:RRcof one independently can control each signal, in both amplitude as in balance with each other. (Mostly all coefficients will have full scale value ($800)).
These 4 coefficients are coefficients in a group out of 20 'fixed' audio coefficients

The values of the YRAM coefficients Y:FLcof .. Y:RRcof are determined by the fader setting.

9.12.2 Calculation of Fader function for Second Processor

Input variables:
- FR: front attenuation. [dB] (attenuation range 0.. ∞ dB)
- RE: rear attenuation. [dB] (attenuation range 0.. ∞ dB)

Output coefficients:
Y:FLcof, Y:FRcof
Y:RLcof, Y:RRcof

$$Y{:}\ FLcof = Y{:}\ FRcof = -10^{-\frac{FR}{20}}$$

$$Y{:}\ RLcof = Y{:}\ RRcof = -10^{-\frac{RE}{20}}$$

Examples:

Table 9.34 gives some attenuation and coefficient values as a function of the fader setting.

Attenuation [dB] FR	RE	Y:FLcof Y:FRcof	Y:RLcof Y:RRcof
30	0	$FC0	$800
6	0	$BFE	$800
0	0	$800	$800
0	30	$800	$FC0
0	99	$800	$000 (rear channel muted)

Table 9.34 Coefficient values Fader for second processor

9.12.3 Control actions Second Processor

Second processor **off**.

A) Digital line out (Subwoofer disabled) — See equalizer section 9.1.6.4.1

B) no Equalizer (Subwoofer enabled) — See equalizer section 9.1.6.4.2

C) 4*5 bands Equalizer (Subwoofer enabled) — See equalizer section 9.1.6.4.2

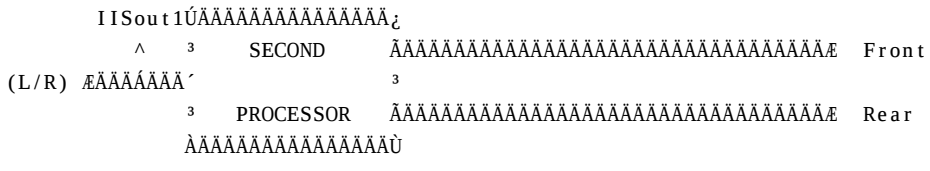
D) 2*10 bands Equalizer (Subwoofer enabled) — See equalizer section 9.1.6.4.2

9.12.4 **Required action controls Equalizer** (second processor on)

- equalizer **off**

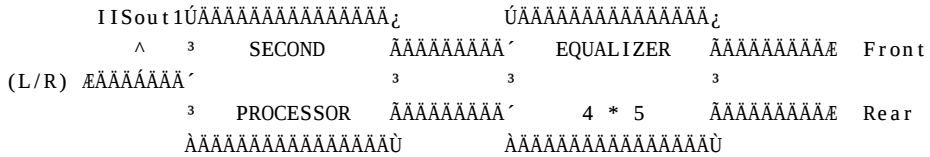
After using equalizer change EqualizerGain in steps of max. 1 dB towards EqualizerGain= 0. (flat response)

To start next configuration <2nd Processor,DAC and no equalizer>:
- load Y:OutSwi = $A8C
- bit TWO-FOUR of IIC_AD register= don't care.



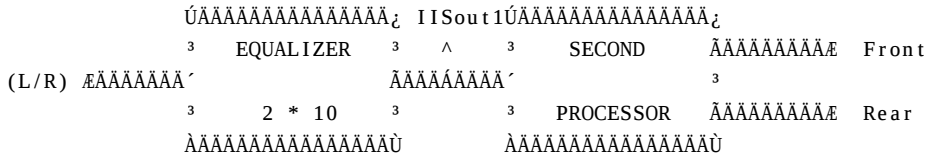
- equalizer 4*5 bands **on**

To start next configuration <2nd Processor,DAC and 4*5 bands equalizer>:
- load Y:OutSwi = $A9A
- bit TWO-FOUR of IIC_AD register = 0.



- equalizer 2*10 bands **on**

To start next configuration <2nd Processor,DAC and 2* 10 bands equalizer>:
- load Y:OutSwi = $A8F
- bit TWO-FOUR of IIC_AD register= 1.



9.13 Transparant mode

9.13.1Functional description

With this mode it is possible to connect each (stereo) source directly to the (stereo) audio processing block WITHOUT any additional source processing.
This mode can be used for instance:

if an external AM stereo decoder is used	together with AM_L and AM_R inputs
if an external DOLBY C decoder is used	together with TAPE-L and TAPE_R inputs or with CD_L and CD_R inputs
for handling external DAB signals	together with CD-1 or CD-2 channels

9.13.2Required control actions

For this mode no additional Easy Programming set has to be downloaded. All Audio processing related coefficients are present, directly after leaving the initial waitloop after RESET, or are already initialized to the wishes of the user. (section 9.1)

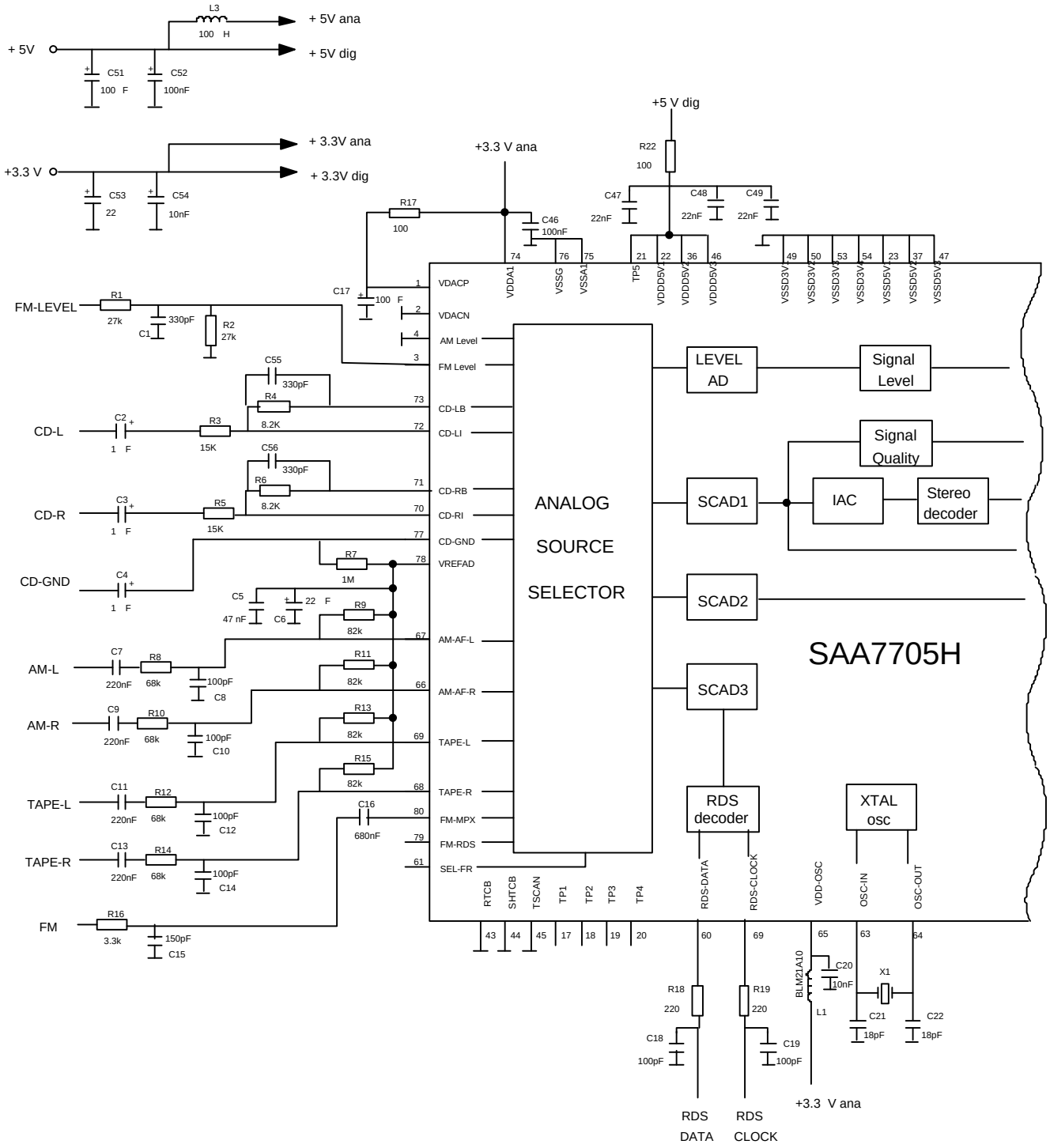
With the help of tables in par. 9.0.2 (Hardware configuration of the SAA7705H) one can select each (stereo) source.
By sending X:modpntr= #00400 that selected source is directly coupled to the Audio block.

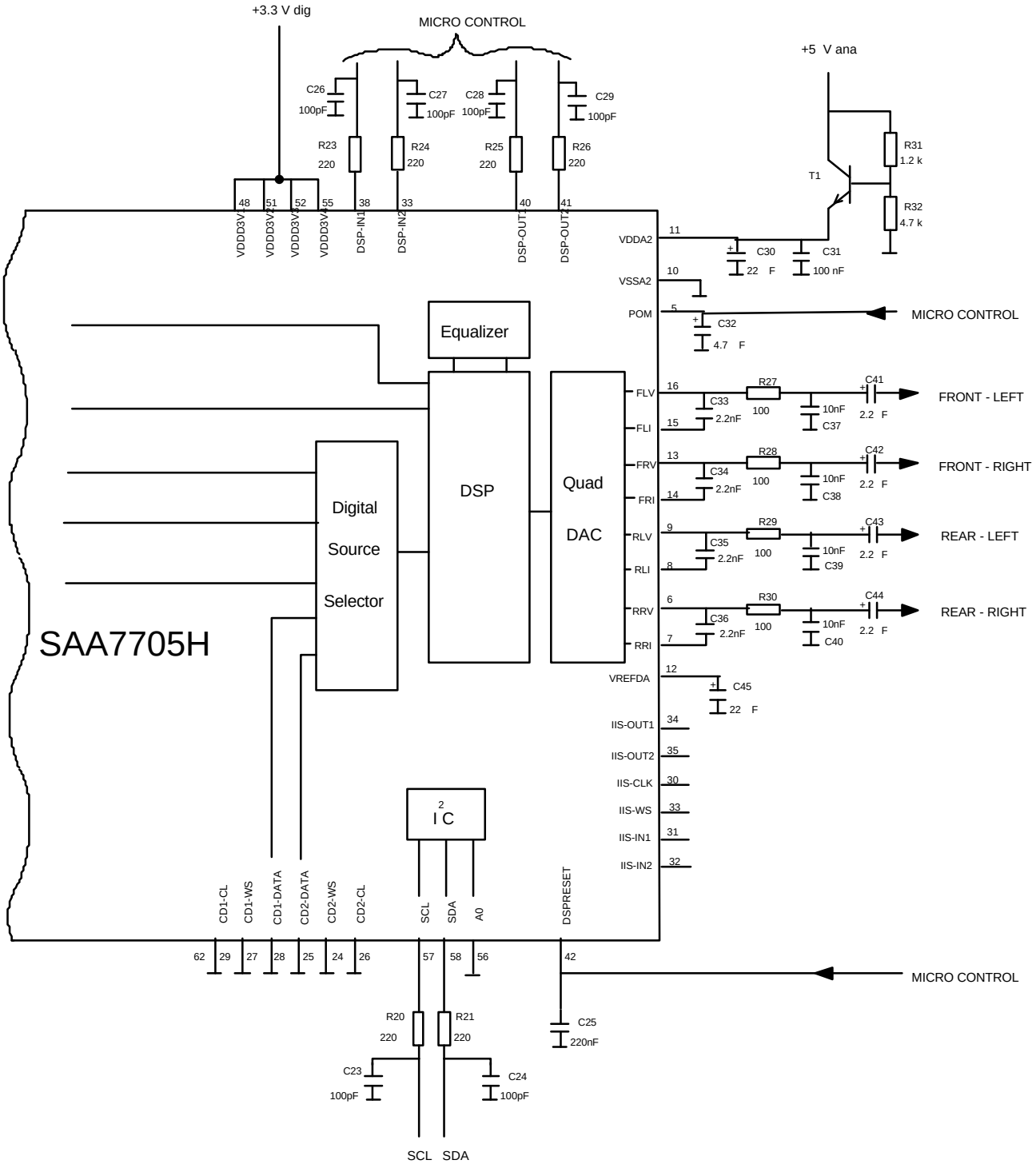
10 Literature

10.1 Data sheet SAA7705H
10.2 Data sheet SAA7740H
10.3 Usermanual evaluation board & software (AN 9604)
10.4 Application note AN9602

11 Appendices

11.1 Application diagram of the SAA7705




+3.3 V dig
MICRO CONTROL
+5 V ana
C26
100pF
C27
100pF
C28
100pF
C29
100pF
R23
220
R24
220
R25
220
R26
220
R31
1.2 k
R32
4.7 k
T1
48
51
52
55
38
33
40
41
VDDD3V1
VDDD3V2
VDDD3V3
VDDD3V4
DSP-IN1
DSP-IN2
DSP-OUT1
DSP-OUT2
VDDA2
VSSA2
POM
11
10
5
C30
22 F
C31
100 nF
C32
4.7 F
MICRO CONTROL
Equalizer
DSP
Quad
DAC
Digital
Source
Selector
SAA7705H
FLV
FLI
FRV
FRI
RLV
RLI
RRV
RRI
16
15
13
14
9
8
6
7
R27
R28
R29
R30
100
C33
2.2nF
C34
2.2nF
C35
2.2nF
C36
2.2nF
C37
10nF
C38
10nF
C39
10nF
C40
10nF
C41
2.2 F
C42
2.2 F
C43
2.2 F
C44
2.2 F
FRONT - LEFT
FRONT - RIGHT
REAR - LEFT
REAR - RIGHT
VREFDA
12
C45
22 F
IIS-OUT1
IIS-OUT2
IIS-CLK
IIS-WS
IIS-IN1
IIS-IN2
34
35
30
33
31
32
I2C
CD1-CL
CD1-WS
CD1-DATA
CD2-DATA
CD2-WS
CD2-CL
SCL
SDA
A0
DSPRESET
62
29
27
28
25
24
26
57
58
56
42
MICRO CONTROL
R20
220
R21
220
C23
100pF
C24
100pF
C25
220nF
SCL SDA

11.2 Partslist belonging to the SAA7701H application diagram

Component reference designator	Component Value	Max. Tolerance (see note)	Material/ Type
R1,R2	27K	10 %	RC11 / SMD
R3,R5	15K	10 %	RC11 / SMD
R4,R6	8K2	10 %	RC11 / SMD
R9,R11,R13,R15	82K	10 %	RC11 / SMD
R7	1M	10 %	RC11 / SMD
R8,R10,R12,R14	68K	10 %	RC11 / SMD
R16	3K3	10 %	RC11 / SMD
R18,R19,R20,R21,R23, R24,R25,R26	220E	20 %	RC11 / SMD
R17, R22	100E	10 %	RC11 / SMD
R27,R28,R29,R30	100E	20 %	RC11 / SMD
R31	1K2	10 %	RC11 / SMD
R32	4K7	10 %	RC11 / SMD
C1	330 pF	10 %	NP0 / SMD
C7,C9,C11,C13,C25	220 nF	10 %	MKT / FILM
C2,C3,C4	1 µF	10 %	
C5	47 nF	10 %	NP0 / SMD
C8,C10,C12,C14	100 pF	10 %	NP0 / SMD
C6,C30,C53	22 µF	10 %	
C15	150 pF	10 %	NP0 / SMD
C16	680 nF	10 %	MKT / FILM
C18,C19,C23,C24, C26,C27,C28,C29	100 pF	20 %	NP0 / SMD
C21,C22	18 pF	10 %	NP0 / SMD
C31,C46,C52	100 nF	20 %	X7R / SMD
C32	4.7 µF	10 %	
C33,C34,C35,C36	2.2 nF	5 %	X7R / SMD
C20,C37,C38,C39,C40,C54	10 nF	20 %	NP0 / SMD
C41,C42,C43,C44	2.2 µF	10 %	
C47,C48,C49	22 nF	20 %	X7R / SMD
C55,C56	330 pF	10 %	NP0 / SMD
C17,C51	100 µF	20 %	
C45	22 µF	10 %	
L1			BLM21A10
L3	100 µH	20 %	microchoke
T1			BC548
X1	11.2896 MHz	± 100 ppm	

note: tolerance within required operating temperature range.

11.3 Listing of XRAM and YRAM default coefficients

*** X-MEMORY DECLARATION *** ALL / Audio / Tonegenerator

XMEM address	label	dec	hex	fract	line
$0	modpntr	0	0	0.000000	729
$1	levn	0	0	0.000000	832
$2	leva	0	0	0.000000	833
$3	hdf1	0	0	0.000000	834
$4	hdf2	0	0	0.000000	835
$5	mltf	0	0	0.000000	836
$6	mlta	0	0	0.000000	837
$7	mltflim	0	0	0.000000	838
$8	dc_inl	0	0	0.000000	866
$9	dc_outl2	0	0	0.000000	867
$A	dc_outl	0	0	0.000000	868
$B	dc_outr2	0	0	0.000000	869
$C	dc_outr	0	0	0.000000	870
$D	dc_inr	0	0	0.000000	871
$5D	din_L	0	0	0.000000	5439
$5E	din_R	0	0	0.000000	5440
$5F	COMPRdelay	8202	200A	0.062576	570
$60	LoudnXL	7559	1D87	0.057671	571
$61	LoudnXR	8071	1F87	0.061577	572
$62	btrebXL	15751	3D87	0.120171	573
$63	btrebXR	16263	3F87	0.124077	574
$64	pntrDAi	12804	3204	0.097687	576
$65	pntrDAo	13060	3304	0.099640	577
$66	pntrLou	15936	3E40	0.121582	578
$67	pntrMax	14656	3940	0.111816	579
$68	audiol	14848	3A00	0.113281	581
$69	audior	15104	3B00	0.115234	582
$6A	audioc	11264	2C00	0.085938	583
$6B	audios	15572	3CD4	0.118805	584
$6C	YSW0pntr	13386	344A	0.102127	586
$6D	YSW1pntr	5194	144A	0.039627	587
$6E	ldf1Pntr	4104	1008	0.031311	588
$6F	min0999	-131072	20000	-1.000000	589
$76	LoL1L	0	0	0.000000	320
$77	S0QPD0	0	0	0.000000	321
$7E	LoR1L	0	0	0.000000	325
$7F	S1QPD0	0	0	0.000000	326
$C4	samZh	0	0	0.000000	329
$C5	samZl	0	0	0.000000	330
$C6	maxFi	0	0	0.000000	331
$C7	maxRi	0	0	0.000000	332
$C8	FLin	0	0	0.000000	336
$C9	FRin	0	0	0.000000	337
$CA	RLin	0	0	0.000000	338
$CB	RRin	0	0	0.000000	339

*** X-MEMORY DECLARATION *** ALL (continued)					
XMEM address	label	dec	hex	fract	line
$CC	FLout	0	0	0.000000	343
$CD	FRout	0	0	0.000000	344
$CE	RLout	0	0	0.000000	345
$CF	RRout	0	0	0.000000	346
$D6	Ldf	0	0	0.000000	352
$D7	XSW0pntr	13703	3587	0.104546	353
$D8	SubWoof	0	0	0.000000	354
$D9	Center	0	0	0.000000	355
$DA	maxDAT1	0	0	0.000000	358
$DB	DAT1h	0	0	0.000000	359
$DC	DAT1l	0	0	0.000000	360
$DD	maxDAT	0	0	0.000000	362
$DE	DATh	0	0	0.000000	363
$DF	DATl	0	0	0.000000	364
$E1	LafterBT	0	0	0.000000	371
$E2	RafterBT	0	0	0.000000	372
$E3	afterSclL	0	0	0.000000	373
$E4	afterSclR	0	0	0.000000	374
$E5	maxLR	0	0	0.000000	375
$E6	DYLvi	0	0	0.000000	376
$E7	DYLvu	0	0	0.000000	377
$E8	left1	0	0	0.000000	381
$E9	MTL	0	0	0.000000	382
$EA	KTL	0	0	0.000000	383
$EB	Lb4VOL	0	0	0.000000	384
$EC	right1	0	0	0.000000	386
$ED	MTR	0	0	0.000000	387
$EE	KTR	0	0	0.000000	388
$EF	Rb4VOL	0	0	0.000000	389
$F6	btYL1l	0	0	0.000000	393
$F7	S0QPD1	0	0	0.000000	394
$FE	btYR1l	0	0	0.000000	398
$FF	S1QPD1	0	0	0.000000	399
$106	gpLdat	0	0	0.000000	555
$107	Lgp_pntr	391	187	0.002983	556
$10E	gpRdat	0	0	0.000000	560
$10F	Rgp_pntr	903	387	0.006889	561
$116	CENdat	0	0	0.000000	565
$117	XSW1pntr	1415	587	0.010796	566
$11B	SinusA	0	0	0.000000	609
$11F	SinusB	0	0	0.000000	613
$120	stepSize	1	1	0.000008	617
$121	counterX	0	0	0.000000	618
$122	plusmax	16320	3FC0	0.124512	619
$123	minmax	-16320	3C040	-0.124512	620
$124	dlyOffs	0	0	0.000000	621
$125	samOneh	0	0	0.000000	623
$126	samOnel	0	0	0.000000	624

*** X-MEMORY DECLARATION *** ALL (continued)

XMEM address	label	dec	hex	fract	line
$127	samTwoh	0	0	0.000000	625
$128	samTwol	0	0	0.000000	626
$129	pSam1	0	0	0.000000	628
$12A	pSam2	0	0	0.000000	629
$12B	pntrSINA	0	0	0.000000	630
$12C	pntrSINB	0	0	0.000000	631
$12D	reg_4	0	0	0.000000	632
$12E	reg_5	0	0	0.000000	633
$12F	gp_cofPntr	204	CC	0.001556	592
$130	addTfnFL	0	0	0.000000	596
$131	addTfnFR	0	0	0.000000	597
$132	addTfnRL	0	0	0.000000	598
$133	addTfnRR	0	0	0.000000	599

*** Y-MEMORY DECLARATION *** ALL / Audio / Tonegenerator

YMEM address	label	dec	hex	fract	line
$0	mod00	1	1	0.000488	224
$1	mod01	86	56	0.041992	225
$2	mod02	521	209	0.254395	226
$3	mod03	560	230	0.273438	227
$4	mod04	363	16B	0.177246	228
$5	mod05	97	61	0.047363	229
$6	mod06	108	6C	0.052734	230
$7	mod07	97	61	0.047363	231
$8	mod08	1962	7AA	0.958008	232
$9	mod09	1942	796	0.948242	233
$A	mod10	1946	79A	0.950195	234
$B	mod11	360	168	0.175781	235
$C	mod12	357	165	0.174316	236
$D	mod13	86	56	0.041992	237
$E	mod14	86	56	0.041992	238
$F	mod15	86	56	0.041992	239
$10	mod16	90	5A	0.043945	240
$11	mod17	86	56	0.041992	241
$12	mod18	86	56	0.041992	242
$13	mod19	86	56	0.041992	243
$14	mod20	97	61	0.047363	244
$15	mod21	310	136	0.151367	246
$16	mod22	1743	6CF	0.851074	247
$17	mod23	1796	704	0.876953	248
$18	mod24	1548	60C	0.755859	249
$19	mod25	1856	740	0.906250	250

*** Y-MEMORY DECLARATION *** ALL (continued)

YMEM address	label	dec	hex	fract	line
$1A	mi_one12	-2048	800	-1.000000	721
$1B	pl_one12	2047	7FF	0.999512	722
$1C	half12	1024	400	0.500000	723
$1D	p1	873	369	0.426270	841
$1E	q1	-413	E63	-0.201660	842
$1F	c21	1997	7CD	0.975098	844
$20	c20	102	66	0.049805	846
$21	c1	-974	C32	-0.475586	848
$22	c11	-2048	800	-1.000000	851
$23	c2	-524	DF4	-0.255859	852
$24	c3	476	1DC	0.232422	853
$25	c41	2030	7EE	0.991211	854
$26	c4	1573	625	0.768066	855
$27	tr11	10	A	0.004883	856
$28	tr12	264	108	0.128906	857
$29	ta011	528	210	0.257813	858
$2A	c_dc1	2046	7FE	0.999023	875
$2B	scratY	0	0	0.000000	726
$AC	KML1h	20	14	0.009766	405
$AD	KML1l	1998	7CE	0.975586	406
$AE	KPL1h	-2038	80A	-0.995117	407
$AF	KPL1l	1959	7A7	0.956543	408
$B0	Ctl0	115	73	0.056152	412
$B1	Cth0	2008	7D8	0.980469	413
$B2	Btl0	876	36C	0.427734	414
$B3	Bth0	-985	C27	-0.480957	415
$B4	At00	0	0	0.000000	416
$B5	At10	0	0	0.000000	417
$B6	At20	0	0	0.000000	418
$B7	KTrt0	684	2AC	0.333984	419
$B8	KTft0	1366	556	0.666992	420
$B9	KTmid0	2047	7FF	0.999512	421
$BA	KTbas0	0	0	0.000000	422
$BB	KTtre0	0	0	0.000000	423
$BC	BALL0	256	100	0.125000	424
$BD	BALR0	256	100	0.125000	425
$BE	Ctl1	115	73	0.056152	429
$BF	Cth1	2008	7D8	0.980469	430
$C0	Btl1	876	36C	0.427734	431
$C1	Bth1	-985	C27	-0.480957	432
$C2	At01	0	0	0.000000	433
$C3	At11	0	0	0.000000	434
$C4	At21	0	0	0.000000	435
$C5	KTrt1	684	2AC	0.333984	436
$C6	KTft1	1366	556	0.666992	437
$C7	KTmid1	2047	7FF	0.999512	438
$C8	KTbas1	0	0	0.000000	439
$C9	KTtre1	0	0	0.000000	440

*** Y-MEMORY DECLARATION *** ALL (continued)

YMEM address	label	dec	hex	fract	line
$CA	BALL1	256	100	0.125000	441
$CB	BALR1	256	100	0.125000	442
$CC	KMLh	20	14	0.009766	446
$CD	KMLl	1998	7CE	0.975586	447
$CE	KPLh	-2038	80A	-0.995117	448
$CF	KPLl	1959	7A7	0.956543	449
$D0	ca11l	1722	6BA	0.840820	453
$D1	ca11h	2016	7E0	0.984375	454
$D2	ca12l	1806	70E	0.881836	455
$D3	ca12h	-994	C1E	-0.485352	456
$D4	cb10l	141	8D	0.068848	457
$D5	cb10h	0	0	0.000000	458
$D6	cb11l	283	11B	0.138184	459
$D7	cb11h	0	0	0.000000	460
$D8	cb12l	141	8D	0.068848	461
$D9	cb12h	0	0	0.000000	462
$DA	whichSAM	-1697	95F	-0.828613	464
$DB	volSubW	-128	F80	-0.062500	465
$DC	volCenter	0	0	0.000000	466
$DD	centerOnly	0	0	0.000000	468
$DE	audSs	-1710	952	-0.834961	469
$DF	IIS2outs	-1339	AC5	-0.653809	470
$E0	VGA	-128	F80	-0.062500	478
$E1	KLCl	1046	416	0.510742	479
$E2	KLCh	2037	7F5	0.994629	480
$E3	KLBl	431	1AF	0.210449	481
$E4	KLBh	-1014	C0A	-0.495117	482
$E5	KLA0l	215	D7	0.104980	483
$E6	KLA0h	5	5	0.002441	484
$E7	KLA2l	215	D7	0.104980	485
$E8	KLA2h	5	5	0.002441	486
$E9	KLtre	0	0	0.000000	487
$EA	KLbas	0	0	0.000000	488
$EB	kLmid	512	200	0.250000	489
$EC	VAT	0	0	0.000000	490
$ED	SAM	0	0	0.000000	492
$EE	OutSwi	-1418	A76	-0.692383	493
$EF	FLcof	-2048	800	-1.000000	494
$F0	FRcof	-2048	800	-1.000000	495
$F1	RLcof	-2048	800	-1.000000	496
$F2	RRcof	-2048	800	-1.000000	497
$F3	SrcScal	1024	400	0.500000	498
$F4	samCl	1716	6B4	0.837891	503
$F5	samCh	2044	7FC	0.998047	504
$F6	delta	81	51	0.039551	505
$F7	switch	0	0	0.000000	507
$F8	rounding	-1025	BFF	-0.500488	508

*** Y-MEMORY DECLARATION *** ALL (continued)

YMEM address	label	dec	hex	fract	line
$F9	louSwi	-1779	90D	-0.868652	512
$FA	statLou	2047	7FF	0.999512	513
$FB	OFFS	256	100	0.125000	514
$FC	KPDL	-2023	819	-0.987793	515
$FD	KMDL	35	23	0.017090	516
$FE	Cllev	1024	400	0.500000	517
$FF	Ctre	341	155	0.166504	518
$100	gainPT	0	0	0.000000	523
$101	gainST	-2048	800	-1.000000	524
$102	gp_a11l	117	75	0.057129	525
$103	gp_a11h	2024	7E8	0.988281	526
$104	gp_a12l	1364	554	0.666016	527
$105	gp_a12h	-1001	C17	-0.488770	528
$106	gp_b10l	200	C8	0.097656	529
$107	gp_b10h	1012	3F4	0.494141	530
$108	gp_b11l	1647	66F	0.804199	531
$109	gp_b11h	-2025	817	-0.988770	532
$10A	gp_b12l	200	C8	0.097656	533
$10B	gp_b12h	1012	3F4	0.494141	534
$10C	scalCenter	128	80	0.062500	535
$11B	polarO	0	0	0.000000	638
$11C	ssSinus	-1857	8BF	-0.906738	639
$11D	ClipAmax	0	0	0.000000	641
$11E	ClipAmin	0	0	0.000000	642
$11F	ClipA	0	0	0.000000	643
$120	coefAl	0	0	0.000000	644
$121	coefAh	0	0	0.000000	645
$122	ClipBmax	0	0	0.000000	647
$123	ClipBmin	0	0	0.000000	648
$124	ClipB	0	0	0.000000	649
$125	coefBL	0	0	0.000000	650
$126	coefBH	0	0	0.000000	651
$127	scalS1_	2047	7FF	0.999512	653
$128	scalS1	2047	7FF	0.999512	654
$129	scalS2	0	0	0.000000	655
$12A	cpyS1	-1797	8FB	-0.877441	657
$12B	cpyS1_	-1797	8FB	-0.877441	658
$12C	cpyS2	-1797	8FB	-0.877441	659
$12D	absNorm	-1931	875	-0.942871	661
$12E	c3sin	0	0	0.000000	662
$12F	c1sin	0	0	0.000000	663
$130	addMpy	-1926	87A	-0.940430	664
$131	c0sin	2047	7FF	0.999512	665
$132	c2sin	2047	7FF	0.999512	666
$133	VLsin	0	0	0.000000	667
$134	VRsin	0	0	0.000000	668

*** Y-MEMORY DECLARATION *** ALL (continued)

YMEM address	label	dec	hex	fract	line
$135	IClipAmax	128	80	0.062500	670
$136	IClipAmin	128	80	0.062500	671
$137	IcoefAl	138	8A	0.067383	672
$138	IcoefAh	2020	7E4	0.986328	673
$139	IClipBmax	128	80	0.062500	675
$13A	IClipBmin	128	80	0.062500	676
$13B	IcoefBL	138	8A	0.067383	677
$13C	IcoefBH	2020	7E4	0.986328	678
$13D	samDecl	895	37F	0.437012	680
$13E	samDech	2047	7FF	0.999512	681
$13F	deltaD	34	22	0.016602	682
$140	switchD	0	0	0.000000	683
$141	samAttl	1138	472	0.555664	685
$142	samAtth	2026	7EA	0.989258	686
$143	deltaA	210	D2	0.102539	687
$144	switchA	210	D2	0.102539	688
$145	scratYup	0	0	0.000000	690
$146	iSinusWant	-2006	82A	-0.979492	691
$147	sinusMode	-1894	89A	-0.924805	693
$148	tfnFL	0	0	0.000000	694
$149	tfnFR	0	0	0.000000	695
$14A	tfnRL	0	0	0.000000	696
$14B	tfnRR	0	0	0.000000	697
$14C		0	0	0.000000	538
$150	pa11l	1668	684	0.814453	541
$151	pa11h	2034	7F2	0.993164	542
$152	pa12l	1855	73F	0.905762	543
$153	pa12h	-1012	C0C	-0.494141	544
$154	pb10l	143	8F	0.069824	545
$155	pb10h	0	0	0.000000	546
$156	pb11l	286	11E	0.139648	547
$157	pb11h	0	0	0.000000	548
$158	pb12l	143	8F	0.069824	549
$159	pb12h	0	0	0.000000	550
$17F	VersionNr	2	2	0.000977	718

*** X-MEMORY DECLARATION *** FM part

XMEM address	label	dec	hex	fract	line
$E	pltd	0	0	0.000000	1437
$F	pltflt	0	0	0.000000	1441
$10	devbpf	0	0	0.000000	1442
$11	devc	0	0	0.000000	1443
$12	deeml1	0	0	0.000000	1447
$13	deeml2	0	0	0.000000	1448
$14	deemr1	0	0	0.000000	1449
$15	deemr2	0	0	0.000000	1450
$16	mltflimh	0	0	0.000000	1454
$17	mltcnt	0	0	0.000000	1455
$18	mltsmt	0	0	0.000000	1456
$19	leva_u	0	0	0.000000	1457
$1A	noisflt_u	0	0	0.000000	1458
$1B	mltflim_u	0	0	0.000000	1459
$1C	noisflt	0	0	0.000000	1461
$1D	noish	0	0	0.000000	1462
$1E	noiscnt	0	0	0.000000	1463
$1F	noissmt	0	0	0.000000	1464
$20	noisflt2	0	0	0.000000	1465
$21	levh	0	0	0.000000	1467
$22	smtlf	0	0	0.000000	1468
$23	levsmt	0	0	0.000000	1469
$24	levsmt2	0	0	0.000000	1470
$25	mlts	0	0	0.000000	1472
$26	mltp	0	0	0.000000	1473
$27	mltcnt2	0	0	0.000000	1474
$28	strnf	0	0	0.000000	1475
$29	strnf2	0	0	0.000000	1476
$2A	strlf	0	0	0.000000	1478
$2B	levstr	0	0	0.000000	1479
$2C	levstr2	0	0	0.000000	1480
$2D	devc_str	0	0	0.000000	1481
$2E	mltrsp	0	0	0.000000	1483
$2F	mltrsp2	0	0	0.000000	1484
$30	rsplf	0	0	0.000000	1485
$31	levrsp	0	0	0.000000	1486
$32	levrsp2	0	0	0.000000	1487
$33	PT1attack	0	0	0.000000	2750
$34	PT2Alattack	0	0	0.000000	2751
$35	PT2attack	0	0	0.000000	2752
$36	PMinLev	826	33A	0.006302	2754
$37	PCounter	90	5A	0.000687	2755
$38		1	1	0.000008	2756
$39	PCountMax	90	5A	0.000687	2757
$3A	PAttack	10	A	0.000076	2758
$3B	DEVBPFpntr	0	0	0.000000	1496
$3F	DEVBPFbuf	0	0	0.000000	1500

*** X-MEMORY DECLARATION *** FM (continued)

XMEM address	label	dec	hex	fract	line
$47		0	0	0.000000	1683
$48		0	0	0.000000	1685
$49		26756	6884	0.204132	1686
$4A		24580	6004	0.187531	1687
$4B		0	0	0.000000	1688
$4C		0	0	0.000000	1689
$4D		0	0	0.000000	1690
$4E		131071	1FFFF	0.999992	1693
$4F		0	0	0.000000	1414
$50		0	0	0.000000	1415
$51		0	0	0.000000	1416
$52		0	0	0.000000	1417
$53		0	0	0.000000	1418
$80		0	0	0.000000	1676
$A2		0	0	0.000000	1678

*** Y-MEMORY DECLARATION *** FM part

YMEM address	label	dec	hex	fract	line
$1F	c21	1997	7CD	0.975098	844
$20	c20	102	66	0.049805	846
$2C	subspntr	0	0	0.000000	1505
$2D		-277	EEB	-0.135254	1507
$2E		-468	E2C	-0.228516	1509
$2F		1412	584	0.689453	1510
$30	c5	256	100	0.125000	1512
$31	scor	1168	490	0.570313	1516
$32	strc	2047	7FF	0.999512	1518
$33	smtc	2047	7FF	0.999512	1519
$34	rspc2	1208	4B8	0.589844	1520
$35	rspc1	628	274	0.306641	1521
$36	rspc3	-1024	C00	-0.500000	1522
$37		0	0	0.000000	1526
$38		2047	7FF	0.999512	1527
$39		1449	5A9	0.707520	1532
$3A	tr21	-163	F5D	-0.079590	1533
$3B	tr22	20	14	0.009766	1534
$3C	ta2	8	8	0.003906	1535
$3D	tresh1	1843	733	0.899902	1536
$3E	c_nf1	450	1C2	0.219727	1539
$3F	c_nf2	1678	68E	0.819336	1540
$40	p7	-1290	AF6	-0.629883	1541
$41	q7	348	15C	0.169922	1542
$42	minsmtcn	676	2A4	0.330078	1543

*** Y-MEMORY DECLARATION *** FM (continued)

YMEM address	label	dec	hex	fract	line
$43	tr71	-163	F5D	-0.079590	1544
$44	tr72	20	14	0.009766	1545
$45	ta7	0	0	0.000000	1546
$46		676	2A4	0.330078	1548
$47	tr101	-29	FE3	-0.014160	1549
$48	tr102	20	14	0.009766	1550
$49	ta10	5	5	0.002441	1551
$4A	trshTSW	327	147	0.159668	1554
$4B	tr33	532	214	0.259766	1555
$4C	tr34	126	7E	0.061523	1556
$4D	p2	617	269	0.301270	1557
$4E	q2	4	4	0.001953	1558
$4F	minsmtc	163	A3	0.079590	1561
$50	tr32	532	214	0.259766	1562
$51	tr31	20	14	0.009766	1563
$52	ta3	-5	FFB	-0.002441	1564
$53	p4	-1088	BC0	-0.531250	1566
$54	q4	728	2D8	0.355469	1567
$55	tr61	29	1D	0.014160	1568
$56	tr62	20	14	0.009766	1569
$57	ta6	-5	FFB	-0.002441	1570
$58	tr111	-163	F5D	-0.079590	1571
$59	tr112	20	14	0.009766	1572
$5A	ta11	0	0	0.000000	1573
$5B		2047	7FF	0.999512	1578
$5C	p9	-1290	AF6	-0.629883	1579
$5D	q9	348	15C	0.169922	1580
$5E	tr91	29	1D	0.014160	1581
$5F	tr92	20	14	0.009766	1582
$60	ta9	-5	FFB	-0.002441	1583
$61	p3	840	348	0.410156	1586
$62	q3	-307	ECD	-0.149902	1587
$63	minstr	0	0	0.000000	1588
$64	tr42	20	14	0.009766	1592
$65	tr41	29	1D	0.014160	1593
$66	ta4	-16	FF0	-0.007813	1594
$67	E_strnf_str	0	0	0.000000	1595
$68	E_mltp_str	0	0	0.000000	1596
$69	stro	2047	7FF	0.999512	1597
$6A	tr121	29	1D	0.014160	1600
$6B	tr122	20	14	0.009766	1604
$6C	ta12	-86	FAA	-0.041992	1605
$6D	p5	929	3A1	0.453613	1609
$6E	q5	-160	F60	-0.078125	1610
$6F	tr52	29	1D	0.014160	1611
$70	tr51	20	14	0.009766	1612
$71	ta5	-5	FFB	-0.002441	1613
$72	E_strnf_rsp	0	0	0.000000	1614
$73	E_mltp_rsp	0	0	0.000000	1615

*** Y-MEMORY DECLARATION *** FM (continued)

YMEM address	label	dec	hex	fract	line
$74	sdr_d_c	0	0	0.000000	1616
$75	tresh_sdr	-1024	C00	-0.500000	1617
$76	p6	286	11E	0.139648	1619
$77	q6	552	228	0.269531	1620
$78	p61	1101	44D	0.537598	1621
$79	q61	434	1B2	0.211914	1622
$7A	c9	1536	600	0.750000	1623
$7B	c91	839	347	0.409668	1624
$7C	c6	-1024	C00	-0.500000	1625
$7D	c61	1208	4B8	0.589844	1626
$7E	lvtrsh	245	F5	0.119629	1629
$7F	c8	2043	7FB	0.997559	1631
$80	c7	5	5	0.002441	1632
$81	p10	1200	4B0	0.585938	1633
$82	q10	0	0	0.000000	1634
$83	tr82	-20	FEC	-0.009766	1635
$84	tr81	54	36	0.026367	1636
$85	ta8	72	48	0.035156	1637
$86		0	0	0.000000	1638
$87	E_MUTE	2047	7FF	0.999512	1642
$88		1841	731	0.898926	2764
$89		102	66	0.049805	2765
$8A		102	66	0.049805	2766
$8B		1841	731	0.898926	2767
$8C		0	0	0.000000	1698
$8D		0	0	0.000000	1699
$8E		0	0	0.000000	1700
$8F		0	0	0.000000	1701
$90		1055	41F	0.515137	1705
$91		1061	425	0.518066	1706
$92		1079	437	0.526855	1707
$93		1085	43D	0.529785	1708
$94		1102	44E	0.538086	1709
$95		1108	454	0.541016	1710
$96		1126	466	0.549805	1711
$97		34	22	0.016602	1713
$98		13	D	0.006348	1714
$99		34	22	0.016602	1715
$9A		-690	D4E	-0.336914	1716
$9B		1629	65D	0.795410	1717
$9C		337	151	0.164551	1718
$9D		-396	E74	-0.193359	1719
$9E		337	151	0.164551	1720
$9F		-861	CA3	-0.420410	1721
$A0		1591	637	0.776855	1722
$A1		731	2DB	0.356934	1723
$A2		-1029	BFB	-0.502441	1726
$A3		731	2DB	0.356934	1729
$A4		-983	C29	-0.479980	1730
$A5		1585	631	0.773926	1731

*** Y-MEMORY DECLARATION *** FM (continued)

YMEM address	label	dec	hex	fract	line
$A6		0	0	0.000000	1733
$A7		60	3C	0.029297	1734
$A8		2047	7FF	0.999512	1735
$A9		0	0	0.000000	1736
$AA		0	0	0.000000	1737
$AB		0	0	0.000000	1740
$10D	lock_thresh	1638	666	0.799805	1421
$10E	E_MuteF1	2047	7FF	0.999512	1422
$10F	Mte_F1Del	4	4	0.001953	1425
$110	Mte_cnt	-2048	800	-1.000000	1426
$111	Decr_cnt	1	1	0.000488	1427
$112	FM_b0	2047	7FF	0.999512	1428
$113	FM_b1	0	0	0.000000	1429
$114	FM_a0	0	0	0.000000	1430

*** X-MEMORY DECLARATION *** Other 1 (TAPE)

XMEM address	label	dec	hex	fract	line
$E	audio_L2	0	0	0.000000	1077
$F	audio_R2	0	0	0.000000	1078
$19					
$1A					
$1B					
$1C					
$1D					
$1E					
$1F					
$20					
$21	DOLBY_LEV_L	0	0	0.000000	1983
$22					
$23					
$24					
$25					
$26					
$27					
$28					
$29					
$2A	DOLBY_LEV_R	0	0	0.000000	1985
$4C	T1attack	0	0	0.000000	2101
$4D	T2Alattack	0	0	0.000000	2102
$4E	T2attack	0	0	0.000000	2103
$4F	MinLev	2330	91A	0.017776	2105
$50	Counter	2500	9C4	0.019073	2106
$51	MSSdecr	1	1	0.000008	2107
$52	CountMax	2500	9C4	0.019073	2108
$53	Attack	70	46	0.000534	2109

*** Y-MEMORY DECLARATION *** Other 1 (TAPE)

YMEM address	label	dec	hex	fract	line
$1F	c21	1997	7CD	0.975098	844
$20	c20	102	66	0.049805	846
$37	dlbyry0st_0	-640	D80	-0.312500	1990
$38	dlbyry0st_1	1152	480	0.562500	1991
$39	dlbyry0st_2	150	96	0.073242	1992
$3A	dlbyry0st_3	-1370	AA6	-0.668945	1993
$3B	dlbyry0st_4	32	20	0.015625	1995
$3C	dlbyry0st_5	1175	497	0.573730	1996
$3D	dlbyry0st_6	2047	7FF	0.999512	1997
$3E	K3val	2	2	0.000977	1999
$3F	K1val	2046	7FE	0.999023	2000
$40	dlbyry0st_9	1024	400	0.500000	2003
$41	cL0	380	17C	0.185547	2004
$42	dlbyry0st_11	-1515	A15	-0.739746	2005
$43	dlbyry0st_12	1659	67B	0.810059	2006
$44	dlbyry0st_13	-513	DFF	-0.250488	2007
$45	dlbyry0st_14	-2048	800	-1.000000	2008
$46	cL4	0	0	0.000000	2009
$47	dlbyry0st_16	1402	57A	0.684570	2010
$48	dlbyry0st_17	1904	770	0.929688	2011
$49	a0sL	1392	570	0.679688	2014
$4A	b1sL	1840	730	0.898438	2015
$4B	b1aL	2047	7FF	0.999512	2016
$4C	a0aL	1	1	0.000488	2017
$4D	logalabel1LL	187	BB	0.091309	2018
$4E	a0sR	1392	570	0.679688	2019
$4F	b1sR	1840	730	0.898438	2020
$50	b1aR	2047	7FF	0.999512	2021
$51	a0aR	1	1	0.000488	2022
$52	logalabel1RR	283	11B	0.138184	2023
$53	DLBY_L	1024	400	0.500000	1074
$54	DLBY_R	1024	400	0.500000	1075
$55	MSSy0	2036	7F4	0.994141	2115
$56	MSSy1	9	9	0.004395	2116
$57	MSSy2	9	9	0.004395	2117
$58	MSSy3	2036	7F4	0.994141	2118

*** X-MEMORY DECLARATION *** Other 2 (CD)

XMEM address	label	dec	hex	fract	line
$2D	xDMFl	0	0	0.000000	1853
$2E	yDMFl	0	0	0.000000	1854
$2F	xDMFr	0	0	0.000000	1855
$30	yDMFr	0	0	0.000000	1856
$31					
$32					
$33					
$34					
$35					
$36					
$37					
$38					
$39	COMPRX0ST_8	264	108	0.002014	2179
$3A	COMPRX0ST_9	4154	103A	0.031693	2180
$3B	COMPRX0ST_10	131071	1FFFF	0.999992	2181
$3C					
$3D					
$3E					
$80					
$81					
$82					
$83					
$84					
$85					
$86					
$87					
$88					
$89					
$8A					

*** Y-MEMORY DECLARATION *** Other 2 (CD)

YMEM address	label	dec	hex	fract	line
$1F	c21	1997	7CD	0.975098	844
$20	c20	102	66	0.049805	846
$36	dmfViaRAM	0	0	0.000000	1846
$37	dmfB0	942	3AE	0.459961	1847
$38	dmfB1	-435	E4D	-0.212402	1848
$39	dmfA1	1306	51A	0.637695	1849
$3A	COMPRY0ST_0	1024	400	0.500000	2188
$3B	COMPRY0ST_1	247	F7	0.120605	2189
$3C	COMPRY0ST_2	31	1F	0.015137	2190
$3D	COMPRY0ST_3	1801	709	0.879395	2191
$3E	COMPRY0ST_4	2047	7FF	0.999512	2192
$3F	COMPRY0ST_5	1998	7CE	0.975586	2195
$40	COMPRY0ST_6	1024	400	0.500000	2199
$41	COMPRY0ST_7	218	DA	0.106445	2200
$42	COMPRY0ST_8	-672	D60	-0.328125	2201
$43	COMPRY0ST_9	1049	419	0.512207	2202
$44	COMPRY0ST_10	-898	C7E	-0.438477	2203
$45	COMPRY0ST_11	303	12F	0.147949	2204
$46	COMPRY0ST_12	-2048	800	-1.000000	2205
$47	COMPRY0ST_13	-2048	800	-1.000000	2206
$48	COMPRY0ST_14	-2048	800	-1.000000	2207
$49	COMPRY0ST_15	-1024	C00	-0.500000	2208
$4A	COMPRY0ST_16	-921	C67	-0.449707	2209
$4B	COMPRY0ST_17	505	1F9	0.246582	2210
$4C	COMPRY0ST_18	1559	617	0.761230	2211
$4D	COMPRY0ST_19	1823	71F	0.890137	2212
$4E	COMPRY0ST_20	758	2F6	0.370117	2213
$4F	COMPRY0ST_21	31	1F	0.015137	2214
$50	COMPRY0ST_22	0	0	0.000000	2215
$51	COMPRY0ST_23	0	0	0.000000	2216
$52	COMPRY0ST_24	3	3	0.001465	2217
$53	COMPRY0ST_25	2042	7FA	0.997070	2218
$54	COMPRY0ST_26	0	0	0.000000	2219
$55	COMPRY0ST_27	1024	400	0.500000	2221
$56	COMPRY0ST_28	90	5A	0.043945	1808

*** X-MEMORY DECLARATION *** Other 4 (AM)

XMEM address	label	dec	hex	fract	line
$10					
$11					
$12					
$13					
$14					
$15	AMhpbuf	0	0	0.000000	1415
$18					
$19					
$1A					
$1B					
$1C					
$1D					
$1E					
$1F	AMdelbuf	0	0	0.000000	1420
$20					
$21					
$22					
$23	AMButbuf	0	0	0.000000	1425
$24	AMhpPntr	1350	546	0.010300	1428
$25	AMdelPntr	1992	7C8	0.015198	1429
$26	AMButPntr	2244	8C4	0.017120	1430
$27	HP41_out	0	0	0.000000	1431
$47	AMldf1buf	0	0	0.000000	1437
$48	AMsmtc	131071	1FFFF	0.999992	1440
$49	AMrspc	0	0	0.000000	1441
$4A	AMx1	0	0	0.000000	1442
$4B	AMy1	0	0	0.000000	1443
$4C	AMH1	0	0	0.000000	1445
$4D	AMH2	0	0	0.000000	1446
$4E	AML1	0	0	0.000000	1447
$4F	AML2	0	0	0.000000	1448
$50	Gatetime	0	0	0.000000	1449
$51	GateDuty	0	0	0.000000	1450
$52	Feedback	0	0	0.000000	1451
$53	AML3	0	0	0.000000	1452
$54	IAC_out	0	0	0.000000	1453
$55	LPdet	0	0	0.000000	1455
$56	AM_delay	0	0	0.000000	1456
$57	IAC_Butw	0	0	0.000000	1457

*** Y-MEMORY DECLARATION *** Other 4 (AM)

YMEM address	label	dec	hex	fract	line
$1F	c21	2037	7F5	0.994629	844
$20	c20	22	16	0.005371	846
$37	p12	0	0	0.000000	1461
$38	q12	2047	7FF	0.999512	1462
$39	AMminsmtc	287	11F	0.140137	1463
$3A	AMts	10	A	0.004883	1464
$3B	AMtr11	34	22	0.016602	1465
$3C	AMta11	347	15B	0.169434	1466
$3D	p13	0	0	0.000000	1467
$3E	q13	2047	7FF	0.999512	1468
$3F	AMtr12	7	7	0.003418	1469
$40	AMta12	69	45	0.033691	1470
$41	q14	292	124	0.142578	1471
$42	p14	603	25B	0.294434	1472
$43	AMb0	896	380	0.437500	1473
$44	AMa1	251	FB	0.122559	1474
$45	AMb02	81	51	0.039551	1477
$46	AMb01	47	2F	0.022949	1478
$47	AMb00	81	51	0.039551	1479
$48	AMa02	-435	E4D	-0.212402	1480
$49	AMa01	1249	4E1	0.609863	1481
$4A	AMb12	436	1B4	0.212891	1482
$4B	AMb11	-449	E3F	-0.219238	1483
$4C	AMb10	436	1B4	0.212891	1484
$4D	AMa12	-747	D15	-0.364746	1485
$4E	AMa11	1347	543	0.657715	1486
$4F	AMb22	775	307	0.378418	1487
$50	AMb21	-995	C1D	-0.485840	1488
$51	AMb20	775	307	0.378418	1489
$52	AMa22	-956	C44	-0.466797	1490
$53	AMa21	1426	592	0.696289	1491
$54		540	21C	0.263672	1493
$55		-1079	BC9	-0.526855	1494
$56		540	21C	0.263672	1495
$57		-227	F1D	-0.110840	1496
$58		907	38B	0.442871	1497
$59		699	2BB	0.341309	1498
$5A		-1397	A8B	-0.682129	1499
$5B		699	2BB	0.341309	1500
$5C		-597	DAB	-0.291504	1501
$5D		1174	496	0.573242	1502
$5E		1809	711	0.883301	1504
$5F		1570	622	0.766602	1505
$60		65	41	0.031738	1507
$61		1916	77C	0.935547	1508
$62	IACsens	128	80	0.062500	1510
$63		1	1	0.000488	1511
$64	countN	54	36	0.026367	1512

*** Y-MEMORY DECLARATION *** AM (continued)

YMEM address	label	dec	hex	fract	line
$65		170	AA	0.083008	1513
$66	Gfeedb	336	150	0.164063	1514
$67		16	10	0.007813	1515
$68		88	58	0.042969	1517
$69		1959	7A7	0.956543	1518
$6A	BWb2	75	4B	0.036621	1520
$6B	BWa2	-402	E6E	-0.196289	1521
$6C	BWb0	75	4B	0.036621	1522
$6D	BWb1	151	97	0.073730	1523
$6E	BWa1	1124	464	0.548828	1524
$6F	HPb2	-1809	8EF	-0.883301	1526

11.4 Audio path block diagram SAA7705H