Overview
The homework for September 24th 2013 is a 4-bit adder. This document describes my implementation for the homework.

Requirements
A 4-bit adder circuit capable of adding two 4-bit inputs and providing a 5-bit sum is required, using Logicly.
The adder needs to be tested with two banks of 4 input switches with an output display of the sums.
Each of the 4-bit inputs should be displayed on a single hexadecimal digit display.
The output should be displayed on both five lamps and a two-digit hexadecimal display.

Outline Design
My design for the 4-bit adder circuit is based first on a half adder circuit; this circuit adds two single bits together and produces a sum and a carry out. Two half adder circuits are combined to produce a full adder, which takes three single bit inputs and produces a two-bit result (viewed as sum and carry out).
Four full adders are chained to produce a 4-bit adder.

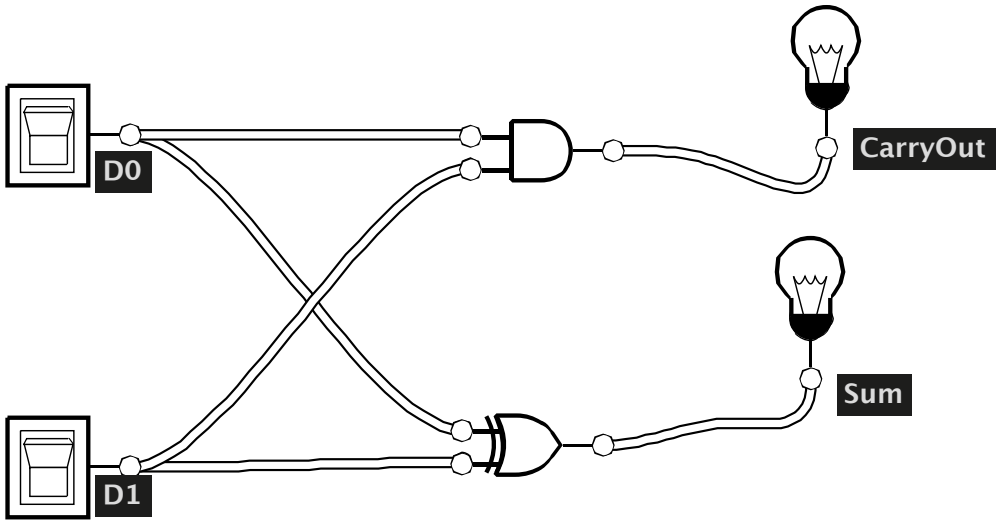
Detailed Design

Half adder

The half adder circuit takes two data bits in and produces a sum and carry out. The truth table is:

D0	D1	CarryOut	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

The logic for the CarryOut is clearly D0 & D1.
The logic for the Sum is D0 XOR D1.



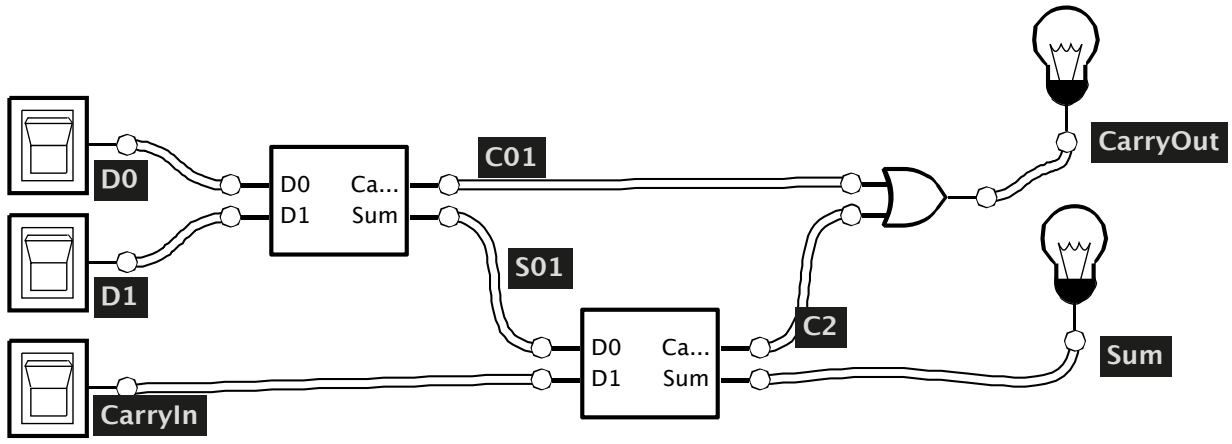
Full adder

A full adder takes two half adders two provide three data bits in (D0, D1 and CarryIn) and it provides a full two bit result in Sum and CarryOut.
The first half adder is used for D0 and D1, and produces C01 and S01 (for CarryOut and Sum). Note that S01 is effectively a ‘units’ value, and C01 is effectively a ‘twos’ value, in a binary representation of the answer.
The second half adder takes the CarryIn and S01, since these are both ‘unit’ values. It provides outputs of Sum and C2. Here, Sum is the output signal, and it is the ‘ones’ value of the adder. C2 is a ‘twos’ value. Here is a truth table for these signals.

D0	D1	CarryIn	C01	S01	C2	CarryOut	Sum
0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	1
0	1	0	0	1	0	0	1
0	1	1	0	1	1	1	0

D0	D1	CarryIn	C01	S01	C2	CarryOut	Sum
1	0	0	0	1	0	0	1
1	0	1	0	1	1	1	0
1	1	0	1	0	0	1	0
1	1	1	1	0	0	1	1

From inspection of the truth table, we can see that CarryOut is the OR of C01 and C2. So the equation for CarryOut is C01 | C2.



4-bit adder

For the 4-bit adder we need to chain four full adders. The inputs are A0-3 and B0-3. The output is R0-4

The first full adder needs to add A0 and B0, and it produces R0 and C0. R0 is effectively a ‘units’ value, and C0 is a ‘twos’ value.

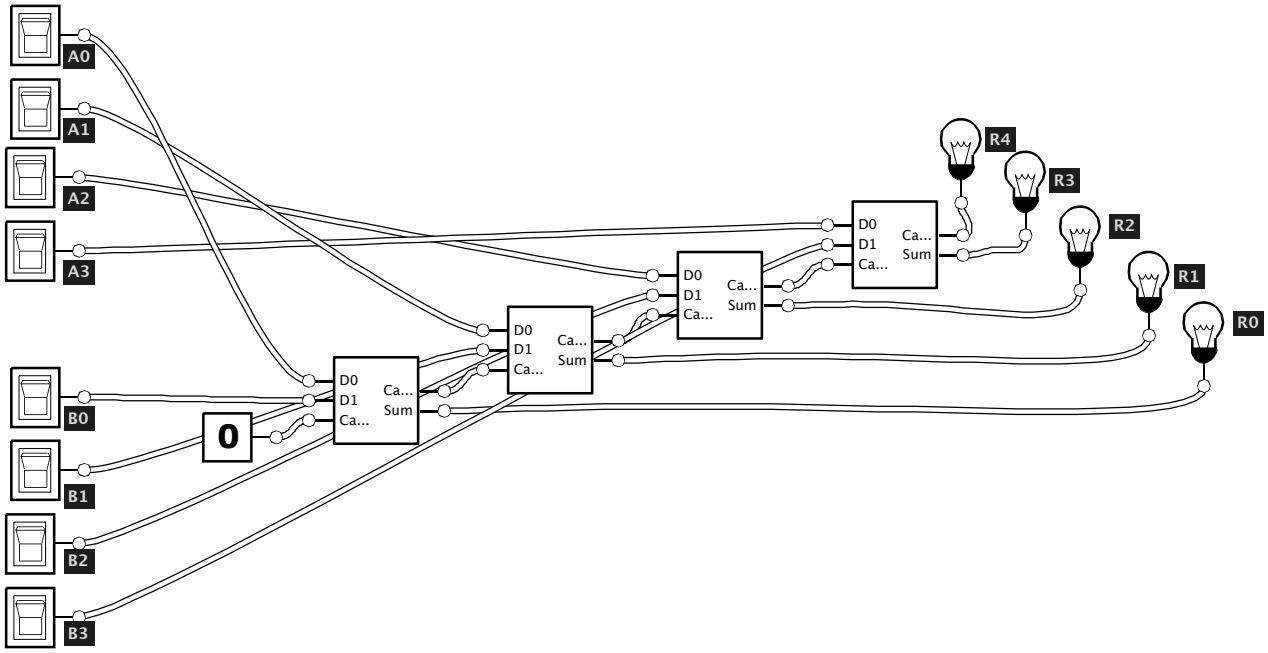
The second full adder needs to add A1, B1 and C0 - which are all of the ‘twos’ values to be added. The result of this is R1 (a ‘twos’ value) and C1 (a ‘fours’ value).

The third full adder needs to add A2, B2 and C1 - which are all of the ‘fours’ values to be added. The result of this is R2 (a ‘fours’ value) and C2 (an ‘eights’ value).

The fourth full adder needs to add A3, B3 and C2 - which are all of the ‘eights’ values to be added. The result of this is R3 (an ‘eights’ value) and C3 (a ‘sixteens’ value).

The final carry out, C3, is also the final output bit R4.

Note that the first adder requires three data inputs, and we only require two. There are two options here: we could use a half adder instead of a full adder, or we can supply the CarryIn input as a zero. We chose to do the latter, as this leads to symmetry in the design which makes it easier to see the circuit is correct.

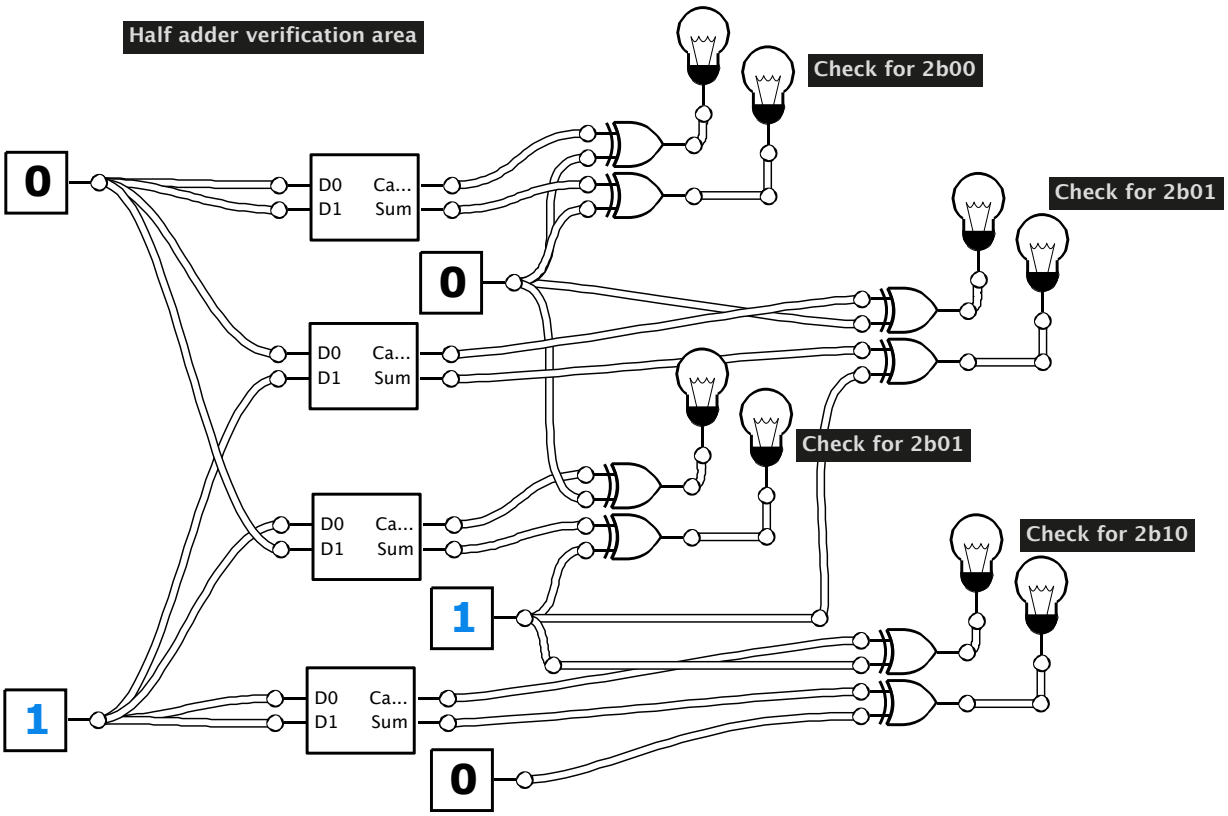

A0
A1
A2
A3
B0
B1
B2
B3
0
D0
D1
Ca...
Ca...
Sum
R4
R3
R2
R1
R0

Testing

Testing is performed at two levels currently.

Half adder

The half adder is placed in a circuit with four instances, with each instance having different inputs. The outputs are XORed with the expect values, and lamps light if there are any failures.



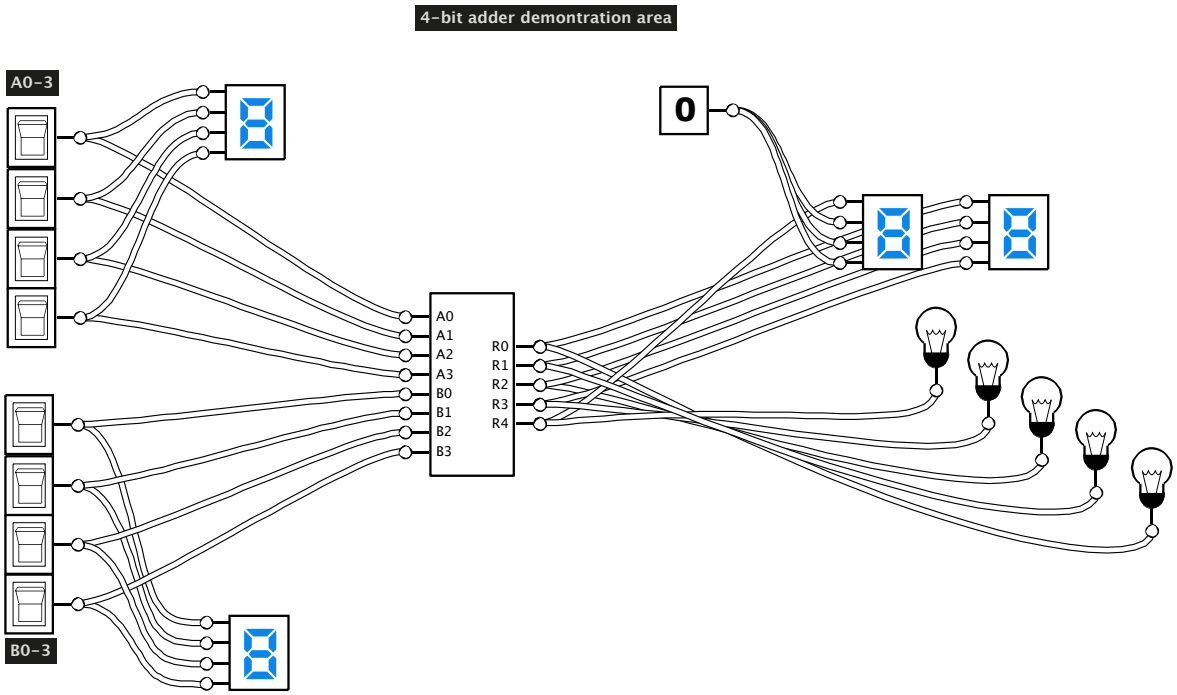
Full adder

Currently there is no specific test circuit for the full adder.

4-bit adder

The test circuit for the 4-bit adder has two banks of 4 input switches, one bank providing A0-3 and one bank providing B0-3. The output of the 4-bit adder is five bits, and this is displayed on five lamps.

Additionally, for easy of visual testing, the inputs are displayed on two single hexadecimal digit displays.



The actual testing is performed by hand. The testing includes the following tests:

A0-3	B0-3	R0-4
0	0	0
F	F	1E
1	0	1
2	0	2
4	0	4
8	0	8
0	1	1
0	2	2
0	4	4
0	8	8
5	A	F
A	5	F
1	1	2
2	2	4
4	4	8

A0-3	B0-3	R0-4
8	8	10