

EECS251B

Advanced Digital Circuits and Systems

Lecture 1 – Introduction

Vladimir Stojanović

Tuesdays and Thursdays 9:30-11am

Cory 521



Class Goals and Expected Outcomes

Practical Information

- **Instructor:**

- **Vladimir Stojanović**

Office hours: 513 Cory, Tuesdays 11am-noon

vlada@berkeley.edu

- **GSIs:**

- **Paul Kwon and Sunjin Choi**
 - **eecs251b_sp23@berkeley.edu**

Class Discussion

<https://edstem.org/us/courses/34616/discussion/>

Sign up for ED!

Class Web page

inst.eecs.berkeley.edu/~eecs251b

Class Topics

- This course aims to convey a knowledge of **advanced concepts of digital circuit and system design in state-of-the-art technologies.**
 - Emphasis is on the circuit and system design and optimization for both energy efficiency and high performance for use in a broad range of applications, from edge computing to datacenters. Special attention will be devoted to the most important challenges facing digital circuit designers in the coming decade. The course is accompanied with practical laboratory exercises that introduce students to modern tool flows.
 - We will use qualitative analysis when practical
 - Many case studies will be used to highlight the enabling design techniques

EECS251A vs. EE251B

- EECS 251A:
 - Emphasis on digital logic design
 - (Very) basic transistor and circuit models
 - Basic circuit design styles
 - First experiences with design – creating a solution given a set of specifications
 - A complete pass through the design process
- EECS 251B:
 - Understanding of technology possibilities and limitations
 - Transistor models of varying accuracy
 - Design under constraints: power-constrained, flexible, robust,...
 - Learning more advanced techniques
 - Study the challenges facing design in the coming years
 - Creating new solutions to challenging design problems, design exploration

Focus Areas

- SoC systems and components
- Current technology issues
- Process variations
- Robust design
- Memory
- Energy efficiency
- Power management

Class Topics

- Module 1: Fundamentals – SoC design template, languages (1.5 weeks)
- Module 2: System interconnects (1.5 weeks)
- Module 3: Models – From devices to gates, logic and systems (2 wks)
- Module 4: Design for performance (1.5 wks)
- Module 5: Memory, SRAM, variability, scaling options (2.5 wks)
- Module 6: Energy-efficient design (3 wks)
- Module 7: Clock and power distribution (1 week)
- Project presentations, final exam (1 week)

Class Organization

- 5 (+/-) assignments, with embedded labs (20%)
- 4 quizzes (10%)
- 1 term-long design project (40%)
 - Phase 1: Teams formed (Jan 31)
 - Phase 2: Study (report by March 17, before Spring break)
 - Phase 3: Design (report in RRR week)
 - Presentations, May 4, BWRC 9am-12:30pm
- Final exam (30%) (Thursday, April 27, in-class)

Class Material

- Recommended text: J. Rabaey, “Low Power Design Essentials,” Springer 2009.
 - Available at link.springer.com
- Other reference books:
 - “VLSI Design Methodology Development” by, T. Dillinger, Pearson 2019.
 - “Design of High-Performance Microprocessor Circuits,” edited by A. Chandrakasan, W. Bowhill, F. Fox (available on-line at Wiley-IEEE), Wiley 2001.
 - “CMOS VLSI Design,” 4th ed, by N.Weste, D. Harris
 - “Digital Integrated Circuits - A Design Perspective”, 2nd ed. by J. M. Rabaey, A. Chandrakasan, B. Nikolić, Prentice-Hall, 2003.

Class Material

- List of background material available on website
- Selected papers will be made available on website
 - Linked from IEEE Xplore and other resources
 - Need to be on campus to access, or use library proxy, library VPN
(check <http://library.berkeley.edu>)
- Class notes on website

Reading Assignments

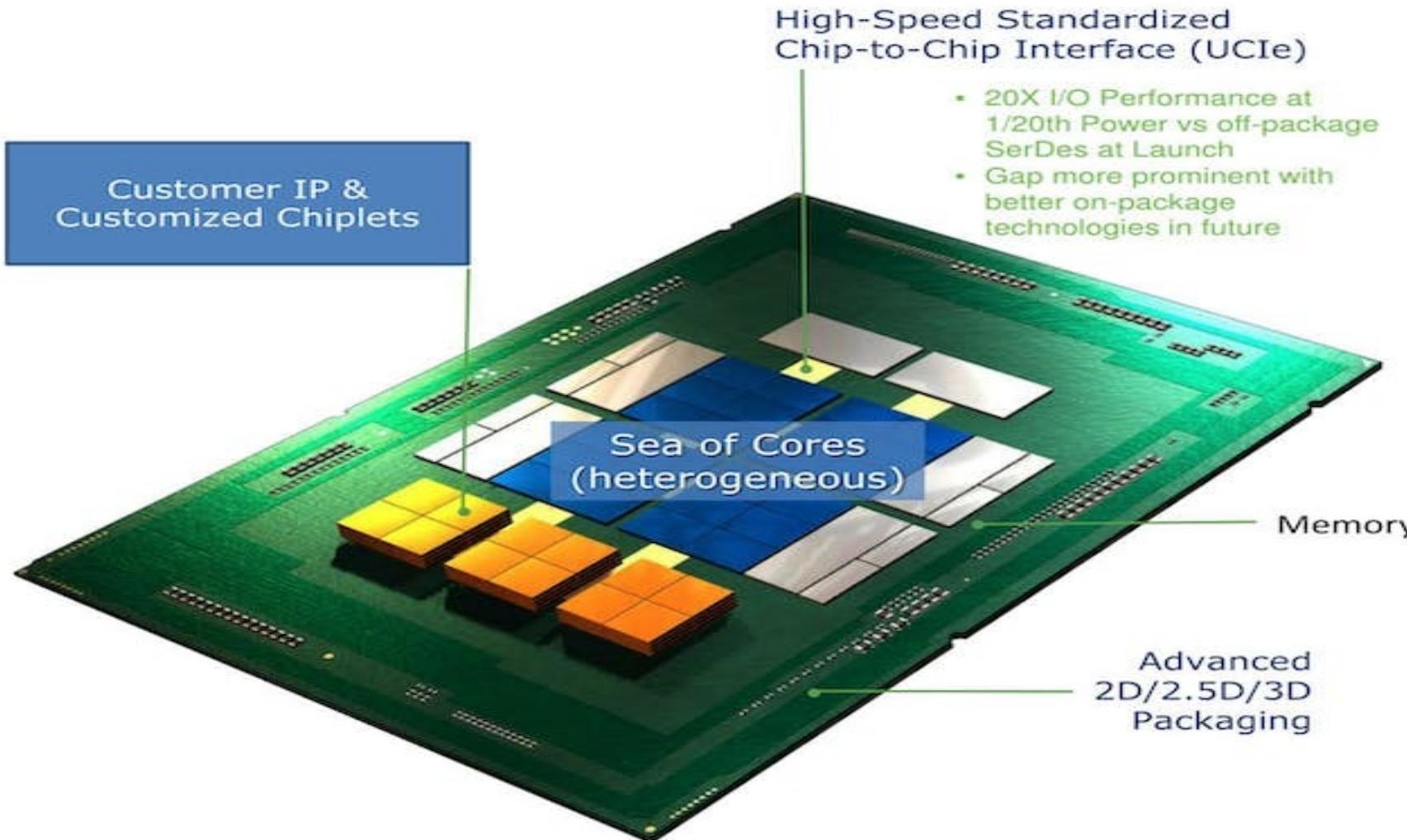
- Three types of readings:
 - **Assigned** reading, that should be read before the class
 - **Recommended** reading that covers the key points covered in lecture in greater detail
 - Occasionally, **background** material will be listed as well

Reading Sources

- IEEE Journal of Solid-State Circuits (JSSC)
- IEEE International Solid-State Circuits Conference (ISSCC)
- Symposium on VLSI Technology and Circuits (VLSI)
- Other conferences and journals

Project Topic: Universal Chiplet Interconnect Express (UCle) Interface

OPEN CHIPLET: PLATFORM ON A PACKAGE

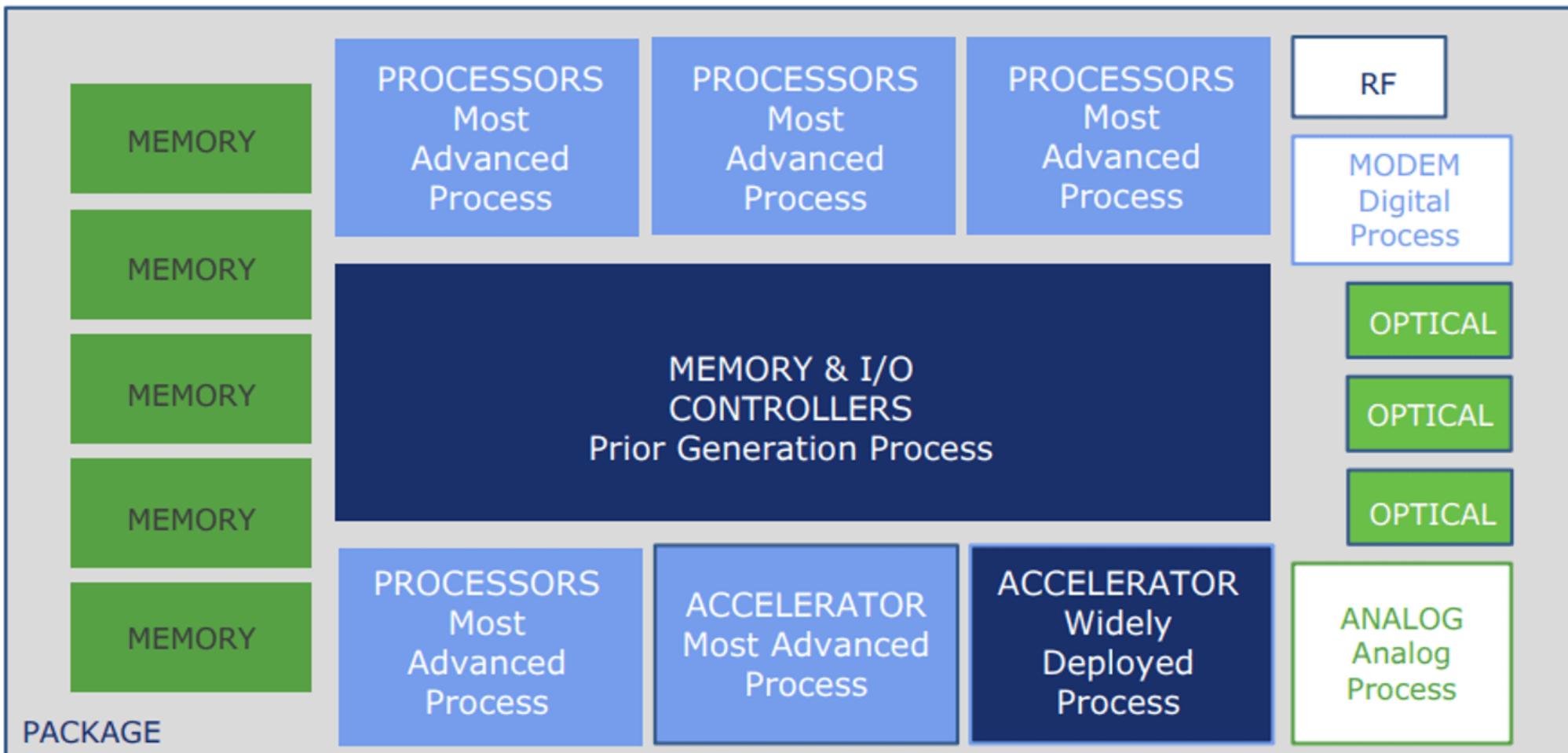


Heterogeneous Integration Fueled by an Open Chiplet Ecosystem
(Mix-and-match chiplets from different process nodes / fabs / companies / assembly)

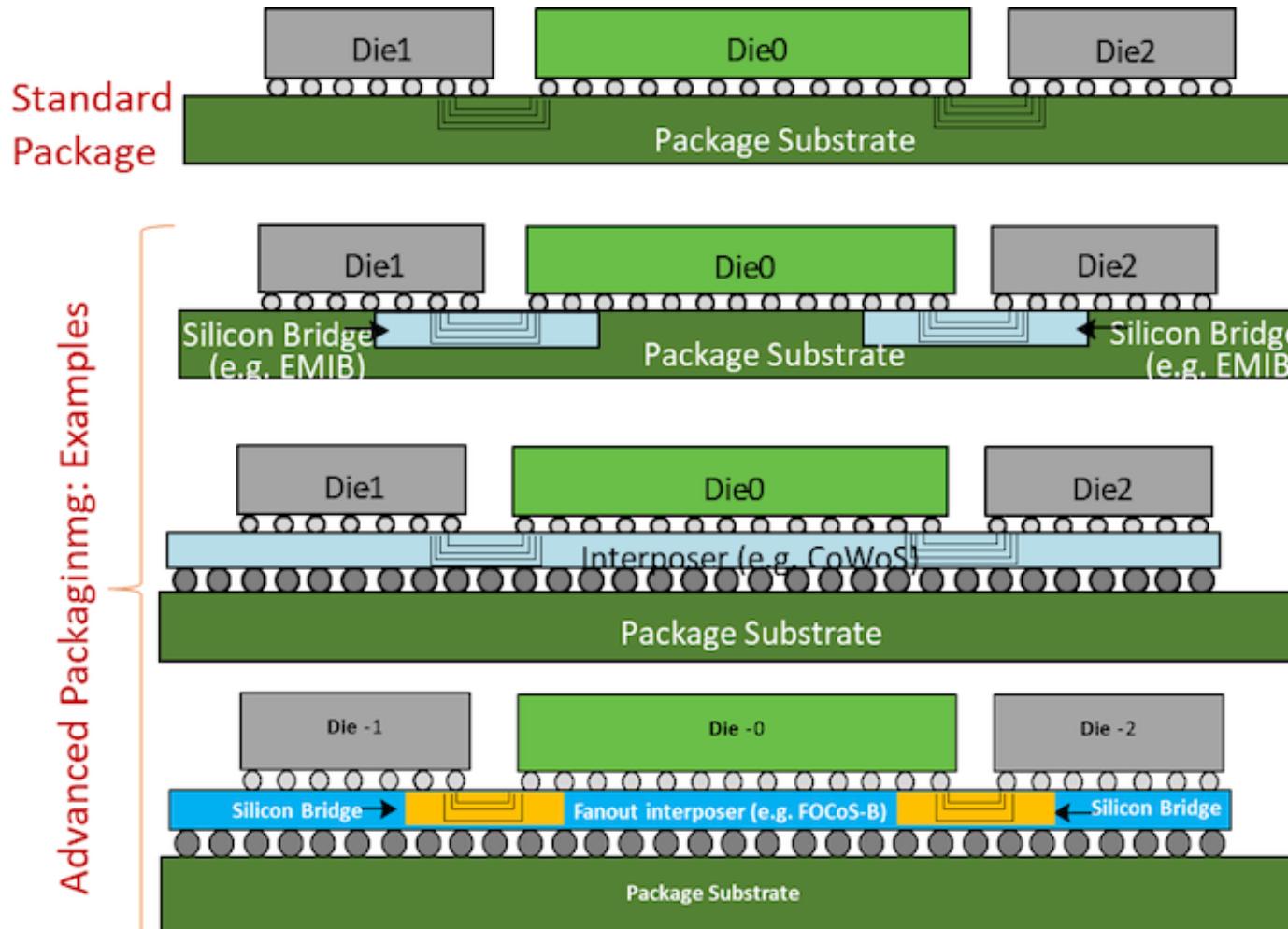
<https://www.uciexpress.org/>

 **UCle**
Universal **Chi**p**l**e
Interconnect Express

Project Topic: Universal Chiplet Interconnect Express (UCle) Interface

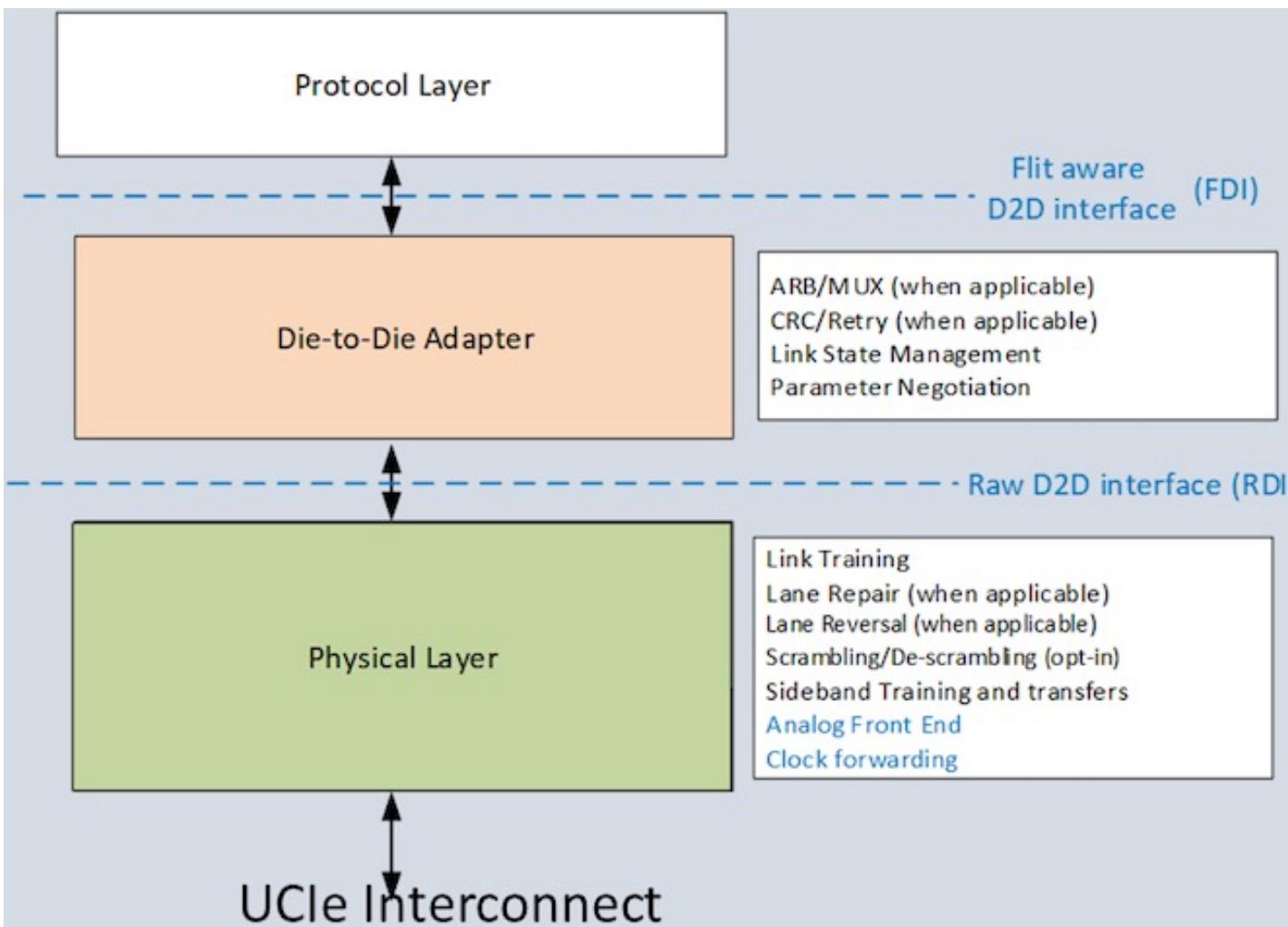


Project Topic: Universal Chiplet Interconnect Express (UCle) Interface



(b. Packaging Options: 2D and 2.5D)

Project Topic: Universal Chiplet Interconnect Express (UCle) Interface



(a. Layering with UCle)

Project Topic: Universal Chiplet Interconnect Express (UCle) Interface

- Variety of building blocks
 - Digital bus/protocol adapters
 - Custom digital – serializer/deserializer, advanced clocking
 - Mixed-signal – transmitter/receiver front-ends
- Project teams: 2+ members, proportional to the size of the project
 - Can also do a bigger project merging with 290C or 252 classes
- More details in Week 2

Tools

- 7nm predictive model (ASAP7), with (mostly) complete design kit
 - Or Intel 16 process if enrolled in 290C as well
- Cadence, Synopsys, available on instructional servers
- Berkeley's open-source flows and tools
 - Chipyard, Hammer
- Other open-source models

Zoom

- Will post recordings. But focus on interactive lectures
 - May pre-record some modules in advance
- Course notes available in advance
- Be engaged in the discussions. You are part of the learning process



Trends and Challenges in Digital Integrated Circuit Design

Reading (Lectures 1 & 2)

- **Assigned**

- Rabaey, LPDE, Ch 1 (Introduction)
- G.E. Moore, *No exponential is forever: but "Forever" can be delayed!* Proc. ISSCC'03, Feb 2003.
- T.-C. Chen, *Where CMOS is going: trendy hype vs. real technology.* Proc. ISSCC'06, Feb 2006.

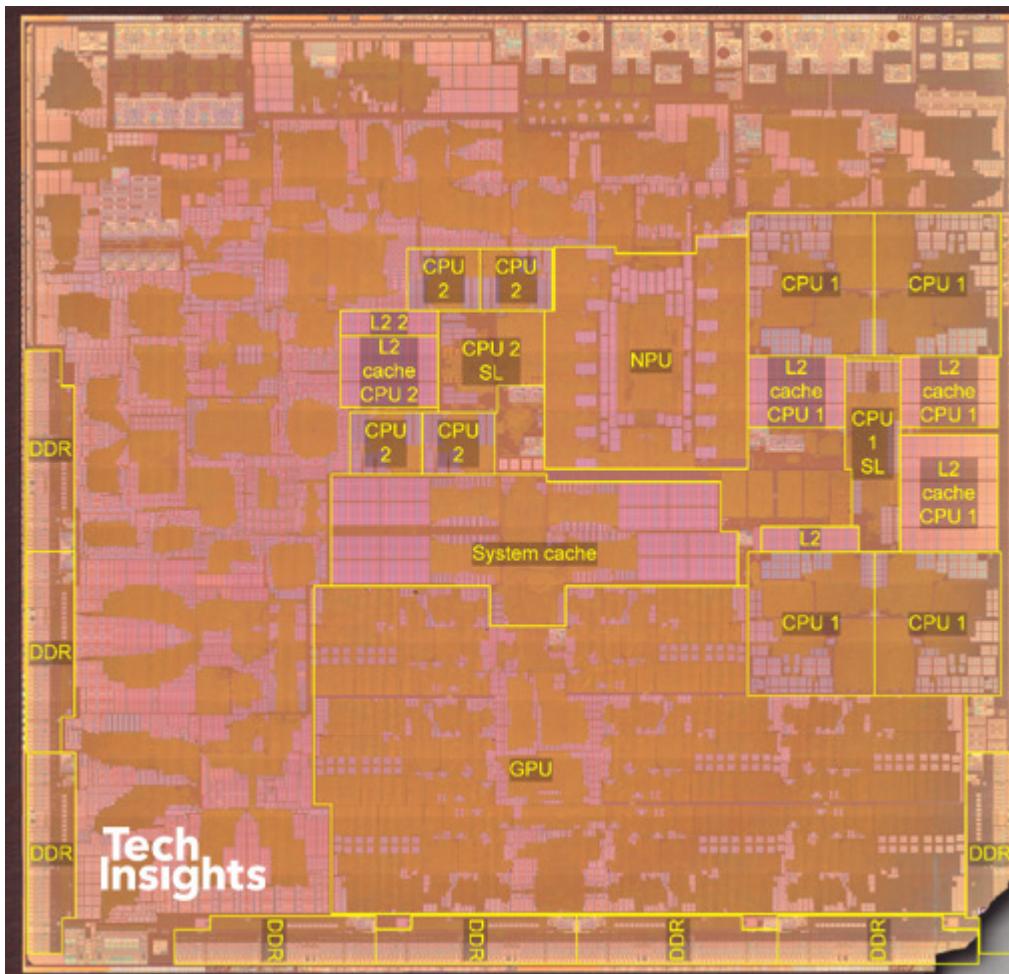
- **Recommended**

- Chandrakasan, Bowhill, Fox, Chapter 1 – Impact of physical technology on architecture (J.H. Edmondson),
- S. Borkar, “Design challenges of technology scaling,” IEEE Micro, vol.19, no.4, p.23-29, July-Aug. 1999.

- **Background:** Rabaey et al, DIC Chapter 3.

- The contributions to this lecture by a number of people (J. Rabaey, S. Borkar, etc) are greatly appreciated.

Class in a Nutshell

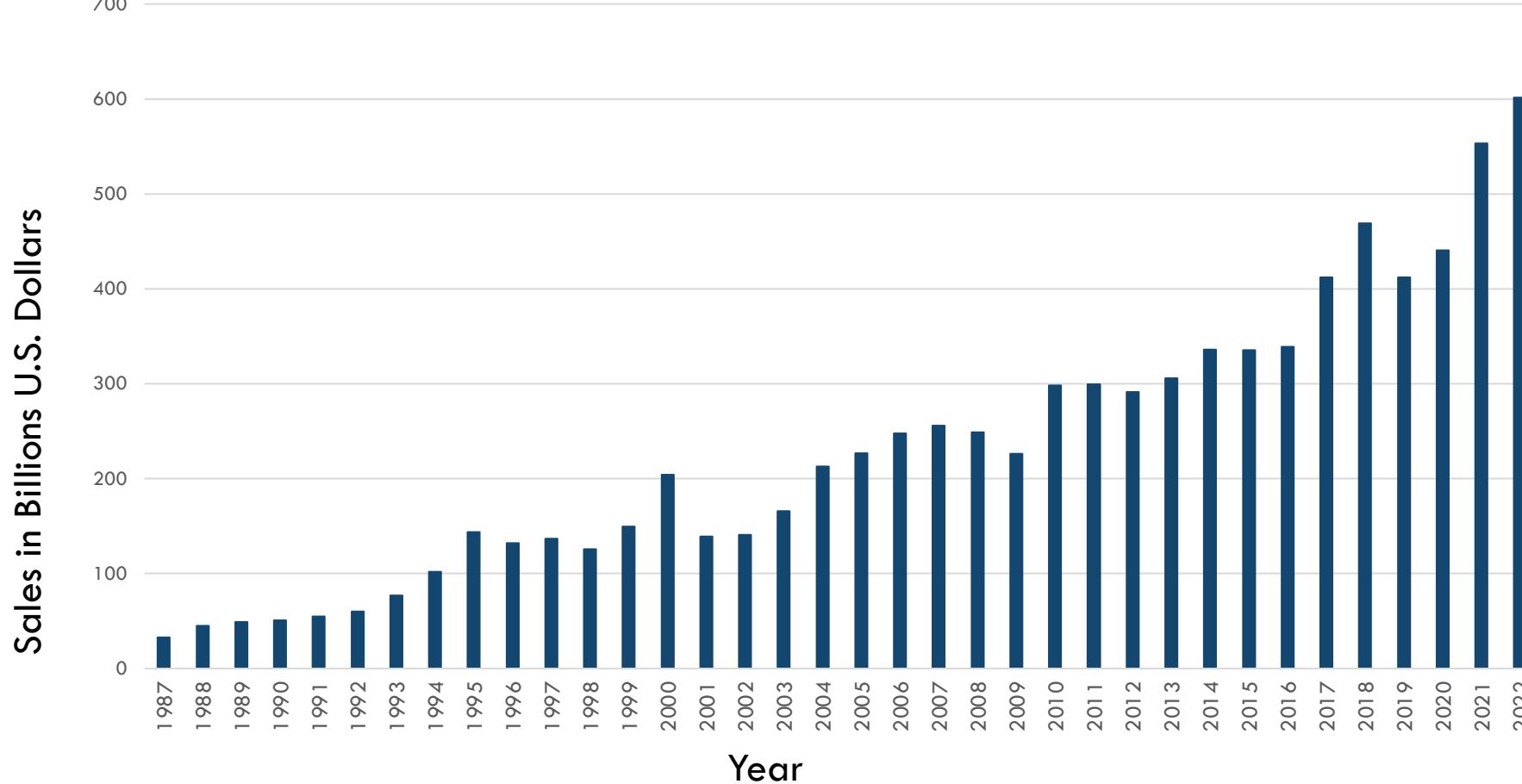


<https://www.techinsights.com/blog/two-new-apple-socs-two-market-events-apple-a14-and-m1>

- Design decisions needed to make a modern SoC
 - CPUs
 - SoC Components
 - Interconnect
 - Clocking
 - Memory
 - Power management

Current State of Semiconductor Industry

Worldwide semiconductor market size, 1987-2022

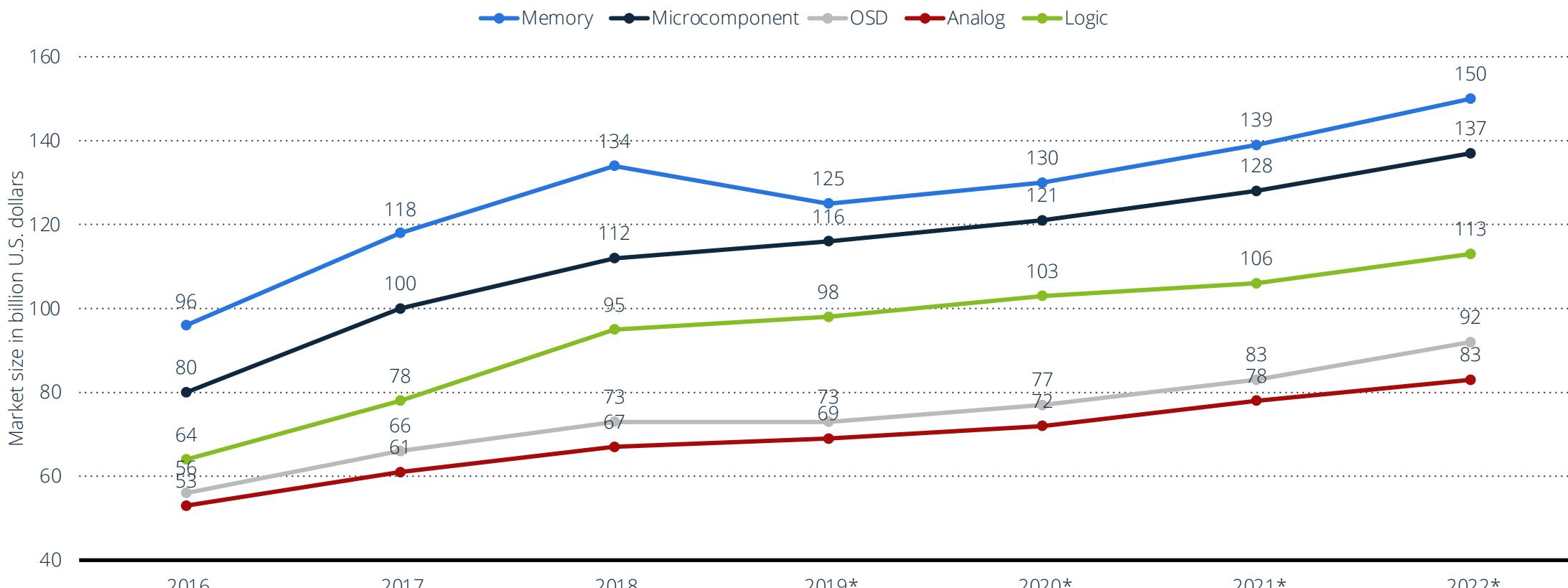


Source: Statista; <https://www.statista.com/statistics/266973/global-semiconductor-sales-since-1988/>

Current gross world product (GWP) ~ 88,000 billion (Wikipedia)

Semiconductor industry market size by component worldwide from 2016 to 2022

Global semiconductor market size by component 2016-2022



Note(s): Worldwide; 2016 to 2019

Further information regarding this statistic can be found on [page 8](#).

Source(s): PwC; [ID 512593](#)

Moore's Law



- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 12 months.
- He made a prediction that semiconductor technology will double its effectiveness every ~~12~~
~~18~~
24 months

"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term, this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000."

Gordon Moore, Cramming more Components onto Integrated Circuits, (1965).

Moore's Law - 1965

Transistors
Per Die

10^{10}
 10^9
 10^8
 10^7
 10^6
 10^5
 10^4
 10^3
 10^2
 10^1
 10^0

1960 1965 1970 1975 1980 1985 1990 1995 2000 2005 2010

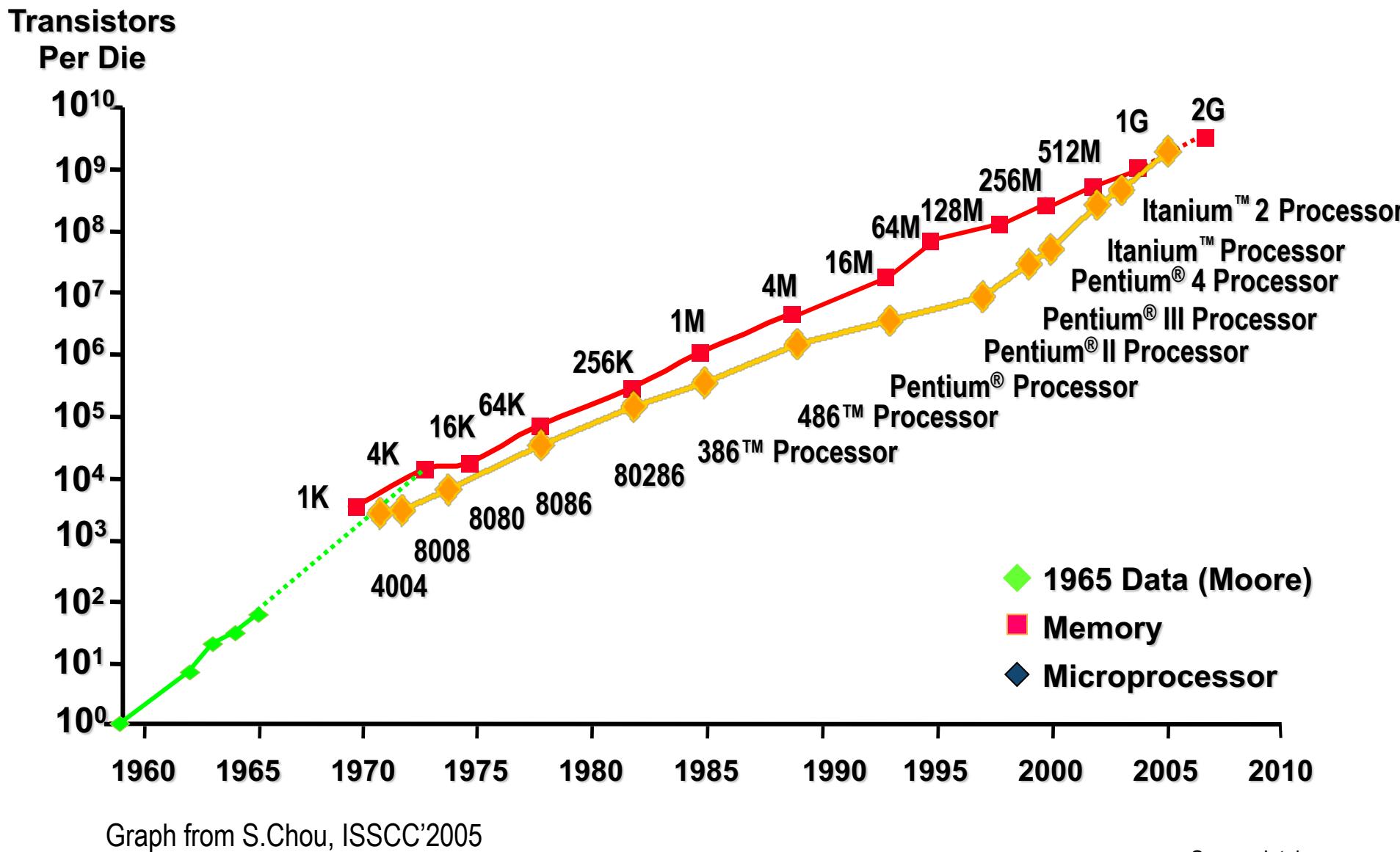
Graph from S.Chou, ISSCC'2005

"Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."
Electronics, Volume 38, Number 8, April 19, 1965

◆ 1965 Data (Moore)

Source: Intel

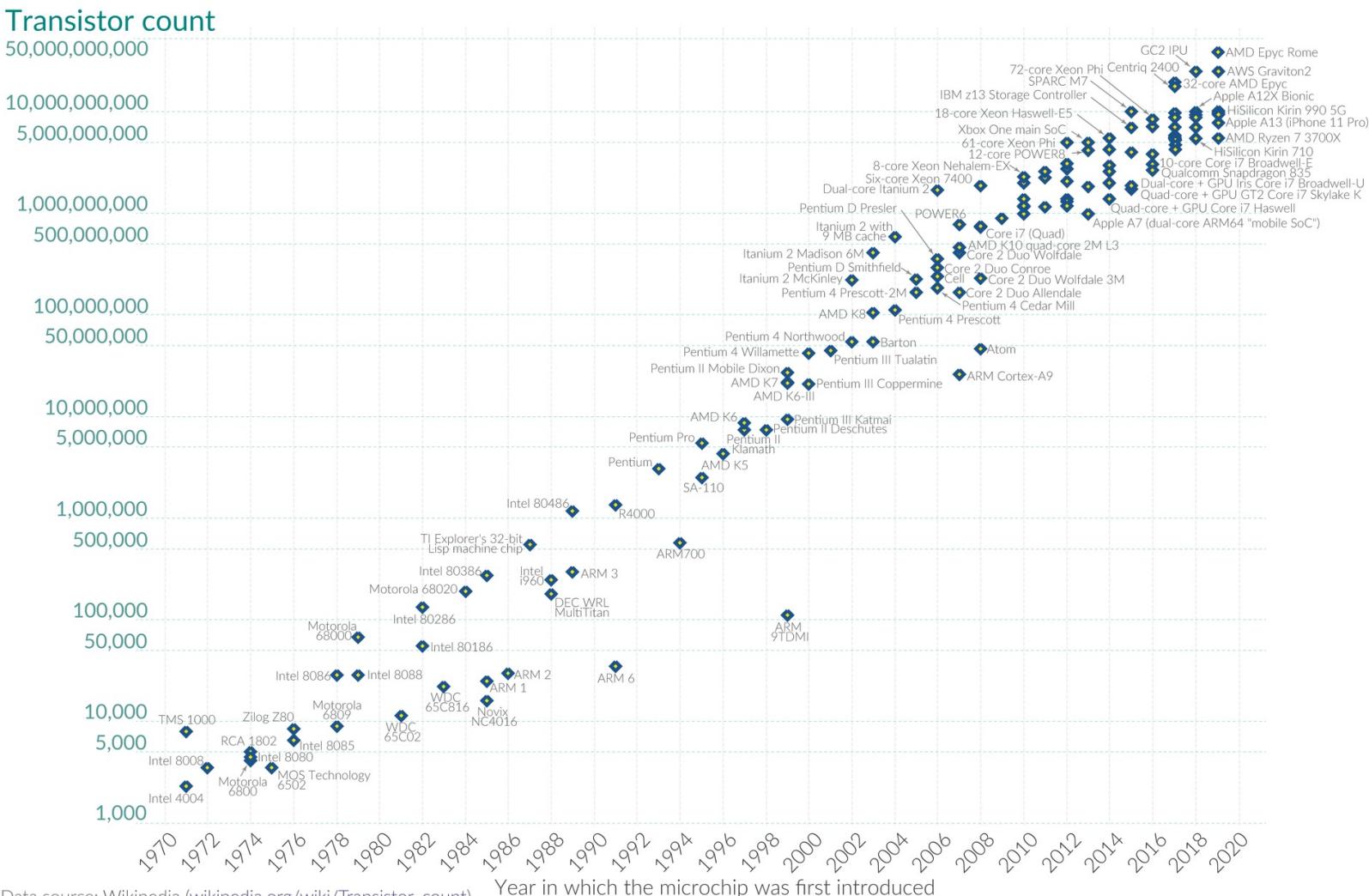
Moore's Law - 2005



Moore's Law - 2020

Moore's Law: The number of transistors on microchips doubles every two years

S Our World
in Data



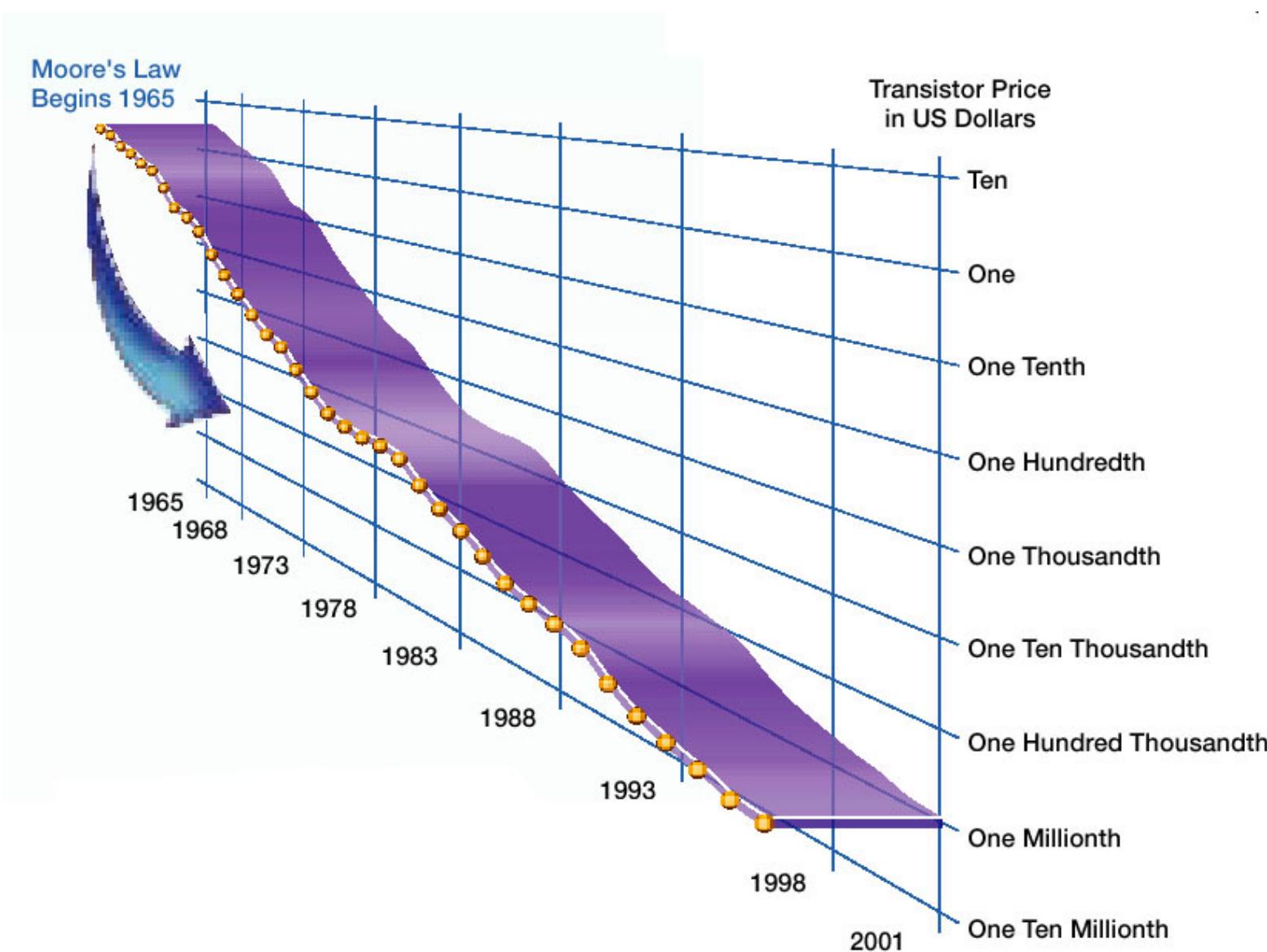
Data source: Wikipedia ([wikipedia.org/wiki/Transistor_count](https://en.wikipedia.org/w/index.php?title=Transistor_count&oldid=1000000000))

OurWorldInData.org – Research and data to make progress against the world's largest problems.

Licensed under CC-BY by the authors Hannah Ritchie and Max Roser.

- Slowdown is apparent, but scaling continues

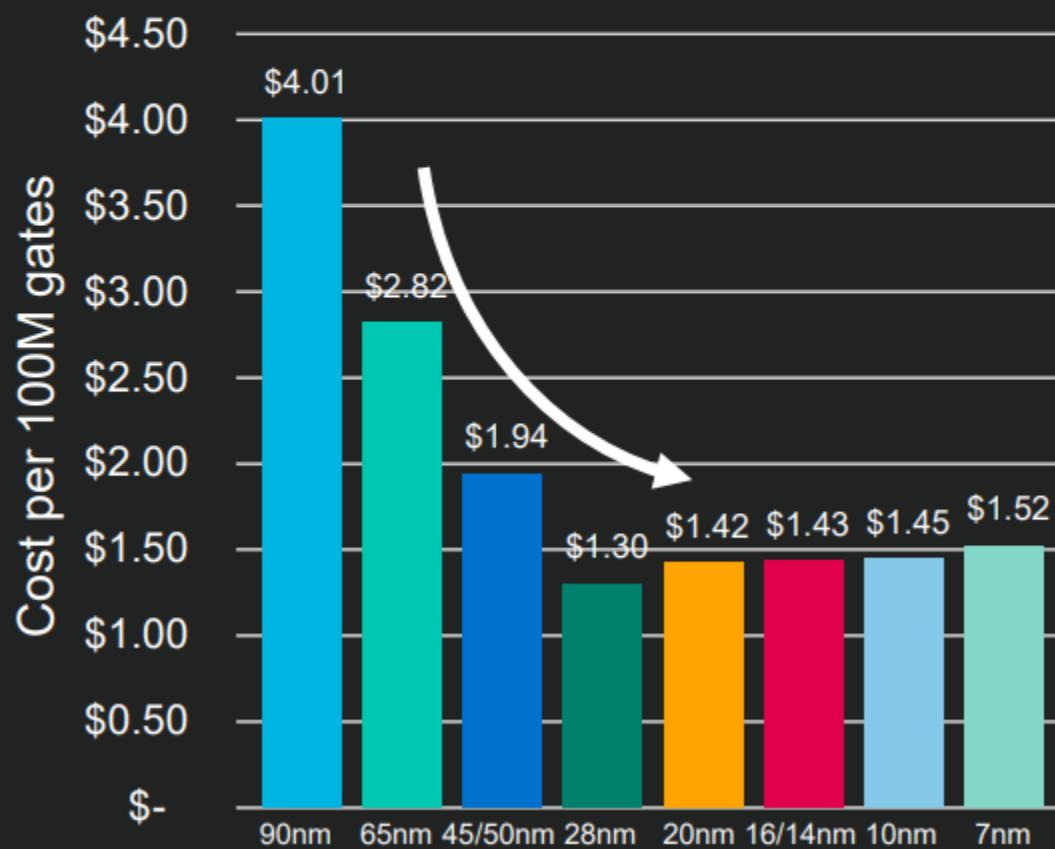
Moore's Law and Cost



Moore's Law and Cost

Moore's law slowing down...

Gate cost trend

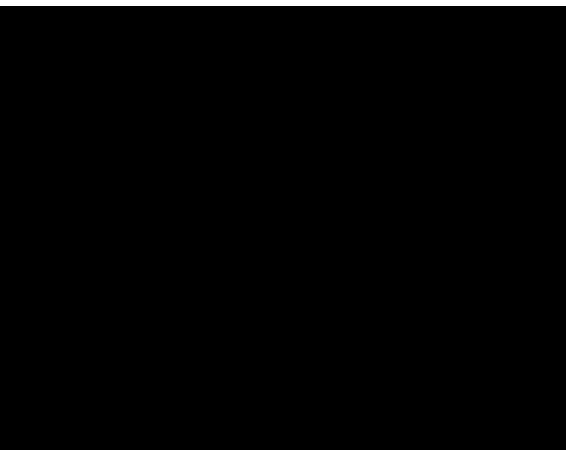


Moore's Law – addendum ...

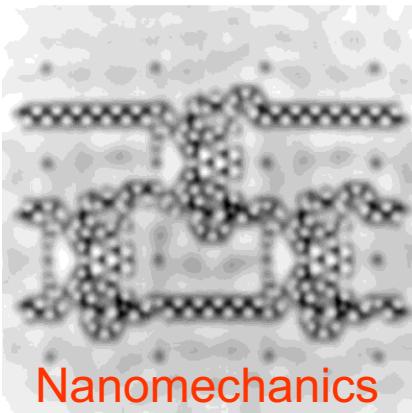


“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.”

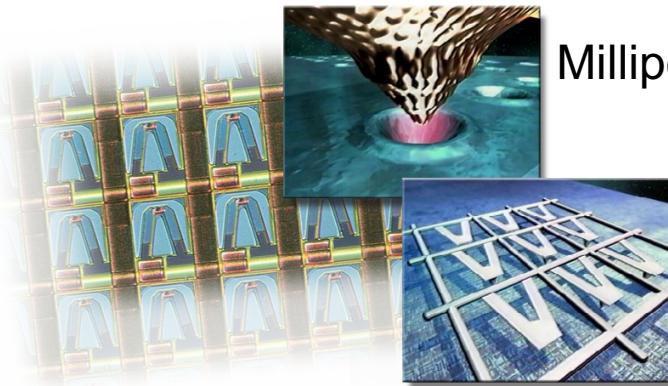
Progress in Nano-Technology



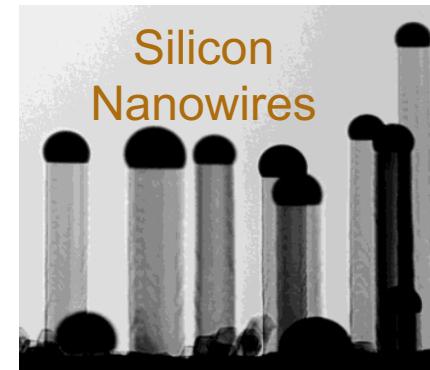
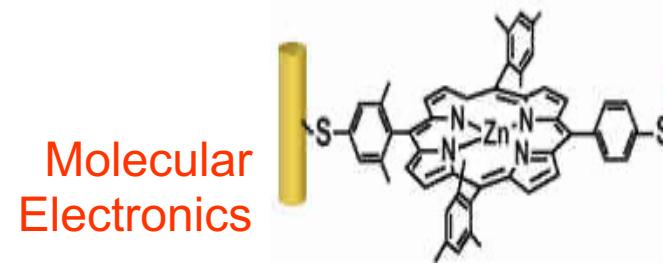
Spintronic Storage



Nanomechanics

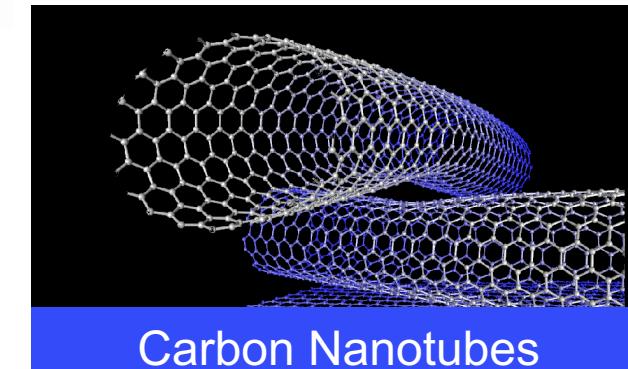
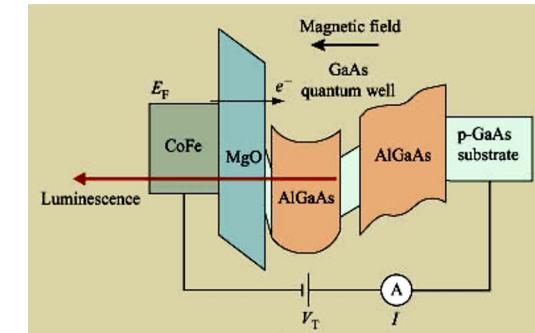


Millipede



Silicon
Nanowires

Spintronic device



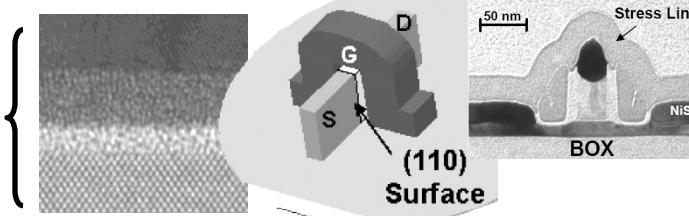
Carbon Nanotubes

Technology Strategy / Roadmap

2000 2005 2010 2015 2020 2025 2030

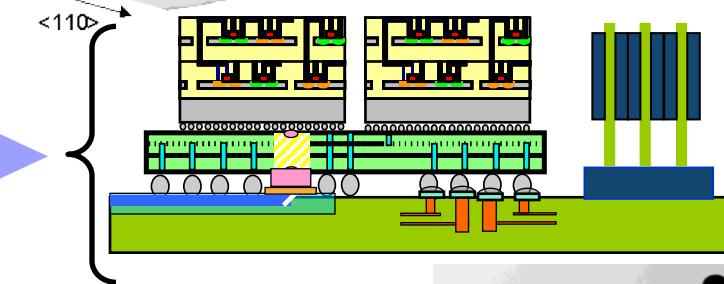
Plan A: Extending Si CMOS

R D



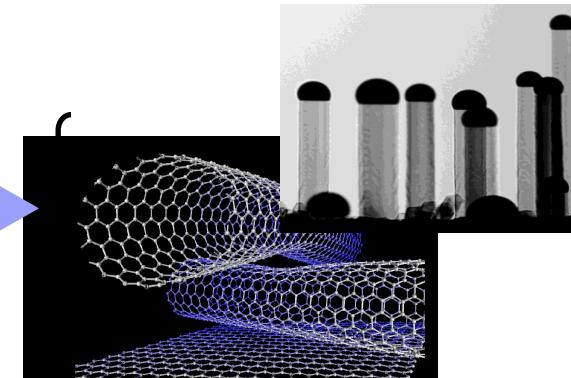
Plan B: Subsystem Integration

R D



Plan C: Post Si CMOS Options

R R&D

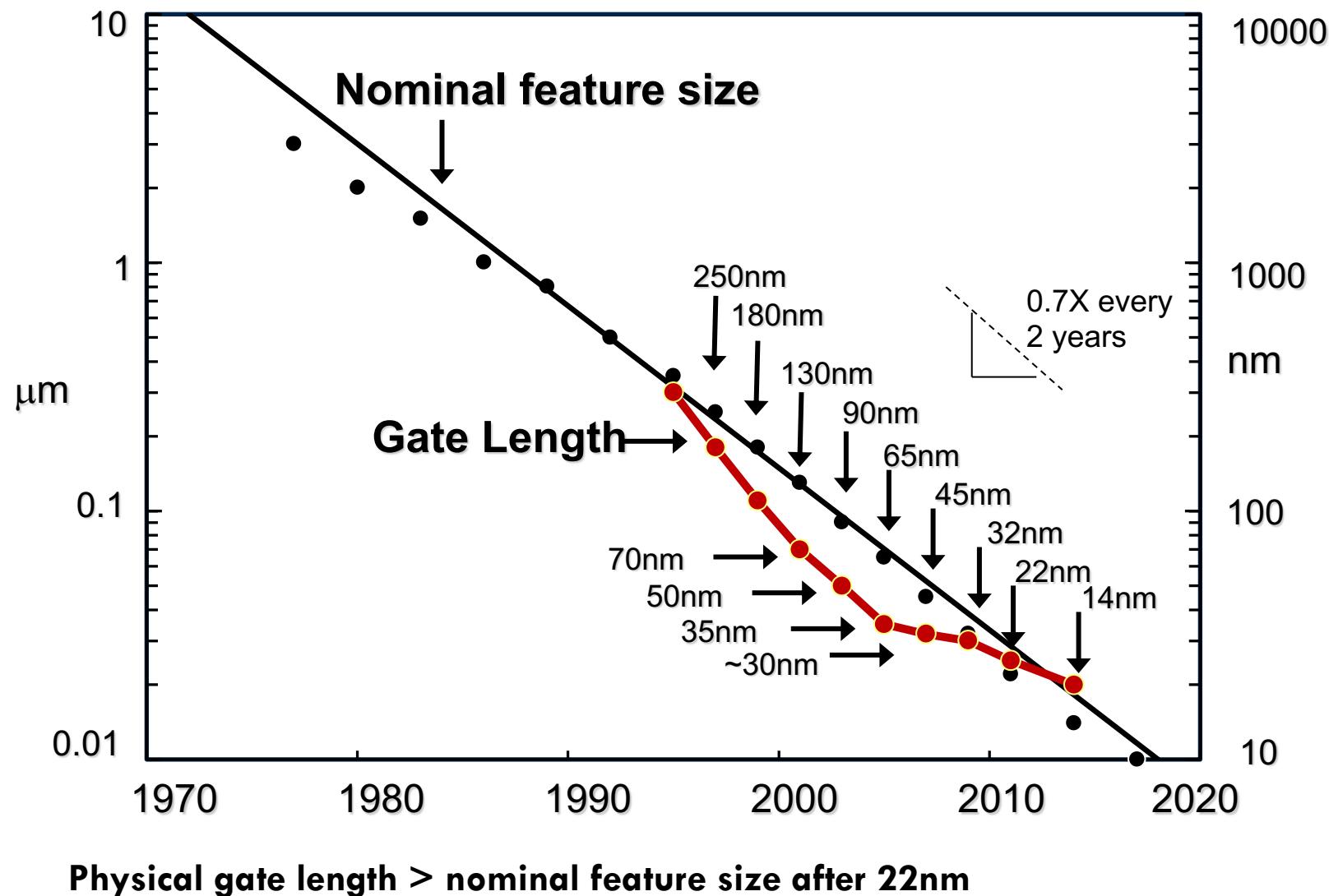


Plan Q: Quantum Computing

R

D

Printed vs. Physical Gate



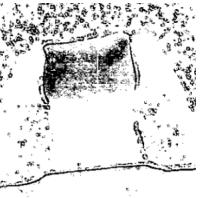
Source: Intel, IEDM presentations

Transistors are Changing

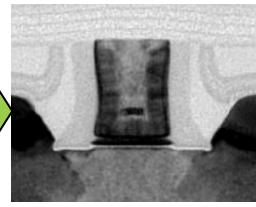
- From bulk to finFET and FDSOI

65/55 nm 45/40 nm 32/28nm 22/20nm 16/14nm 10nm 7nm 5nm

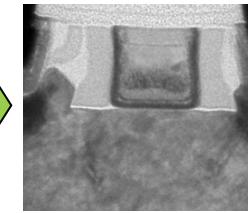
Bulk



SiO_2/SiN
Strain



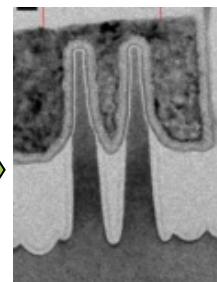
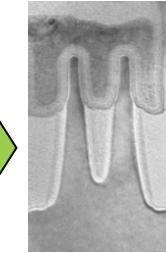
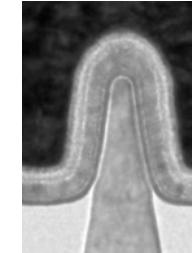
Intel,
IEDM'07
HK/MG
Strain



Intel,
IEDM'09



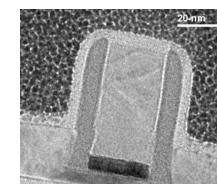
TSMC,
Samsung



Intel,
IEDM'17



TSMC 7nm
(hexus.net)



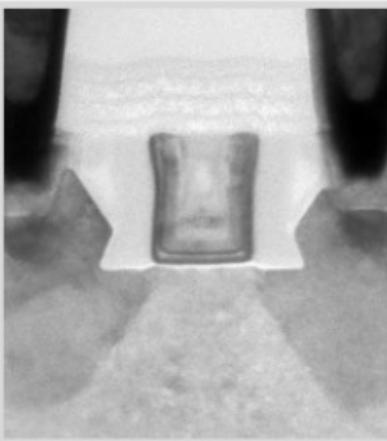
ST,
VLSI'12

Varying Flavors in Each Node

- 32nm (and 28nm): Various flavors - Intel

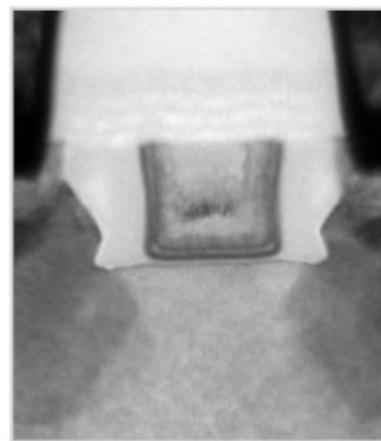
Logic
Transistor

(HP or SP)



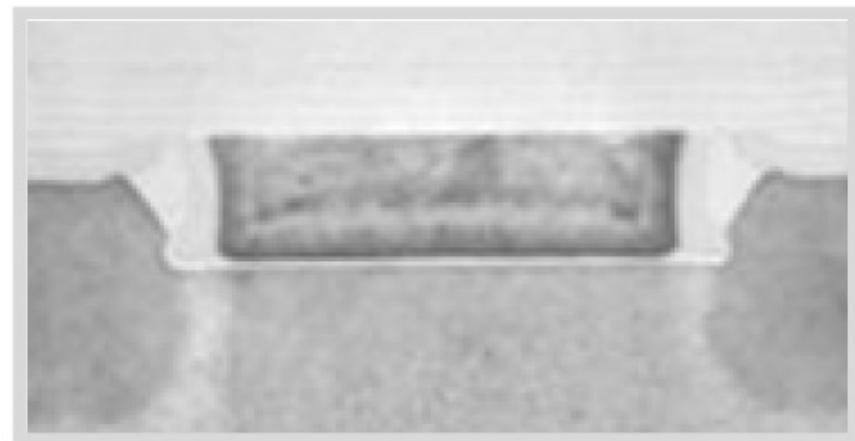
Low Power
Transistor

(LP)



HV I/O
Transistor

(1.8 V or 3.3 V)



$L_g = 30/34\text{nm}$

$L_g = 46\text{nm}$

$L_g > 140\text{nm}$

5nm Flavors

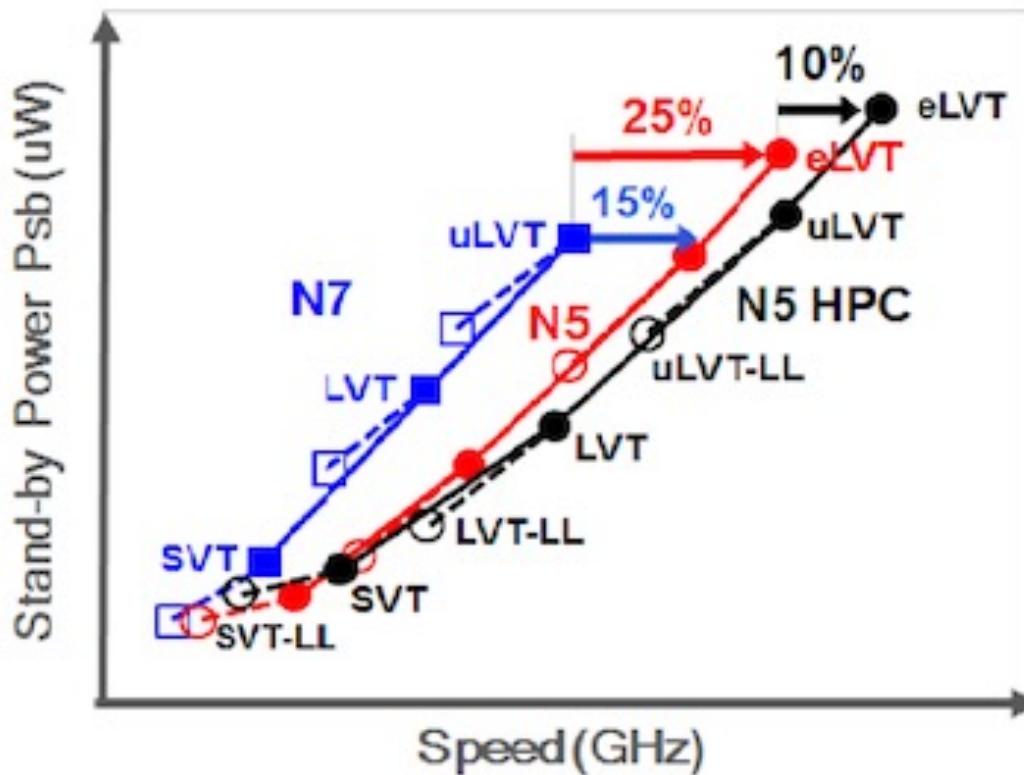
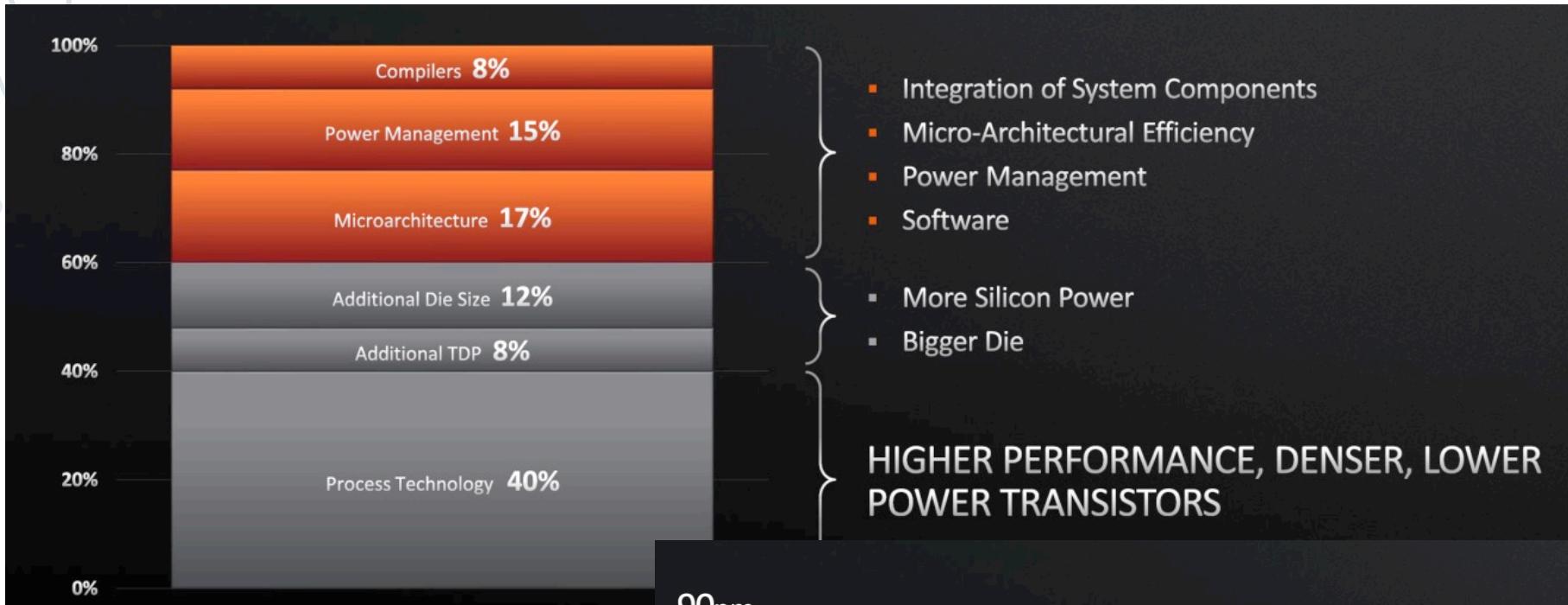


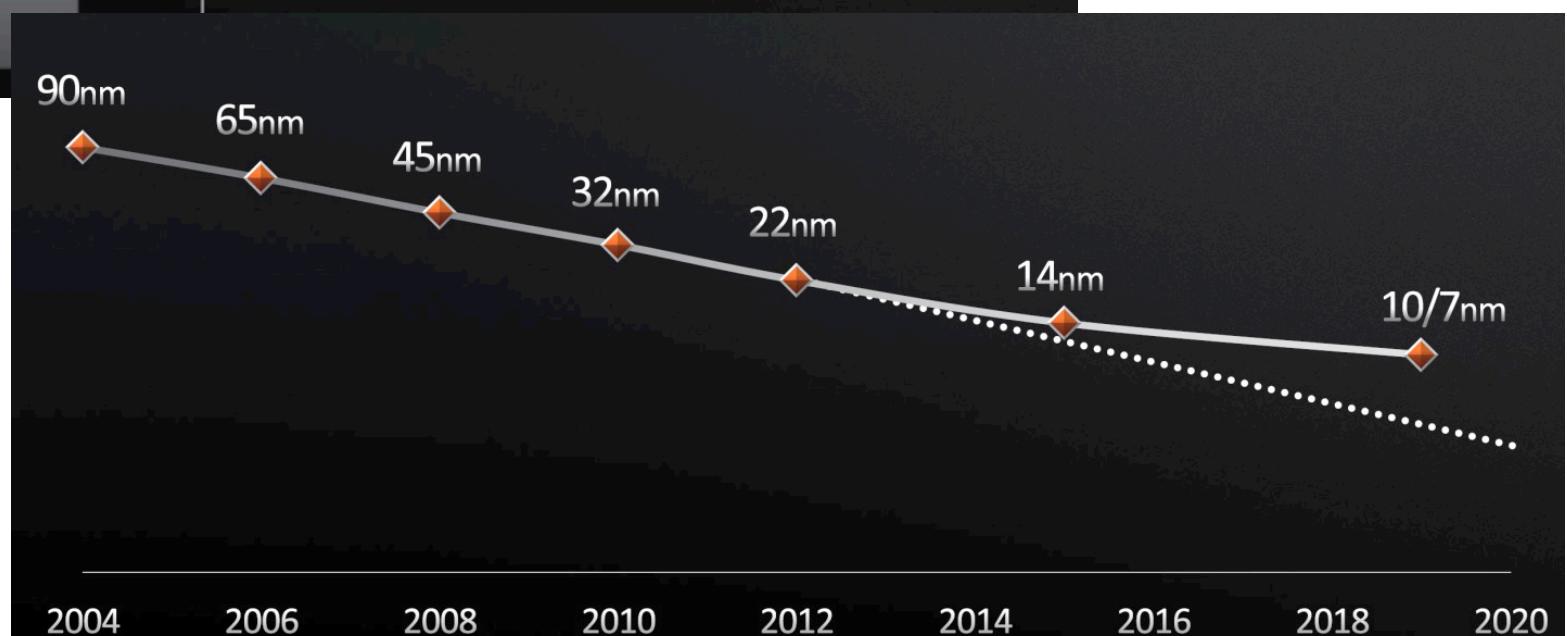
Fig.3 The 5nm also offers a set of critical HPC features. Extremely LVT (eLVT) for 25% faster peak speed over 7nm, and HPC 3-fin standard cell for additional 10% performance.

Putting Scaling in Perspective

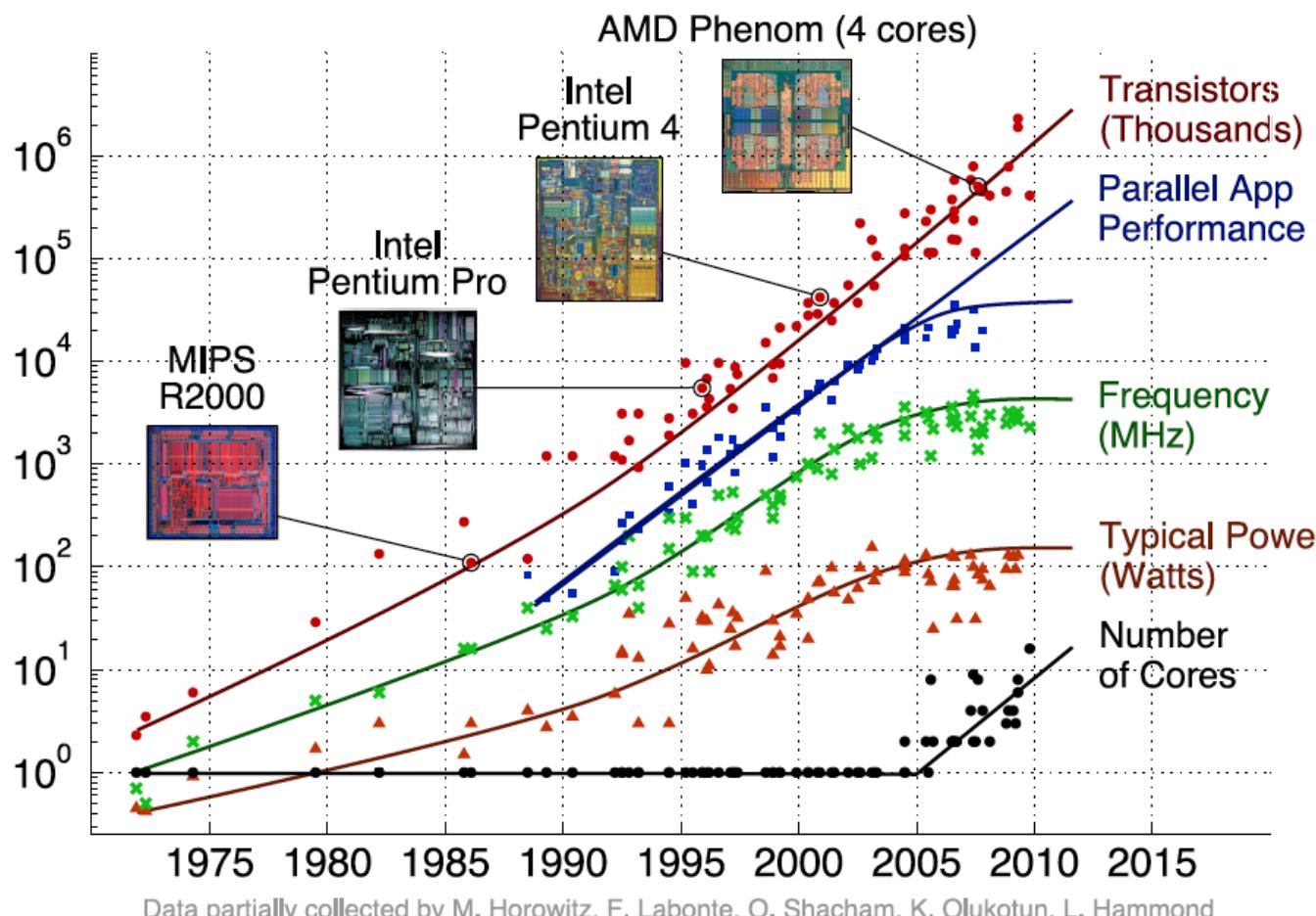


Performance gains
over the past decade

Lisa Su, HotChips'19 keynote



Power and Performance Trends



- What do we do next?

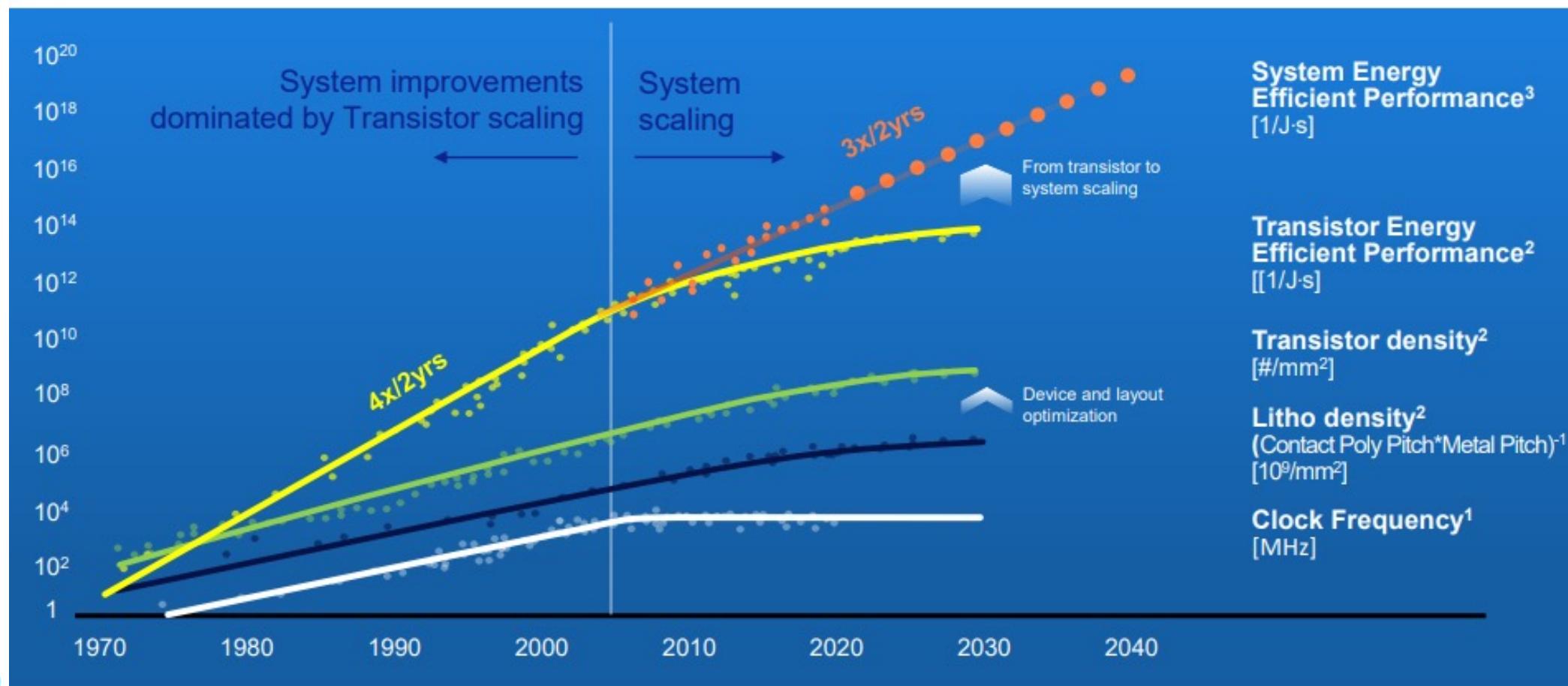
Continued performance system scaling and specialization

Moore's law evolution: the next decade

System scaling to satisfy the need for performance and energy consumption

ASML

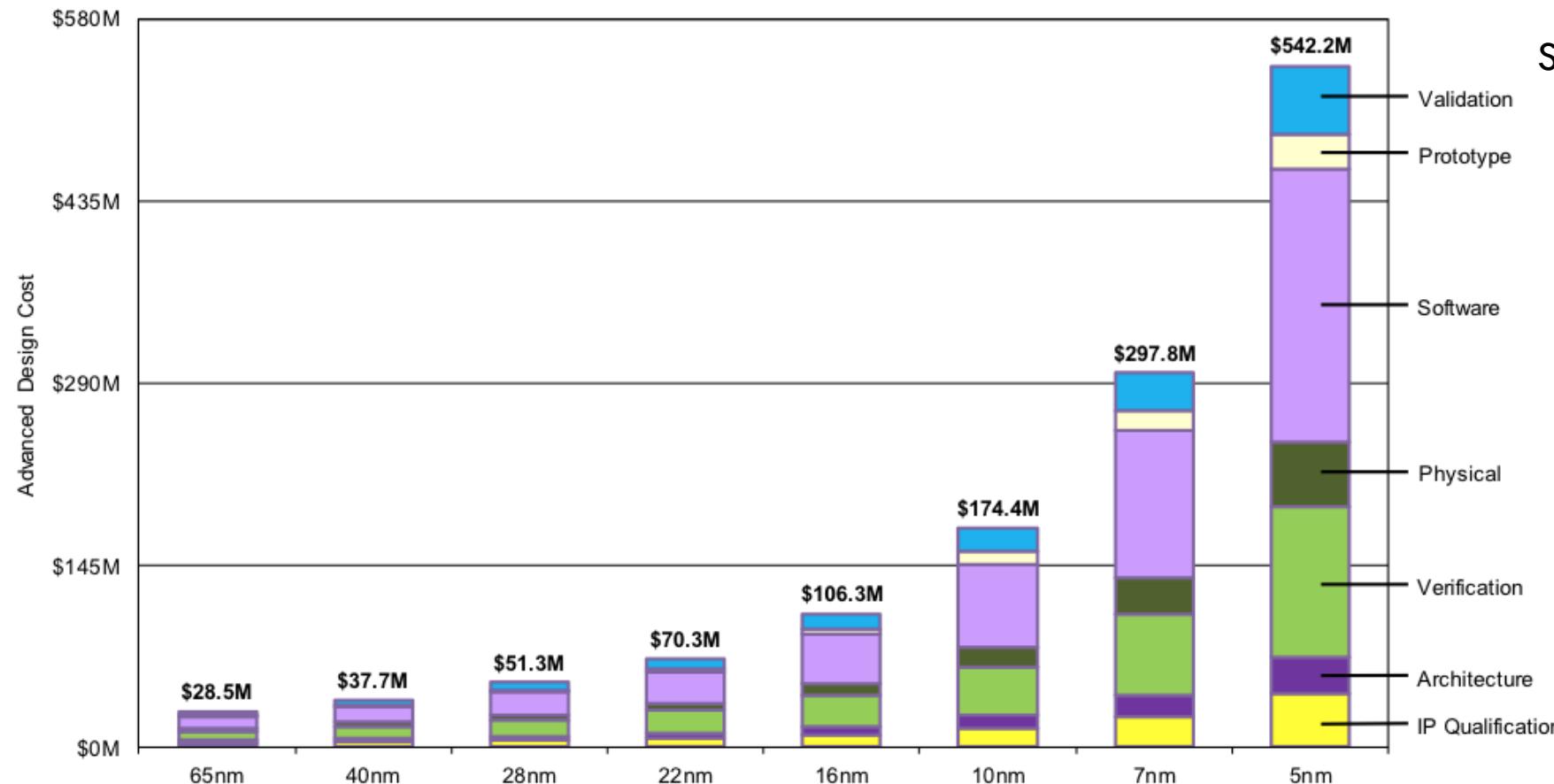
Slide 13
29 Sept. 2021



Sources: ¹Karl Rupp, ²ASML data and projection using Rupp, ³Mark Liu, TSMC, normalized to transistor EEP in 2005.

Public

Cost Of Developing New Products



Source: IBS

- These are non-recurring (NRE) costs, need to be amortized over the lifetime of a product
- We will attempt to dismantle this...

Major Roadblocks

1. Managing complexity

How to design a 10 billion (100 billion) transistor chip?
And what to use all these transistors for?

2. Cost of integrated circuits is increasing

It takes >>\$10M to design a chip
Mask costs are many \$M in 16nm technology
Wafer costs are increasing

3. Power as a limiting factor

End of frequency scaling
Dealing with power, leakages

4. Robustness issues

Variations, SRAM, memory, soft errors, signal integrity

5. The interconnect problem

Next Lecture

- Chipyard as an SoC template