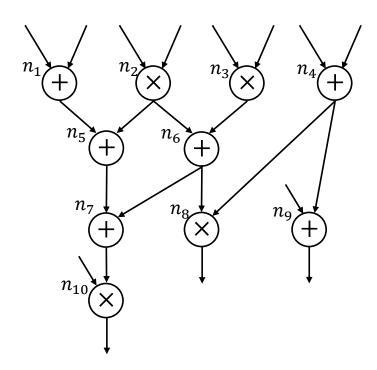
## University of California Irvine

EECS 221: Languages and Compilers for Hardware Accelerators (Winter 2022)

## Homework 2

Due: Monday, February 7, 2022

1. (60 points) **List Scheduling.** Perform list scheduling on the following data-flow graph. Assume there are two adders and one multiplier. An adder needs one clock cycle and a multiplier needs two clock cycles to complete one operation. Show the detailed steps in your work, including ASAP schedule (10 pts), ALAP schedule (10 pts), mobility (or slack) of nodes (10 pts), the values of  $U_{l,k}$  and  $T_{l,k}$  in the scheduling process (20 pts), and final scheduling result (10 pts).



- 2. (40 points) **ILP Scheduling.** In the following DFG, both adder and multiplier take *one* clock cycle to complete one operation. There is one multiplier and two adders available. We would like to find out whether a schedule with latency of 3 clock cycles would be feasible through ILP.
  - (a) (30 points) Define binary variable  $x_{il}$  as explained in the lecture, and then write out all the constraints involved in the ILP.
  - (b) (10 points) What objective function (how to choose c) would minimize the overall latency and why? (hint: dummy sink)

(Note: you don't need to actually solve the formulated ILP problem)

