idle

finish <- 1

address <- 0
in_cnt <- 0
p1_reg <- 0
p2_reg <- 0
p3_reg <- 0
p4_reg <- 0
coef1_reg <- dataROM[13-7]
coef2_reg <- dataROM[6-0]
start <- 0
mul_cnt <- 0
col_cnt <- 0

valid_input = 1

False

True

finish <= 0
in1_reg <- in1_reg << 8 & input
shift_cnt <= 1

store_input

shift_cnt = 0

False

shift_cnt = 1

False

shift_cnt = 2

False

True

True

True

in1_reg <- in1_reg << 8 & input

in2_reg <- in2_reg << 8 & input

in3_reg <- in3_reg << 8 & input

in4_reg <- in4_reg << 8 & input

in_cnt = 30

False

True

shift_cnt <- shift_cnt + 1
in_cnt <- in_cnt + 1

multiply

mul_cnt(0) = 1

False

True

mu_flag = 1

False

True

mu_flag = 1

True

False

p1_reg <- in1_reg(63-56)*coef1_reg + p1_reg
p2_reg <- in2_reg(63-56)*coef1_reg + p2_reg
mu_flag <= 1

p3_reg <- in3_reg(63-56)*coef1_reg + p3_reg
p4_reg <- in4_reg(63-56)*coef1_reg + p4_reg

mul_cnt <- mul_cnt + 1
address <- address + 1
mu_flag <= 0

p3_reg <- in3_reg(63-56)*coef2_reg + p3_reg
p4_reg <- in4_reg(63-56)*coef2_reg + p4_reg

mul_cnt <- mul_cnt + 1
coef1_reg <- dataROM(address)[13-7]
coef2_reg <-dataROM(address)[6-0]
mu_flag <= 0

p1_reg <- in1_reg(63-56)*coef2_reg + p1_reg
p2_reg <- in2_reg(63-56)*coef2_reg + p2_reg
mu_flag <= 1

in1_reg <- in1_reg << 8 & in1_reg(63-56)
in2_reg <- in2_reg << 8 & in2_reg(63-56)
in3_reg <- in3_reg << 8 & in3_reg(63-56)
in4_reg <- in4_reg << 8 & in4_reg(63-56)

mul_cnt = 7

True

False

col_cnt <- col_cnt + 1

load_col

load <= 1

col_cnt = 3

False

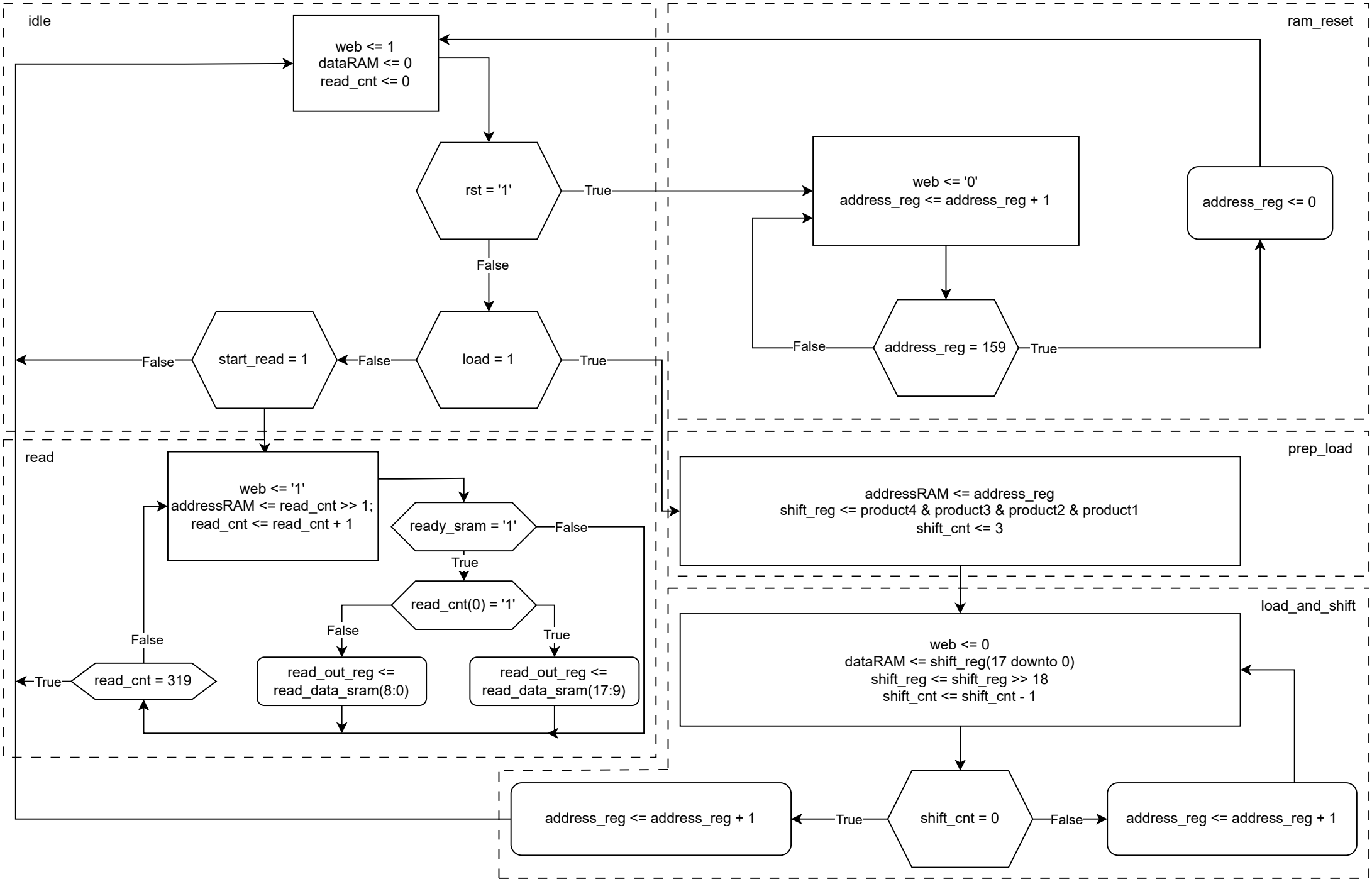
True

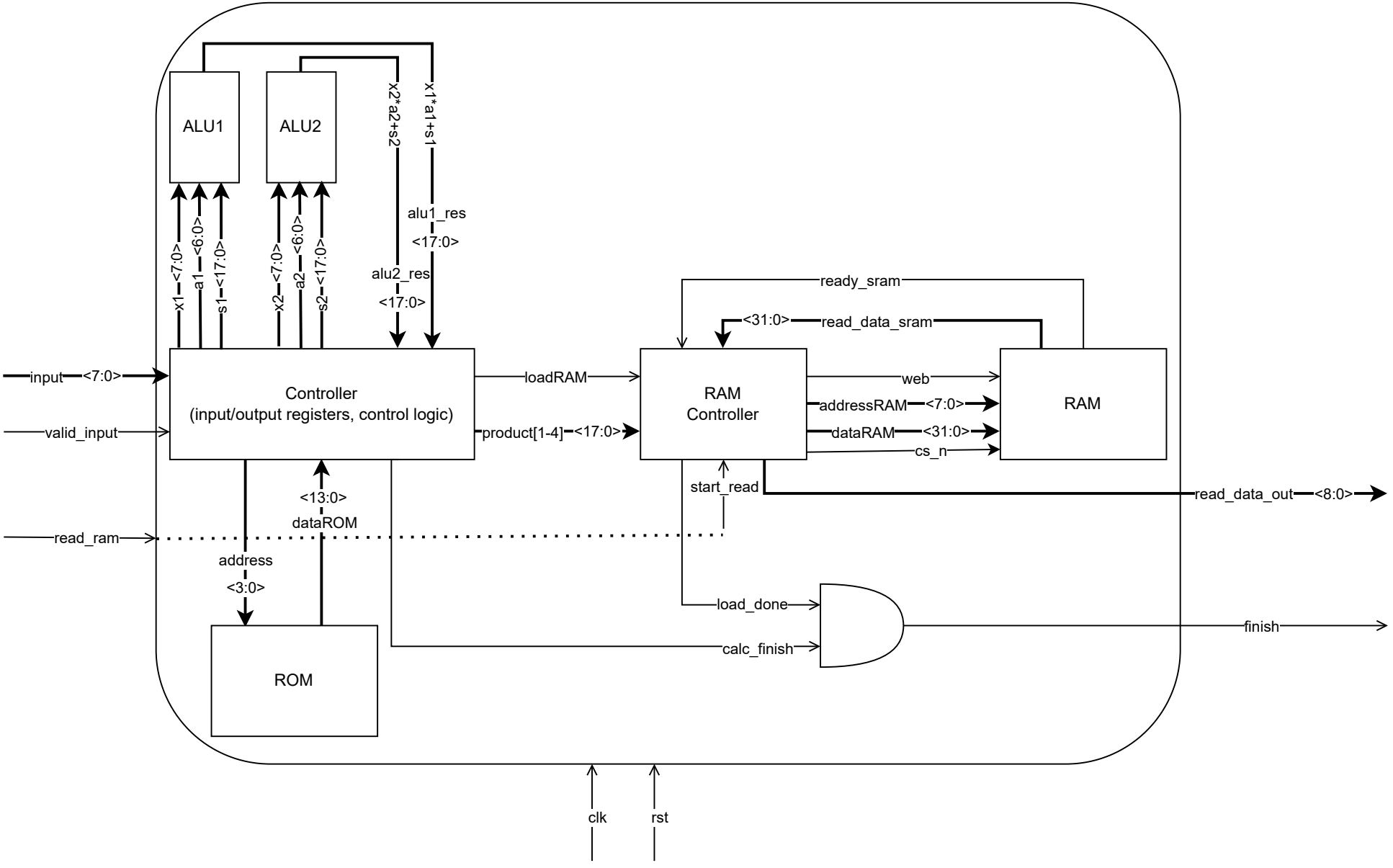
finish <= 1

start_next_column

p1_reg <= 0
p2_reg <= 0
p3_reg <= 0
p4_reg <= 0
mul_cnt <= 0
col_cnt <= col_cnt + 1

RAM Controller




ALU1
ALU2
x1*a1+s1
x2*a2+s2
x1
<7:0>
a1
<6:0>
s1
<17:0>
x2
<7:0>
a2
<6:0>
s2
<17:0>
alu1_res
<17:0>
alu2_res
<17:0>
ready_sram
<31:0>
read_data_sram
input
<7:0>
valid_input
Controller
(input/output registers, control logic)
loadRAM
product[1-4]
<17:0>
RAM
Controller
web
addressRAM
<7:0>
dataRAM
<31:0>
cs_n
RAM
start_read
read_data_out
<8:0>
read_ram
<13:0>
dataROM
address
<3:0>
load_done
calc_finish
finish
ROM
clk
rst