

Experiment - 01.

Title :

Simplify the digital design that accepts 2/3 binary inputs and produces 2 binary outcome.

Problem :- The technique involves simplifying the digital design to accept 2/3 binary inputs A & B and return two outputs sum(S) and carry(C).

Method :

In this experiment, the truth table of 2 bit and 3 bit adder is converted to logical expression & implementing the simplified expression to verify the truth table.

1) Half Adder:

Truth Table

Inputs		Output	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Sum

	\bar{B}	B
\bar{A}	0	1
A	1	0

Carry

	\bar{B}	B
\bar{A}	0	0
A	0	1

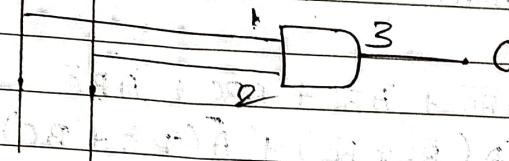
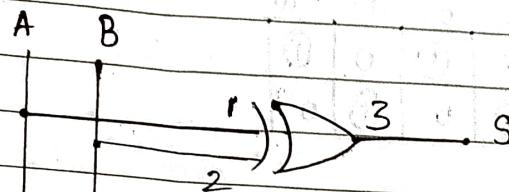
$$S = \bar{A}B + A\bar{B}$$

$$C = AB$$

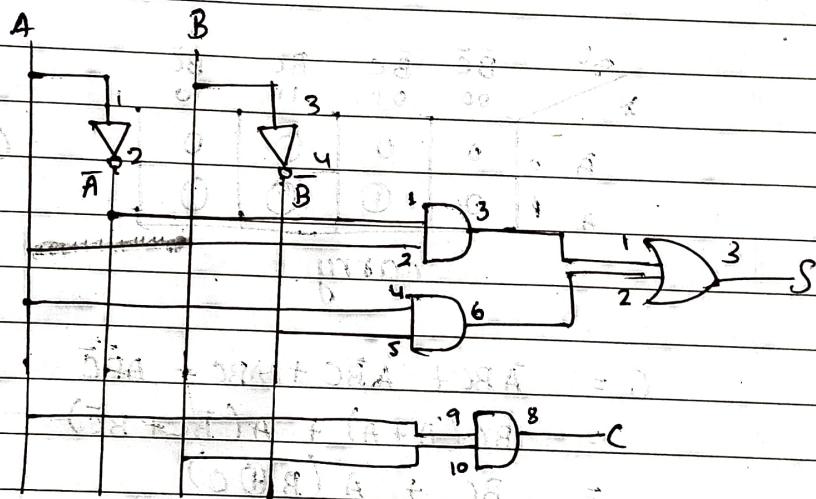
$$S = A \oplus B$$

logical expression.

Logical circuit



Half adder using only basic gates



Truth table

Inputs Output

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

		$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
		00	01	11	10
\bar{A}	0	0	1	0	1
A	1	1	0	1	0

Sum.

$$\begin{aligned}
 S &= A\bar{B}\bar{C} + \bar{A}\bar{B}C + ABC + \bar{A}B\bar{C} \\
 &= \bar{A}(\bar{B}\bar{C} + B\bar{C}) + A(\bar{B}\bar{C} + BC) \\
 &= \bar{A}(B \oplus C) + A(B \oplus C)
 \end{aligned}$$

$$S = A \oplus B \oplus C$$

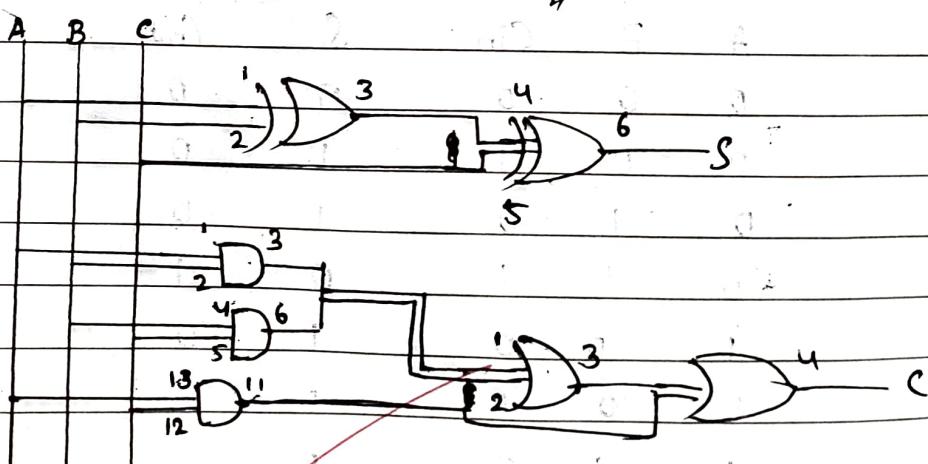
		$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
		00	01	11	10
\bar{A}	0	0	0	1	0
A	1	0	1	1	1

carry.

Carry.

$$\begin{aligned}
 C &= \bar{A}BC + A\bar{B}C + ABC + A\bar{B}\bar{C} \\
 &= \bar{B}C(\bar{A} + A) + A(\bar{B}C + B\bar{C}) \\
 &= BC + A(B \oplus C) \\
 C &= A(B \oplus C) + BC
 \end{aligned}$$

$$C = AB + BC + AC$$



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Title : Design a digital system that connects any one input to the output based on the selection inputs.

Problem description :

A digital system which consists of 8 input lines & at any given time only one input will be connected to output based on select lines.

Methods :

The technique utilized here is to simplify the given expression using multiplexer and connect one among multiple input to output signal based on selected inputs.

Aim :

To are a given 4 variable logic operation, simplify it by using entered variable map and realize the simplified logic expression using 8:1 multiplexer.

$$F(A, B, C, D) = \Sigma(0, 4, 5, 7, 8, 10, 12, 14, 15)$$

A	B	C	D	Y	D
0	0	0	0	1	\bar{D}_1
0	0	0	1	0	\bar{D}_2
0	0	1	0	0	D_1
0	0	1	1	0	D_2
0	1	0	0	1	D_2
0	1	0	1	1	D_2
0	1	1	0	0	D_3
0	1	1	1	1	D_3

A	B	C	D	y	D
1	0	0	0	1	\bar{D}
1	0	0	1	0	\bar{D}
1	0	1	0	1	\bar{D}
1	0	1	1	0	\bar{D}
1	1	0	0	1	\bar{D}
1	1	0	1	0	\bar{D}
1	1	1	0	1	\bar{D}
1	1	1	1	1	\bar{D}

FC A,

Title:
Design

Problem

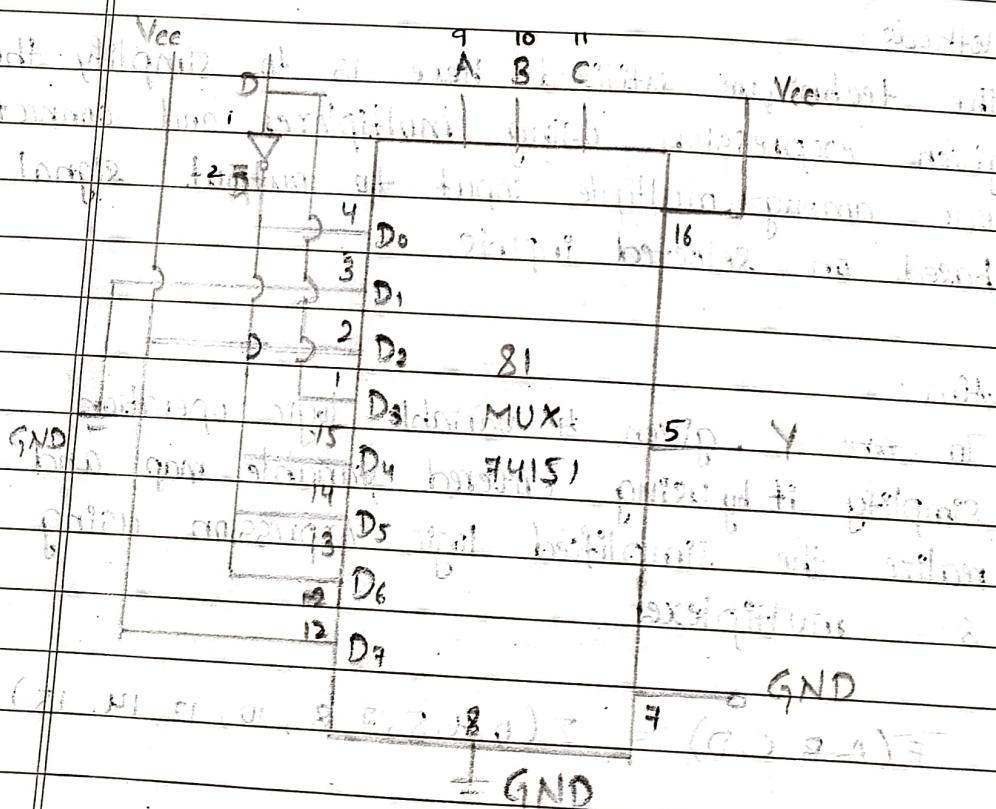
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Method

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Result: Verified the Truth Table

$$f(A, B, C, D) = \sum (0, 3, 4, 5, 8, 9, 10, 12, 13, 14)$$

Title :

Design a code converter circuit

Problem Description:

In this experiment code conversion is done from Binary to Gray and appropriate technique is used to simplify the logic circuit to demonstrate the conversion.

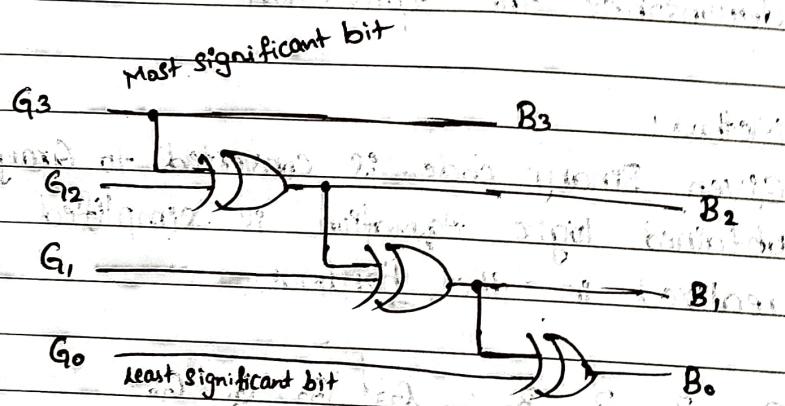
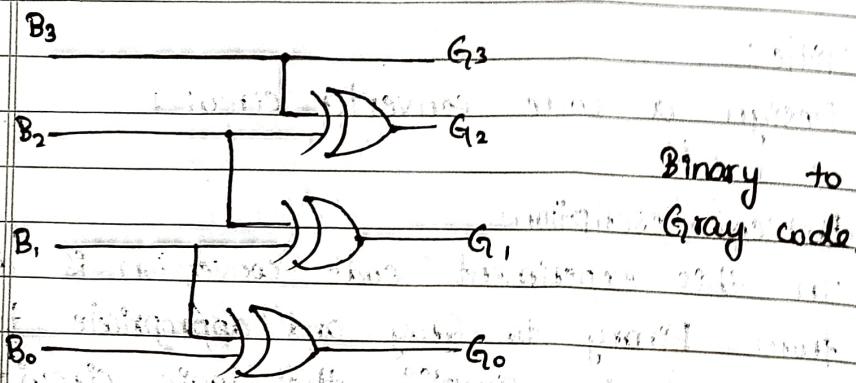
Method :

Given Binary code is converted to Gray code and obtained logic equation is simplified and realized in the hardware.

B ₃	B ₂	B ₁	B ₀	G ₃	G ₂	G ₁	G ₀
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

E ₂ -OR		
0	0	0
0	1	1
1	0	1
1	1	0

Using XOR :



Gray code to Binary

$$B_3 = G_3$$

$$B_3 = G_3$$

$$B_2 = G_3 \oplus G_2$$

$$B_2 = G_3 \oplus G_2$$

$$B_1 = G_2 \oplus G_1$$

$$B_1 = B_2 \oplus G_1$$

$$B_0 = G_1 \oplus G_0$$

$$B_0 = B_1 \oplus G_0$$

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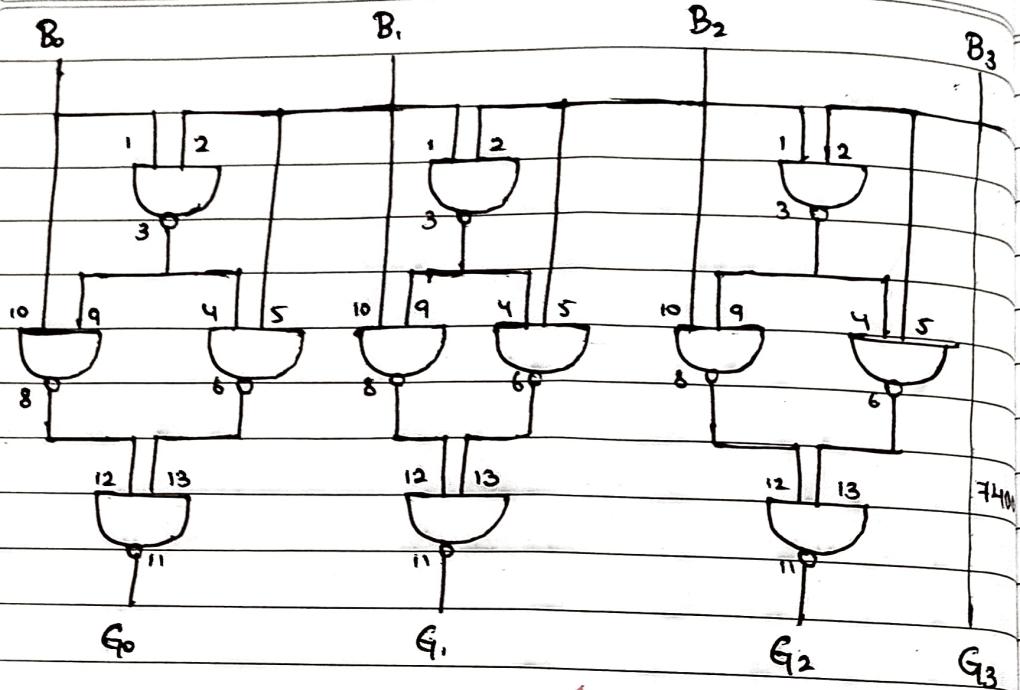
8
8

8
8

8
8

8
8

8
8



Result: Verified Truth Table.

$$G_3 = B_3$$

$$G_2 = B_3 \cdot B_2 + B_2 B_1$$

$$G_1 = B_1 B_2 + B_2 B_1$$

$$G_0 = B_1 B_0 + B_0 B_1$$

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		B ₃ B ₂			
		00	01	11	10
B ₃ B ₂		00	0 0 0 0	0 0 0 0	0 0 0 0
01	0	0	0 0 0 0	0 0 0 0	0 0 0 0
11	1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1
10	1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1

		B ₃ B ₂			
		00	01	11	10
B ₃ B ₂		00	0 0 0 0	0 0 0 0	0 0 0 0
01	0	0	1 1 1 1	1 1 1 1	1 1 1 1
11	1	1	1 1 1 1	1 1 1 1	1 1 1 1
10	1	1	1 1 1 1	1 1 1 1	1 1 1 1

		B ₃ B ₂			
		00	01	11	10
B ₃ B ₂		00	0 0 0 0	0 0 0 0	0 0 0 0
01	1	1	1 1 1 1	1 1 1 1	1 1 1 1
11	1	1	1 1 1 1	1 1 1 1	1 1 1 1
10	0	0	1 1 1 1	1 1 1 1	1 1 1 1

		B ₃ B ₂				
		00	01	11	10	
B ₃ B ₂		00	0	1	0	1
01	0	0	1	0	1	
11	0	1	1	0	1	
10	0	1	1	0	1	

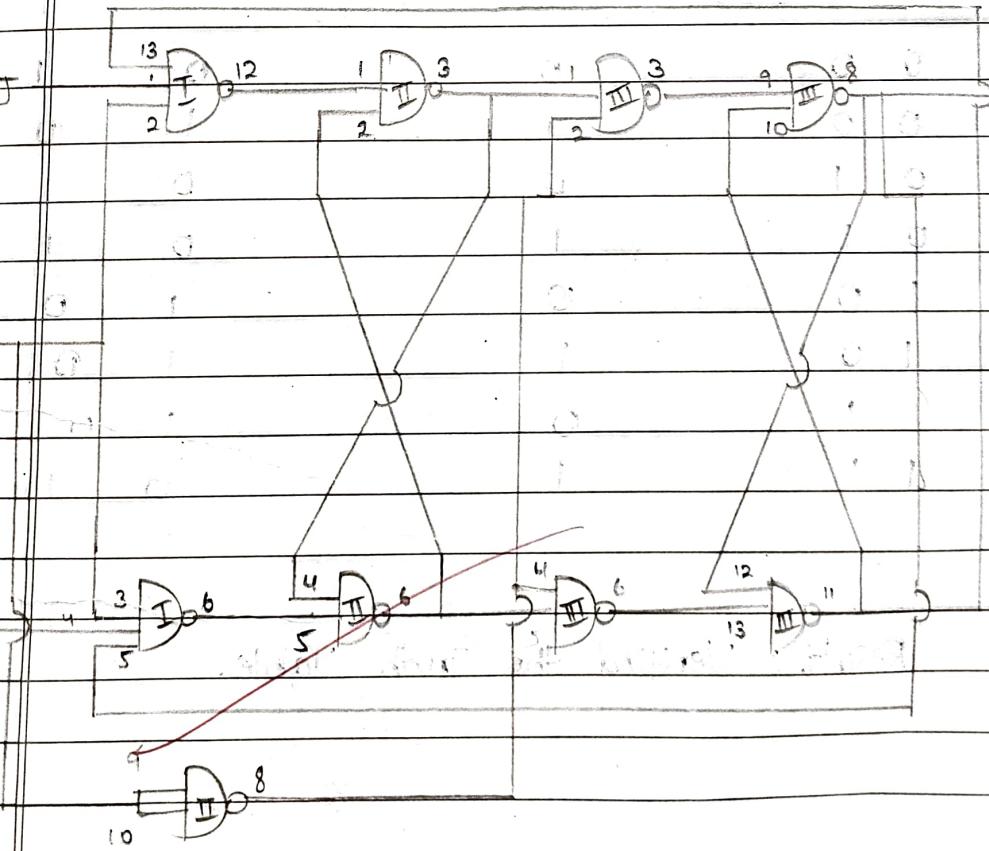
Experiment - 03 : Design JK Flip-flop.

Title: Design a circuit to store one bit of information using universal gates.

Problem Description: Realize the working of flip-flops using universal gates.

Method: In this experiment flip-flops can be built using universal gates in the feed-back path and demonstrate it can be used as storage elements.

Design:



Truth Table:

Inputs	Outputs	Status
J K	$Q(t+1)$	
0 0	0	Hold
0 1	0	reset
1 0	1	Set
1 1	$Q(t)'$	toggle

$$\text{Qnext} = JQ' + K'Q$$

Input	JK master slave flip flop (Establish using preset/clear)		Output	
J K	$Q(t+1)$	$Q(t+1)'$	$Q(t+1)$	$Q(t+1)'$
0 0	0	1	0	1
0 0	1	0	1	0
0 1	0	1	0	1
0 1	1	0	0	1
1 0	0	1	1	0
1 0	1	0	1	0
1 1	0	1	1	0
1 1	1	0	0	1

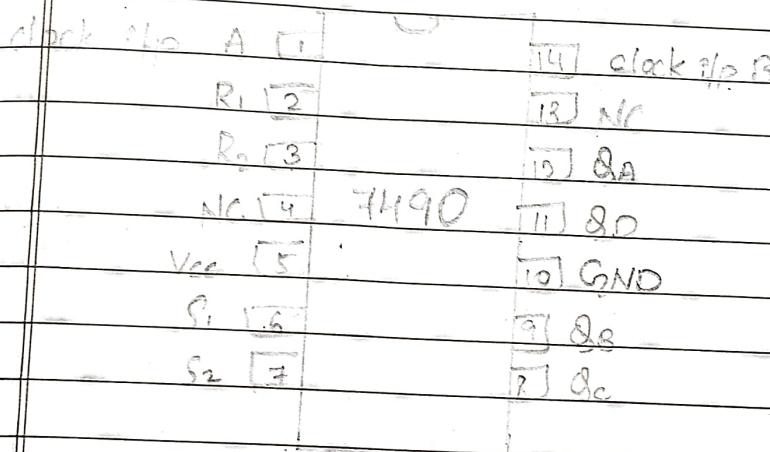
Result: Verified the Truth Table.

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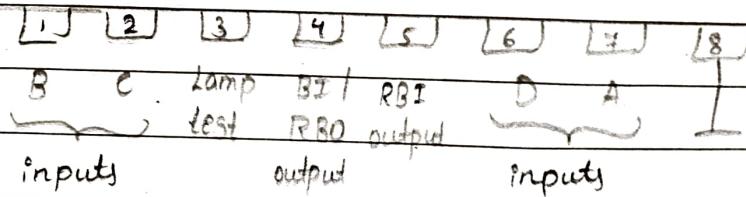
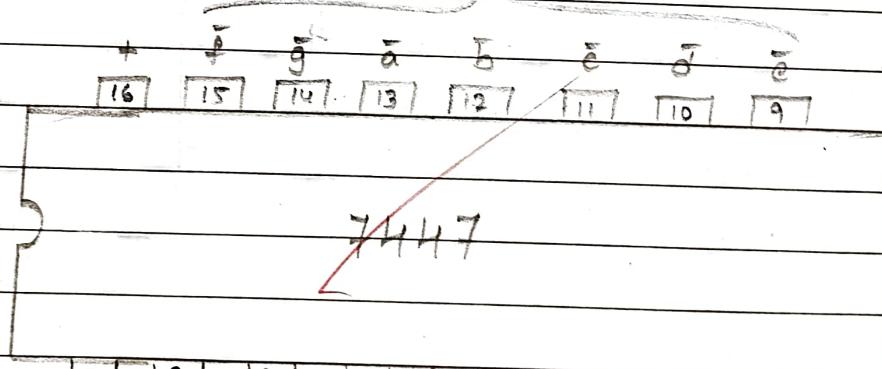
Experiment - 05 : Asynchronous counter.

Title: Design asynchronous counter.

Problem: Design a counter for the sequence 0-1-2-3-4-5-6-7-8-9 & display them on 7 segment LED display.



Outputs



9 f. +Vcc a b

10 9 8 7 6

a

c

c

d

1 2 3 4 5

c d +Vcc e decimal point.

+5V

1kΩ

+5V

3 4 5 16

CLK1

QA

A

13

a

7

CLK2

QB

B

12

b

6

a

MRI

QB

C

4

11

c

4

MR2

QC

D

4

10

d

9

MSI

QD

D

7

9

e

1

MSO

(MSB)

E

15

f

9

d

GND Vcc

14

9

10

10 5

+5V

Result: Verified output on 7 segment LED.

✓

Experiment - 06.

Title : Synchronous counter

Problem description: Given 'n' count, counter is designed to count up from 0 to n up counting

K-Map for J_C

$\bar{C}_n \bar{B}_n$	\bar{A}_n	A_n
$\bar{C}_n B_n$	0 ⁰	0 ¹
$C_n \bar{B}_n$	0 ²	0 ³
$C_n B_n$	0 ⁴	0 ⁵

K-Map for K_C

$\bar{C}_n \bar{B}_n$	\bar{A}_n	A_n
$\bar{C}_n B_n$	X ⁰	X ¹
$C_n \bar{B}_n$	X ²	X ³
$C_n B_n$	X ⁴	X ⁵

K-Map for J_B

\bar{A}_n	A_n
0 ⁰	1 ¹
0 ²	X ²
X ⁶	X ⁷
0 ⁴	0 ⁵

$$J_C = B_n A_n$$

$$K_C = A_n$$

$$J_B = \bar{A}_n \bar{C}_n$$

K-Map for K_B

\bar{A}_n	A_n	
$\bar{C}_n \bar{B}_n$	X	X
$\bar{C}_n B_n$	0	1
$C_n \bar{B}_n$	X	X
$C_n B_n$	X	X

K-Map for J_A

\bar{A}_n	A_n	
$\bar{C}_n \bar{B}_n$	1	X
$\bar{C}_n B_n$	1	X
$C_n \bar{B}_n$	X	X
$C_n B_n$	1	X

K-Map for K_A

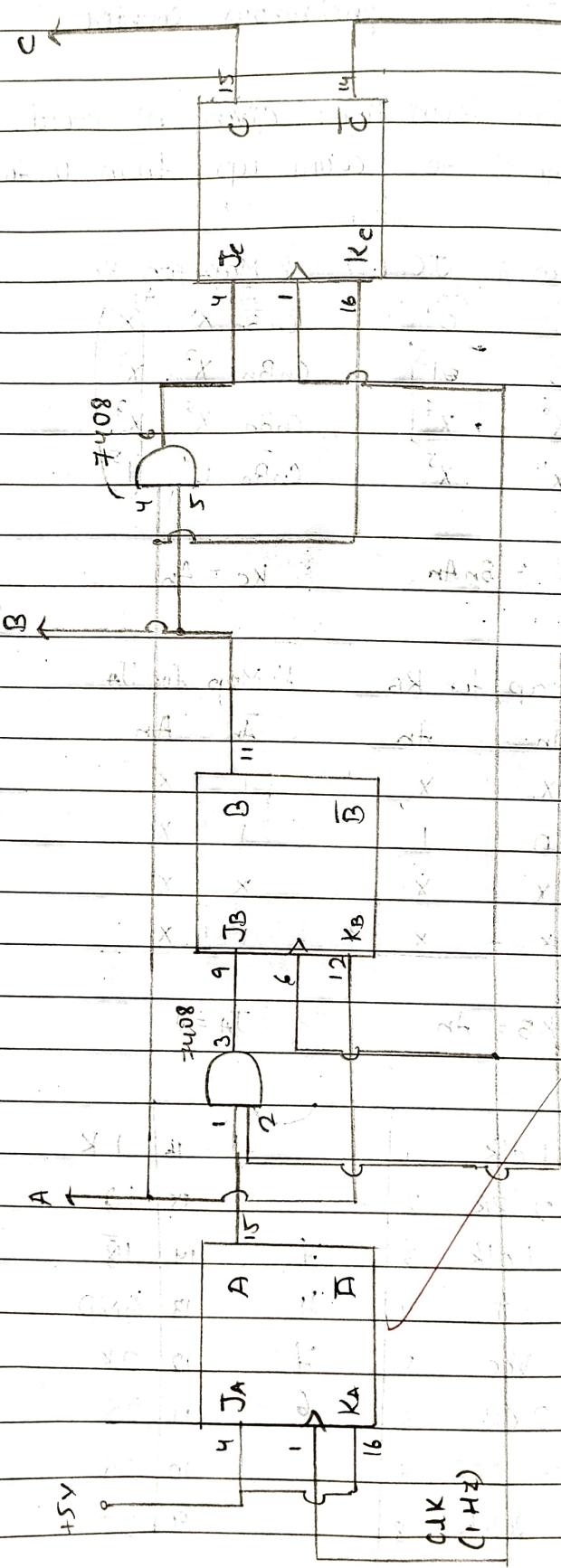
\bar{A}_n	A_n	
$\bar{C}_n \bar{B}_n$	X	1
$\bar{C}_n B_n$	X	1
$C_n \bar{B}_n$	X	X
$C_n B_n$	X	1

$$K_B = A_n$$

$$J_A = 1$$

$$K_A = 1$$

1 clk	1		16	1 K
2 PR	2		15	1 Q
1 clk	3	7	14	1 Q
1 J	4	4	13	GND
Vcc	5	7	12	2 K
2 CLK	6	6	11	2 Q
Preset 2PR	7		10	2 Q
Clear 2CLR	8		9	2 J



Truth table:

C	B	A
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1

~~Result : Truth Table is Verified.~~

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