

# Graphene Field Effect Transistor

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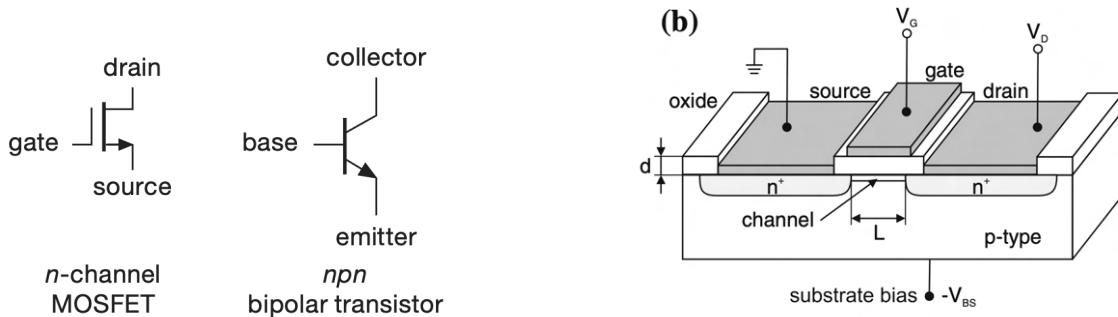
## Abstract

Graphene is a two dimensional hexagonal arrangement of carbon atoms which has the properties that the energy band structure is linear rather than parabolic at low energies and is a zero-gap semiconductor. These two properties lead to a resistivity versus gate voltage curve that exhibits a sharp peak for undoped graphene at zero gate voltage ( $V_G$ ) that then slopes down towards zero as  $V_G$  increases/decreases. To experimentally verify this behavior, we fabricated a graphene field effect transistor (FET) and measured the resistivity of the graphene channel as a function of the gate voltage. In doing so, we gained exposure to the skills of mechanical exfoliation, photolithography, deposition, and lift off. We fabricated two graphene FETs and performed back gate resistivity measurements and found that for one sample (3A) that there may be a resistivity dependence on  $V_G$  that weakly agrees with the expected behavior although curve appears to be broadened and our data is overall noisy. We then discuss the possible reasons: gate leakage in our samples, non ideal graphene samples,

## 1 Background Information

### 1.1 Field Effect Transistor

A transistor is a general circuit device that has two general uses: as a switch and as a signal amplifier. Transistors generally have three or more terminals. For a field effect transistor, the first two are referred to as the source and drain. The source allows for the charge carriers to enter which then leave through the drain via a channel that connects the two and allows for current flow. The third terminal, often called the gate, controls the flow of current from the source terminal to the drain terminal by controlling the number of charge carriers and hence affects the resistivity (equivalently the conductivity) of the channel. This for instance would allow the transistor to act as a switch by taking the resistivity towards infinity and ceasing current flow or conversely letting the resistivity tend towards zero to allow for current to flow [4, pg. 131,115]



(a) Circuit Diagram Representation for a MOSFET, a type of field effect transistor, juxtaposed with a bipolar transistor [4, pg. 131]

(b) Pictorial Representation of a metal-oxide-semiconductor field transistor (MOSFET) with the three terminals: source, drain, and gate represented. In particular, we see that the gate is insulated from the channel by an oxide layer. [3, pg. 804]

Figure 1: Representations of Field Effect Transistors

A field effect transistor (FET) is a specific type of transistor where the concentration of the charge carriers between the source and drain terminals is controlled by an electric field that arises from an applied voltage to the gate terminal.

In particular, for a MOSFET, the structure of the transistor is that of a parallel plate capacitor where the channel and the substrate body form the two conducting plates with the thin layer of oxide (commonly silicon dioxide) sandwiched in between acting as the dielectric. Applying a voltage to the gate then induces charge separation between the two plates and induces charges on the conductive channel and hence affects the number of free carriers.

## 1.2 Graphene

Proper monolayer graphene is a two dimensional, single layer of hexagonal honeycomb arrangement of carbon atoms. Due to this structure, graphene has some significant electronic properties such as high electron mobility on the order of  $15,000 \text{ cm}^2/\text{Vs}$  [2]. Additionally, graphene is a semiconductor with zero-gap between the valence and conduction band (which in this case would make it more like a metal). The energy-momentum dispersion relation takes the linear form

$$E = \hbar k c_* \quad c_* \approx 10^6 \text{ m/s} \quad (1)$$

akin to the dispersion relation for relativistic massless particles like photons for low energies near the Dirac points, the points where the valence and conduction bands meet, as highlighted in the zoomed in region in Figure 2. We can see that the typical parabolic bands are to first order replaced by linear cones, illustrating the linear energy-momentum dispersion relation described in equation (1).

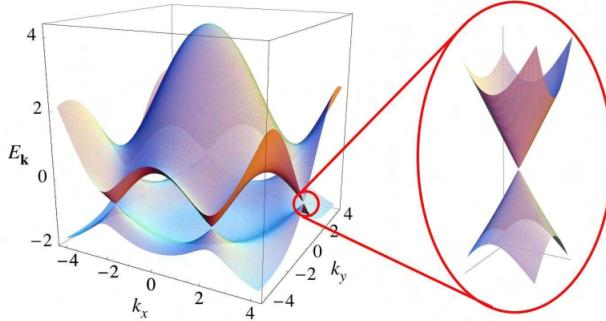


Figure 2: Band Structure Graphene with emphasis on Dirac Points [1]

Likewise for low energies, from the linear energy momentum dispersion relation, the density of states as a function of energy is given approximately by  $\rho(E) \propto |E|$  [5]. Since the number density of carriers is given by

$$n = \int_{-\infty}^E \rho(E) F(E) dE \quad (2)$$

where  $\rho$  is the density of states and  $F(E)$  is the Fermi-Dirac distribution, as the Fermi energy sweeps through the conduction and valence bands, the cone shapes indicate that the number of charge carriers (holes for the valence band and electrons for the conduction band) will decrease as the Fermi energy approaches the Dirac points and increase as it moves further away.

## 1.3 Graphene Field Effect Transistor

A graphene field effect transistor is a field effect transistor where the channel is replaced with a sample of graphene.

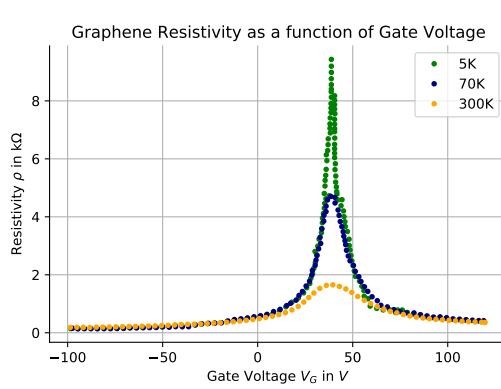
When we apply a voltage to the gate, the electric field effect shifts the position of the Fermi energy by inducing a doping of electrons or holes in the graphene. The number of available states will in turn increase

as the Fermi energy moves away from the Dirac points which increases the conductivity. Conversely, as the Fermi energy approaches the Dirac point, the number of states in principle approaches zero which means that the conductivity goes towards zero, or equivalently the resistance increases to infinity. This idea is visualized in Figure 3a which gives the resistivity as a function of applied gate voltage which demonstrates a sharp peak [5, pg. 667] For few-layer graphene, the resistivity tends towards the order of 100 ohms for high gate voltage and tends towards orders of kilo-ohms as the resistivity approaches its peak [5].

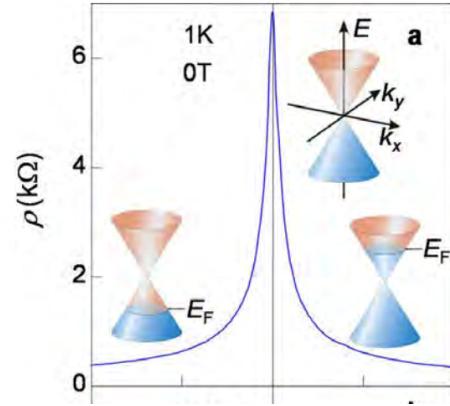
A model describing this effect is presented in [5] where the graphene is treated as a two dimensional metal with the conductance band and valence bands overlapping. When a gate voltage  $V_G$  is applied, the subsequent electric field induces a charge density  $n$  in the graphene where  $n$  is given by

$$n = \frac{\varepsilon_0 \varepsilon V_G}{te} \quad (3)$$

with  $\varepsilon_0, \varepsilon$  are the permittivities of free space and  $\text{SiO}_2$ ,  $e$  is the charge of the electron, and  $t$  is the depth of the insulating layer. As  $V_G$  goes towards zero,  $n$  goes to zero and hence the resistivity increases towards infinity. Likewise, as  $V_G$  increases or decreases further away,  $n$  increases and the resistivity will instead decrease.



(a) Typical Resistivity vs Gate Voltage Curve for Graphene at different temperatures. We see that the resistivity exhibits a peak which corresponds to the point where the fermi energy is equal to the Dirac energy. Data taken from plot in [5, pg. 667]



(b) Resistivity vs Gate Voltage exhibiting the characteristic peak when the Fermi energy is at precisely the Dirac point. For  $V_G < 0$ , the Fermi energy is in the valence band, for  $V_G > 0$ , it's in the conduction band. As the Fermi energy moves away from the Dirac points, the “cross section” of the cone increases and thus the density of states increasing the conductivity. Plot taken from [2]

## 2 Procedure: Graphene FET Fabrication

In the steps below we prepare our graphene field effect transistor whose features are shown in figure 4. This broadly consists of three stages: preparations of the wafer and locating samples of graphene, photolithography, and finally the deposition of gold and lift off to complete the transistor.

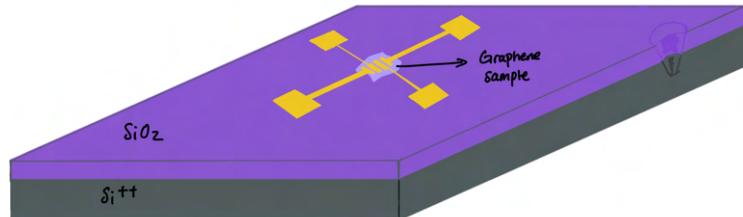
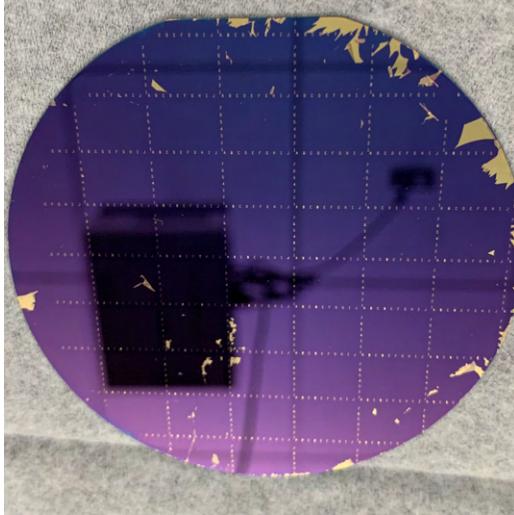


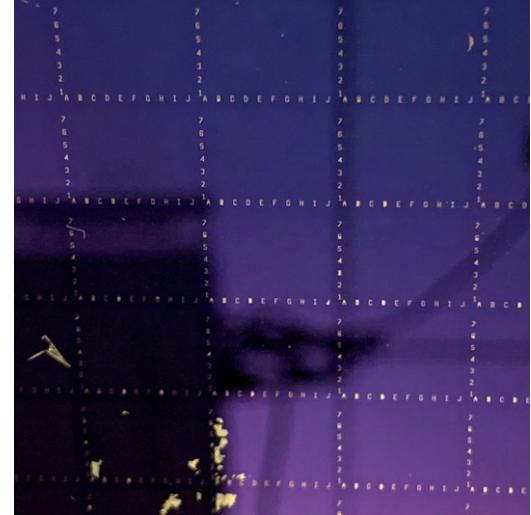
Figure 4: General Sketch of the Graphene FET we are to create. In particular, we want to print a gold circuit on top of a candidate graphene sample

## 2.1 Initial Wafer and Graphene Sample Preparation

1. We prepared rectangular wafers approximately 1.5 cm by 2 cm in size from a 3 inch diameter silicon wafer marked with a grid of letters and numbers which allows for recalling the location of graphene samples. The silicon wafer consists of highly doped silicon (Si++) with a thin surface coat of silicon dioxide (SiO<sub>2</sub>) which acts as a dielectric. We made the cuts by scoring the wafers with a diamond tipped pen to then break the wafer along the scored lines using a small wire taped to a flat surface as a fulcrum.



(a) The entire marked wafer which consists of gold-titanium evaporated onto the silicon disk using the same photolithography process described in section 2.2

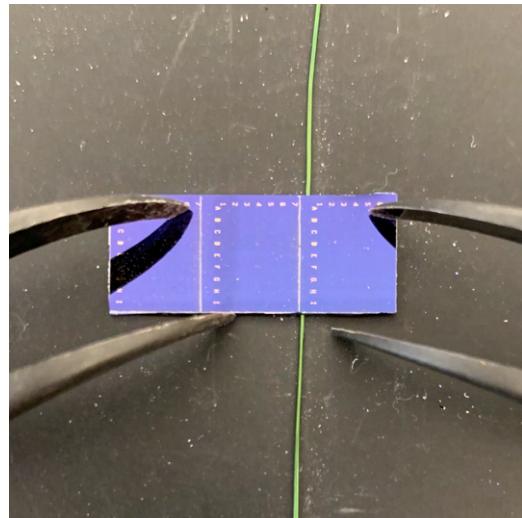


(b) We see more closely the repeating grid of squares where along the  $y$ -axis we have numbers and along the  $x$ -axis we have letters

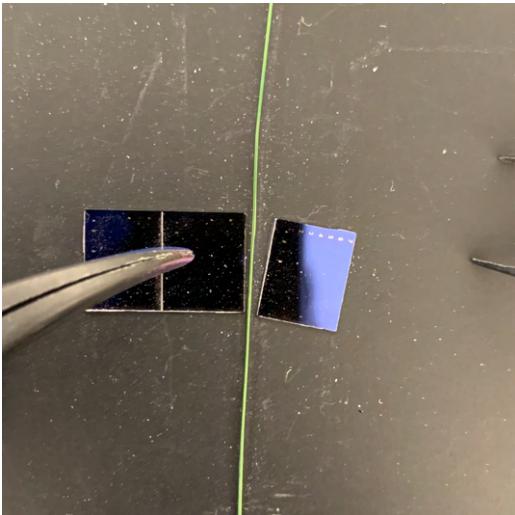
Figure 5: Marked Wafers



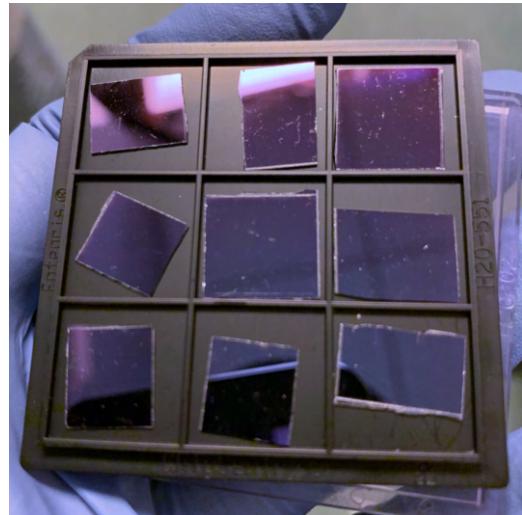
(a) Scoring the wafer by running a diamond tipped scribe over the wafer 2-4 times using a ruler as a guide



(b) Positioning the scored wafer over a strip of wire such that the score lines up with the wire. Then using two tweezers, we press down simultaneously on both sides of the scored line...



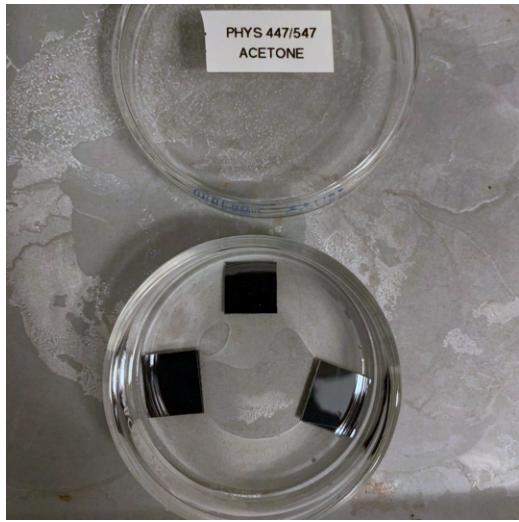
(c) ...which then breaks the wafer cleanly along the scored line



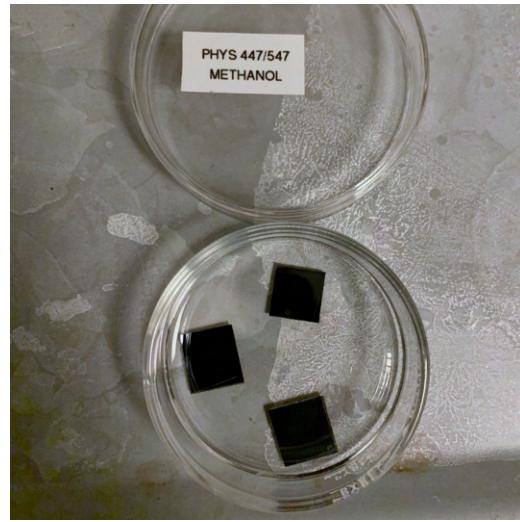
(d) Finally, we store the cut wafers in the sample box for safe keeping. Note the abundance of silicon dust on the wafers which will be removed in the following washing step.

Figure 6: Cutting the individual wafers

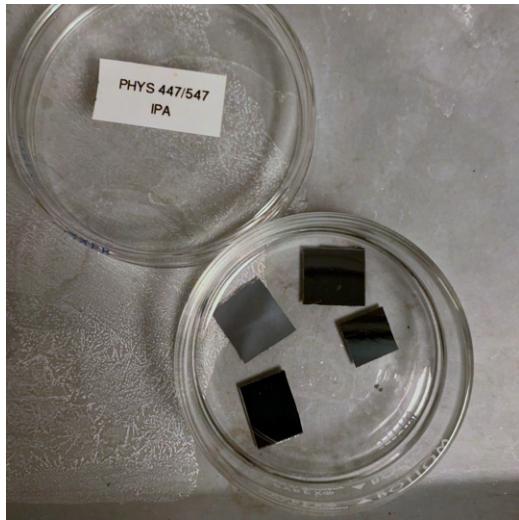
2. After this, we washed the wafers to prepare the substrate for the graphenium exfoliation. Washing consists of a three-step process: submerging the wafer into acetone, methanol, and lastly isopropyl alcohol. The samples were loaded into small glass dishes with the aforementioned chemicals and soaked for 30 seconds per chemical. After the last bath, we dried the samples using jets of air.



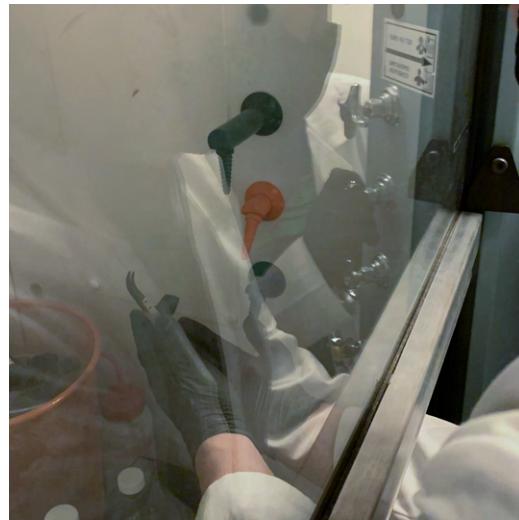
(a) First step: Acetone for 30 seconds



(b) Second step: Methanol for 30 seconds



(c) Third step: Isopropyl Alcohol for 30 seconds



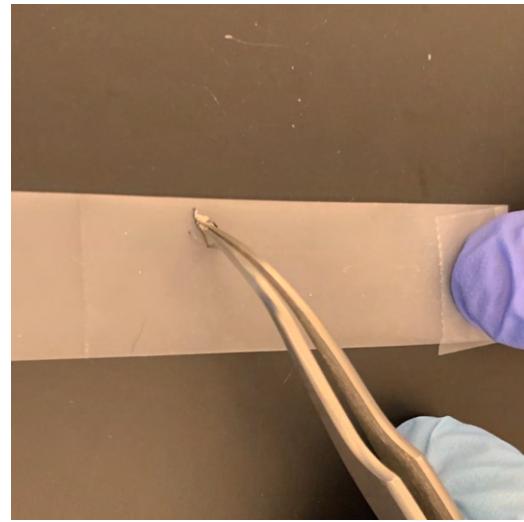
(d) Drying the wafers via a jet of air by holding the wafer tightly with tweezers up to the orange nozzle

Figure 7: Washing Process

3. Once washed, we exfoliated graphenium graphite, a type of highly oriented pyrolytic graphite which lends itself to exfoliation, onto the sample via the Scotch tape method where we loaded flakes of graphenium and pressed and distributed the graphite in scotch tape the goal of which is to lift and distribute layers of graphite and hopefully achieve an incredibly thin layer. After distributing the graphite we then place our wafer, face side down, into the tape as to transfer the graphite onto the wafer.



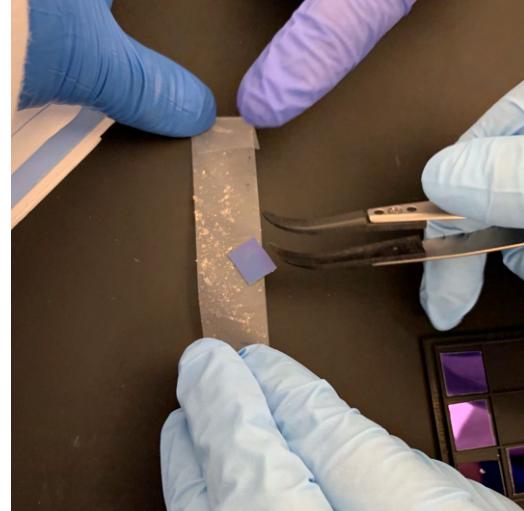
(a) Vial of Graphenium



(b) Loading a small piece of the graphenium crystal onto tape



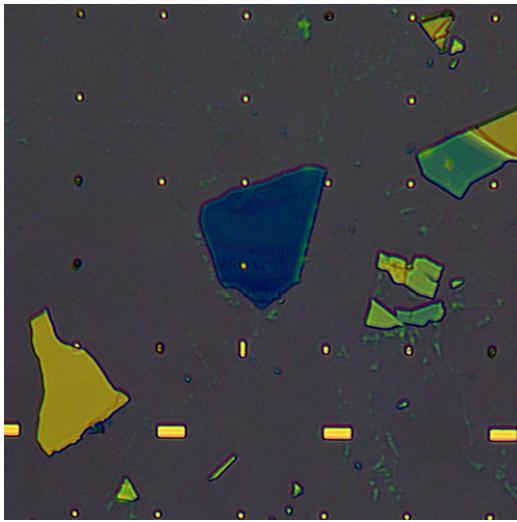
(c) After closing and opening the tape onto itself, the graphite crystals spread out into thinner and thinner layers



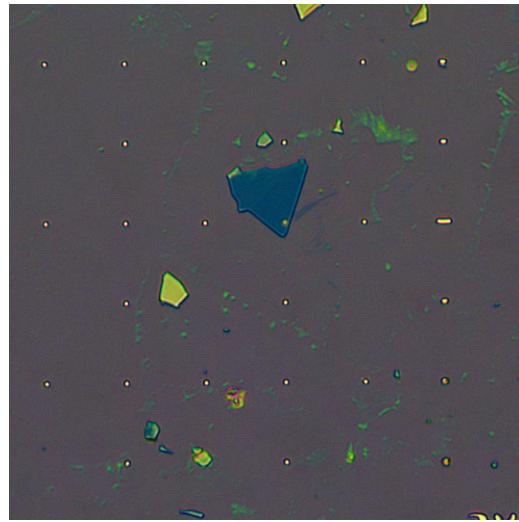
(d) Placing Wafer onto Exfoliated Graphite to transfer onto wafer

Figure 8: Exfoliation Process

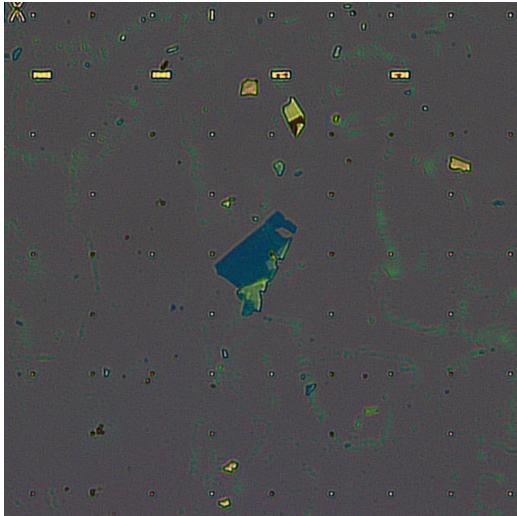
4. Lastly, we looked for samples of graphene using a microscope, searching for patches with a color similar to the substrate, that is, a color that is a darker blue to purple. Though ideal candidates would appear nearly transparent. We found the following samples.



(a) B3/B4 on Wafer 1, Image at 50x



(b) Sample Located near A3, image at 50x



(c) Sample Located at B3

Figure 9: Graphene Samples

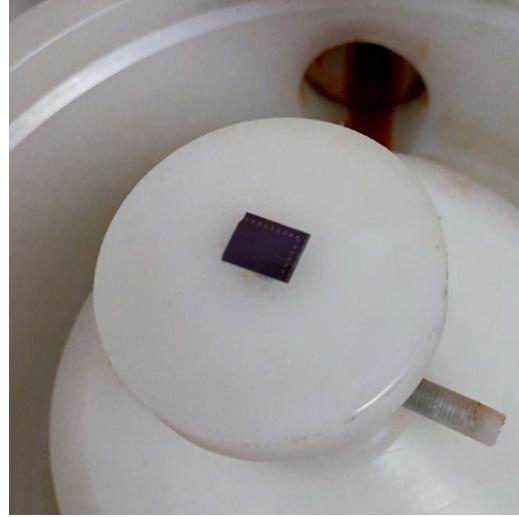
## 2.2 Photolithography

The next process involved photolithography which prints a gold-titanium circuit onto the wafer with the graphene sample at the center of the circuit. All of the following steps takes place in a room with a special filter that filters out UV light.

1. First, we applied a coating of (positive) photoresist, a light sensitive chemical that becomes soluble to the developer after being exposed to ultraviolet light, to the wafers which took place in three stages.
  - First, we placed our wafer into the spin-coat machine, applying a vacuum seal to hold the wafer in place and applied 3 drops of primer to fully coat the wafer. Then we set the machine to run at 4000 rotations per minute (rpm) for 40 seconds.
  - Next, we applied 3 drops of photoresist to the wafer and ran the machine at 7000 rpm for 60 seconds.
  - Finally, we soft baked the wafer on a hot plate at 80° C for two minutes as to stabilize the photoresist for easier handling in the next mask-aligning and exposure step.



(a) Sample Loaded into the Spin Coater

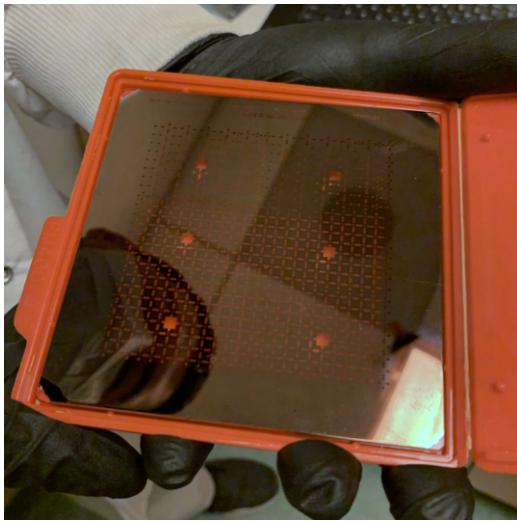


(b) Close up image of our wafer. It is secured in place via vacuum suction

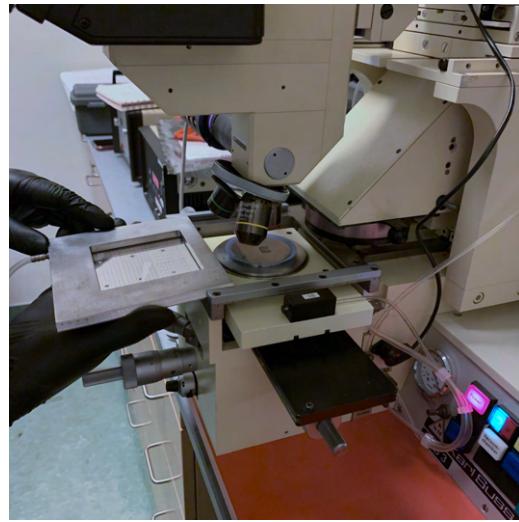
Figure 10: Spin-Coater Stage

2. Next, we aligned a mask with a circuit pattern over our graphene sample and exposed the wafer to ultra-violet (UV) light. The UV light makes the photoresist soluble to the developer so that in the developing step, the parts of the wafer not covered by the mask will wash off exposing the silicon dioxide wafer substrate.

- We loaded the wafer into the mask aligner and located the general location of the graphene sample using the gold letter and number markings on the wafer.
- We loaded the mask into the holder which uses a vacuum to hold the mask in place. Keeping one hand underneath the mask, in the case of vacuum failure, we inserted the mask into the aligner above the sample as demonstrated in Fig. 11b
- Next, we aligned the graphene sample with a finer circuit pattern using a combination of coarse lever controls which move the objectives and fine levers which move the stage in the X and Y directions.
- After having aligned the graphene sample into the center of the circuit pattern, we expose the wafer to UV light for 4.25 seconds.



(a) Mask

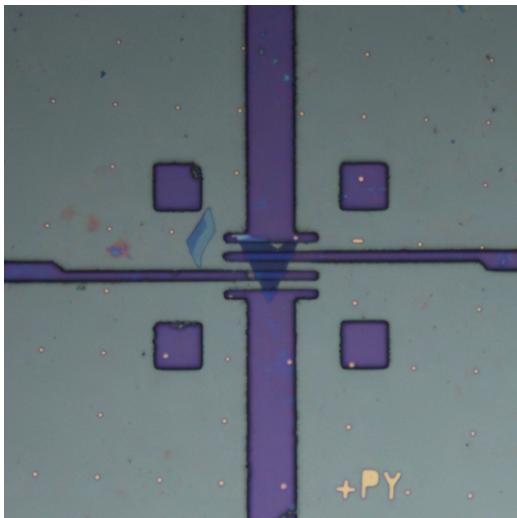


(b) Mask Aligner

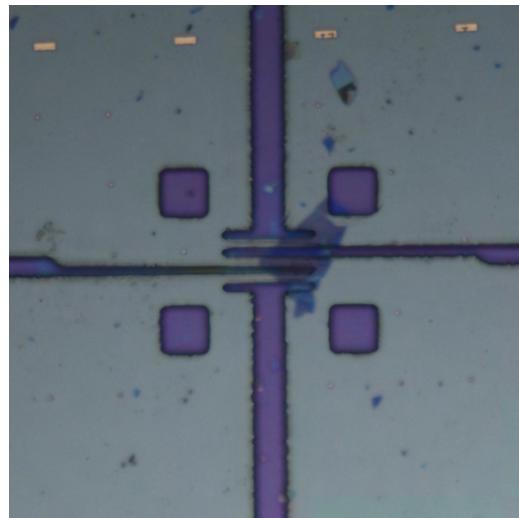
Figure 11: Mask Aligner

3. Next, we developed the wafers which allowed for the exposed photoresist to be washed off and harden the remaining photoresist. This step took place in three stages.

- First, we placed the wafers into a dish with developer for 50 seconds. The developer used was diluted from the original concentration with milli-q water using a ratio of 1 part original developer to 6 parts milli-q water.
- After that, we rinsed the wafers in de-ionized water for 40 seconds before drying the samples using jets of air.
- Then we hard baked the sample at 100° C for two minutes which solidifies the non-exposed photoresist.



(a) Vinh's Sample Located near 3A



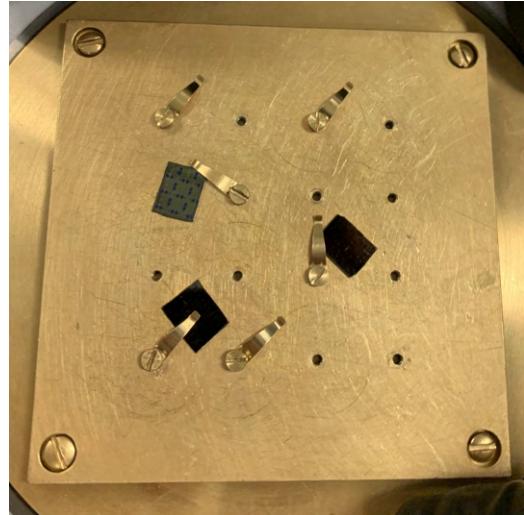
(b) Kam's Sample Located at 3B

Figure 12: Result after development. The yellow background is the baked photoresist. The purple areas correspond to the areas where the photoresist was exposed to UV light which allowed for it to be dissolved off in the development step. In the evaporation step, the purple areas are then to be filled in with gold to construct the circuit. At the centers, we see the graphene samples.

4. Next, we<sup>1</sup> evaporated 4 nm of titanium and afterwards 40 nm of gold onto the wafers. The specific evaporator used is an electron beam evaporator. First, the samples are loaded via retaining pins into a dish which is then attached into the interior of the evaporator and small amounts of titanium and gold are loaded into their respective crucibles. The evaporator is then closed and a vacuum is applied. Then, via a tungsten filament, beam of electrons is sent towards the crucibles heating the metals up and turning them into vapors which then condense and form a thin film onto the wafer.



(a) Evaporator Opened in preparation for loading of the samples

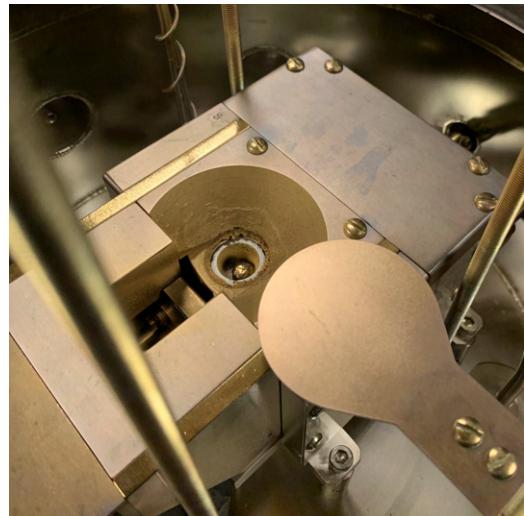


(b) Samples secured into plate. We can faintly see the developed pattern on the top left most wafer.

Figure 13: Initial Loading of Samples into Evaporator



(a) Samples loaded and attached to plate.

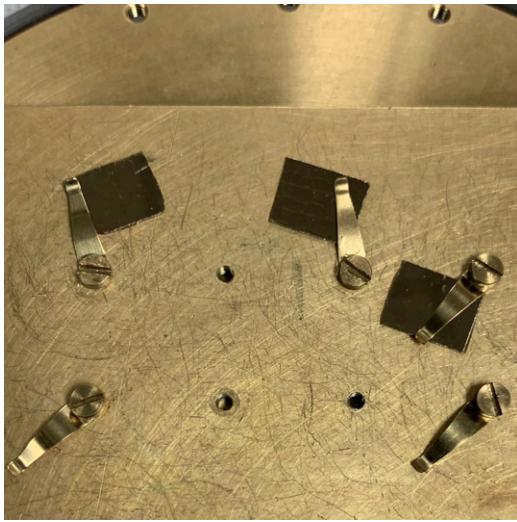


(b) Gold Crucible. The gold pellet inside will be heated via electrons emitted from a tungsten filament with the subsequent gold vapor rising and depositing on the plate in 14a

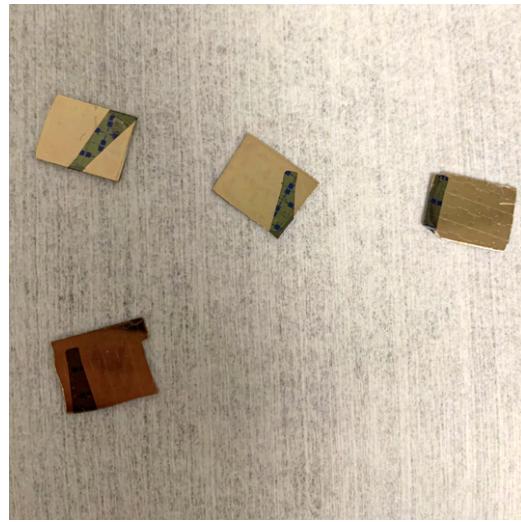
Figure 14: Sample Plate Loaded and Gold Crucible

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<sup>1</sup>Thank you to Derek and Francisco for doing the evaporation for us!



(a) Loaded wafers post evaporation. We see that they're coated in gold now!



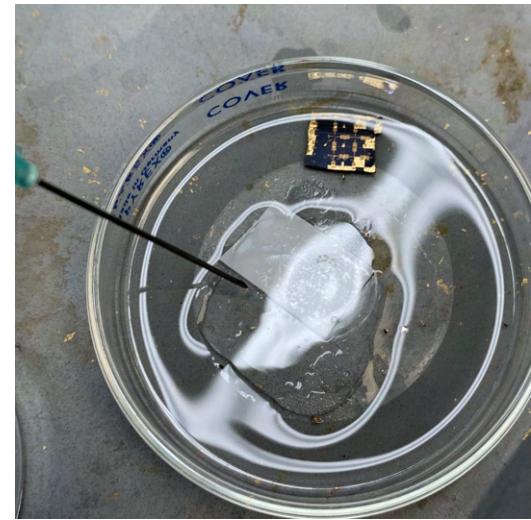
(b) Samples removed from pins. We see clearly the developed mask pattern underneath the gold in purple with the photoresist in the darker yellow.

Figure 15: Samples Post Evaporation

5. Lastly, we perform the lift off wash for the wafers which removes the irrelevant gold, that is, the gold that lays on top of the photoresist, without removing the gold that forms the electrodes. As the photoresist used in this lab is acetone soluble, the lift off wash consists of placing the wafers into a dish of acetone which starts to eat away the photoresist. Then using a syringe, we applied more pressurized jets of acetone to encourage removal of more stubborn bits of gold.



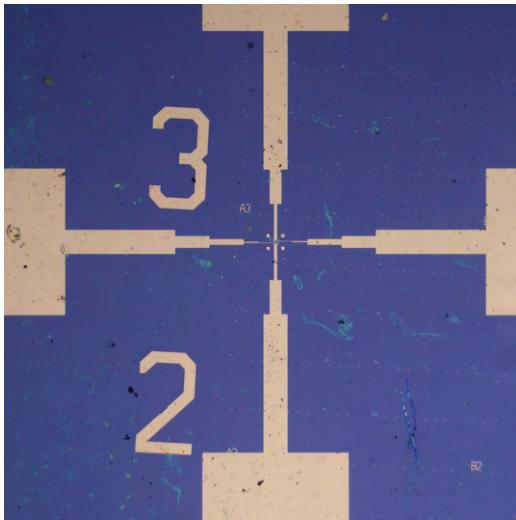
(a) Initial washing of sample with acetone using a syringe without needle to apply gentle pressure to the gold



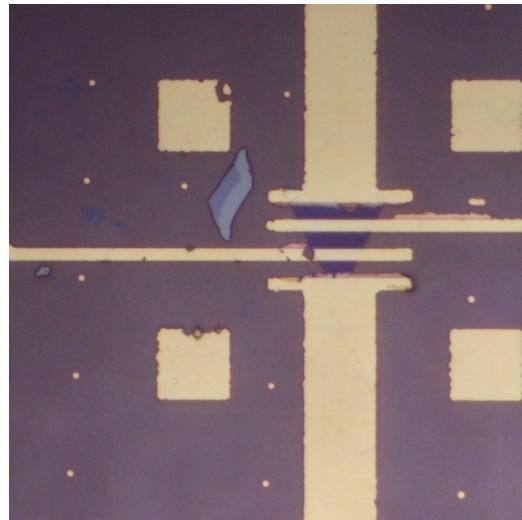
(b) Result after several minutes: majority of the gold has been removed and we switched to a syringe with a needle to apply greater more precise pressure

Figure 16: Lift Off Acetone Bath

6. Finally, after completing the lift off wash we have the following microscope images for our electrodes and samples.



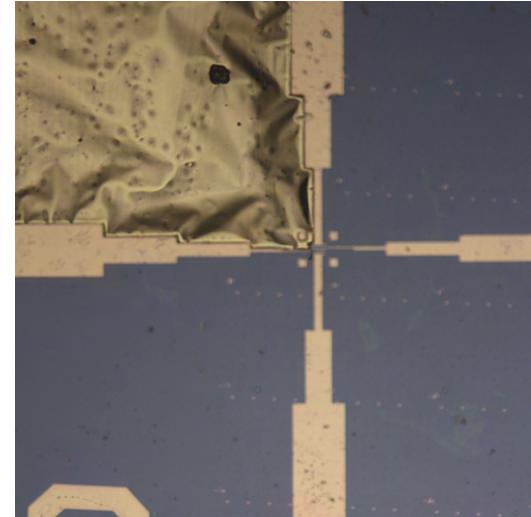
(a) 5X Magnification of the transistor for sample 3A after lift off



(b) 50X magnification of Vinh's Sample at 3A



(c) Sample 3X. We had a small issue with the gold having lifted off partially only to fold back onto another electrode



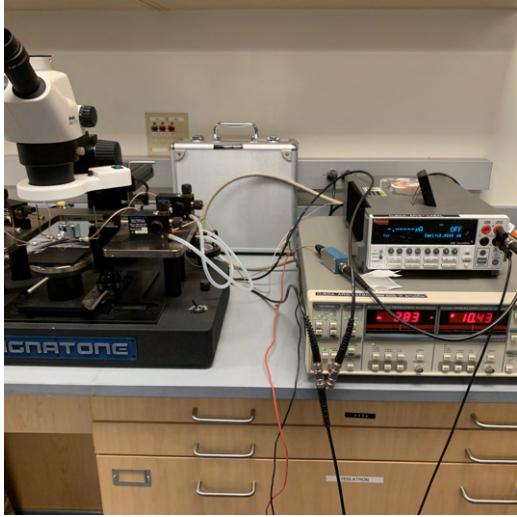
(d) Intermediate Stage: notice the gold appearing puffy as the acetone dissolves away the photoresist underneath the gold

Figure 17: Microscope images of our samples after lift-off. In particular, we see in (a) that the background has returned to the purple color of the wafer substrate

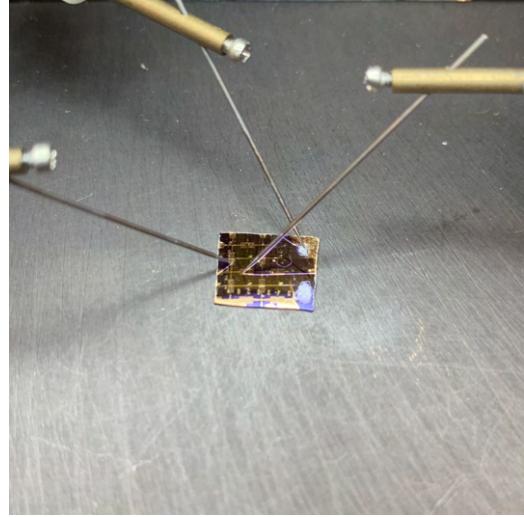
### 2.3 Measurement Procedure

Next, we want to measure both the resistance of the graphene sample as well as the dependence of the resistivity on the gate voltage.

To this end, we place our wafers into the probe station which is then connected to a Keithley multimeter and locked in amplifier in the circuit described in the circuit diagram below. Then, we scratch a circular scratch onto the wafer using a diamond tipped pen as to access the highly doped silicon underneath the silicon dioxide layer on top. This is our gate terminal.



(a) Probe Station on Left, Lock In Amplifier On the Right

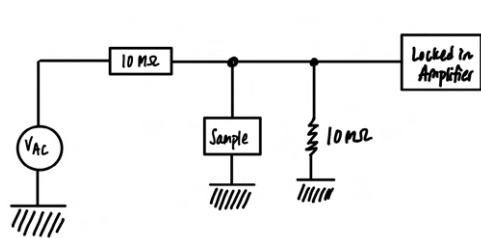


(b) Connecting probe needles to the pads with one connected to the gate

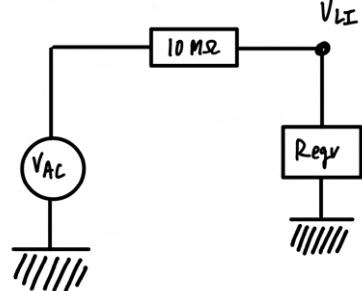
Figure 18: Circuit Implementation

### 2.3.1 Circuit Set up and Derivation of Sample Resistance Expressed in terms of $V_{AC}$ and $V_{LI}$

The circuit used is given by Figure 19a where  $V_{AC}$  is the excitation voltage supplied by an external power supply, sample refers to our graphene sample, and finally connected to this is a locked-in amplifier.



(a) Circuit Diagram of Full Circuit



(b) Equivalent Circuit

Figure 19: Circuit Implementation

We can re-write this circuit as an equivalent circuit as shown in Figure 19b with an equivalent resistor  $R_{eq}$  which using Ohm's law gives us the following condition

$$V_{LI} = IR_{eq} \quad (4)$$

where  $R_{eq}$  is given by

$$\frac{1}{R_{eq}} = \frac{1}{R_{Sample}} + \frac{1}{10 M\Omega} \quad (5)$$

However, since the resistance of graphene is typically on the order of a few kΩ, we have  $R_{Sample} \ll 10 M\Omega$  so that we can simplify the equivalent resistance using the following approximation

$$\frac{1}{R_{eq}} = \frac{1}{R_{Sample}} + \frac{1}{10 M\Omega} \approx \frac{1}{R_{Sample}} \quad \Rightarrow \quad R_{eq} \approx R_{sample} \quad (6)$$

which then gives us

$$V_{LI} \approx IR_{\text{Sample}} \quad (7)$$

We also have Ohm's law as applied to the excitation voltage  $V_{AC}$  which takes the following form

$$V_{AC} = I(10 \text{ M}\Omega + R_{\text{eqv}}) \approx I(10 \text{ M}\Omega + R_{\text{sample}}) \approx I(10 \text{ M}\Omega) \quad R_{\text{sample}} \ll 10 \text{ M}\Omega \quad (8)$$

Now, eliminating the current  $I$  from both expressions gives us an expression for the sample resistance in terms of two controllable parameters: the resistance of the resistor ( $10 \text{ M}\Omega$ ) and the excitation voltage  $V_{AC}$  and one dependent, measurable parameter: the lock-in voltage  $V_{LI}$

$$I = I \quad (9)$$

$$\frac{V_{LI}}{R_{\text{Sample}}} = \frac{V_{AC}}{10 \text{ M}\Omega} \quad (10)$$

$$\Rightarrow R_{\text{sample}} = \frac{V_{LI}}{V_{AC}} \times 10 \text{ M}\Omega \quad (11)$$

Moreover, the  $10 \text{ M}\Omega$  resistor was chosen to match the internal impedance of the lock-in amplifier. Then, in the case of an open circuit, which may occur if our sample was accidentally destroyed by static discharge or high voltages, the lock in voltage would be about half of the excitation voltage

$$V_{LI} = \frac{V_{AC}}{2} \quad (12)$$

which we can immediately see on the lock-in amplifier. This is because the circuit would reduce to Figure 20 and we would have

$$V_{LI} = I(10 \text{ M}\Omega) \quad (13)$$

$$I = \frac{V_{AC}}{10 \text{ M}\Omega + 10 \text{ M}\Omega} \quad (14)$$

which implies that

$$V_{LI} = \frac{V_{AC} \cdot 10 \text{ M}\Omega}{20 \text{ M}\Omega} = \frac{V_{AC}}{2} \quad (15)$$

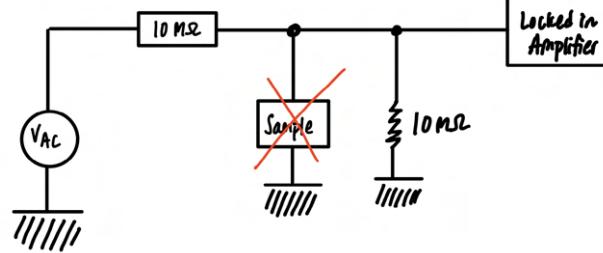


Figure 20: Circuit in the case sample is disconnected

### 2.3.2 Lock-In Amplifier Mechanism of Operation and Importance

The lock-in amplifier is used as we need to extract the signal from the noise. Field effect transistors, as opposed to bipolar transistors, have characteristically high impedance and hence only allow for small currents to flow. To be able to detect the current and hence determine the corresponding voltage via Ohm's law, we want to magnify the current signal using the lock-in and achieve a higher signal to noise ratio.

The lock-in works as follows. The signal of interest, being sinusoidal in nature with some known frequency  $\omega_{AC}$  with possible additional noise terms, is passed to the lock-in. This signal is multiplied by a reference signal

with the same frequency as the signal frequency. Then, time-averaging over the subsequent product, due to the orthogonality of the sinusoidal functions, terms where the phases don't match drop out and yields a DC signal or non periodic signal. In practice, this time averaging is performed by passing the product signal through a low pass filter which attenuates signals with frequencies higher than the cut off frequency.

For instance, suppose the signal we measure from our sample is given by

$$V_{\text{sample}} \sin(\omega_{\text{AC}} t + \theta_{\text{sample}}) + \underbrace{\sum_i V_i \sin(\omega_i t + \theta_i)}_{\text{Noise}} \quad (16)$$

and we multiply it by a reference signal via the lock-in

$$V_L \sin(\omega_L t + \theta_{\text{ref}}) \quad (17)$$

We can re-write the product of these two signals using a trigonometric identity to give us

$$V_{\text{output}} = \frac{1}{2} V_{\text{sample}} V_L \cos((\omega_{\text{AC}} - \omega_L)t + \theta_{\text{sample}} - \theta_{\text{ref}}) \quad (18)$$

$$- \frac{1}{2} V_{\text{sample}} V_L \cos((\omega_{\text{AC}} + \omega_L)t + \theta_{\text{sample}} + \theta_{\text{ref}}) \quad (19)$$

$$+ \text{Noise} \quad (20)$$

When we then pass this signal to a low pass filter with a time constant much longer than a period of the product signal, the low pass filter will both time average the signal and attenuate signals with frequencies higher than the cut off frequency. Thus, noise terms and terms that contains  $\cos(\omega_{\text{AC}} + \omega_L)$  will drop out leaving us with the first term

$$\langle V_{\text{output}} \rangle = \frac{1}{2} \cos(\theta_{\text{sample}} - \theta_{\text{ref}}) \quad (21)$$

which "locks on" to the excitation signal to the reference signal  $\omega_{\text{AC}} = \omega_L$

### 3 Results and Data Analysis

#### 3.1 Resistance Measurement at Zero Gate Voltage

We measured the lock in voltage for sample 3A (Vinh's sample) to be around  $410 \mu\text{V}$  for an excitation voltage of  $0.1 \text{ V}$  using the bottom and right pads for the source and drain. Then, this gives us the resistance of the sample as

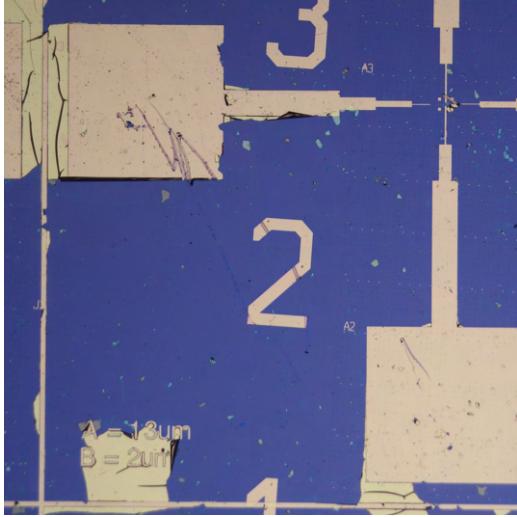
$$R_{3A} = \frac{4.10 \times 10^{-4} \text{ V}}{10^{-1} \text{ V}} 10^7 \Omega = 4.1 \times 10^4 \Omega = 41 \text{ k}\Omega \quad (22)$$

which is on same order of magnitude with the expected resistance for a graphene sample [5].

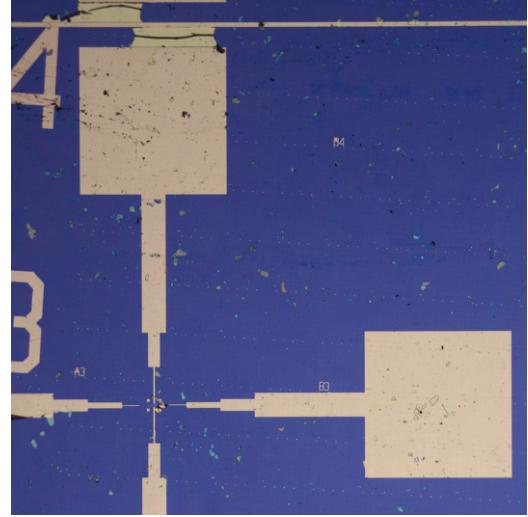
Repeating this for sample 3X (Raza's sample), we have

$$R_{3X} = \frac{5 \times 10^{-7} \text{ V}}{10^{-1} \text{ V}} 10^7 \Omega = 50 \Omega \quad (23)$$

We find that the resistance is much smaller which indicates a possible short in the circuit. First, from Figure 17c, we know that the top, right, and bottom electrodes are shorted. Examining the outer pads, we also see that the top, left, and bottom pads are shorted via excess gold that makes contact with the thin gold "border" that surrounds the pattern as shown in Figure 21. So all electrodes are shorted for this sample unfortunately and we did not have the time to correct these shorts which we could have done by scratching off one or more of the electrodes.



(a) Left and Bottom electrodes connected to the thin gold border by excess gold not removed in the lift off step



(b) Top electrode connected to thin gold border, right pad is free however

Figure 21: Images of Pads for Wafer 3X

### 3.2 Initial Back Gate Measurements

In the next stage, we vary the voltage applied to the gate for the two samples to determine the dependence of the resistivity on the gate voltage as explained in the measurement procedure in the previous section. The shape of this curve should exhibit features similar to the curves in Figure 3a where the resistivity tends towards zero towards the extreme ends of the voltage and rises up sharply in the middle.

We performed initial back gate measurements for two samples: 3A and AX and plot the lock-in voltage  $V_{LI}$  versus applied gate voltage  $V_G$  in Figures 22 and 23 respectively. The resistance of the sample, via equation (2), is directly proportional to the lock-in voltage hence the following plots gives the same data as a resistance versus gate voltage plot.

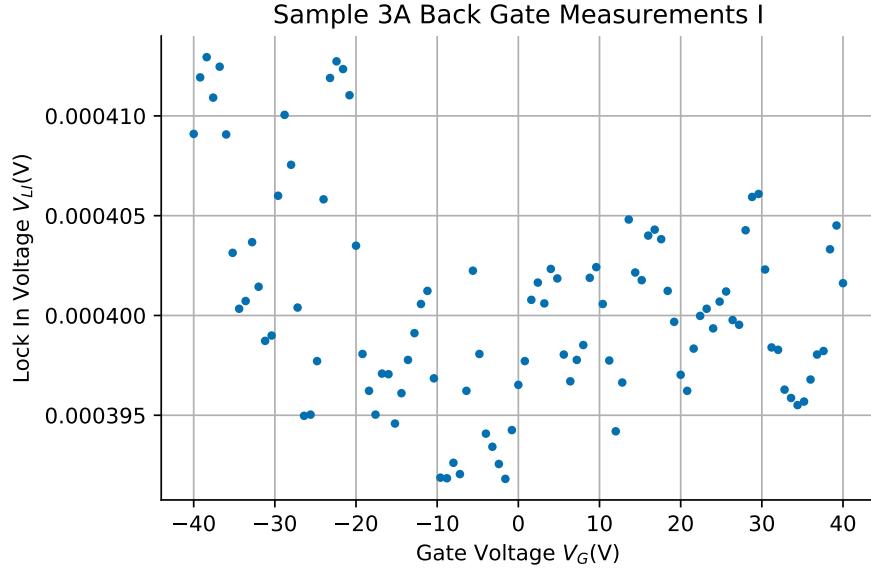


Figure 22: Gate Dependence for Sample 3A for  $-40\text{V}$  to  $40\text{V}$  sampling 100 points with step size  $0.8\text{V}$ . We do not see a strong gate dependence, though towards  $V_G = -40\text{ V}$ , the resistivity rises slightly.

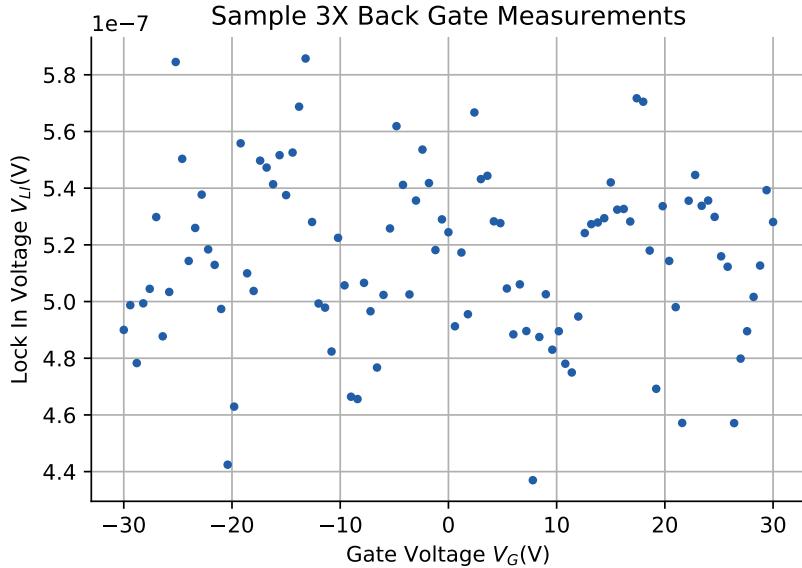


Figure 23: Gate Dependence for Sample AX for  $-30\text{V}$  to  $30\text{V}$  sampling 100 points with step size  $0.6\text{V}$ . The data indicates that there is no dependence on the gate voltage for this sample which is likely due to the shorts mentioned in the previous section

For the 3A sample, though the overall resistance of the sample seems to be on the same order of magnitude as expected for a graphene sample, there does not seem to be an obvious dependence on applied gate voltage. There are a few possibilities why:

- One concern is that the graphene sample could have been doped through our treatment of the wafer through the chemicals used in the photolithography process as well as exposure to excess light among other things. For this wafer, we repeated the lithography process at least *twice* due to poor development the first two times which includes washing in acetone, methanol, and IPA, coating in photoresist, exposure to UV light, and finally developer. Then, the expected resistivity peak may have been shifted as to lay outside of the gate voltage range used in this experiment.
- Another possibility is that there is an issue with the gate leaking. There are a few locations where we may have scratched the pads with the probe station needles as to damage the underlying insulating  $\text{SiO}_2$  layer. Moreover, one of the gold electrode pads makes contact with the edge and hence underlying highly doped surface which could reduce the effective “capacitance” of the parallel plate capacitor formed by the graphene and doped silicon so that an applied gate voltage would not yield a strong electric field effect.
- One last possibility is that our samples were too “thick”, that is, had much more layers than few-layer graphene. In fact, few-layer graphene tends to appear almost transparent when overlayed on the  $\text{SiO}_2$  wafer whereas our samples all appeared to be a deep blue. As a result, the sharp peak exhibited in Figure 3a would have been smoothed out. Moreover, we performed the measurements at room temperature which could also have flattened the curve further which we can see occur in Figure 3a where the resistivity curve smooths out as temperature increases towards 300K.

### 3.3 Back Gate Measurements after attempts at Corrections

To attempt to address these concerns we scratched off the troublesome electrodes for sample 3A as demonstrated in Figure 24 and scratched a deeper gate. Then we repeated the measurements and plotted the results in Figure 25. In this case, we do see a slight increase in the resistivity around  $10\text{-}30\text{ V}$  before it decreases for increased gate voltage. Though the magnitude of the increase is relatively small and the data appears to be very noisy, we can attempt to fit a Lorentzian function  $L(x)$  using  $x_0, \Gamma, h$  as fittable parameters

$$L(x) = \frac{1}{\pi} \frac{\frac{1}{2}\Gamma}{(x - x_0)^2 + (\frac{1}{2}\Gamma)^2} + h \quad (24)$$

to the scattered points by minimizing the square mean error. We chose a Lorentzian function in anticipation of fitting to data with a “peak” (we could have equally chosen a Gaussian). We were not interested in the specific values of the parameters themselves but rather we were trying to determine if there was a curve that fits the points that could highlight features of the graph. Doing so, we maybe observe a small peak centered at around  $V_G = 20$  V. Admittedly, it is not clear if this approach is valid at all.

After this, we make one final attempt at trouble shooting this wafer by again scratching a deeper gate, then cleaning off the conductive sandy residue using pressurized inert gas, and wiping down the probe needles with isopropyl alcohol. The measurements after this last step are plotted in Figure 26 where we again fitted a Lorentzian function against the data and observe a peak centered at around  $V_G = 10$  V in this case.

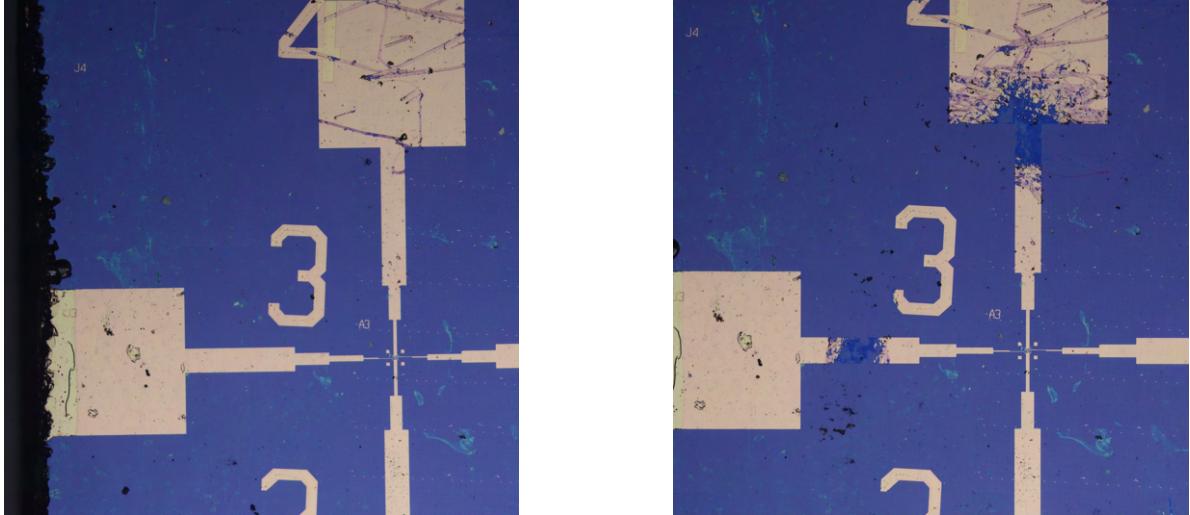


Figure 24: Scratching Off Electrodes/Connections

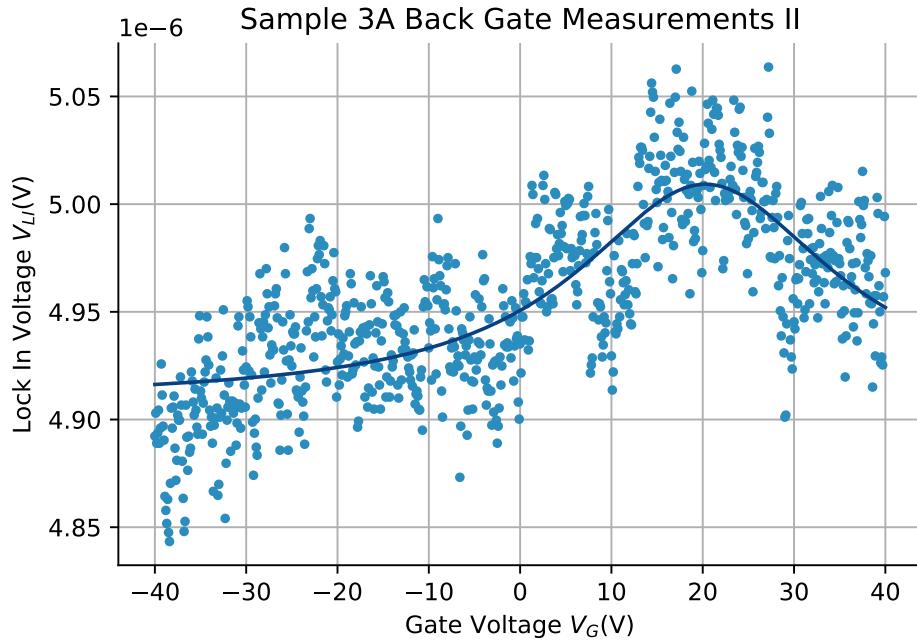


Figure 25: Backgate measurements for 3A second attempt from - 40V to 40V sampling 800 points with step size 0.1V after initial electrode scratching. We see that there is perhaps a small bump at around  $V_G = 20$  V demonstrated by the fitted Lorentzian curve in dark blue.

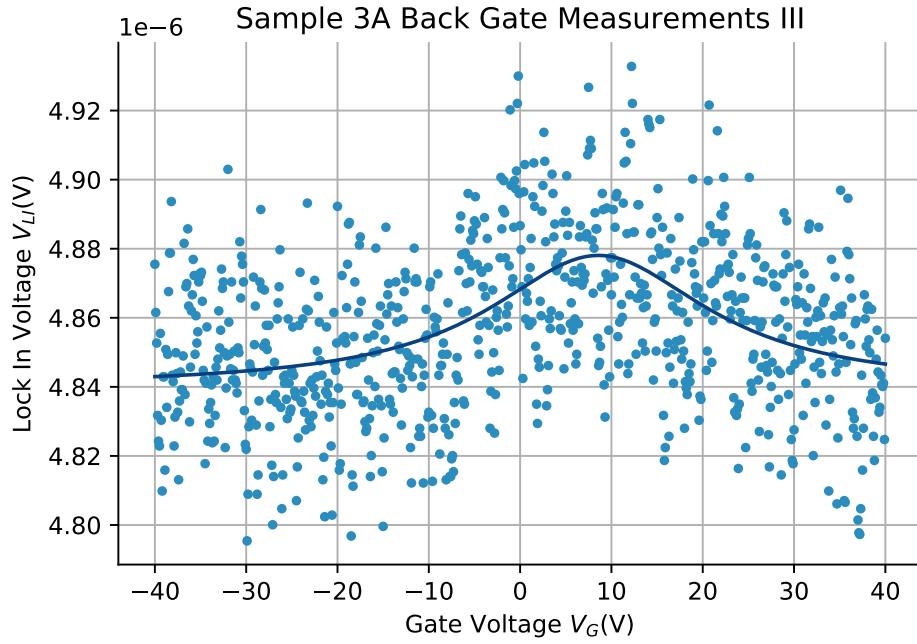


Figure 26: Backgate measurements sample 3A third attempt, - 40V to 40V, 800 points, step size 0.1V after further gate scratch and probe cleaning. There is perhaps a small bump localized at around  $V_G = 10$  V. We fit a Lorentzian function to the data and observe a small peak.

## 4 Other Complications

### 4.1 Sample Preparation

Our initial batch of wafers had a few issues with the initial attempt at lithography where after the development step we had patterns that were “rainbowy” as demonstrated in Fig. 27.

One possible issue was that the initial combination of developer solution strength and development time led to underdeveloped wafers. For the initial batch, the concentration strength was developer diluted by 1 part original developer to eight parts milli-q water with a development time of 35 seconds. The rainbow pattern indicated an incomplete and uneven removal of the photoresist and hence underdevelopment as the remaining layer of photoresist would act as a thin-film over the reflective mirror-like substrate and exhibit thin-film interference.

To remedy this, we took our samples and washed them in acetone, methanol, and isopropyl solutions which completely removed all traces of the photoresist including the hard-baked part and repeated the photolithography. We repeated the development using a stronger concentration of one part developer to six parts milli-q water with a longer development time of 50 seconds which yielded more desirable results.

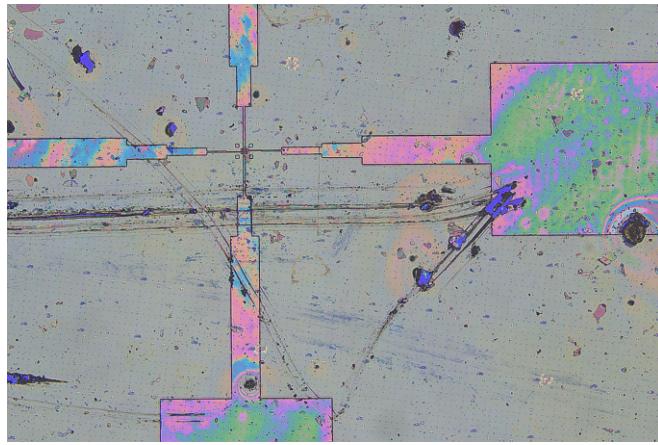


Figure 27: One of our original wafers. We see the same mask pattern but instead with a rainbow color rather than the purple of the substrate. This would not have led to a good “lift off” as the rainbow indicates residual photoresist which would have taken off the printed circuit in the lift off wash as well as the baked photoresist.

### 4.2 Evaporation

The wafer with the graphene sample near B3 (Kam’s sample) had the sample accidentally covered by a retaining pin when put into the evaporator so no gold was able to fill in the electrodes immediately around the sample. Then, when we put the sample into the acetone lift off bath, it took off the photoresist immediately surrounding the sample destroying the pattern.

## 5 Conclusions

To recap, the purpose of this lab was two-fold. First, we became acquainted with the process of fabricating a graphene field effect transistor via mechanical exfoliation of highly oriented graphite and then photolithography, evaporation, and liftoff to print the circuit and finally gain experience with using a lock-in amplifier. Via these steps, we fabricated two graphene FET candidates. Secondly, we wanted to probe the resistivity of the graphene sample as a function of an applied gate voltage in an effort to reproduce resistivity versus gate voltage values that agree with the existing literature.

When performing our back gate measurements, we found that the resistivity of the two graphene samples did not initially exhibit significant back gate dependence. For sample AX, the reason was immediate: all four electrode pads were shorted with each other which yielded an especially low resistance reading for the graphene sample. For sample A3, the sample exhibited proper resistivity at zero gate voltage but did not exhibit significant dependence as the gate voltage was varied.

However, after scratching off problematic electrodes in sample A3 and repeating the back gate measurements, we find a possible dependence of the resistivity for gate voltage as graphed in Figures 25 and 26 where we fitted Lorentzian curves to the data. That being said, the overall shape of the fitted curve is broadened with a wider width and smaller peak than the expected profile for mono layer graphene at zero temperature with the data being overall perhaps too noisy to be able to draw any meaningful resistivity dependence.

We discussed possible reasons for the discrepancy with the existing results: a possible issue with the gate leaking, an issue with the sample not being an ideal “graphene” sample, a possible doping of the sample via our mistakes in the photolithography step, and finally the fact that we perform the measurements at room temperature. All of these reasons could have led to the lowering of the peak height and broadening of the profile width.

Moving forward, if we were to repeat the experiment, we would take extra care in the fabrication step especially with regards to the photolithography to limit exposure of the sample to unnecessary chemicals and UV light which can dope it excessively. Alternatively, we could anneal the finished graphene FET in vacuum which could reverse some of the doping effects as described in [5]. Moreover, we could have better results if we were to find more ideal candidates for graphene, that is, a thinner and more uniform sample. Having experienced the complications detailed previously, we would use a revised developer solution and time to do the development properly the first time and be careful with the location of the sample on the wafer as to not cover the sample with a pin when performing the Ti-Au deposition. In the end, using this same fabrication and back gate measurements, we could probe other properties of graphene! For instance, we could measure the electron mobility  $\mu$  since  $\mu$  is given in terms of the conductivity  $\sigma$  and we measure the resistance from which we can determine the resistivity  $\rho$  and hence  $\sigma$ .

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