Priya Raj

+918924840259 | priya_m241111ec@nitc.ac.in | linkedin.com/in/priya-shahi-bab131173/

Education

National Institute of Technology, Calicut — Kerala, India
Master of Technology in Electronics Design and Technology (ECE), CGPA: 7.65/10 — *2024 - Present*

JSS Academy of Technical Education — Noida, UP
Bachelor of Technology in Electronics and Communication Engineering, CGPA: 7.83/10 — *2020 - 2024*

Internships

Ericsson (Automation Engineer) — Apr 2024 - Aug 2024
- Developed and implemented monitoring protocols for **Orange Belgium** achieving **90%** network availability
- Managed real-time monitoring and troubleshooting of high speed network bands reducing outage incidents by **40%**
- Optimized RAN system performance utilizing **BMC Helix** and diagnostic tools, improving efficiency by **25%**

NIELIT (Trainee) — Jul 2023 - Aug 2023
- Successfully completed specialized training in **VLSI Design** gaining a strong foundation principles & methods
- Acquired practical insights into VLSI Design methods by applying theoretical knowledge to real-world scenarios

Maven Silicon (Trainee) — Oct 2022 - Nov 2022
- Completed a research internship with Maven Silicon, actively engaging in short-term projects that allowed for a concentrated application of VLSI concepts and methodologies, contributing to a practical understanding

Projects

Multimodal Image Fusion
- Benchmarked **DWT, Guided Filter, Max-Min, & PCA** on 10 image pairs, achieving **SSIM** up to 0.90
- Implemented **SOTA Fuzzy-SPD** fusion from scratch, improving QAB/F by 10% over past results.
- Built benchmarking framework with 6 evaluation metrics, enabling 40+ fusion operations and detailed analysis.

FPGA-based Digital Demodulator
- Engineered an FPGA-based digital demodulator for **DRDO**, with **dual-ADC input architecture**.
- Achieved 97% detection accuracy through phase-aligned demodulation and validated outputs with MATLAB.
- Generated synchronized sine and cosine waveforms using **CORDIC** algorithm to enable precise in-phase and quadrature demodulation.

Secure Voting System with FPGA Integration
- Designed and implemented a secure, password-authenticated electronic voting system on FPGA using Verilog HDL, with real-time feedback via 7-segment displays and LED indicators.
- Developed a Finite State Machine (FSM) to control secure voting flow, and integrated modules for clock generation, button debouncing, and binary-to-BCD conversion to ensure accurate, tamper-resistant vote processing.

GasShield: Smart Hazardous Gas Detection & Response System
- Developed threshold-based alert logic aligned with EN50291 standards, enabling real-time alerts via OLED, GSM, and automated emergency response
- Conducted a user survey based on a real-life case study **(Kerala CO accident**), findings on 91% interest and cost sensitivity influenced low-cost hardware optimization

Positions of Responsibility

Robotics And Automation Society (IEEE)
Chairperson
- Demonstrated strong leadership, organizing impactful robotics events for IEEE RAS Student Branch Chapter
- Supervised workshops and conferences fostering deeper understanding of robotics and automation among members

Technical Skills & Coursework

Languages: Verilog, System Verilog, C/C++, Python
Tools: Vivado, Cadence, Ansys HFSS,
Coursework: Design of Digital Systems, Embedded System, Computer Architecture (Processor pipeline), Digital Logic Design, STA, Operating System, Verification, Digital Integrated Circuit, VlSI Design Flow.